

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC4017BP, TC4017BF

TC4017BP / TC4017BF DECADE COUNTER / DIVIDER

TC4017BP / BF is decimal Johnson counter consisting of 5 stage D-type flip-flop equipped with the decoder to convert the output to decimal.

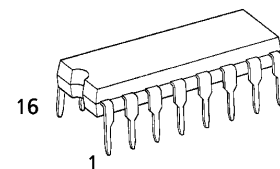
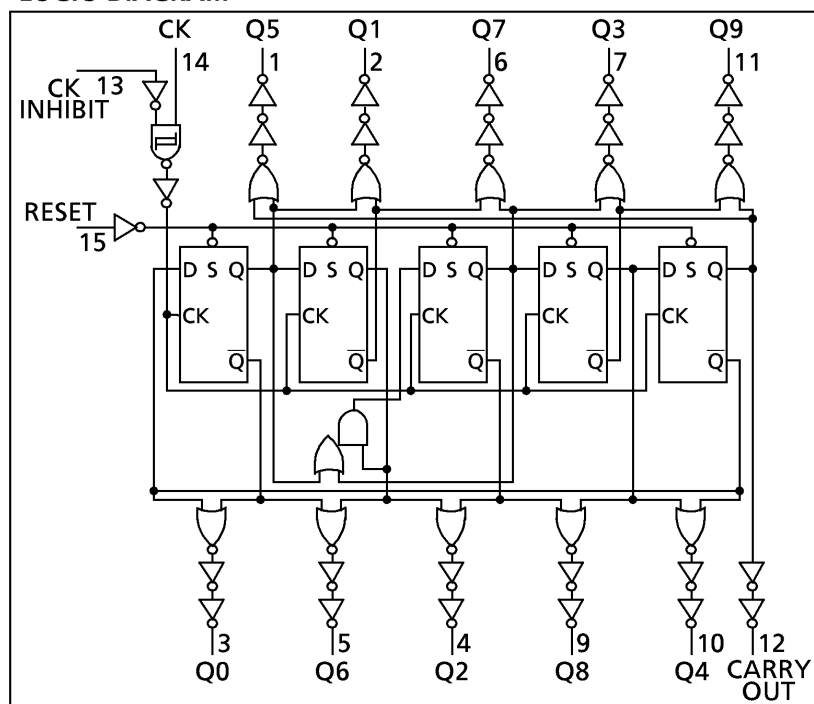
Depending on the number of count pulses fed to CLOCK or CLOCK INHIBIT one output among 10 output lines "Q0" through "Q9" becomes "H" level.

The counter advances its state at rising edge of CLOCK (CLOCK INHIBIT="L") or falling edge of CLOCK INHIBIT (CLOCK="H"). RESET input to "H" level resets the counter to Q0="H" and Q1 through Q9="L" regardless of CLOCK and CLOCK INHIBIT.

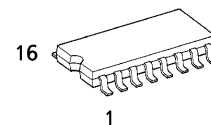
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	$V_{SS} - 0.5 \sim V_{SS} + 20$	V
Input Voltage	V_{IN}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
Output Voltage	V_{OUT}	$V_{SS} - 0.5 \sim V_{DD} + 0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	300 (DIP) / 180 (SOIC)	mW
Operating Ambient Temperature Range	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

LOGIC DIAGRAM

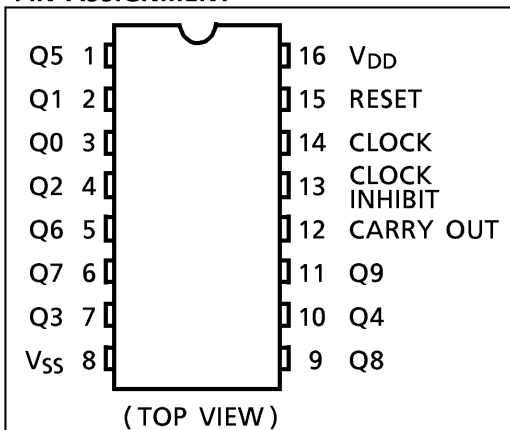


P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

PIN ASSIGNMENT



TRUTH TABLE

INPUTS			SELECTED OUTPUT
CLOCK Δ	CLOCK INHIBIT Δ	RESET	
※	※	H	Q0
※	H	L	Qn (NC)
L	※	L	Qn (NC)
$\uparrow$	L	L	Qn + 1
$\downarrow$	L	L	Qn (NC)
H	$\uparrow$	L	Qn (NC)
H	$\downarrow$	L	Qn + 1

Δ ; Level Change

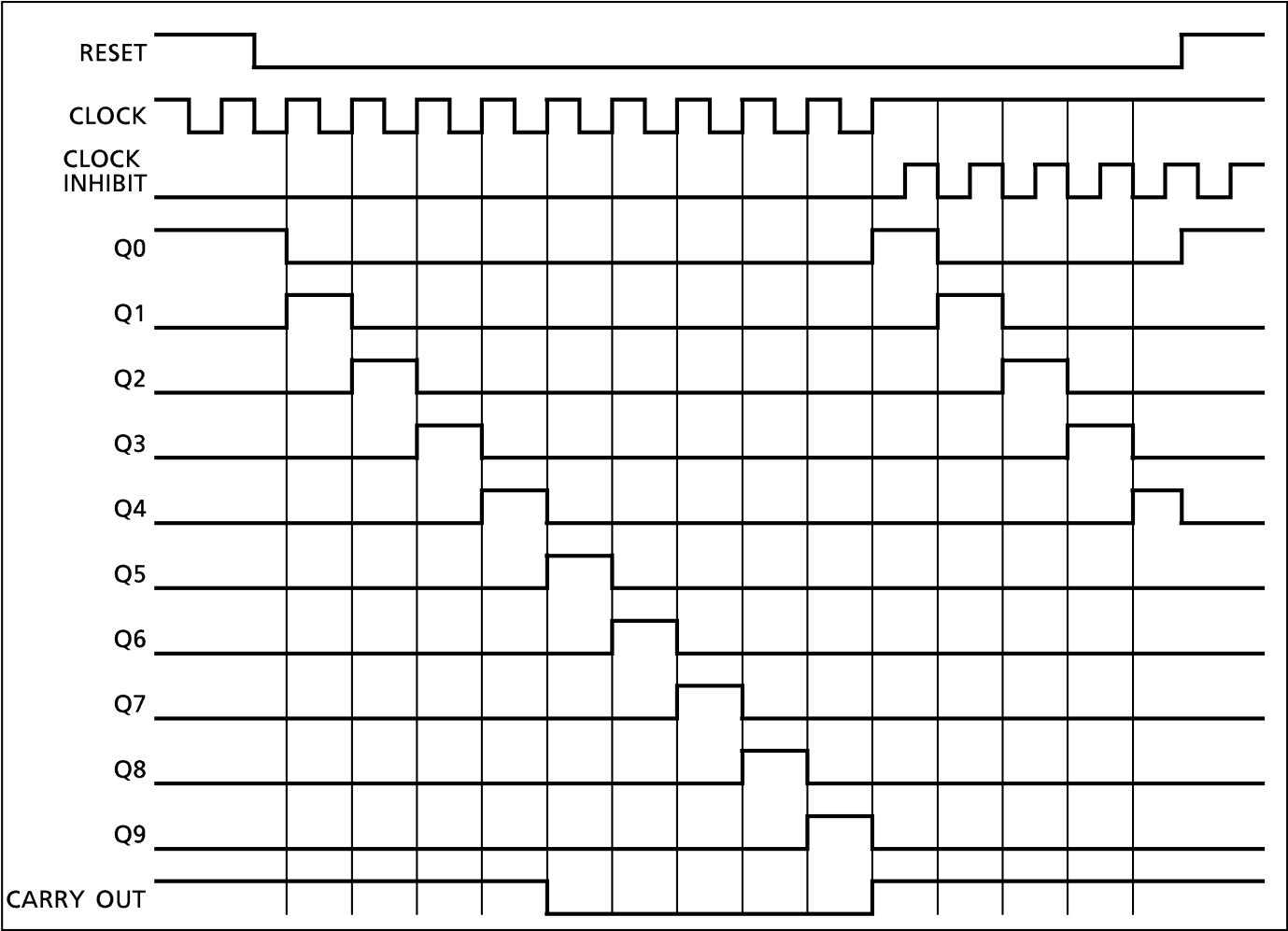
※ ; Don't Care

NC ; No Change

CARRY OUT { "H" Q0 ~ Q4 = "H"

"L" Q5 ~ Q9 = "H"

TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V _{DD}		3	—	18	V
Input Voltage	V _{IN}		0	—	V _{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS} = 0V)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V _{DD} (V)	−40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V _{OH}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-Level Output Voltage	V _{OL}	I _{OUT} < 1μA V _{IN} = V _{SS} , V _{DD}	5	—	0.05	—	0.00	0.05	—	0.05	
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS} = 0V$)

CHARACTERISTIC	SYM-BOL	TEST CONDITION	V_{DD} (V)	- 40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	
Output High Current	I_{OH}	$V_{OH} = 4.6V$	5	-0.61	—	-0.51	-1.0	—	-0.42	—	mA
		$V_{OH} = 2.5V$	5	-2.50	—	-2.10	-4.0	—	-1.70	—	
		$V_{OH} = 9.5V$	10	-1.50	—	-1.30	-2.2	—	-1.10	—	
		$V_{OH} = 13.5V$	15	-4.00	—	-3.40	-9.0	—	-2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output Low Current	I_{OL}	$V_{OL} = 0.4V$	5	0.61	—	0.51	1.5	—	0.42	—	mA
		$V_{OL} = 0.5V$	10	1.50	—	1.30	3.8	—	1.10	—	
		$V_{OL} = 1.5V$	15	4.00	—	3.40	15.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input High Voltage	V_{IH}	$V_{OUT} = 0.5V, 4.5V$	5	3.5	—	3.5	2.75	—	3.5	—	V
		$V_{OUT} = 1.0V, 9.0V$	10	7.0	—	7.0	5.50	—	7.0	—	
		$V_{OUT} = 1.5V, 13.5V$	15	11.0	—	11.0	8.25	—	11.0	—	
		$ I_{OUT} < 1\mu A$									
Input Low Voltage	V_{IL}	$V_{OUT} = 0.5V, 4.5V$	5	—	1.5	—	2.25	1.5	—	1.5	V
		$V_{OUT} = 1.0V, 9.0V$	10	—	3.0	—	4.50	3.0	—	3.0	
		$V_{OUT} = 1.5V, 13.5V$	15	—	4.0	—	6.75	4.0	—	4.0	
		$ I_{OUT} < 1\mu A$									
Input Current	"H" Level	I_{IH}	$V_{IH} = 18V$	18	—	0.1	—	10^{-5}	0.1	—	μA
	"L" Level	I_{IL}	$V_{IL} = 0V$	18	—	-0.1	—	-10^{-5}	-0.1	—	
Quiescent Supply Current	I_{DD}	$V_{IN} = V_{SS}, V_{DD} *$	5	—	5	—	0.005	5	—	150	μA
			10	—	10	—	0.010	10	—	300	
			15	—	15	—	0.015	20	—	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ C$, $V_{SS} = 0V$, $C_L = 50pF$)

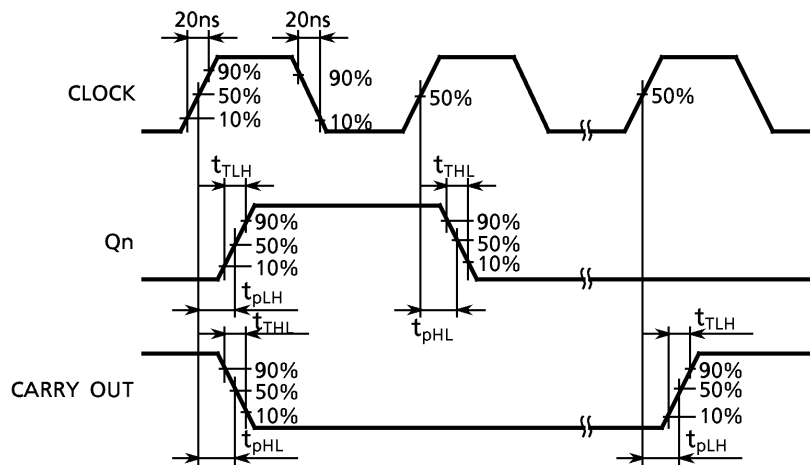
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	—	80	200	ns
			10	—	50	100	
			15	—	40	80	
Output Transition Time (High to Low)	t_{THL}		5	—	80	200	
			10	—	50	100	
			15	—	40	80	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta = 25°C, Vss = 0V, CL = 50pF)

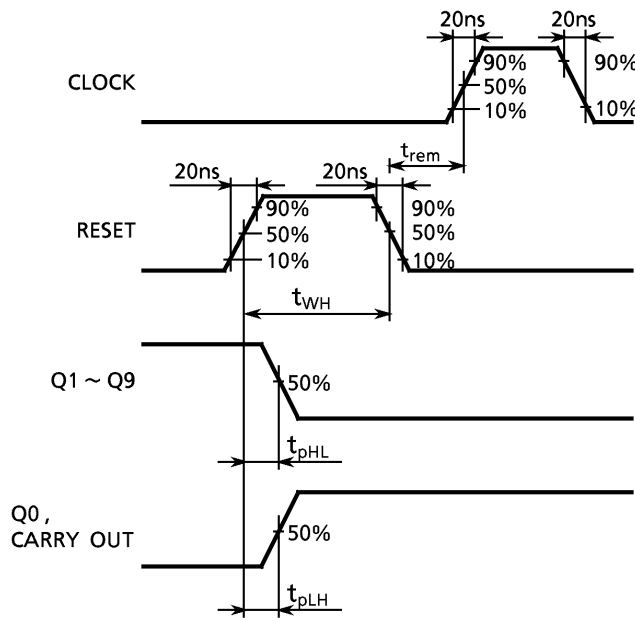
CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time (CLOCK - Qn)	t _{pLH} t _{pHL}		5	—	325	650	ns
			10	—	135	270	
			15	—	85	170	
Propagation Delay Time (CLOCK - CARRY OUT)	t _{pLH} t _{pHL}		5	—	280	600	
			10	—	110	250	
			15	—	75	160	
Propagation Delay Time (RESET - Qn RESET - CARRY OUT)	t _{pLH} t _{pHL}		5	—	265	530	
			10	—	115	230	
			15	—	85	170	
Max. Clock Frequency	f _{CL}		5	2.5	6.0	—	MHz
			10	5.0	12.0	—	
			15	6.7	13.5	—	
Min. Clock Pulse Width	t _W		5	—	85	200	ns
			10	—	40	90	
			15	—	35	60	
Min. Pulse Width (RESET)	t _{WH}		5	—	50	260	
			10	—	20	110	
			15	—	15	60	
Max. Clock Rise Time Max. Clock Fall Time	t _{rCL} t _{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time (CLOCK INHIBIT - CLOCK)	t _{SU}		5	—	30	230	ns
			10	—	15	100	
			15	—	10	70	
Min. Removal Time (RESET - CLOCK)	t _{rem}		5	—	– 55	400	ns
			10	—	– 20	275	
			15	—	– 15	150	
Input Capacitance	C _{IN}			—	5	7.5	pF

WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

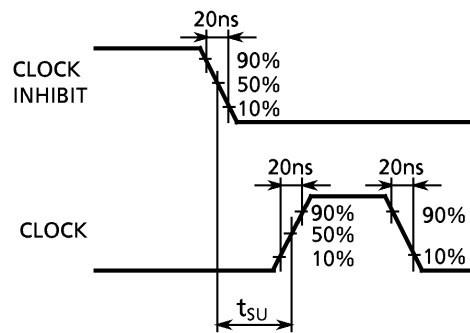
WAVEFORM 1.



WAVEFORM 2.

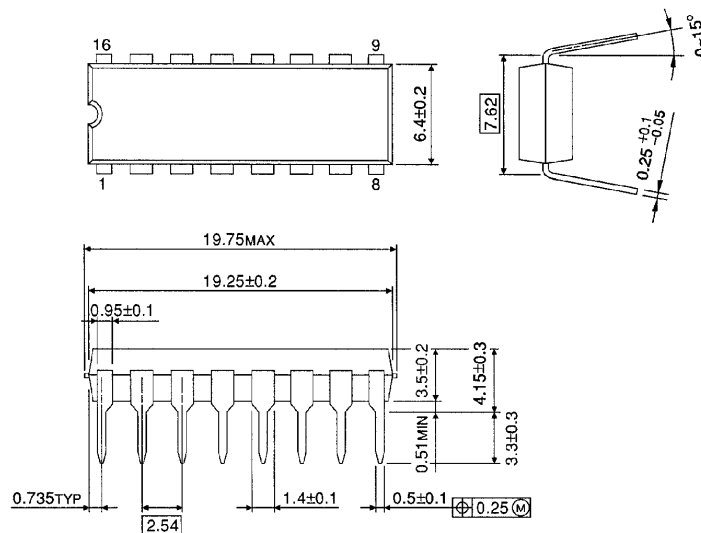


WAVEFORM 3.



DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

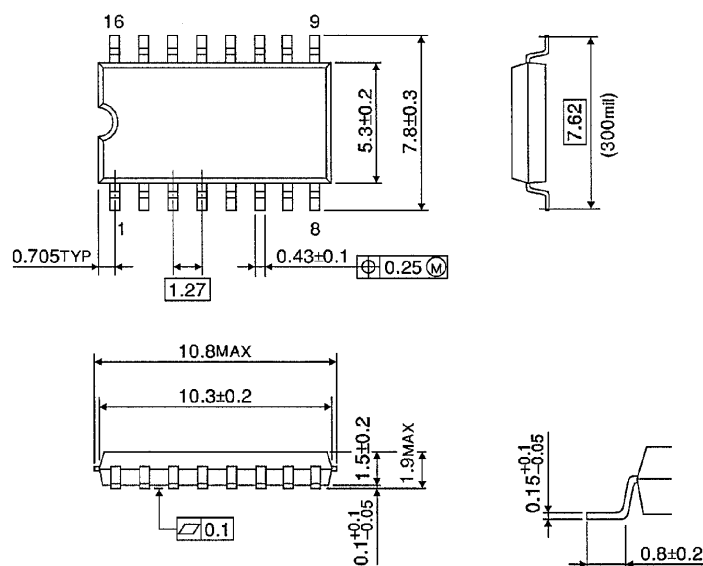
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



Weight : 0.18g (Typ.)

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000707EBA

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