

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62707F

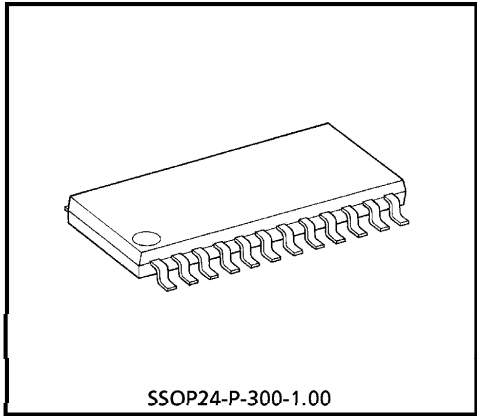
8BIT LATCHES & CONSTANT CURRENT DRIVERS

The TB62707F is specifically designed for LED and LED DISPLAY constant current drivers.

This constant current output is able to set up external resistor ($I_{OUT} = 90\text{mA MAX.}$).

This IC is monolithic integrated circuit designed to be used together with Bi-CMOS process.

The devices consist of 8bit latches, AND-GATE and Constant Current Drivers.



SSOP24-P-300-1.00

Weight : 0.32g (Typ.)

FEATURES

- Constant Current Output :
Can set up all output current with one resistor for 5 to 90mA.
- Constant Output Current Matching :

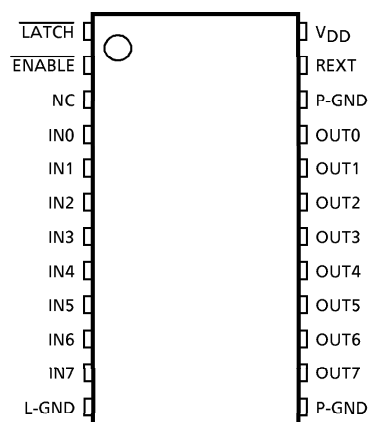
OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
≥ 0.4 [V]	± 6.0 [%]	5~40mA
≥ 0.7 [V]	± 6.0 [%]	40~90mA

- 5V CMOS Compatible Input
- Package : SSOP24-P-300

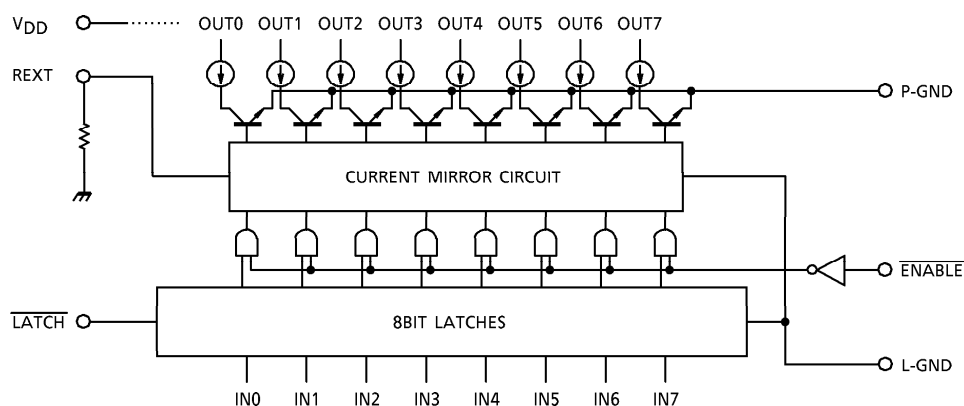
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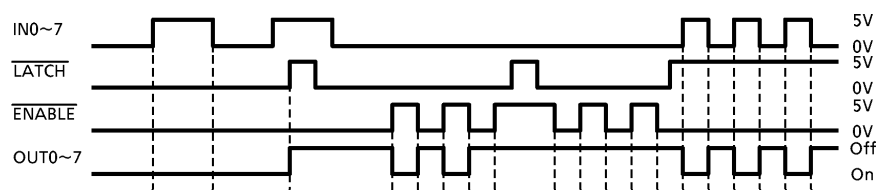
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM



(Note) Latches are level sensitive, not rising edge sensitive and not synchronous CLOCK.
 Input of $\overline{\text{LATCH}}$ -terminal to "H" level, data passes latches, and input to "L" level, data hold latches.
 Input of $\overline{\text{ENABLE}}$ -terminal to "H" level, all output (OUT0~7) do off.

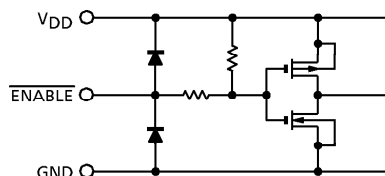
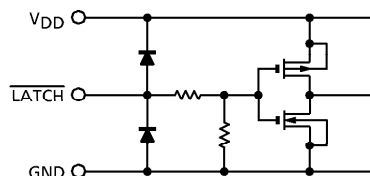
TERMINAL DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	$\overline{\text{LATCH}}$	Input terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$ -terminal, and hold data with "L" level input.
2	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$ -terminal, and do on with "L" level input.
4~11	IN0~7	Input terminal of a parallel-data for latches.
3	NC	No connection.
12	L-GND	GND terminal for controll logic.
13	P-GND	GND terminal for output constant current drivers.
14~21	OUT0~7	Output terminals.
22	P-GND	GND terminal for output constant current drivers.
23	REXT	Input terminal of connects with a resister for to set up all output current.
24	V _{DD}	5V Supply voltage terminal

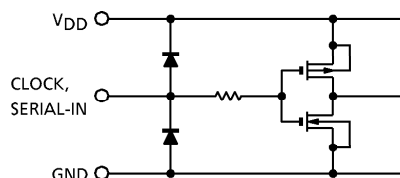
TRUTH TABLE

IN0~7	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	OUT0~7
L	L	L	OFF
H	L	L	OFF
L	H	L	OFF
H	H	L	ON
L		L	OFF
H		L	ON
H		H	OFF

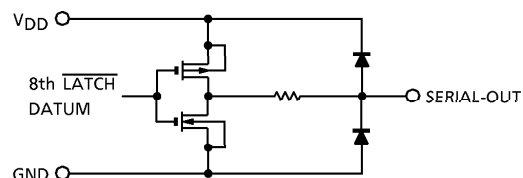
EQUIVALENT CIRCUIT OF INPUTS

1. $\overline{\text{ENABLE}}$ terminal2. $\overline{\text{LATCH}}$ terminal

3. CLOCK、SERIAL-IN terminal



4. SERIAL-OUT terminal

MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V
Output Current	I_O	90.0	mA
Output Voltage	V_O	$-0.3 \sim 17.0$	V
GND Terminal Current	I_{GND}	720	mA
Power Dissipation	P_D	780 (*)	mW
Operating Temperature	T_{opr}	$-40 \sim 85$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \sim 150$	$^\circ\text{C}$

(*) On PCB (50 × 50 × 1.6mm Cu 30% Glass Epoxy PCB)

Ambient temperature delated above 25°C in the proportion of $6.66\text{mW}/^\circ\text{C}$

RECOMMENDED OPERATING CONDITION (Ta = -40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{DD}	—	4.5	5.0	5.5	V
Output Voltage	V _O	—	—	—	15.0	V
Output Current	I _{OUT}	DC1 circuit	5.0	—	88	mA
	I _{OH}	SERIAL-OUT	—	—	-1.0	mA
	I _{OL}	SERIAL-OUT	—	—	1.0	mA
Input Voltage	V _{IH}	—	0.7 V _{DD}	—	V _{DD} + 0.3	V
	V _{IL}	—	-0.3	—	0.3 V _{DD}	
LATCH Pulse Width	t _w LAT	V _{DD} = 4.5V~5.5V	100	—	—	ns
	t _w LAT		100	—	—	
INPUT Pulse Width	t _w IN		4500	—	—	ns
	t _w IN		4500	—	—	
ENABLE Pulse Width	t _w EN		4500	—	—	ns
	t _w IN		4500	—	—	
Set-Up Time for LATCH	t _{setup} (L)		100	—	—	ns
Hold Time for ENABLE	t _{hold} (L)		100	—	—	ns
Power Dissipation	P _D	ON PCB, Ta = 85°C	—	—	0.60	W

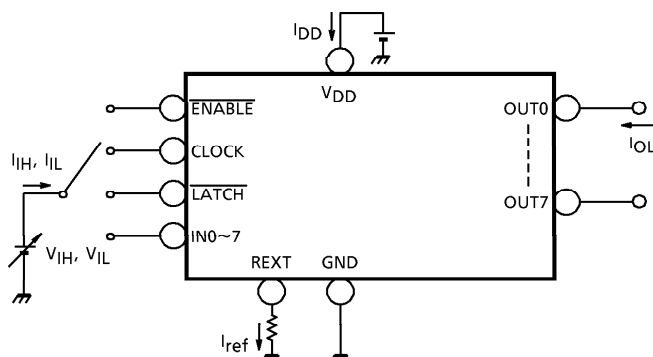
ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, Ta = 25°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}	—	0.7 V _{DD}	—	V _{DD}	V
	"L" Level	V _{IL}	—	GND	—	0.3 V _{DD}	
Output Leakage Current	I _{OH}	—	V _{OH} = 15.0V	—	—	10	μA
Output Voltage	SERIAL-OUT	V _{OL}	I _{OL} = 1.0mA	—	—	0.4	V
		V _{OH}	I _{OL} = -1.0mA	4.6	—	—	V
Output Current 1		I _{OL1}	V _{CE} = 0.7V, R _{EXT} = 620Ω	35.7	42.0	48.3	mA
		I _{OL2}	V _{CE} = 0.4V, (Include skew)	68.0	80.0	92.0	mA
	Current Skew	ΔI _{OL1}	I _O = 40mA, V _{CE} = 0.4V, R _{EXT} = 620Ω	—	±1.5	±6.0	%
Output Current 2		I _{OL3}	V _{CE} = 0.7V, R _{EXT} = 330Ω	64.2	75.5	86.8	mA
		I _{OL4}	V _{CE} = 0.7V, (Include skew)	63.8	75.0	86.2	mA
	Current Skew	ΔI _{OL2}	I _O = 75mA, V _{CE} = 0.7V, R _{EXT} = 330Ω	—	±1.5	±6.0	%
Supply Voltage Regulation	% / V _{DD}	—	R _{EXT} = 470Ω, Ta = -40~85°C	—	+5.0	—	% / V
Reference Voltage	V _{ref}	—	—	—	1.26	—	V
Supply Current "OFF"	I _{DD} (off) 1	—	R _{EXT} = OPEN, OUT1~8 = off, V _{DD} = 4.5V, ENABLE = "H"	—	0.6	1.2	mA
	I _{DD} (off) 2	—	R _{EXT} = 500Ω, OUT1~8 = off, V _{DD} = 4.5V, ENABLE = "H"	6.0	8.0	10.0	
	I _{DD} (off) 3	—	R _{EXT} = 280Ω, OUT1~8 = off, V _{DD} = 4.5V, ENABLE = "H"	12.0	15.0	18.0	
Supply Current "ON"	I _{DD} (on) 1	—	R _{EXT} = 500Ω, OUT1~8 = on, V _{DD} = 4.5V, ENABLE = "L"	8.0	13.0	20.0	mA
	I _{DD} (on) 2	—	R _{EXT} = 280Ω, OUT1~8 = on, V _{DD} = 4.5V, ENABLE = "L"	18.0	25.0	35.0	

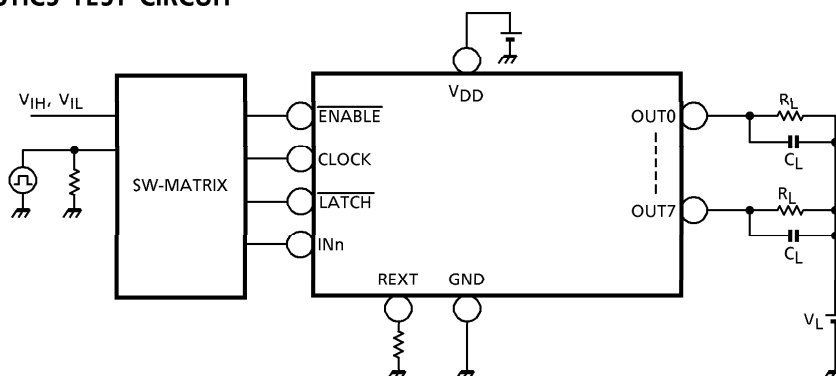
SWITCHING CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	IN-OUTn	t_{pLH}	—	$V_{DD} = 5.0V$ $V_{CE} = 0.4V$ $V_{IH} = V_{DD}$ $V_{IL} = 0V$ $R_{EXT} = 500\Omega$ $I_{OUT} = 40mA$ $V_L = 3.0V$ $R_L = 65\Omega$ $C_L = 10.5pF$	—	600	1200	ns
	LATCH-OUTn		—		—	600	1200	
	ENABLE-OUTn		—		—	600	1200	
Propagation Delay Time ("H" to "L")	IN-OUTn	t_{pHL}	—		—	300	1200	ns
	LATCH-OUTn		—		—	300	1200	
	ENABLE-OUTn		—		—	300	1200	
Pulse Width	IN	t_w IN, $\overline{IN}$	—		—	2000	3500	ns
	LATCH	t_w LAT, $\overline{LAT}$	—		—	25	50	
	ENABLE	t_w ENA, $\overline{ENA}$	—		—	2000	3500	
Set-Up Time for LATCH & CLOCK	L-H	t_{setup} $\overline{LAT}$	—		—	25	50	ns
	H-L		—		—	25	50	
Hold Time for LATCH & CLOCK	L-H	t_{hold} $\overline{LAT}$	—		—	0	15	ns
	H-L		—		—	0	15	
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs
Maximum CLOCK Fall Time		t_f	—		—	—	10	μs
Output Rise Time		t_{or}	—		200	1000	1200	ns
Output Fall Time		t_{of}	—		200	1000	1200	ns

DC CHARACTERISTICS TEST CIRCUIT



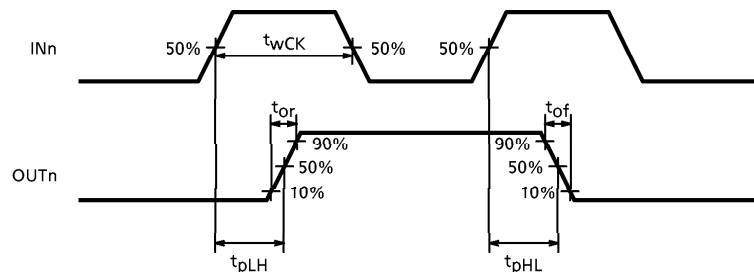
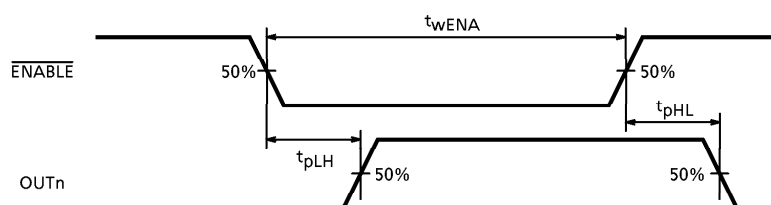
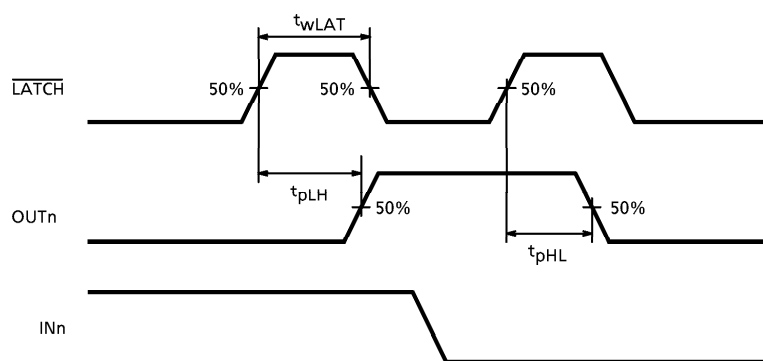
AC CHARACTERISTICS TEST CIRCUIT

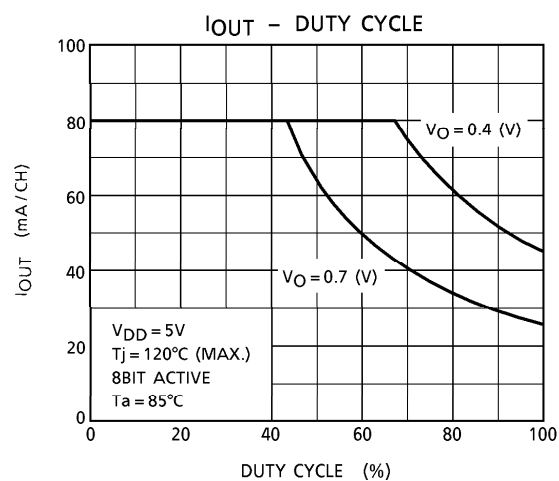
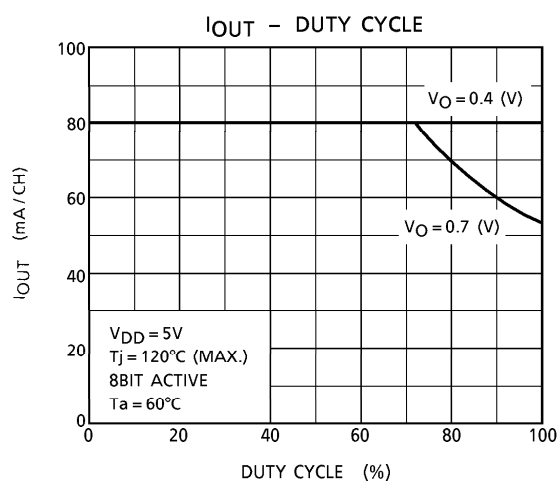
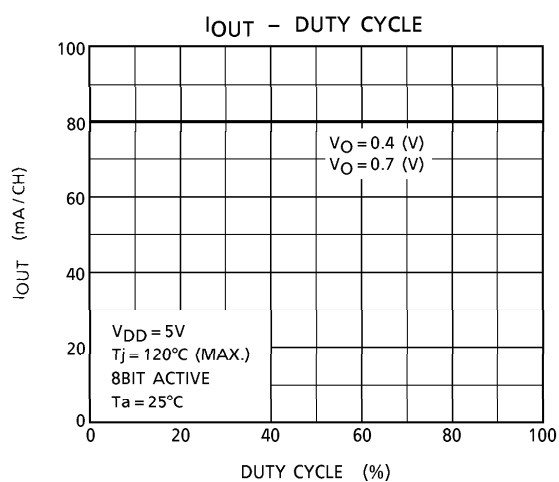


PRECAUTIONS for USING

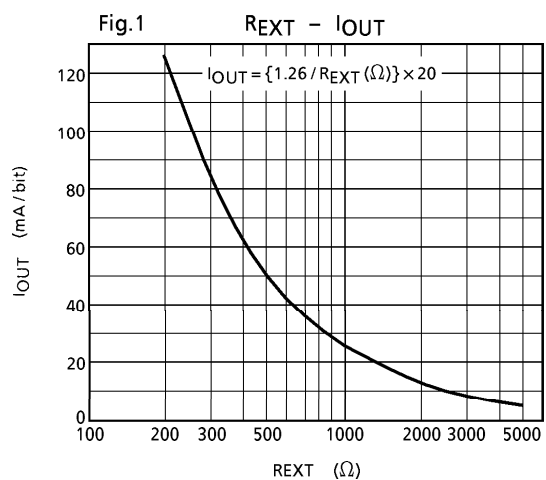
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND (L-GND, P-GND) line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

1. INn-OUTn 2. $\overline{\text{ENABLE}}\text{-OUTn}$ 3. $\overline{\text{LATCH}}\text{-OUTn}$ 



LED DRIVER TB6270X SERIES APPLICATION NOTE



[1] Output current (I_{OUT})

I_{OUT} is set by the external resistor (R-EXT) as shown in Fig.1.

[2] Total supply voltage (V_{LED})

This device can operate 0.4~0.7V (V_O).

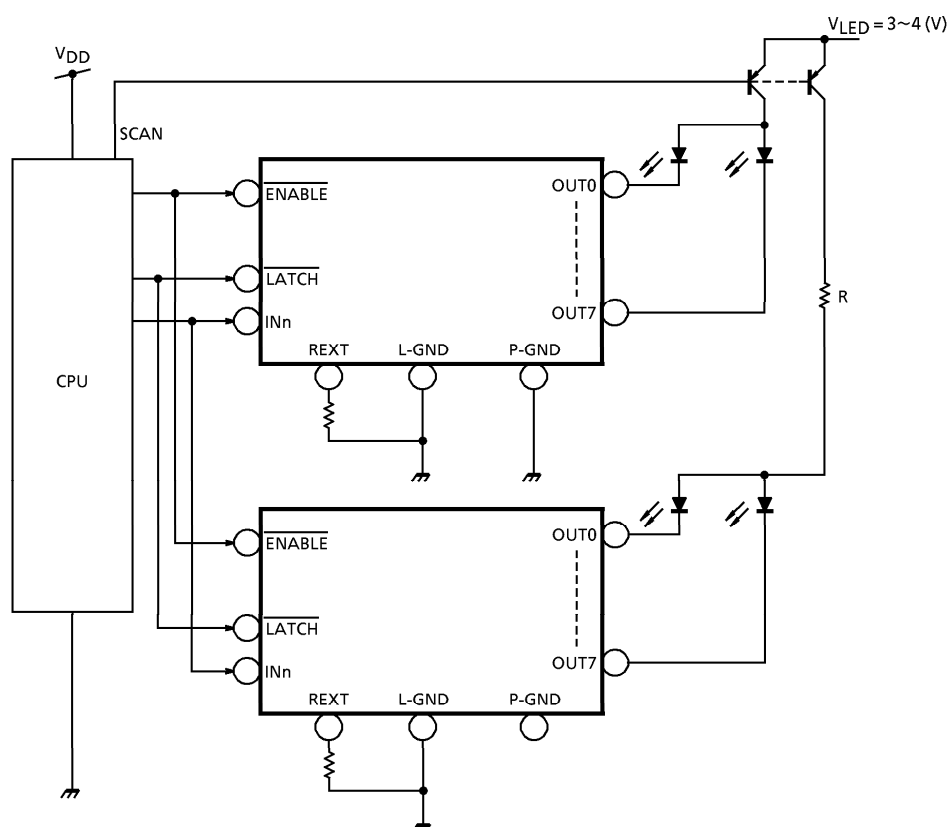
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.

In order to minimize power dissipation and loss, we would like to recommended to set the total supply voltage as shown below.

$$V_{LED} \text{ (Total supply voltage)} \\ = V_{CE} (Tr V_{sat}) + V_f \text{ (LED Forward voltage)} + V_O \text{ (IC supply voltage)}$$

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).

APPLICATION



[3] Pattern layout

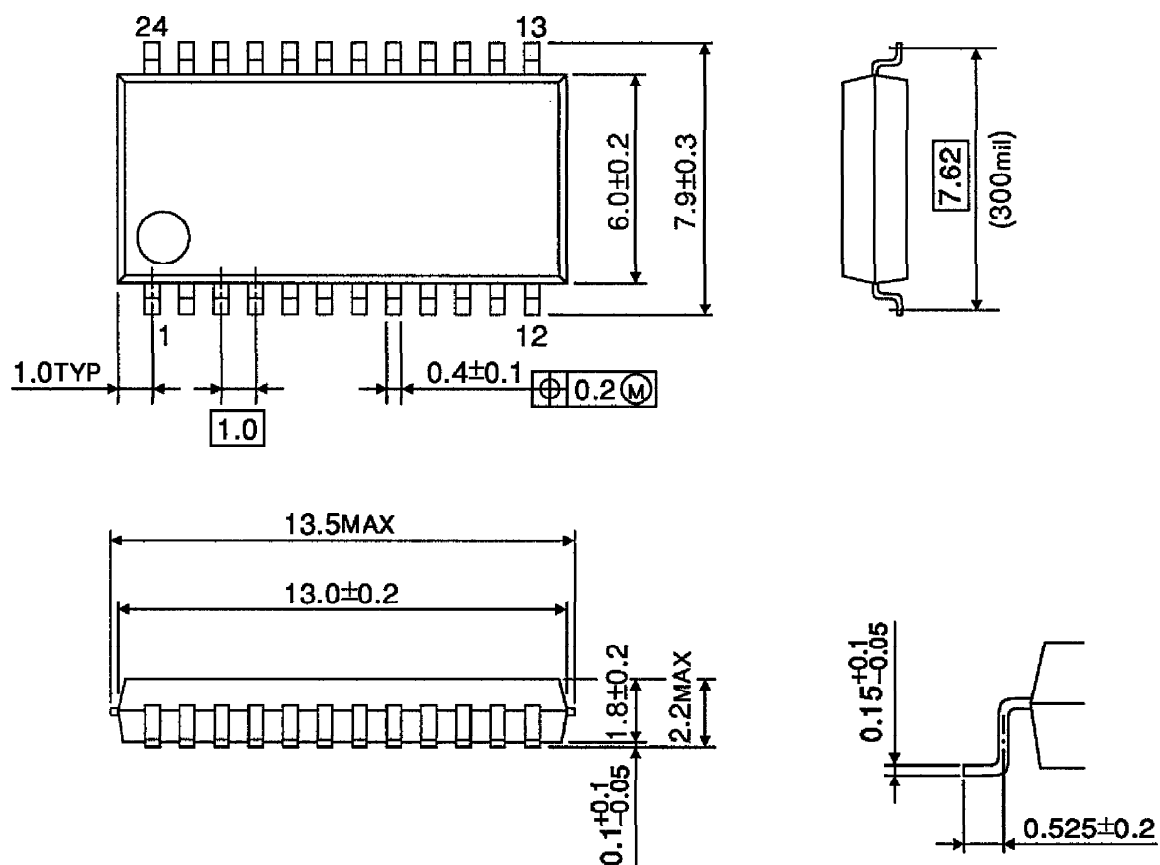
This device owns only one ground pin that means signal ground pin and power ground pin are common.

If ground pattern layout contains large inductance and impedance and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate. So we would like you to pay attention to pattern layout to minimize inductance.

OUTLINE DRAWING

SSOP24-P-300-1.00

Unit : mm



Weight : 0.32g (Typ.)