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TOSHIBA Field Effect Transistor Silicon P/N Channel MOS Type
(P Channel U-MOSII/N Channel U-MOSII)

TPC8403

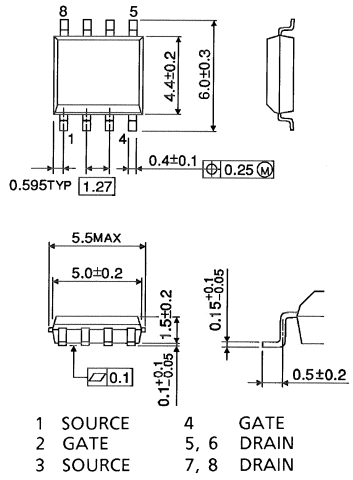
Motor Drive Applications

Notebook PC Applications

Portable Equipment Applications

- Low drain-source ON resistance: P Channel $R_{DS\ (ON)}$ = 45 mΩ (typ.)
  N Channel $R_{DS\ (ON)}$ = 25 mΩ (typ.)
- High forward transfer admittance: P Channel $|Y_{fs}|$ = 6.2 S (typ.)
  N Channel $|Y_{fs}|$ = 7.8 S (typ.)
- Low leakage current: P Channel I_{DSS} = −10 μA (V_{DS} = −30 V)
  N Channel I_{DSS} = 10 μA (V_{DS} = 30 V)
- Enhancement mode
  : P Channel V_{th} = −1.0~−2.2 V (V_{DS} = −10 V, I_D = −1 mA)
  : N Channel V_{th} = 1.3~2.5 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.080 g (typ.)

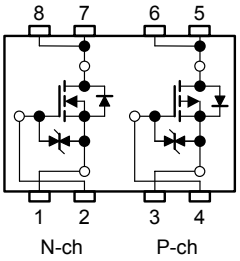
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating		Unit
			P Channel	N Channel	
Drain-source voltage		V_{DSS}	−30	30	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−30	30	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	DC (Note 1)	I_D	−4.5	6	A
	Pulse (Note 1)	I_{DP}	−18	24	
Drain power dissipation (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$P_{D(1)}$	1.5	1.5	W
	Single-device value at dual operation (Note 3b)	$P_{D(2)}$	1.1	1.1	
Drain power dissipation (t = 10s) (Note 2b)	Single-device operation (Note 3a)	$P_{D(1)}$	0.75	0.75	
	Single-device value at dual operation (Note 3b)	$P_{D(2)}$	0.45	0.45	
Single pulse avalanche energy		E_{AS}	26.3 (Note 4a)	46.8 (Note 4b)	mJ
Avalanche current		I_{AR}	−4.5	6	A
Repetitive avalanche energy Single-device value at operation (Note 2a, 3b, 5)		E_{AR}	0.11		mJ
Channel temperature		T_{ch}	150		°C
Storage temperature range		T_{stg}	−55~150		°C

Note 1, Note 2ab, Note 3ab, Note 4and Note 5: See the next page.

This transistor is an electrostatic-sensitive device. Please handle with caution.

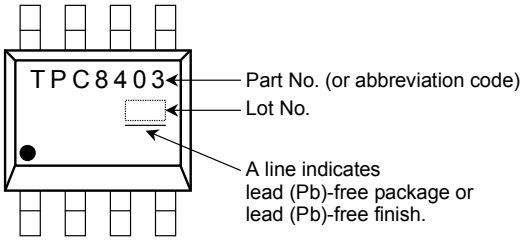
Circuit Configuration



Thermal Characteristics

Characteristics		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	114	
Thermal resistance, channel to ambient (t = 10s) (Note 2b)	Single-device operation (Note 2a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 2b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

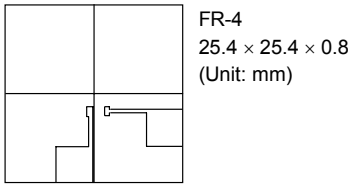
Marking



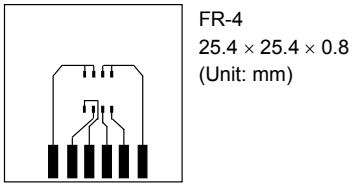
Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2:

a) Device mounted on a glass-epoxy board (a) b) Device mounted on a glass-epoxy board (b)



(a)



(b)

Note 3:

a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.).

b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.).

Note 4:

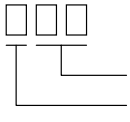
a) V_{DD} = −24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = −4.5 A

b) V_{DD} = 24 V, T_{ch} = 25°C (Initial), L = 1.0 mH, R_G = 25 Ω, I_{AR} = 6.0 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on lower left of the marking indicates Pin 1.

※ Weekly code: (Three digits)

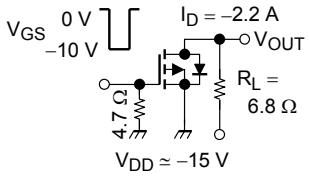


Week of manufacture
(01 for the first week of a year: sequential number up to 52 or 53)

Year of manufacture
(The last digit of a year)

P-channel

Electrical Characteristics (Ta = 25°C)

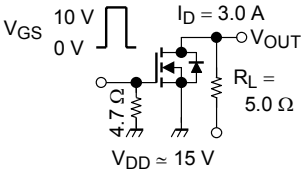
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = −30 V, V_{GS} = 0 V	—	—	−10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−30	—	—	V
		$V_{(BR)\ DSX}$	I_D = −10 mA, V_{GS} = 20 V	−15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−1.0	—	−2.2	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4.5 V, I_D = −2.2 A	—	66	90	mΩ
			V_{GS} = −10 V, I_D = −2.2 A	—	45	55	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.2 A	3.1	6.2	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	940	—	pF
Reverse transfer capacitance		C_{rss}		—	270	—	
Output capacitance		C_{oss}		—	390	—	
Switching time	Rise time	t_r	 Duty ≦ 1%, t_w = 10 μs	—	13	—	ns
	Turn-ON time	t_{on}		—	21	—	
	Fall time	t_f		—	25	—	
	Turn-OFF time	t_{off}		—	73	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ −24 V, V_{GS} = −10 V, I_D = −4.5 A	—	18	—	nC
Gate-source charge 1		$Q_{gs}1$		—	4	—	
Gate-drain (“miller”) charge		Q_{gd}		—	4	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	−18	A
Forward voltage (diode)		V_{DSF}	I_{DR} = −4.5 A, V_{GS} = 0 V	—	—	1.2	V

N-channel

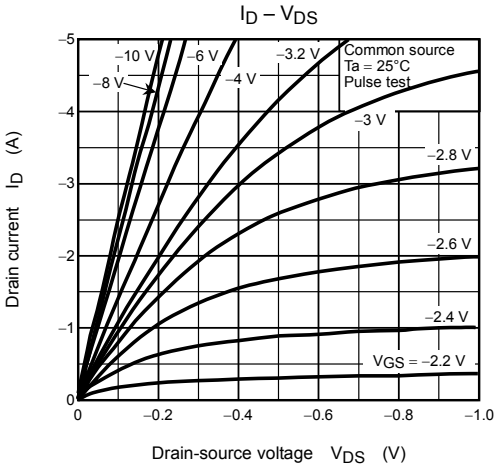
Electrical Characteristics (Ta = 25°C)

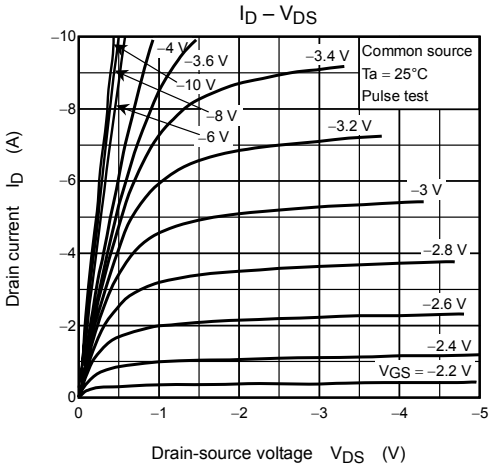
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-OFF current		I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	30	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	15	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.3	—	2.5	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 3 A	—	38	46	mΩ
			V_{GS} = 10 V, I_D = 3 A	—	25	33	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 3 A	3.9	7.8	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	850	—	pF
Reverse transfer capacitance		C_{rss}		—	180	—	
Output capacitance		C_{oss}		—	270	—	
Switching time	Rise time	t_r		—	11	—	ns
	Turn-ON time	t_{on}		—	18	—	
	Fall time	t_f		—	6.5	—	
	Turn-OFF time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	27	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≃ 24 V, V_{GS} = 10 V, I_D = 6 A	—	17	—	nC
Gate-source charge 1		$Q_{gs}1$		—	3	—	
Gate-drain (“miller”) charge		Q_{gd}		—	4	—	

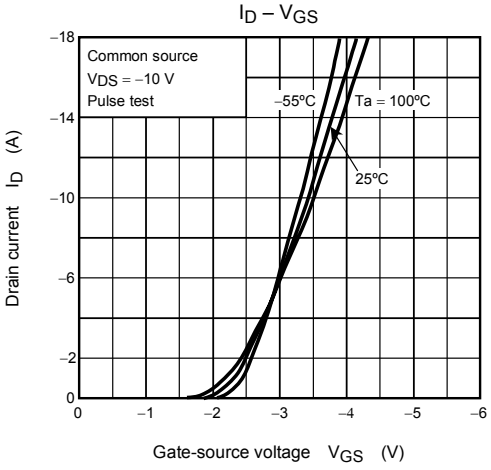
Source-Drain Ratings and Characteristics (Ta = 25°C)

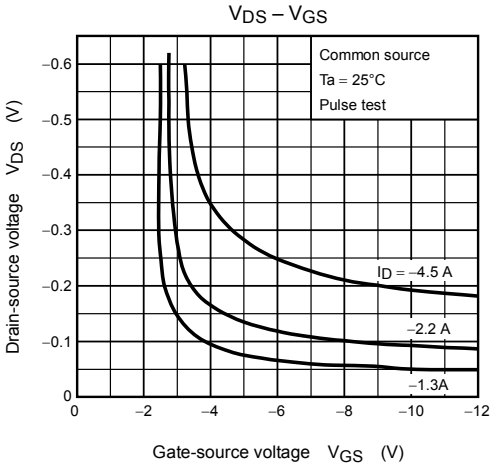
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	24	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 6 A, V_{GS} = 0 V	—	—	−1.2	V

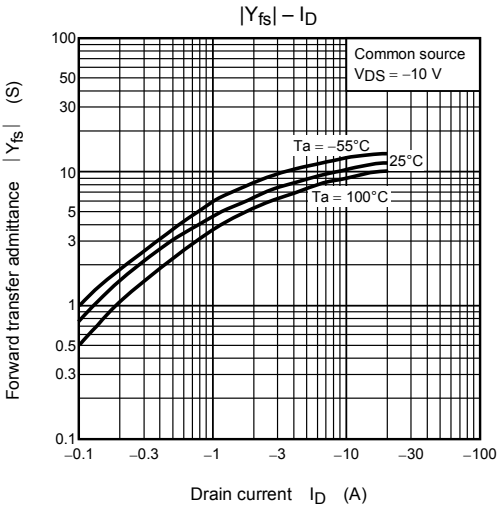
P-channel

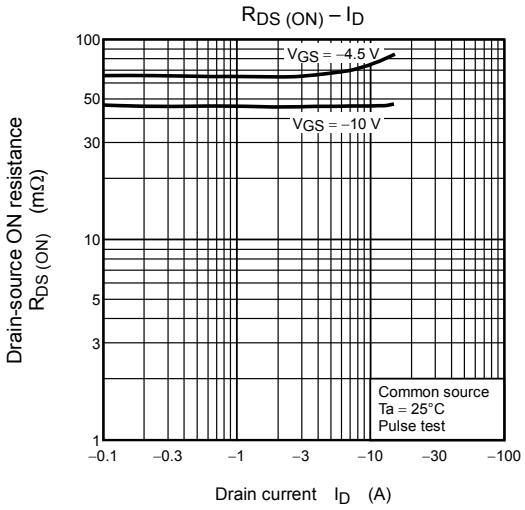

$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
−10 V
−8 V
−6 V
−4 V
−3.2 V
−3 V
−2.8 V
−2.6 V
−2.4 V
V_{GS} = −2.2 V
Drain current I_D (A)
Drain-source voltage V_{DS} (V)


$I_D - V_{DS}$
Common source
Ta = 25°C
Pulse test
−4 V
−3.6 V
−10 V
−8 V
−6 V
−3.4 V
−3.2 V
−3 V
−2.8 V
−2.6 V
−2.4 V
V_{GS} = −2.2 V
Drain current I_D (A)
Drain-source voltage V_{DS} (V)


$I_D - V_{GS}$
Common source
V_{DS} = −10 V
Pulse test
−55°C
Ta = 100°C
25°C
Drain current I_D (A)
Gate-source voltage V_{GS} (V)

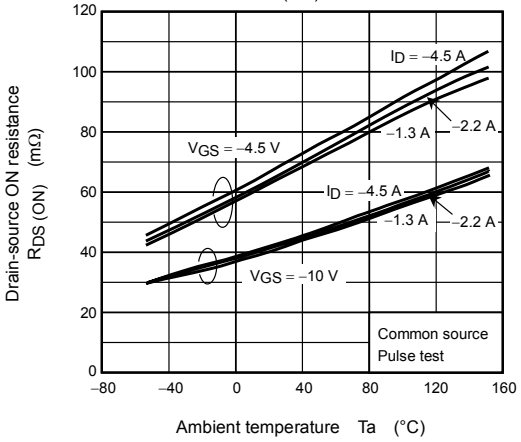

$V_{DS} - V_{GS}$
Common source
Ta = 25°C
Pulse test
I_D = −4.5 A
−2.2 A
−1.3A
Drain-source voltage V_{DS} (V)
Gate-source voltage V_{GS} (V)


$|Y_{fs}| - I_D$
Common source
V_{DS} = −10 V
Ta = −55°C
25°C
Ta = 100°C
Forward transfer admittance $|Y_{fs}|$ (S)
Drain current I_D (A)

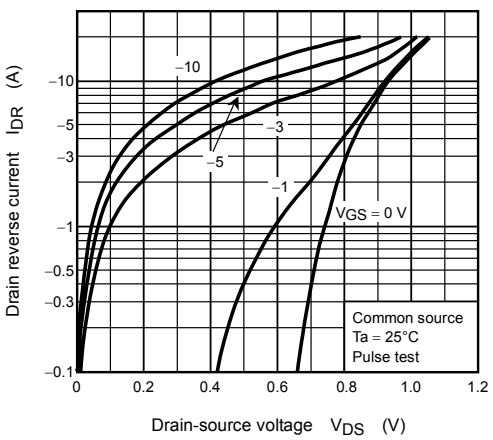

$R_{DS\ (ON)} - I_D$
V_{GS} = −4.5 V
V_{GS} = −10 V
Common source
Ta = 25°C
Pulse test
Drain-source ON resistance $R_{DS\ (ON)}$ (mΩ)
Drain current I_D (A)

P-channel

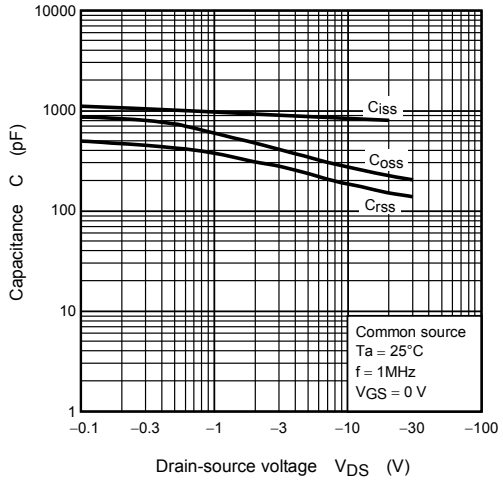
$R_{DS\ (ON)}$ – Ta



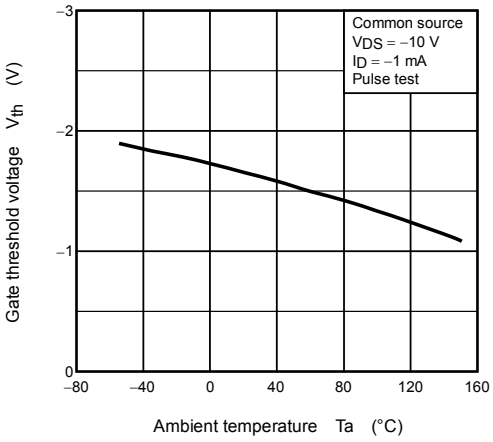
I_{DR} – V_{DS}



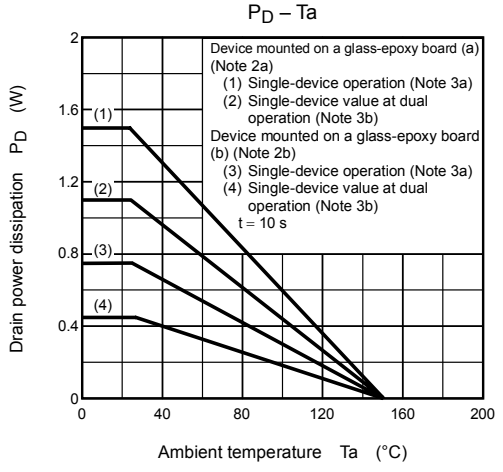
Capacitance – V_{DS}



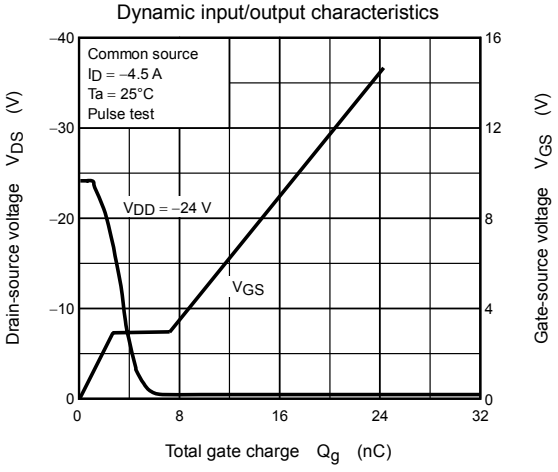
V_{th} – Ta



P_D – Ta

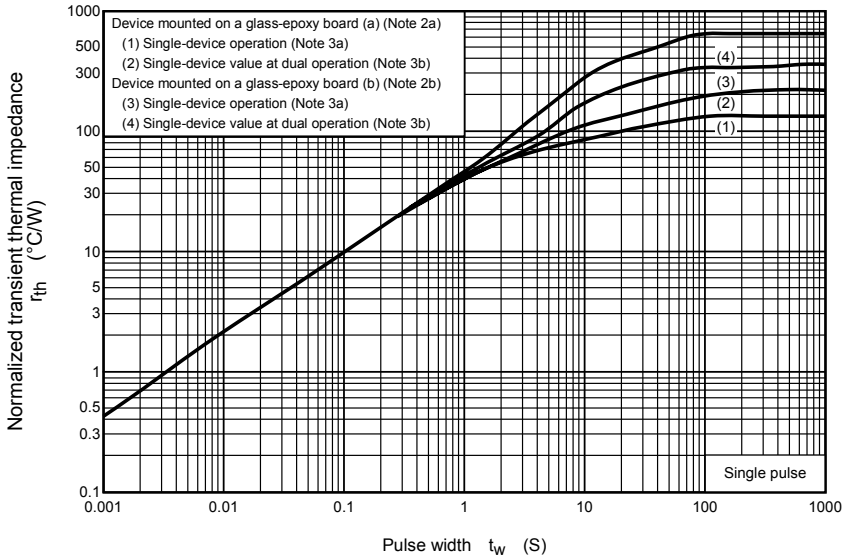


Dynamic input/output characteristics

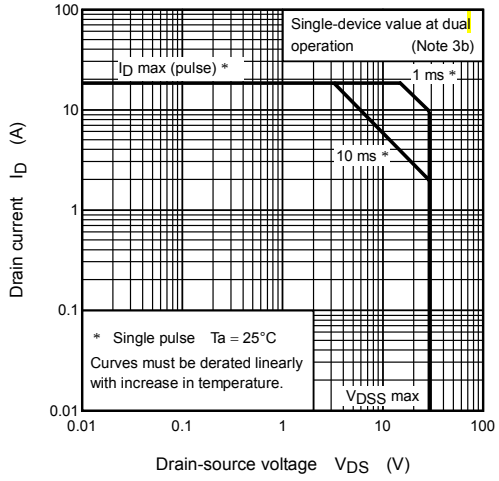


P-channel

$r_{th} - t_w$

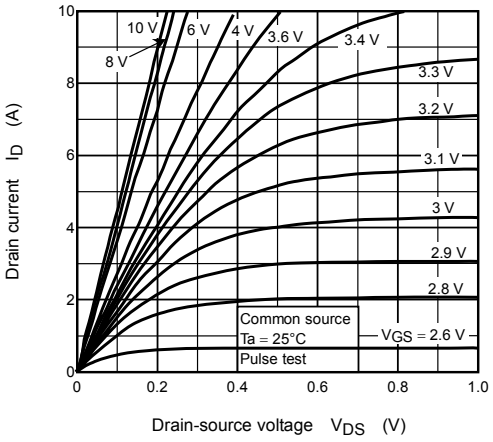


Safe operating area

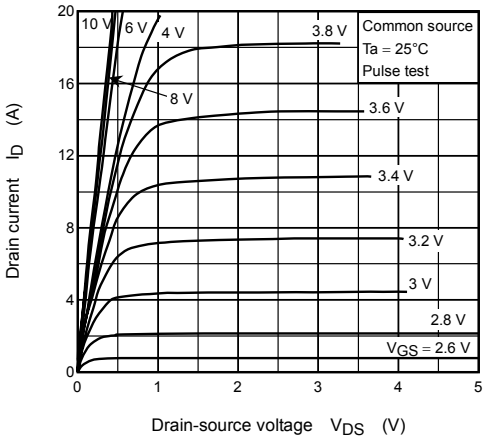


N-channel

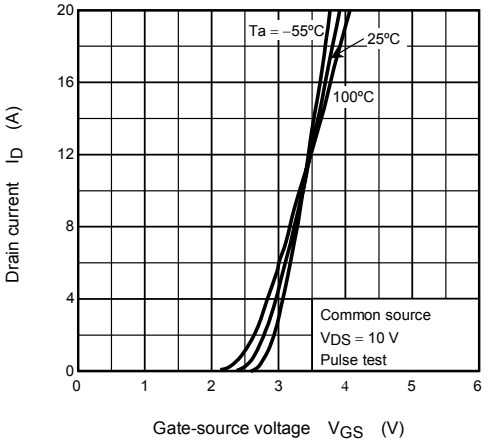
$I_D - V_{DS}$



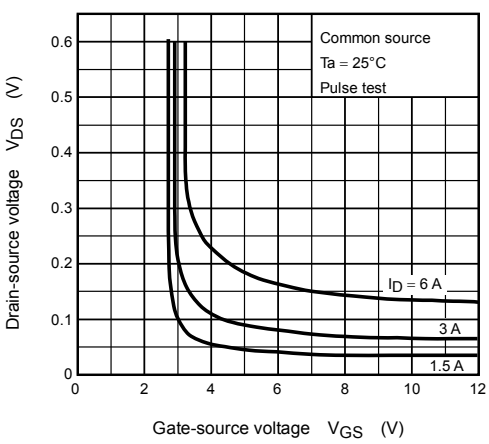
$I_D - V_{DS}$



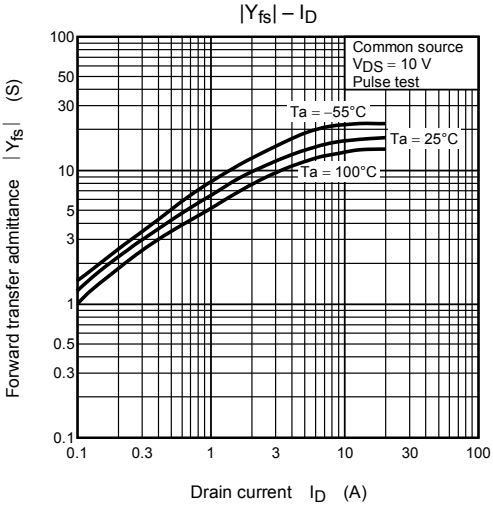
$I_D - V_{GS}$



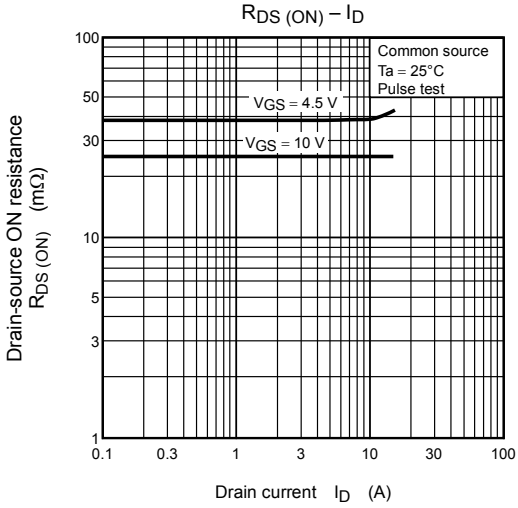
$V_{DS} - V_{GS}$



$|Y_{fs}| - I_D$

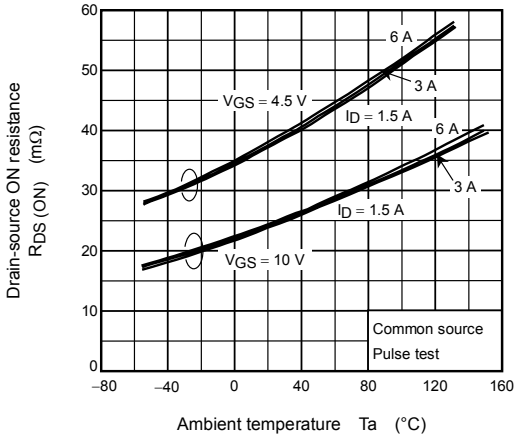


$R_{DS\ (ON)} - I_D$

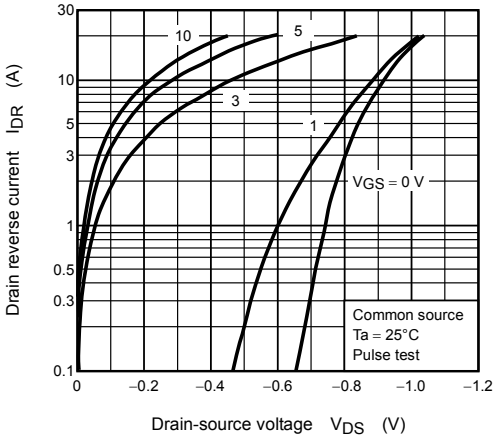


N-channel

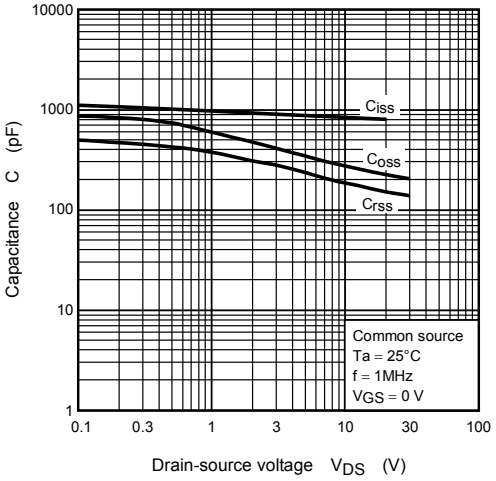
$R_{DS\ (ON)}$ – Ta



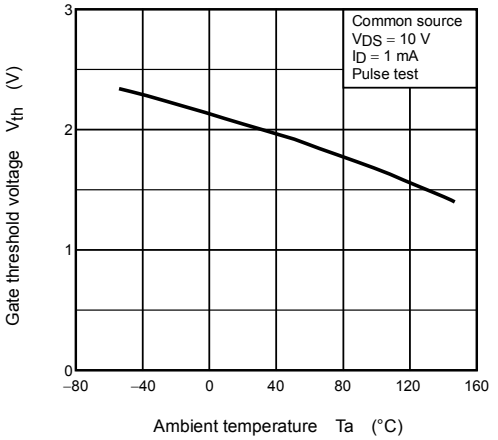
I_{DR} – V_{DS}



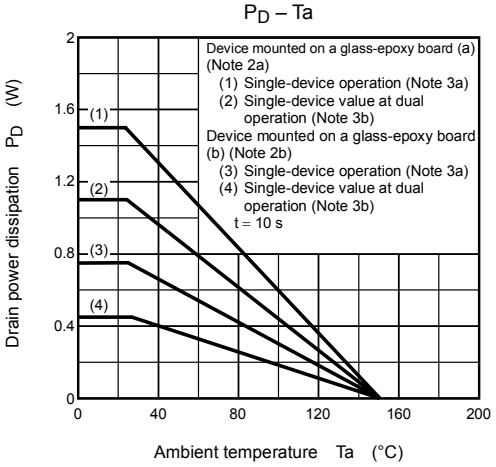
Capacitance – V_{DS}



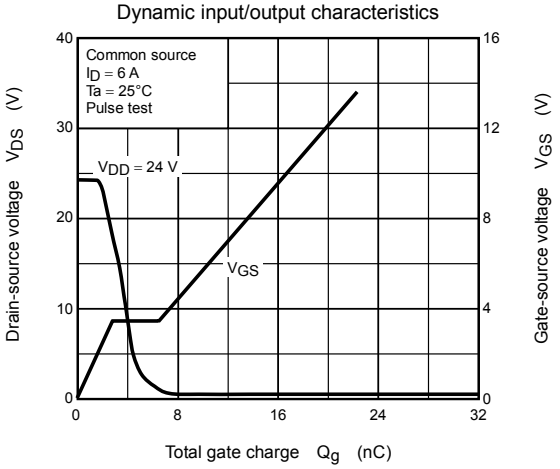
V_{th} – Ta



P_D – Ta

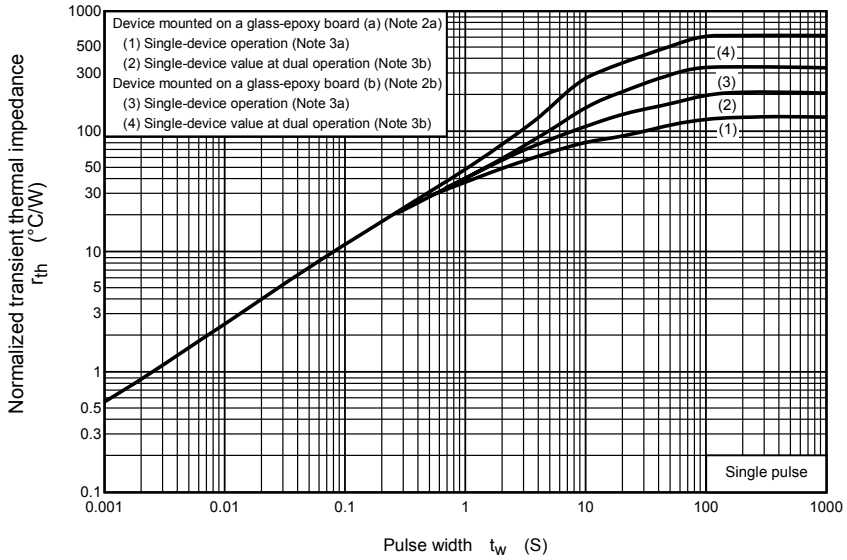


Dynamic input/output characteristics

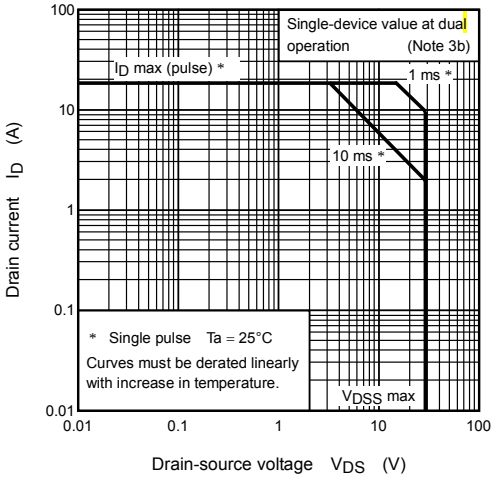


N-channel

$r_{th} - t_w$



Safe operating area



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