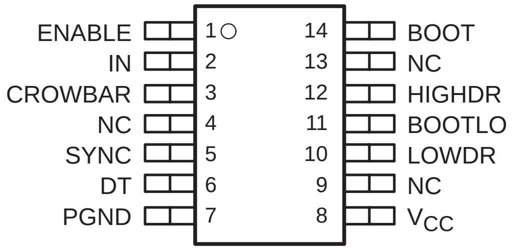
查询TPS2830供应商

TPS2830, TPS2831
FAST SYNCHRONOUS-BUCK MOSFET DRIVERS WITH DEADTIME CONTROL

SLVS196B – JANUARY1999 – REVISED SEPTEMBER 1999

- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Active Deadtime Control**
- **50-ns Max Rise/Fall Times and 100-ns Max Propagation Delay — 3-nF Load**
- **Ideal for High-Current Single or Mutiphase Applications**
- **2.4-A Typ Peak Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **Internal Schottky Bootstrap Diode**
- **SYNC Control for Synchronous or Nonsynchronous Operation**
- **CROWBAR for OVP, Protects Against Faulted High-Side Power FETs**
- **Low Supply Current . . . 3-mA Typ**
- **–40°C to 125°C Junction-Temperature Operating Range**

D OR PWP PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TPS2830 and TPS2831 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using a switching controller that does not include suitable MOSFET drivers on the chip. The drivers are designed to deliver 2.4-A peak currents into large capacitive loads. Higher currents can be controlled by using multiple drivers in a multiphase configuration. The high-side driver can be configured as a ground-reference driver or as a floating bootstrap driver. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, and provides high efficiency for the buck regulator. The TPS2830/31 drivers have additional control functions: ENABLE, SYNC, and CROWBAR. Both drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for over-voltage protection against faulted high-side power FETs.

The TPS2830 has a noninverting input. The TPS2831 has an inverting input. The TPS2830/31 drivers are available in 14-terminal SOIC and TSSOP packages and operate over a junction temperature range of –40°C to 125°C.

AVAILABLE OPTIONS

T_J	PACKAGED DEVICES	
	SOIC (D)	**TSSOP (PWP)**
–40°C to 125°C	TPS2830D TPS2831D	TPS2830PWP TPS2831PWP

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2830DR)

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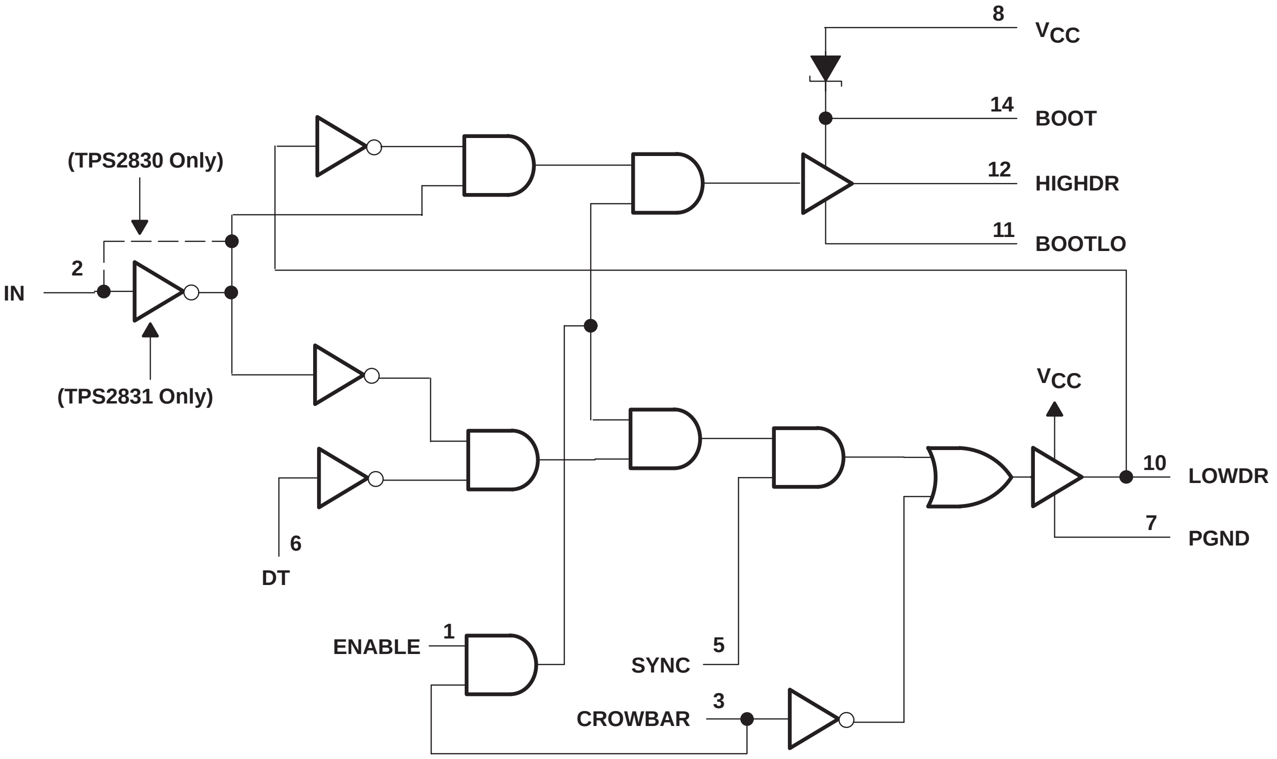
functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT	14	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO terminals to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 μF and 1 μF. A 1-MΩ resistor should be connected across the bootstrap capacitor to provide a discharge path when the driver has been powered down.
BOOTLO	11	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
CROWBAR	3	I	CROWBAR can to be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals.
DT	6	I	Deadtime control terminal. Connect DT to the junction of the high-side and low-side MOSFETs.
ENABLE	1	I	If ENABLE is low, both drivers are off.
HIGHDR	12	O	Output drive for the high-side power MOSFET
IN	2	I	Input signal to the MOSFET drivers (noninverting input for the TPS2830; inverting input for the TPS2831).
LOWDR	10	O	Output drive for the low-side power MOSFET
NC	4, 9, 13		
PGND	7		Power ground. Connect to the FET power ground
SYNC	5	I	Synchronous Rectifier Enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V_{CC}	8	I	Input supply. Recommended that a 1-μF capacitor be connected from V_{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low Rds(on) N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

deadtime (DT) control†

Deadtime control prevents shoot through current from flowing through the main power FETs during switching transitions by controlling the turn-on times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrn) is low; the DT terminal connects to the junction of the power FETs.

ENABLE†

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low.

IN†

The IN terminal is the input control signal for the drivers. The TPS2830 has a noninverting input; the TPS2831 has an inverting input.

SYNC†

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off.

CROWBAR†

The CROWBAR terminal overrides the normal operation of the driver. When the CROWBAR terminal is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against over voltages due to a short across the high-side FET. V_{IN} should be fused to protect the low-side FET.

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† High-level input voltages on ENABLE, SYNC, CROWBAR, IN, and DT must be greater than or equal to V_{CC}.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		–0.3 V to 16 V
Input voltage range:	BOOT to PGND (high-side driver ON)	–0.3 V to 30 V
	BOOTLO to PGND	–0.3 V to 16 V
	BOOT to BOOTLO	–0.3 V to 16 V
	ENABLE, SYNC, and CROWBAR (see Note 2)	–0.3 V to 16 V
	IN (see Note 2)	–0.3 V to 16 V
	DT (see Note 2)	–0.3 V to 30 V
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		–40°C to 125°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Unless otherwise specified, all voltages are with respect to PGND.
2. High-level input voltages on the ENABLE, SYNC, CROWBAR, IN, and DT terminals must be greater than or equal to V_{CC}.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	760 mW	7.6 mW/°C	420 mW	305 mW
PWP	2400 mW	25 mW/°C	1275 mW	900 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		15	V
Input voltage	BOOT to PGND	4.5		28	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		4.5		15	V
V_{CC}	Quiescent current	V_{ENABLE} = LOW, V_{CC} =15 V			100	µA
		V_{ENABLE} = HIGH, V_{CC} =15 V		0.1		mA
		V_{ENABLE} = HIGH, V_{CC} =12 V, f_{SWX} = 200 kHz, BOOTLO grounded, C_{HIGHDR} = 50 pF, C_{LOWDR} = 50 pF, See Note 3		3		

NOTE 3: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

output drivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output-current	High-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V	0.7	1.1		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 5 V	1.1	1.5		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 10.5 V	2	2.4		
	High-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5V	1.2	1.4		A
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 1.5 V	1.3	1.6		
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 1.5 V	2.3	2.7		
	Low-side sink (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 4 V	1.3	1.8		A
			V_{CC} = 6.5 V, V_{LOWDR} = 5 V	2	2.5		
			V_{CC} = 12 V, V_{LOWDR} = 10.5 V	3	3.5		
	Low-side source (see Note 4)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 3)	V_{CC} = 4.5 V, V_{LOWDR} = 0.5V	1.4	1.7		A
			V_{CC} = 6.5 V, V_{LOWDR} = 1.5 V	2	2.4		
			V_{CC} = 12 V, V_{LOWDR} = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 0.5 V			5	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 0.5 V			5	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} = 0.5 V			5	
	High-side source (see Note 4)		$V_{BOOT} - V_{BOOTLO}$ = 4.5 V, V_{HIGHDR} = 4 V			45	Ω
			$V_{BOOT} - V_{BOOTLO}$ = 6.5 V, V_{HIGHDR} = 6 V			45	
			$V_{BOOT} - V_{BOOTLO}$ = 12 V, V_{HIGHDR} =11.5 V			45	
	Low-side sink (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 0.5 V			9	Ω
			V_{DRV} = 6.5 V V_{LOWDR} = 0.5 V			7.5	
			V_{DRV} = 12 V, V_{LOWDR} = 0.5 V			6	
	Low-side source (see Note 4)		V_{DRV} = 4.5 V, V_{LOWDR} = 4 V			45	Ω
			V_{DRV} = 6.5 V, V_{LOWDR} = 6 V			45	
			V_{DRV} = 12 V, V_{LOWDR} = 11.5 V			45	

NOTES: 3. Ensured by design, not production tested.

4. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the Rds(on) of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

deatime control

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOWDR	High-level input voltage	Over the V_{CC} range (see Note 3)	2			V
	Low-level input voltage				1	V
DT	High-level input voltage	Over the V_{CC} range	2			V
	Low-level input voltage				1	V

NOTE 3: Ensured by design, not production tested.

digital control terminals

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	Over the V_{CC} range	2			V
Low-level input voltage				1	V

switching characteristics over recommended operating virtual junction temperature range, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V, V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Fall time	HIGHDR output (see Note 3)	V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V			60	ns
		V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V			50	
		V_{BOOT} = 12 V, V_{BOOTLO} = 0 V			50	
	LOWDR output (see Note 3)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Propagation delay time	HIGHDR going low (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V			130	ns
		V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V			100	
		V_{BOOT} = 12 V, V_{BOOTLO} = 0 V			75	
	LOWDR going high (excluding deadtime) (see Note 3)	V_{BOOT} = 4.5 V, V_{BOOTLO} = 0 V			80	ns
		V_{BOOT} = 6.5 V, V_{BOOTLO} = 0 V			70	
		V_{BOOT} = 12 V, V_{BOOTLO} = 0 V			60	
Propagation delay time	LOWDR going low (excluding deadtime) (see Note 3)	V_{CC} = 4.5 V			80	ns
		V_{CC} = 6.5 V			70	
		V_{CC} = 12 V			60	
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 3)	V_{CC} = 4.5 V	40		170	ns
		V_{CC} = 6.5 V	25		135	
		V_{CC} = 12 V	15		85	

NOTE 3: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

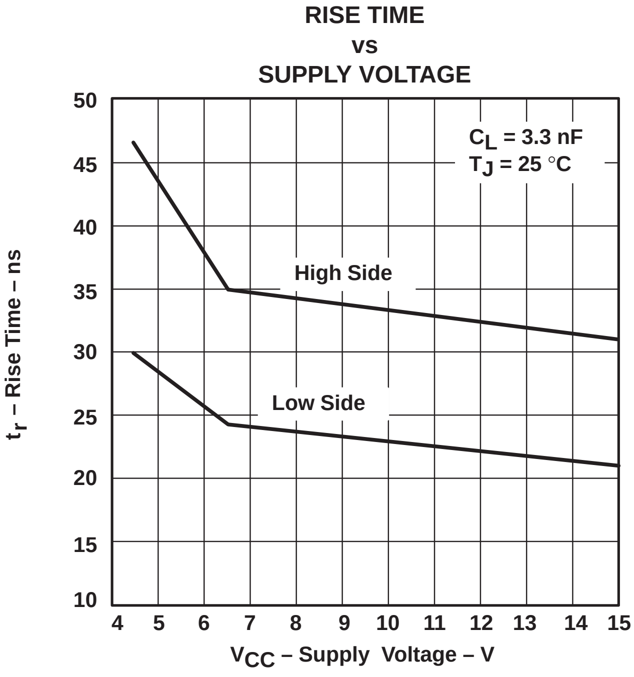


Figure 1

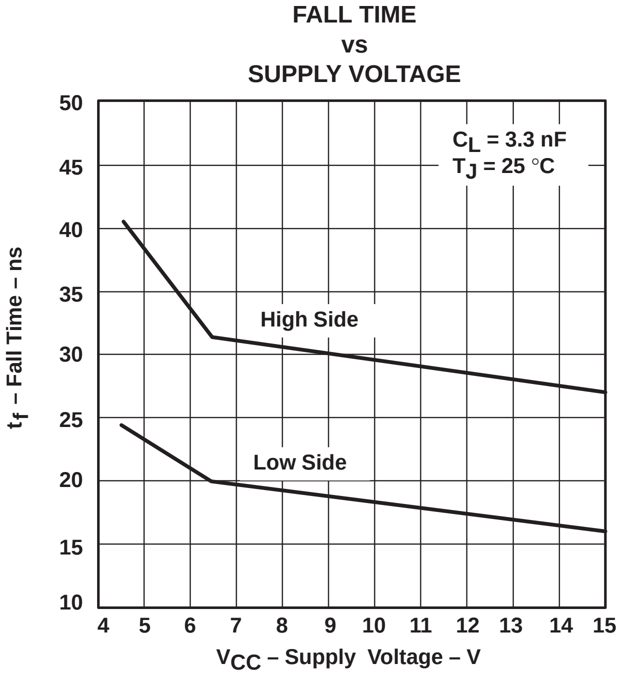


Figure 2

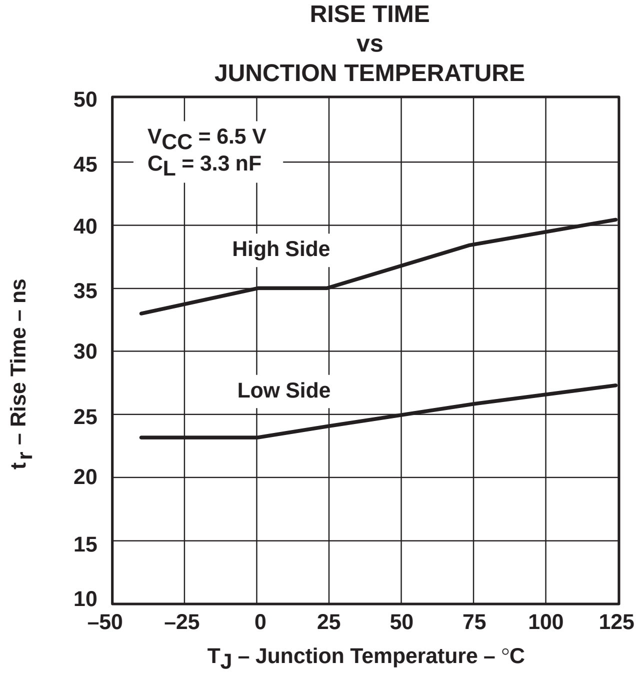


Figure 3

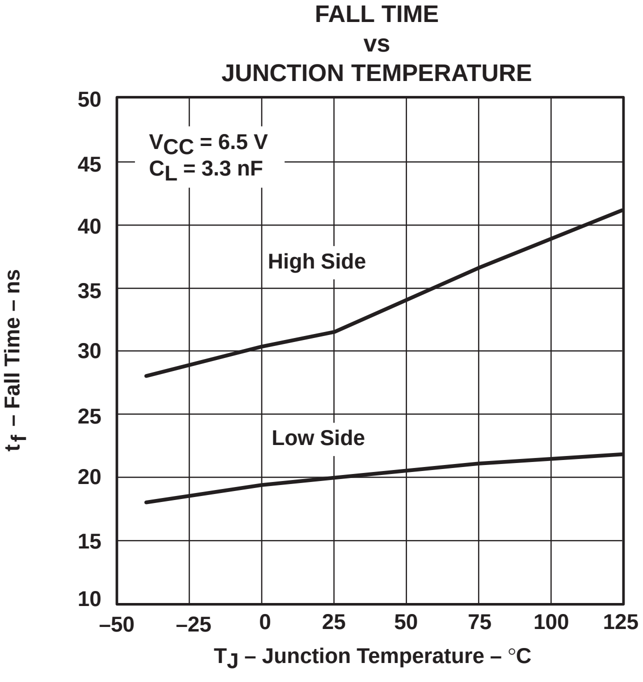


Figure 4

TYPICAL CHARACTERISTICS

LOW-TO-HIGH PROPAGATION DELAY TIME vs SUPPLY VOLTAGE, LOW TO HIGH LEVEL

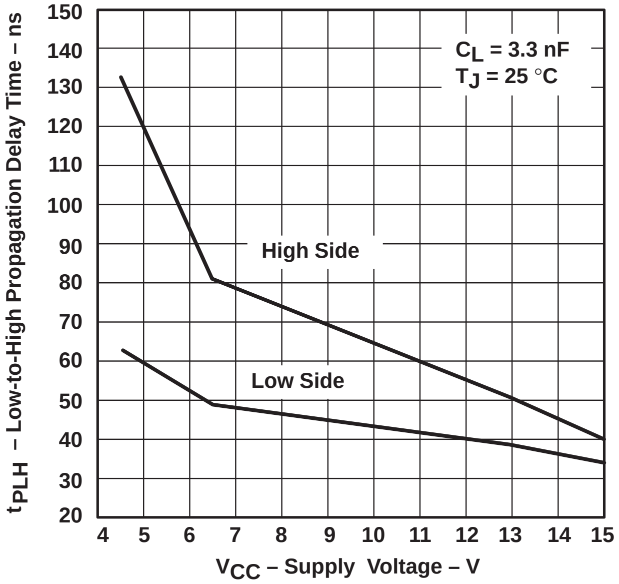


Figure 5

HIGH-TO-LOW PROPAGATION DELAY TIME vs SUPPLY VOLTAGE, HIGH TO LOW LEVEL

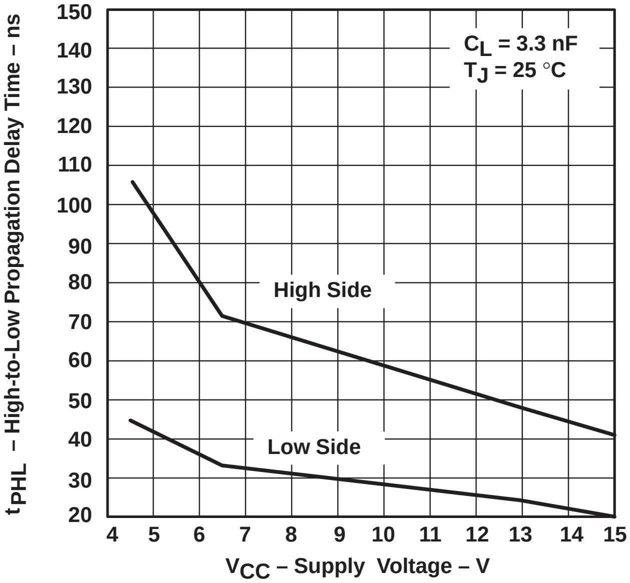


Figure 6

LOW-TO-HIGH PROPAGATION DELAY TIME vs JUNCTION TEMPERATURE

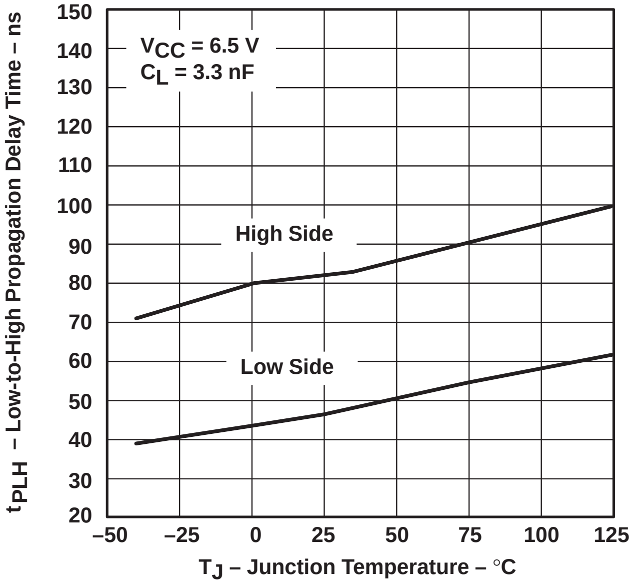


Figure 7

HIGH-TO-LOW PROPAGATION DELAY TIME vs JUNCTION TEMPERATURE

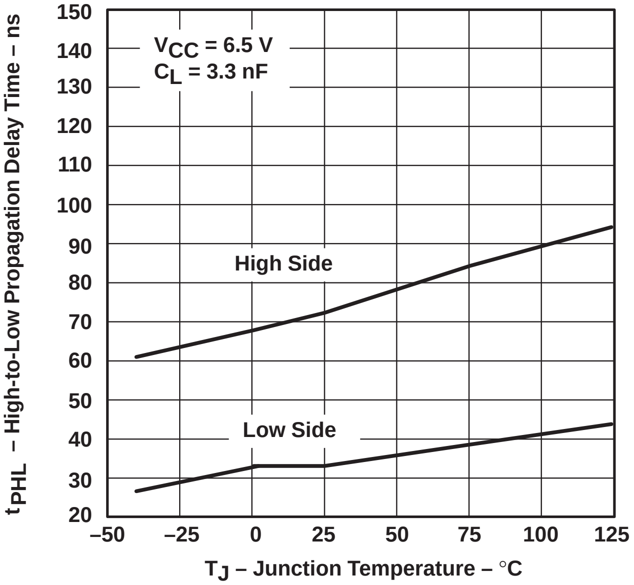


Figure 8

TYPICAL CHARACTERISTICS

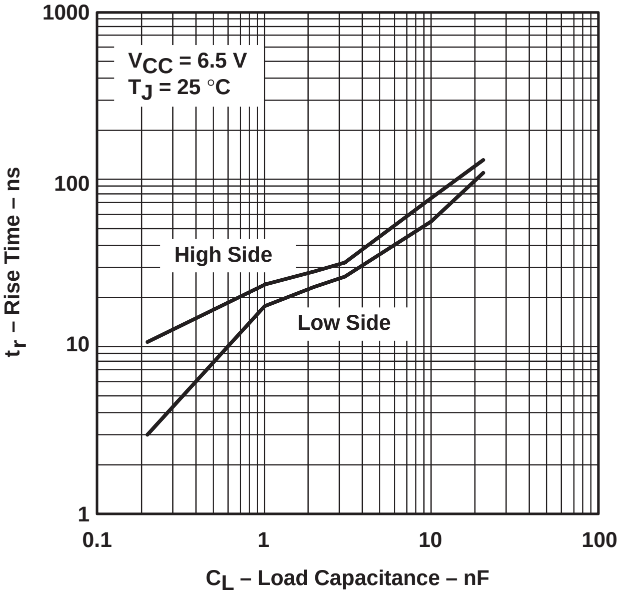

RISE TIME
vs
LOAD CAPACITANCE

Figure 9

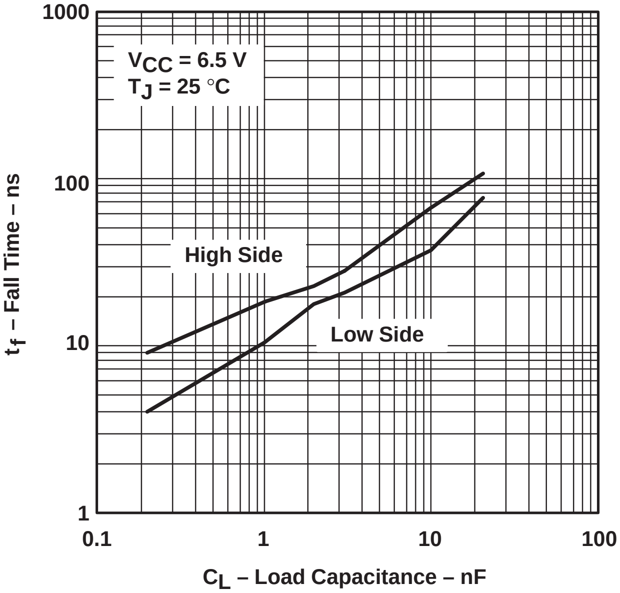

FALL TIME
vs
LOAD CAPACITANCE

Figure 10

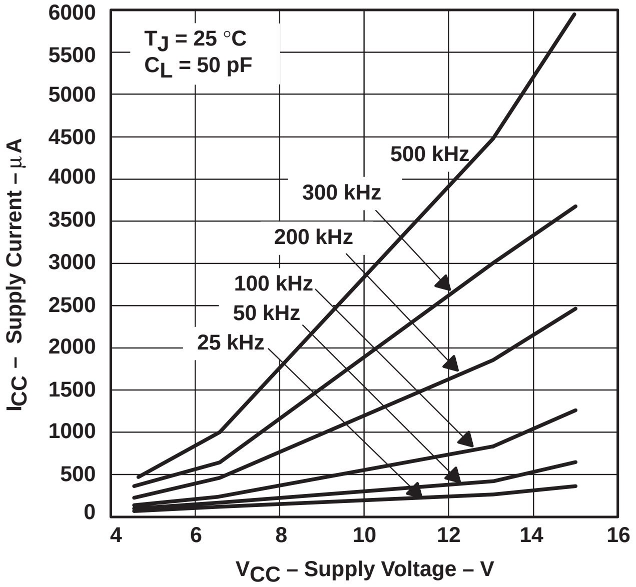

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 11

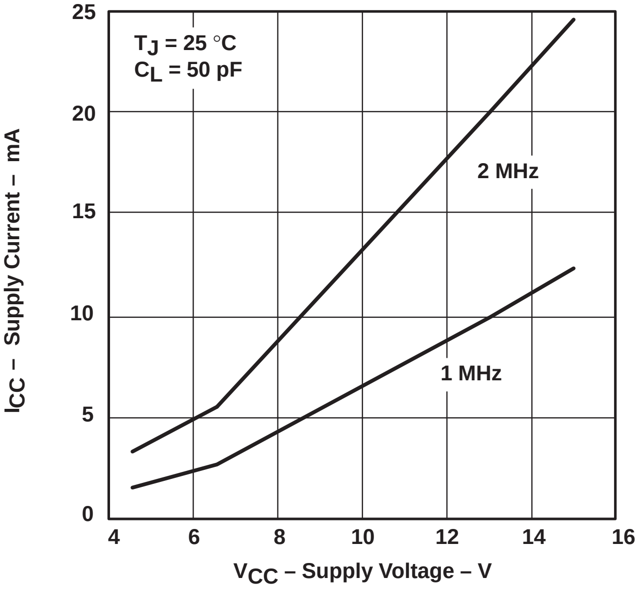

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 12

TYPICAL CHARACTERISTICS

PEAK SOURCE CURRENT vs DRIVE VOLTAGE

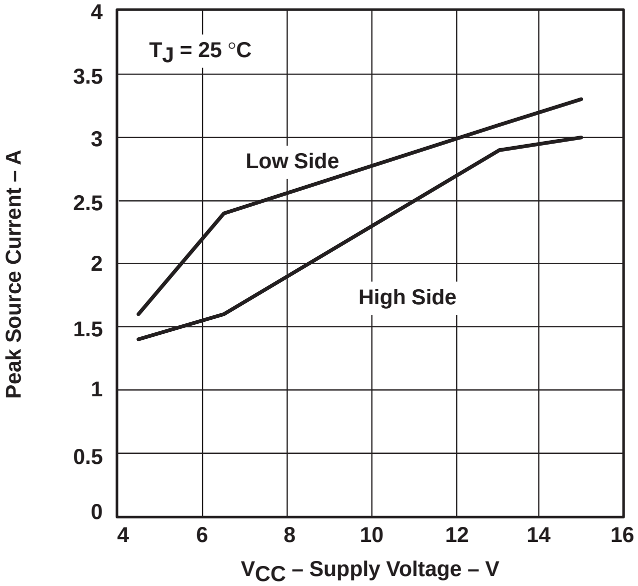


Figure 13

PEAK SINK CURRENT vs DRIVE VOLTAGE

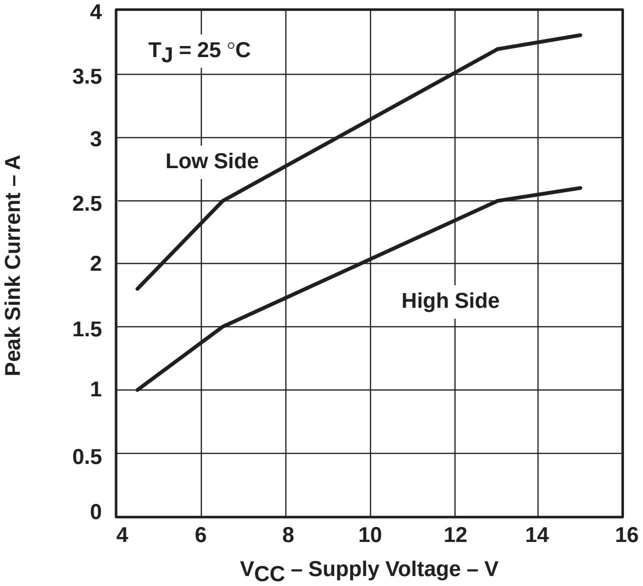


Figure 14

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

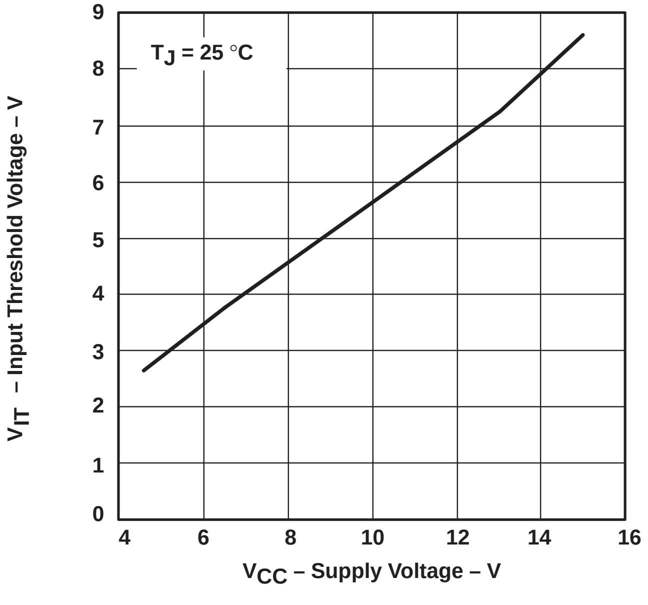


Figure 15

APPLICATION INFORMATION

Figure 15 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2831 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_{load}=1 A, and 93% for V_{in} = 5 V, I_{load} = 3 A.

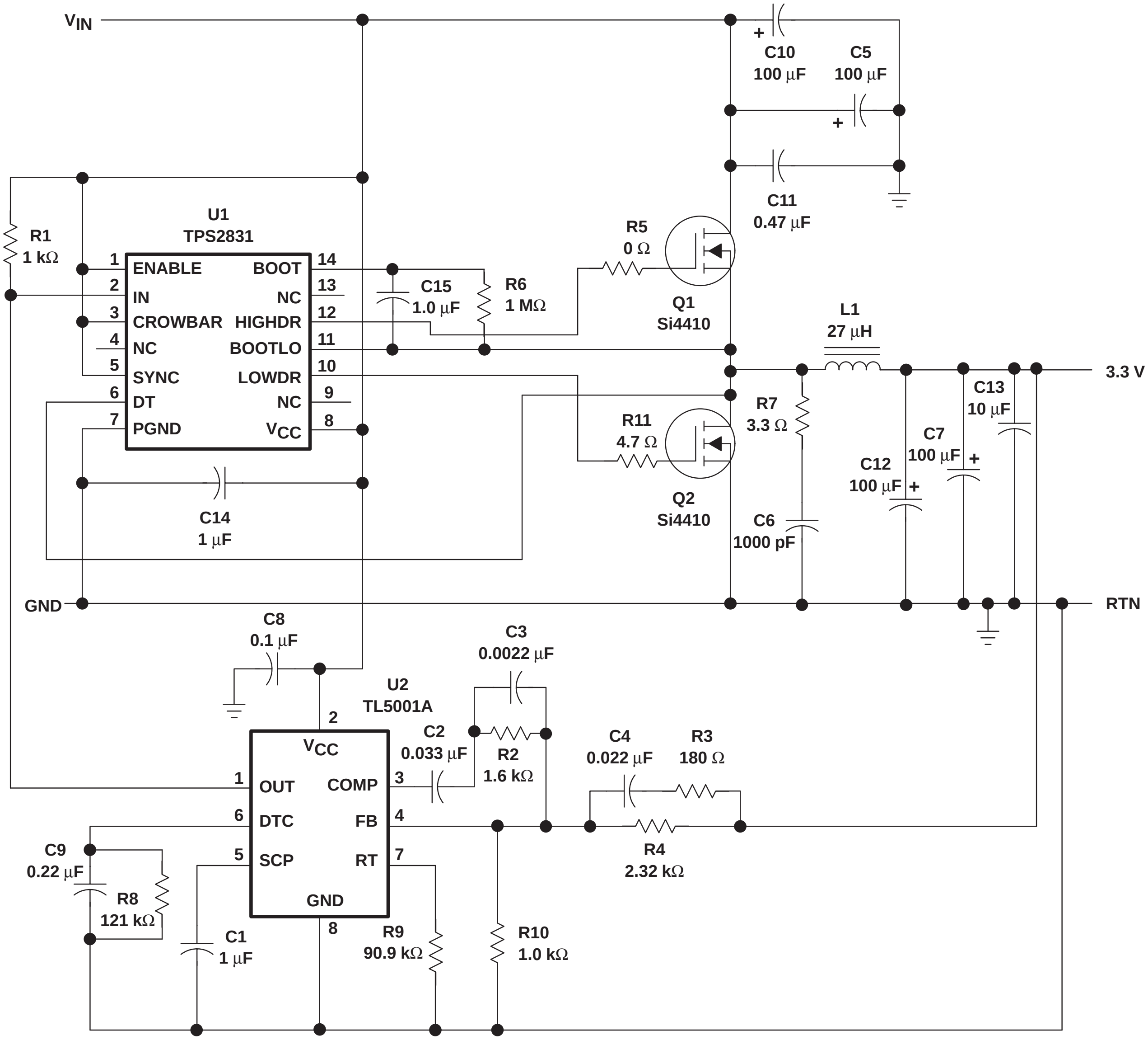

VIN
C10
100 µF
C5
100 µF
C11
0.47 µF
R1
1 kΩ
U1
TPS2831
1 ENABLE
2 IN
3 CROWBAR
4 NC
5 SYNC
6 DT
7 PGND
14 BOOT
13 NC
12 HIGHDR
11 BOOTLO
10 LOWDR
9 NC
8 VCC
C15
1.0 µF
R6
1 MΩ
R5
0 Ω
Q1
Si4410
L1
27 µH
3.3 V
R11
4.7 Ω
Q2
Si4410
R7
3.3 Ω
C6
1000 pF
C12
100 µF
C7
100 µF
C13
10 µF
C14
1 µF
GND
RTN
C8
0.1 µF
C3
0.0022 µF
U2
TL5001A
2 VCC
1 OUT
6 DTC
5 SCP
3 COMP
4 FB
7 RT
GND 8
C2
0.033 µF
R2
1.6 kΩ
C4
0.022 µF
R3
180 Ω
R4
2.32 kΩ
C9
0.22 µF
R8
121 kΩ
C1
1 µF
R9
90.9 kΩ
R10
1.0 kΩ

Figure 16. 3.3-V 3-A Synchronous-Buck Converter Circuit

APPLICATION INFORMATION

Great care should be taken when laying out the pc board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

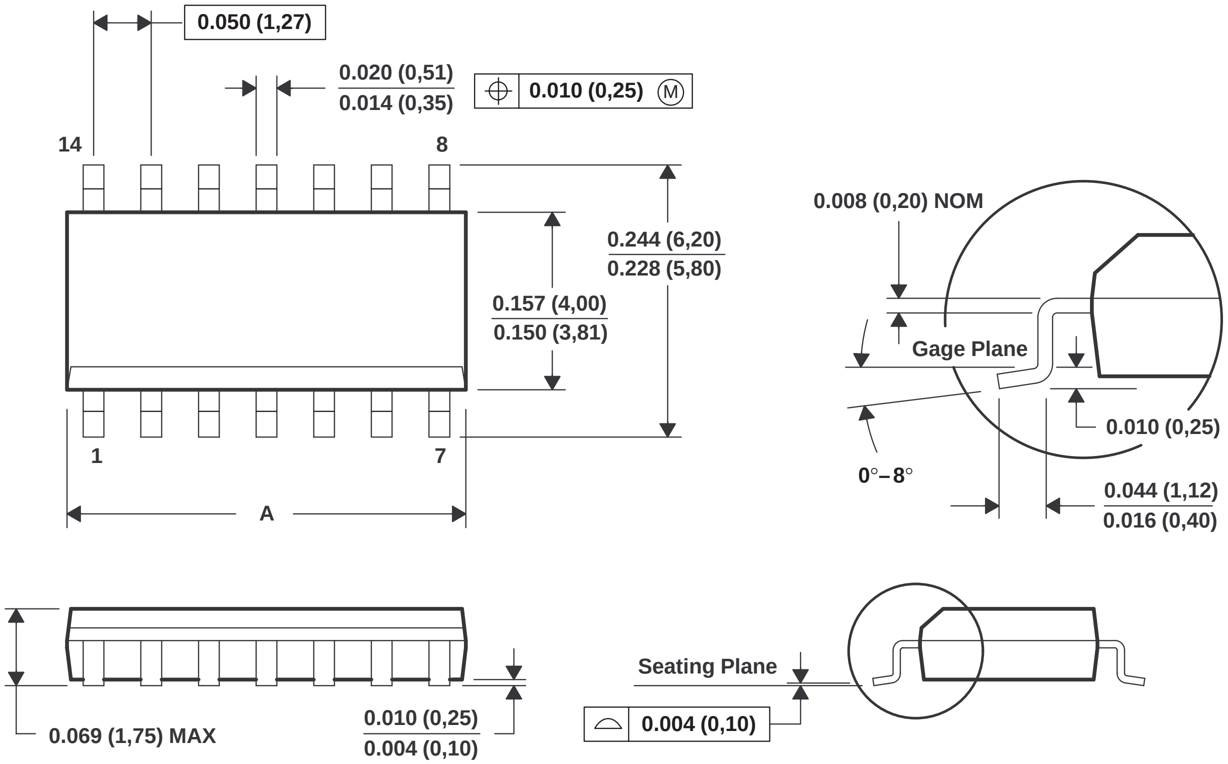
Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A) This node is very sensitive to noise pick up and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have any other EMI problems and the power supply will be relatively free of noise.

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN


0.050 (1,27)
0.020 (0,51)
0.014 (0,35)
0.010 (0,25) M
14
8
1
7
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,81)
A
0.008 (0,20) NOM
Gage Plane
0.010 (0,25)
0°–8°
0.044 (1,12)
0.016 (0,40)
Seating Plane
0.069 (1,75) MAX
0.010 (0,25)
0.004 (0,10)
0.004 (0,10)

PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

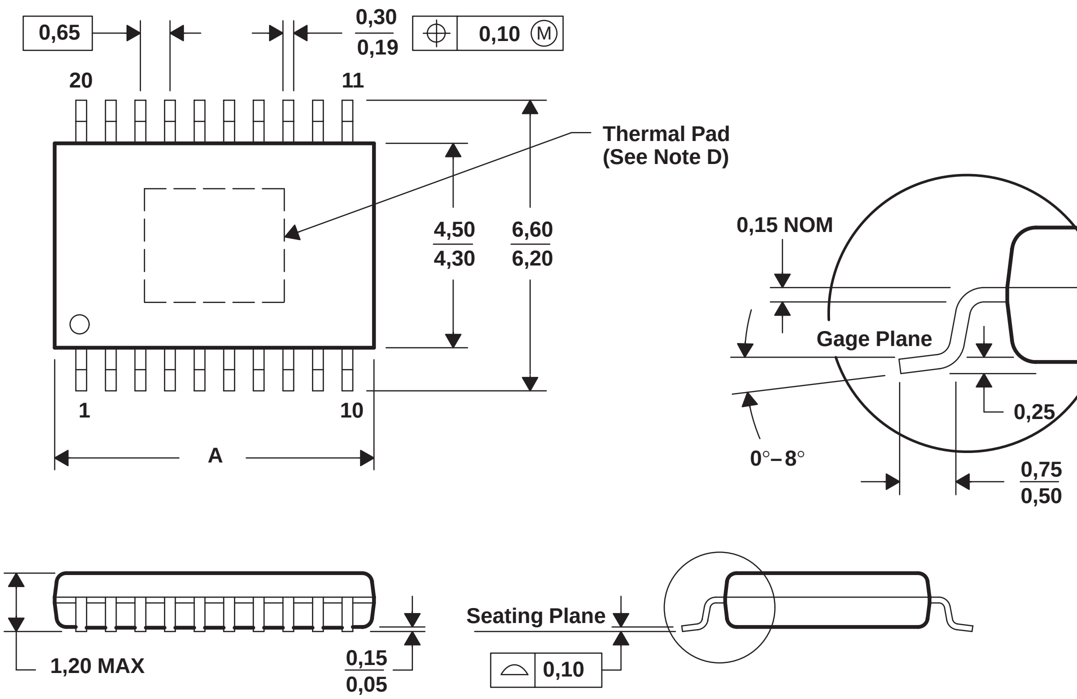
4040047 / D 10/96

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012

MECHANICAL DATA

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20-PIN SHOWN


0,65
0,30
0,19
0,10 M
20
11
Thermal Pad
(See Note D)
4,50
4,30
6,60
6,20
1
10
A
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
0,10

PINS ** / DIM	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/E 03/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions.
- D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
- E. Falls within JEDEC MO-153

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