TPS1100, TPS1100Y
SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

SLVS078C – DECEMBER 1993 – REVISED AUGUST 1995

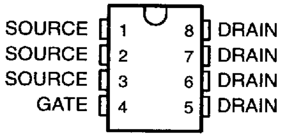
- **Low $r_{DS(on)}$ . . . 0.18 Ω Typ at V_{GS} = −10 V**
- **3 V Compatible**
- **Requires No External V_{CC}**
- **TTL and CMOS Compatible Inputs**
- **$V_{GS(th)}$ = −1.5 V Max**
- **Available in Ultrathin TSSOP Package (PW)**
- **ESD Protection Up to 2 kV Per MIL-STD-883C, Method 3015**

description

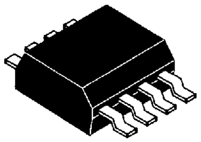
The TPS1100 is a single P-channel enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of Texas Instruments LinBiCMOS™ process. With a maximum $V_{GS(th)}$ of −1.5 V and an I_{DSS} of only 0.5 µA, the TPS1100 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low $r_{DS(on)}$ and excellent ac characteristics (rise time 10 ns typical) make the TPS1100 the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version with its smaller footprint and reduction in height fits in places where other P-channel MOSFETs cannot. The size advantage is especially important where board real estate is at a premium and height restrictions do not allow for an small-outline integrated circuit (SOIC) package.

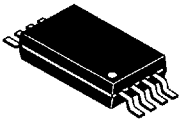
D OR PW PACKAGE
(TOP VIEW)



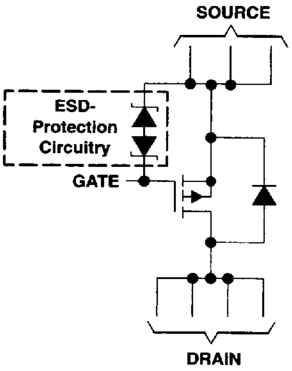
D PACKAGE



PW PACKAGE



schematic



NOTE A. For all applications, all source pins should be connected and all drain pins should be connected.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	
−40°C to 85°C	TPS1100D	TPS1100PWLE	TPS1100Y

The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1100DR). The PW package is available only left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1100PWLE). The chip form is tested at 25°C.

Caution. This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

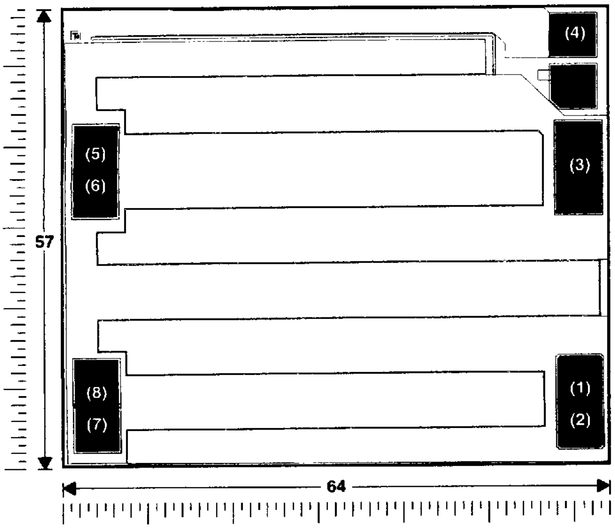
description (continued)

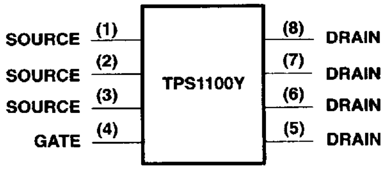
Such applications include notebook computers, personal digital assistants (PDAs), cellular telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other p-channel MOSFETs in SOIC packages.

TPS1100Y chip information

This chip, when properly assembled, displays characteristics similar to the TPS1100. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

					UNIT
Drain-to-source voltage, V_{DS}				−15	V
Gate-to-source voltage, V_{GS}				2 or −15	V
Continuous drain current (T_J = 150°C), I_D‡	V_{GS} = −2.7 V	D package	T_A = 25°C	±0.41	A
			T_A = 125°C	±0.28	
		PW package	T_A = 25°C	±0.4	
			T_A = 125°C	±0.23	
	V_{GS} = −3 V	D package	T_A = 25°C	±0.6	
			T_A = 125°C	±0.33	
		PW package	T_A = 25°C	±0.53	
			T_A = 125°C	±0.27	
	V_{GS} = −4.5 V	D package	T_A = 25°C	±1	
			T_A = 125°C	±0.47	
		PW package	T_A = 25°C	±0.81	
			T_A = 125°C	±0.37	
	V_{GS} = −10 V	D package	T_A = 25°C	±1.6	
			T_A = 125°C	±0.72	
		PW package	T_A = 25°C	±1.27	
			T_A = 125°C	±0.58	
Pulsed drain current, I_D‡			T_A = 25°C	±7	A
Continuous source current (diode conduction), I_S			T_A = 25°C	−1	A
Storage temperature range, T_{stg}				−55 to 150	°C
Operating junction temperature range, T_J				−40 to 150	°C
Operating free-air temperature range, T_A				−40 to 125	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				260	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq$ 25°C POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	504 mW	4.03 mW/°C	323 mW	262 mW	101 mW

‡ Maximum values are calculated using a derating factor based on $R_{\theta JA}$ = 158°C/W for the D package and $R_{\theta JA}$ = 248°C/W for the PW package. These devices are mounted on an FR4 board with no special thermal considerations when tested.

electrical characteristics at T_J = 25°C (unless otherwise noted)

static

PARAMETER		TEST CONDITIONS			TPS1100			TPS1100Y			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$,	$I_D = -250\ \mu A$		−1	−1.25	−1.50		−1.25		V
V_{SD}	Source-to-drain voltage (diode-forward voltage)†	$I_S = -1$ A,	$V_{GS} = 0$ V			−0.9			−0.9		V
I_{GSS}	Reverse gate current, drain short circuited to source	$V_{DS} = 0$ V,	$V_{GS} = -12$ V				±100				nA
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = -12$ V,	$V_{GS} = 0$ V	T_J = 25°C			−0.5				µA
				T_J = 125°C			−10				
$r_{DS(on)}$	Static drain-to-source on-state resistance†	$V_{GS} = -10$ V	$I_D = -1.5$ A			180			180		mΩ
		$V_{GS} = -4.5$ V	$I_D = -0.5$ A			291	400		291		
		$V_{GS} = -3$ V	$I_D = -0.2$ A			476	700		476		
		$V_{GS} = -2.7$ V				606	850		606		
g_{fs}	Forward transconductance†	$V_{DS} = -10$ V,	$I_D = -2$ A			2.5			2.5		S

† Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2%

dynamic

PARAMETER		TEST CONDITIONS			TPS1100, TPS1100Y			UNIT
					MIN	TYP	MAX	
Q_g	Total gate charge	$V_{DS} = -10$ V,	$V_{GS} = -10$ V,	$I_D = -1$ A		5.45		nC
Q_{gs}	Gate-to-source charge					0.87		
Q_{gd}	Gate-to-drain charge					1.4		
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -10$ V, $R_G = 6\ \Omega$,	$R_L = 10\ \Omega$, See Figures 1 and 2	$I_D = -1$ A,		4.5		ns
$t_{d(off)}$	Turn-off delay time					13		ns
t_r	Rise time					10		ns
t_f	Fall time					2		
$t_{rr(SD)}$	Source-to-drain reverse recovery time	$I_F = 5.3$ A,	di/dt = 100 A/µs			16		

PARAMETER MEASUREMENT INFORMATION

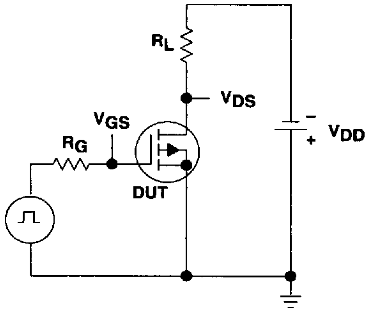


Figure 1. Switching-Time Test Circuit

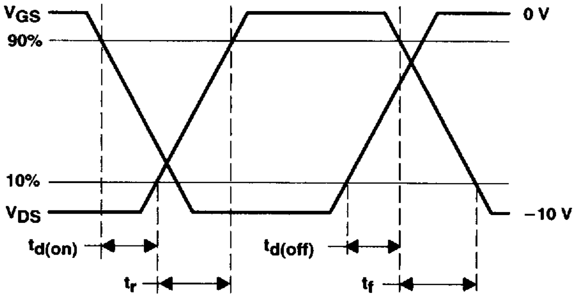


Figure 2. Switching-Time Waveforms

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

TYPICAL CHARACTERISTICS

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

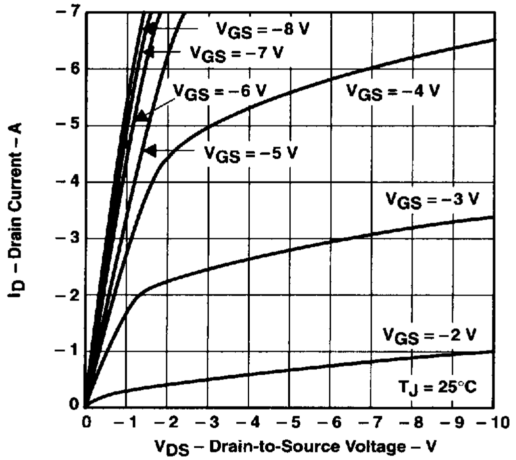


Figure 3

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

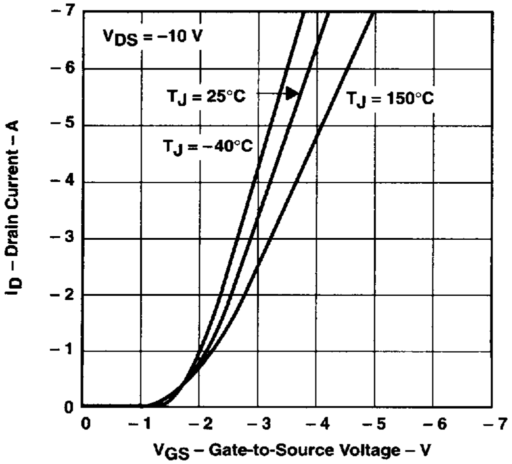


Figure 4

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
DRAIN CURRENT

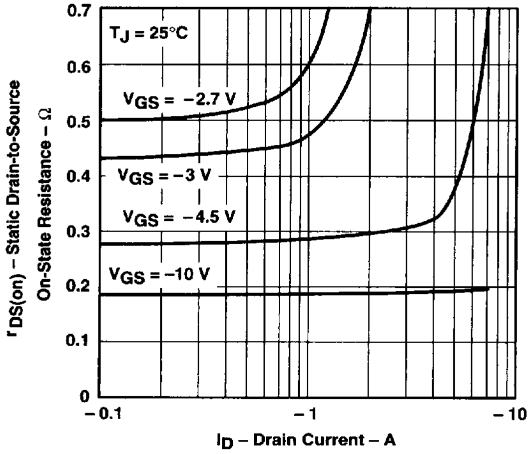
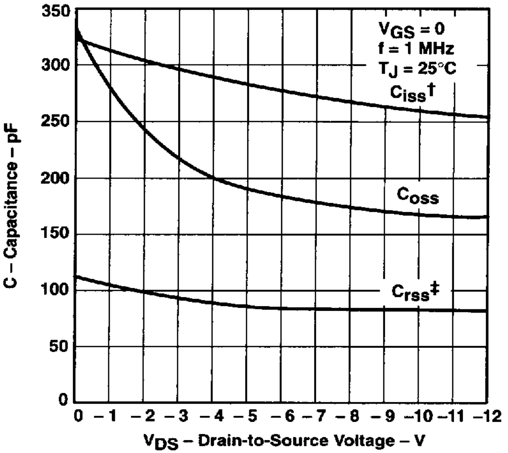


Figure 5

CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE



† $C_{iss} = C_{gs} + C_{gd}$, $C_{ds(shorted)}$

‡ $C_{rss} = C_{gd}$, $C_{oss} = C_{ds} + \frac{C_{gs}\,C_{gd}}{C_{gs} + C_{gd}} \approx C_{ds} + C_{gd}$

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED) vs JUNCTION TEMPERATURE

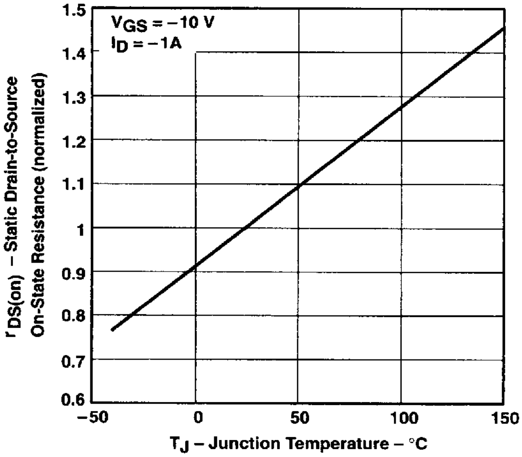


Figure 7

SOURCE-TO-DRAIN DIODE CURRENT vs SOURCE-TO-DRAIN VOLTAGE

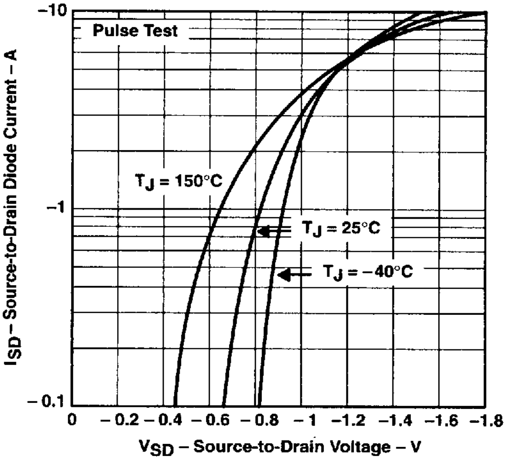


Figure 8

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE vs GATE-TO-SOURCE VOLTAGE

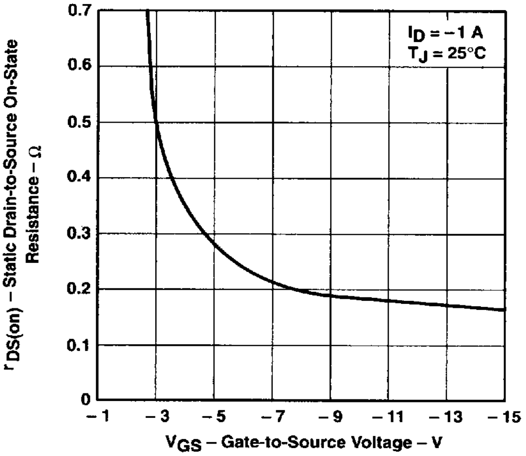


Figure 9

GATE-TO-SOURCE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

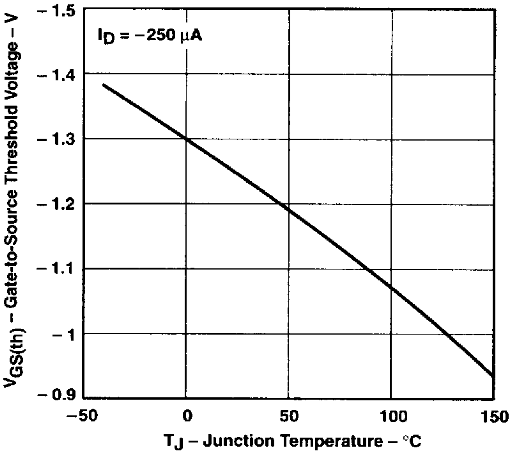


Figure 10

TYPICAL CHARACTERISTICS

GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE

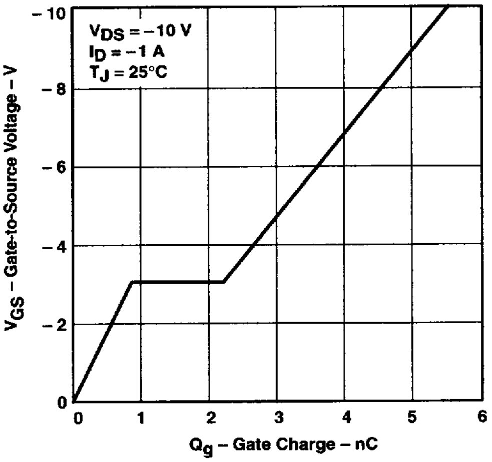


Figure 11

THERMAL INFORMATION

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

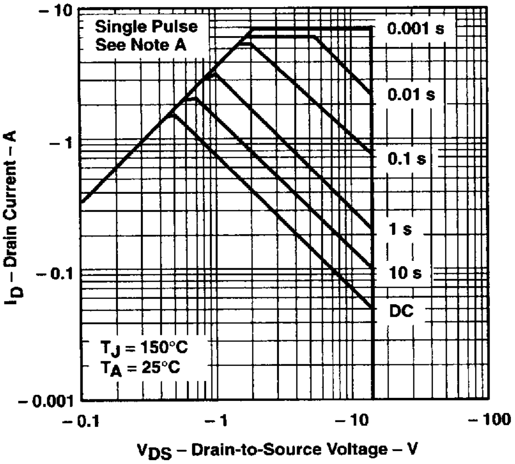


Figure 12

TRANSIENT JUNCTION-TO-AMBIENT
THERMAL IMPEDANCE
vs
PULSE DURATION

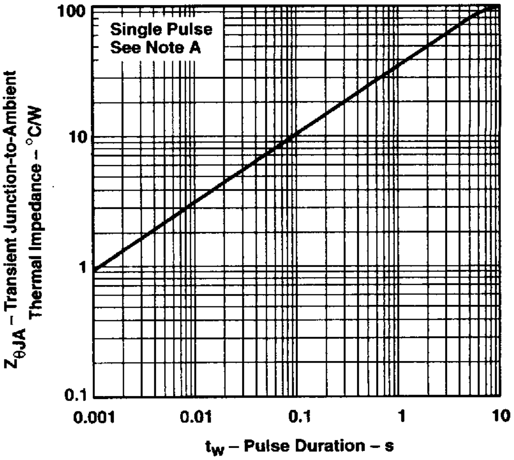


Figure 13

NOTE A. Values are for the D package and are FR4-board mounted only.

APPLICATION INFORMATION

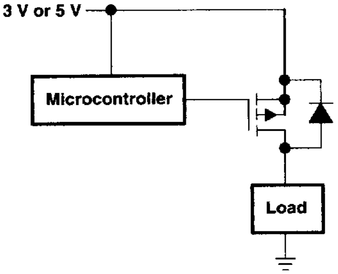


Figure 14. Notebook Load Management

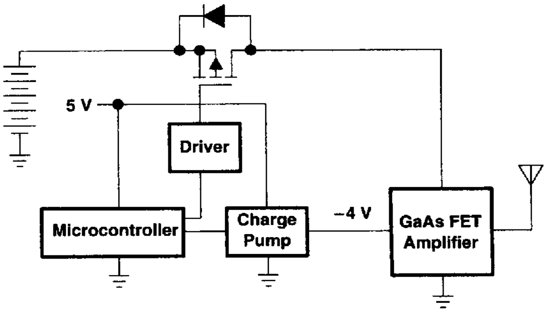


Figure 15. Cellular Phone Output Drive