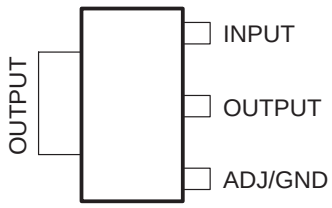
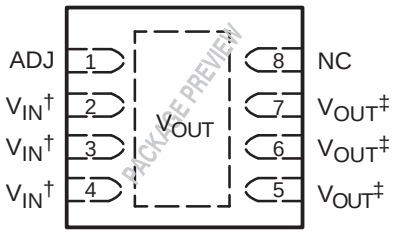
- **1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V, and Adjustable Output Voltage Options**
- **Output Current of 800 mA**
- **Operates Down to 1.1-V Dropout**
- **Specified Dropout Voltage at Multiple Current Levels**
- **0.2% Line Regulation Maximum**
- **0.4% Load Regulation Maximum**

DCY (SOT-223) PACKAGE
(TOP VIEW)

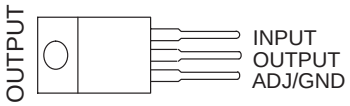


DRJ (QFN) PACKAGE
(TOP VIEW)

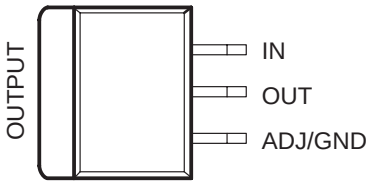


† V_{IN} pins (2, 3, 4) must be connected together.
‡ V_{OUT} pins (5, 6, 7) must be connected together.

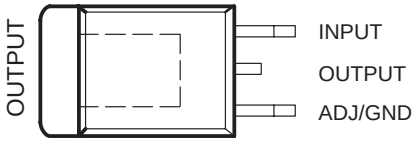
KCS (TO-220) PACKAGE
(TOP VIEW)



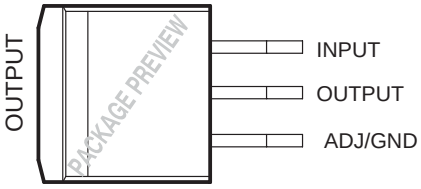
KTE (PowerFLEX™) PACKAGE
(TOP VIEW)



KTP (PowerFLEX™/TO-252) PACKAGE
(TOP VIEW)



KTT (TO-263) PACKAGE
(TOP VIEW)



description/ordering information

The TLV1117 is a positive low-dropout voltage regulator, designed to provide up to 800 mA of output current. The device is available in 1.5 V, 1.8 V, 2.5 V, 3.3 V, 5 V, and adjustable output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

The low-profile surface-mount KTP package allows the device to be used in applications where space is limited. The TLV1117 requires a minimum of 10 μF of output capacitance for stability. Output capacitors of this size or larger normally are included in most regulator designs.

Unlike pnp-type regulators, where up to 10% of the output current is wasted as quiescent current, the quiescent current of the TLV1117 flows into the load, increasing efficiency.

The TLV1117C device is characterized for operation over the virtual junction temperature range of 0°C to 125°C, and the TLV1117I device is characterized for operation over the virtual junction temperature range of −40°C to 125°C.

description/ordering information (continued)

TLV1117C ORDERING INFORMATION

T_J	V_O TYP (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	1.5 V	QFN (DRJ)	Reel of 1000	TLV1117-15CDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-15CDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-15CKTTR	PREVIEW
	1.8 V	QFN (DRJ)	Reel of 1000	TLV1117-18CDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-18CDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-18CKTTR	PREVIEW
	2.5 V	QFN (DRJ)	Reel of 1000	TLV1117-25CDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-25CDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-25CKTTR	PREVIEW
	3.3 V	QFN (DRJ)	Reel of 1000	TLV1117-33CDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-33CDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-33CKTTR	PREVIEW
	5 V	QFN (DRJ)	Reel of 1000	TLV1117-50CDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-50CDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-50CKTTR	PREVIEW
	ADJ	PowerFLEX (KTE)	Reel of 2000	TLV1117CKTER	TLV1117C
		PowerFLEX/TO-252‡ (KTP)	Reel of 2000	TLV1117CKTPR	TV1117
		QFN (DRJ)	Reel of 1000	TLV1117CDRJR	PREVIEW
		SOT-223 (DCY)	Tube of 80	TLV1117CDCY	V4
			Reel of 2500	TLV1117CDCYR	
		TO-220 (KCS)	Tube of 50	TLV1117CKCS	TLV1117C
		TO-263 (KTT)	Reel of 2000	TLV1117CKTTR	PREVIEW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
‡ Complies with TO-252, variation AC.

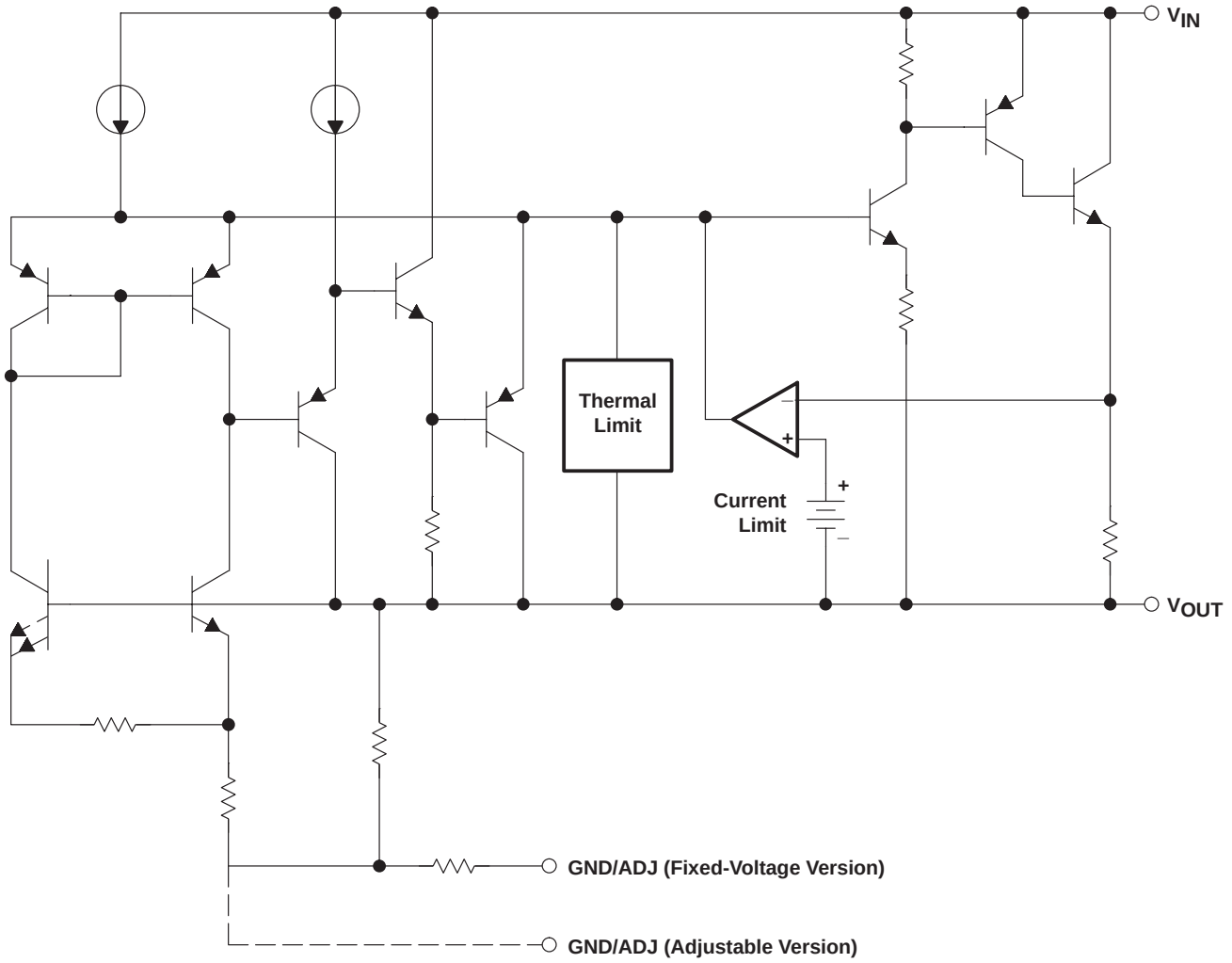
TLV1117I ORDERING INFORMATION

T_J	V_O TYP (V)	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	1.5 V	QFN (DRJ)	Reel of 1000	TLV1117-15IDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-15IDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-15IKTTR	PREVIEW
	1.8 V	QFN (DRJ)	Reel of 1000	TLV1117-18IDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-18IDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-18IKTTR	PREVIEW
	2.5 V	QFN (DRJ)	Reel of 1000	TLV1117-25IDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-25IDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-25IKTTR	PREVIEW
	3.3 V	QFN (DRJ)	Reel of 1000	TLV1117-33IDRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-33IDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-33IKTTR	PREVIEW
	5 V	QFN (DRJ)	Reel of 1000	TLV1117-50DRJR	PREVIEW
		SOT-223 (DCY)	Reel of 2500	TLV1117-50IDCYR	PREVIEW
		TO-263 (KTT)	Reel of 2000	TLV1117-50IKTTR	PREVIEW
	ADJ	PowerFLEX (KTE)	Reel of 2000	TLV1117IKTER	TLV1117I
		PowerFLEX/TO-252‡ (KTP)	Reel of 2000	TLV1117IKTPR	TY1117
		QFN (DRJ)	Reel of 1000	TLV1117IDRJR	PREVIEW
		SOT-223 (DCY)	Tube of 80	TLV1117IDCY	V2
			Reel of 2500	TLV1117IDCYR	
		TO-220 (KCS)	Tube of 50	TLV1117IKCS	TLV1117I
		TO-263 (KTT)	Reel of 2000	TLV1117IKTTR	PREVIEW

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ Complies with TO-252, variation AC.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Continuous input voltage . . . . . 20 V
Operating virtual junction temperature . . . . . 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

package thermal data (see Note 1)

PACKAGE	BOARD	θ_{JP}†	θ_{JC}	θ_{JA}
PowerFLEX (KTE)	High K, JESD 51-5	2.7°C/W		23°C/W
PowerFLEX/TO-252 (KTP)	High K, JESD 51-5	3°C/W		28°C/W
QFN (DRJ)	High K, JESD 51-5	TBD		TBD
SOT (DCY)	High K, JESD 51-7		4°C/W	53°C/W
TO-263 (KTT)	High K, JESD 51-5	TBD		TBD
TO-220 (KCS)	High K, JESD 51-5	3°C/W		19°C/W

† For packages with exposed thermal pads, such as QFN, PowerPAD, and PowerFLEX, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

NOTE 1: Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

recommended operating conditions

			MIN†	MAX	UNIT
V_{IN}	Input voltage	TLV1117	2.7	15	V
		TLV1117-15	2.9	15	
		TLV1117-18	3.2	15	
		TLV1117-25	3.9	15	
		TLV1117-33	4.7	15	
		TLV1117-50	6.4	15	
I_{OUT}	Output current			0.8	A
T_J	Operating virtual junction temperature range	TLV1117C	0	125	°C
		TLV1117I	−40	125	

† The input-to-output differential across the regulator should provide for some margin against regulator operation at the maximum dropout (for a particular current value). This margin is needed to account for tolerances in both the input voltage (lower limit) and the output voltage (upper limit). The absolute minimum V_{IN} for a desired maximum output current can be calculated by the following:

$V_{IN(min)} = V_{OUT(max)} + V_{DO(max\ @\ rated\ current)}$

TLV1117C electrical characteristics, T_J = 0°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage, V_{OUT}	V_{IN} − V_{OUT} = 2 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117	1.238	1.25	1.262	V
	I_{OUT} = 10 mA to 800 mA, V_{IN} − V_{OUT} = 1.4 V to 10 V	TLV1117	1.225	1.25	1.27	
	V_{IN} = 3.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-15	1.485	1.5	1.515	
	V_{IN} = 2.9 V to 10 V, I_{OUT} = 0 to 800 mA	TLV1117-15	1.47	1.5	1.53	
	V_{IN} = 3.8 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-18	1.782	1.8	1.818	
	V_{IN} = 3.2 V to 10 V, I_{OUT} = 0 to 800 mA	TLV1117-18	1.764	1.8	1.836	
	V_{IN} = 4.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-25	2.475	2.5	2.525	
	V_{IN} = 3.9 V to 10 V, I_{OUT} = 0 to 800 mA	TLV1117-25	2.45	2.5	2.55	
	V_{IN} = 5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-33	3.267	3.3	3.333	
	V_{IN} = 4.75 V to 10 V, I_{OUT} = 0 to 800 mA	TLV1117-33	3.235	3.3	3.365	
	V_{IN} = 7 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-50	4.95	5	5.05	
	V_{IN} = 6.5 V to 12 V, I_{OUT} = 0 to 800 mA	TLV1117-50	4.9	5	5.1	
Line regulation	I_{OUT} = 10 mA, V_{IN} − V_{OUT} = 1.5 V to 13.75 V	TLV1117		0.035	0.2	%
	I_{OUT} = 0 mA, V_{IN} = 2.9 V to 10 V	TLV1117-15		1	6	mV
	I_{OUT} = 0 mA, V_{IN} = 3.2 V to 10 V	TLV1117-18		1	6	
	I_{OUT} = 0 mA, V_{IN} = 3.9 V to 10 V	TLV1117-25		1	6	
	I_{OUT} = 0 mA, V_{IN} = 4.75 V to 15 V	TLV1117-33		1	6	
	I_{OUT} = 0 mA, V_{IN} = 6.5 V to 15 V	TLV1117-50		1	10	
Load regulation	I_{OUT} = 10 mA to 800 mA, V_{IN} − V_{OUT} = 3 V	TLV1117		0.2	0.4	%
	I_{OUT} = 0 to 800 mA, V_{IN} = 2.9 V	TLV1117-15		1	10	mV
	I_{OUT} = 0 to 800 mA, V_{IN} = 3.2 V	TLV1117-18		1	10	
	I_{OUT} = 0 to 800 mA, V_{IN} = 3.9 V	TLV1117-25		1	10	
	I_{OUT} = 0 to 800 mA, V_{IN} = 4.75 V	TLV1117-33		1	10	
	I_{OUT} = 0 to 800 mA, V_{IN} = 6.5 V	TLV1117-50		1	15	
Dropout voltage, V_{DO} (see Note 2)	I_{OUT} = 100 mA			1.1	1.2	V
	I_{OUT} = 500 mA			1.15	1.25	
	I_{OUT} = 800 mA			1.2	1.3	
Current limit	V_{IN} − V_{OUT} = 5 V, T_J = 25°C‡		0.8	1.2	1.5	A
Minimum load current	V_{IN} = 15 V	TLV1117		1.7	5	mA
Quiescent current	V_{IN} ≤ 15 V	All fixed-voltage options		5	10	mA
Thermal regulation	30 ms pulse, T_A = 25°C			0.01	0.1	%/W
Ripple rejection	V_{IN} − V_{OUT} = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz		60	78		dB

† All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

‡ Current limit test specified under recommended operating conditions

NOTE 2: Dropout is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at V_{IN} = $V_{OUT(nom)}$ + 1.5 V.

TLV1117C electrical characteristics, T_J = 0°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
ADJUSTMENT pin current			80	120	μA
Change in ADJUSTMENT pin current	I_{OUT} = 10 mA to 800 mA, $V_{IN} - V_{OUT}$ = 1.4 V to 10 V		0.2	5	μA
Temperature stability	T_J = full range		0.5		%
Long-term stability	1000 hrs, No load, T_A = 125°C		0.3		%
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz		0.003		%

† All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

TLV1117I electrical characteristics, T_J = -40°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage, V_{OUT}	V_{IN} − V_{OUT} = 2 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117	1.238	1.25	1.262	V
	I_{OUT} = 10 mA to 800 mA, V_{IN} − V_{OUT} = 1.4 V to 10 V		1.2	1.25	1.29	
	V_{IN} = 3.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-15	1.485	1.5	1.515	
	V_{IN} = 2.9 V to 10 V, I_{OUT} = 0 to 800 mA		1.44	1.5	1.56	
	V_{IN} = 3.8 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-18	1.782	1.8	1.818	
	V_{IN} = 3.2 V to 10 V, I_{OUT} = 0 to 800 mA		1.728	1.8	1.872	
	V_{IN} = 4.5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-25	2.475	2.5	2.525	
	V_{IN} = 3.9 V to 10 V, I_{OUT} = 0 to 800 mA		2.4	2.5	2.6	
	V_{IN} = 5 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-33	3.267	3.3	3.333	
	V_{IN} = 4.75 V to 10 V, I_{OUT} = 0 to 800 mA		3.168	3.3	3.432	
	V_{IN} = 7 V, I_{OUT} = 10 mA, T_J = 25°C	TLV1117-50	4.95	5	5.05	
	V_{IN} = 6.5 V to 12 V, I_{OUT} = 0 to 800 mA		4.8	5	5.2	
Line regulation	I_{OUT} = 10 mA, V_{IN} − V_{OUT} = 1.5 V to 13.75 V	TLV1117		0.035	0.3	%
	I_{OUT} = 0 mA, V_{IN} = 2.9 V to 10 V	TLV1117-15		1	4.5	mV
	I_{OUT} = 0 mA, V_{IN} = 3.2 V to 10 V	TLV1117-18		1	5.5	
	I_{OUT} = 0 mA, V_{IN} = 3.9 V to 10 V	TLV1117-25		1	7.5	
	I_{OUT} = 0 mA, V_{IN} = 4.75 V to 15 V	TLV1117-33		1	10	
	I_{OUT} = 0 mA, V_{IN} = 6.5 V to 15 V	TLV1117-50		1	15	
Load regulation	I_{OUT} = 10 mA to 800 mA, V_{IN} − V_{OUT} = 3 V	TLV1117		0.2	0.5	%
	I_{OUT} = 0 to 800 mA, V_{IN} = 2.9 V	TLV1117-15		1	7.5	mV
	I_{OUT} = 0 to 800 mA, V_{IN} = 3.2 V	TLV1117-18		1	9	
	I_{OUT} = 0 to 800 mA, V_{IN} = 3.9 V	TLV1117-25		1	12.5	
	I_{OUT} = 0 to 800 mA, V_{IN} = 4.75 V	TLV1117-33		1	15	
	I_{OUT} = 0 to 800 mA, V_{IN} = 6.5 V	TLV1117-50		1	20	
Dropout voltage, V_{DO} (see Note 2)	I_{OUT} = 100 mA			1.1	1.3	V
	I_{OUT} = 500 mA			1.15	1.35	
	I_{OUT} = 800 mA			1.2	1.4	
Current limit	V_{IN} − V_{OUT} = 5 V, T_J = 25°C‡		0.8	1.2	1.5	A
Minimum load current	V_{IN} = 15 V	TLV1117		1.7	5	mA
Quiescent current	V_{IN} ≤ 15 V	All fixed-voltage options		5	15	mA
Thermal regulation	30-ms pulse, T_A = 25°C			0.01	0.1	%/W
Ripple rejection	V_{IN} − V_{OUT} = 3 V, V_{ripple} = 1 V_{pp}, f = 120 Hz		60	75		dB

† All characteristics are measured with a 10-µF capacitor across the input and a 10-µF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

‡ Current limit test specified under recommended operating conditions

NOTE 2: Dropout is defined as the V_{IN} to V_{OUT} differential at which V_{OUT} drops 100 mV below the value of V_{OUT}, measured at V_{IN} = $V_{OUT(nom)}$ + 1.5 V.

TLV1117I electrical characteristics, T_J = 40°C to 125°C, all typical values are at T_J = 25°C (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
ADJUSTMENT pin current			80	120	μA
Change in ADJUSTMENT pin current	I_{OUT} = 10 mA to 800 mA, $V_{IN} - V_{OUT}$ = 1.4 V to 10 V		0.2	10	μA
Temperature stability	T_J = full range		0.5		%
Long-term stability	1000 hrs, No load, T_A = 125°C		0.3		%
Output noise voltage (% of V_{OUT})	f = 10 Hz to 100 kHz		0.003		%

† All characteristics are measured with a 10-μF capacitor across the input and a 10-μF capacitor across the output. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.

TYPICAL CHARACTERISTICS (GRAPHS PREVIEW)

Figure 1. Short-Circuit Current vs (V_{IN} − V_{OUT})

Figure 2. Load Regulation vs Temperature

Figure 3. Ripple Rejection vs Frequency (ADJ Version)

Figure 4. Ripple Rejection vs Current (ADJ Version)

Figure 5. Temperature Stability

Figure 6. ADJ Pin Current vs Temperature

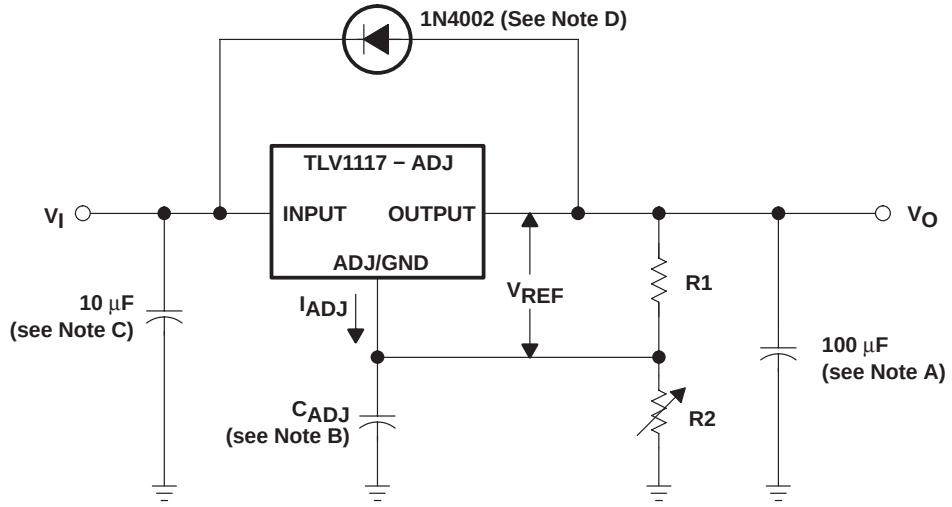
Figure 7. TLV1117-25 Load Transient Response

Figure 8. TLV1117-25 Line Transient Response

Figure 9. TLV1117-33 Load Transient Response

Figure 10. TLV1117-33 Line Transient Response

APPLICATION INFORMATION



V_{OUT} is calculated as:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + (I_{ADJ} \times R2)$$

Because I_{ADJ} typically is 55 μA, it is negligible in most applications.

NOTES: A. Output capacitor selection is critical for regulator stability. The recommended minimum is 10-μF tantalum or 50-μF aluminum electrolytic, with either one having an ESR between 0.3 Ω and 22 Ω. Larger C_{OUT} values benefit the regulator by improving transient response and loop stability.

B. C_{ADJ} can be used to improve ripple rejection. Ensure that the impedance of C_{ADJ} $\left(X_{CADJ} = \frac{1}{2\pi f_{ripple} C_{ADJ}}\right)$ is < R1 to prevent the ripple from being amplified. If C_{ADJ} is used, then a larger C_{OUT} is required (22-μF tantalum or 150-μF aluminum electrolytic).

C. C_{IN} is recommended if TLV1117 is not located near the power-supply filter.

D. An external diode is recommended to protect the regulator if the input instantaneously is shorted to GND.

Figure 11. Basic Adjustable Regulator

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV1117-15CDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-15CDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117-15CKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-15IDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-15IDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117-15IKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-18CDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-18CDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117-18CKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-18IDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-18IDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117-18IKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-25CKTPR	PREVIEW	PFM	KTP	2	3000	TBD	Call TI	Call TI
TLV1117-33CDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-33CDCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117-33CKC	PREVIEW	TO-220	KC	3	50	TBD	Call TI	Call TI
TLV1117-33CKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-33CKTT	PREVIEW	DDPAK/ TO-263	KTT	3	50	TBD	Call TI	Call TI
TLV1117-33CKTTR	PREVIEW	DDPAK/ TO-263	KTT	3	1000	TBD	Call TI	Call TI
TLV1117-33DCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-33IKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-50CDCY	PREVIEW	SOT-223	DCY	4	80	TBD	Call TI	Call TI
TLV1117-50CKCS	PREVIEW	TO-220	KCS	3	50	TBD	Call TI	Call TI
TLV1117-50CKTER	PREVIEW	PFM	KTE	3	2000	TBD	Call TI	Call TI
TLV1117-50CKTPR	PREVIEW	PFM	KTP	2	3000	TBD	Call TI	Call TI
TLV1117-50CKTT	PREVIEW	DDPAK/ TO-263	KTT	3	50	TBD	Call TI	Call TI
TLV1117-50CKTTR	PREVIEW	DDPAK/ TO-263	KTT	3		TBD	Call TI	Call TI
TLV1117-50DCYR	PREVIEW	SOT-223	DCY	4	2500	TBD	Call TI	Call TI
TLV1117CDCY	ACTIVE	SOT-223	DCY	4	80	TBD	CU	Level-2-235C-1 YEAR
TLV1117CDCYR	ACTIVE	SOT-223	DCY	4	2500	TBD	CU	Level-2-235C-1 YEAR
TLV1117CKC	PREVIEW	TO-220	KC	3	50	TBD	Call TI	Call TI
TLV1117CKCS	ACTIVE	TO-220	KCS	3	50	TBD	Call TI	Level-NC-NC-NC
TLV1117CKTER	ACTIVE	PFM	KTE	3	2000	TBD	Call TI	Level-1-220C-UNLIM
TLV1117CKTPR	ACTIVE	PFM	KTP	2	3000	TBD	Call TI	Level-1-220C-UNLIM
TLV1117IDCY	ACTIVE	SOT-223	DCY	4	80	TBD	CU	Level-2-235C-1 YEAR
TLV1117IDCYR	ACTIVE	SOT-223	DCY	4	2500	TBD	CU	Level-2-235C-1 YEAR
TLV1117IKCS	ACTIVE	TO-220	KCS	3	50	TBD	Call TI	Level-NC-NC-NC
TLV1117IKTER	ACTIVE	PFM	KTE	3	2000	TBD	Call TI	Level-1-220C-UNLIM
TLV1117IKTPR	ACTIVE	PFM	KTP	2	3000	TBD	Call TI	Level-1-220C-UNLIM

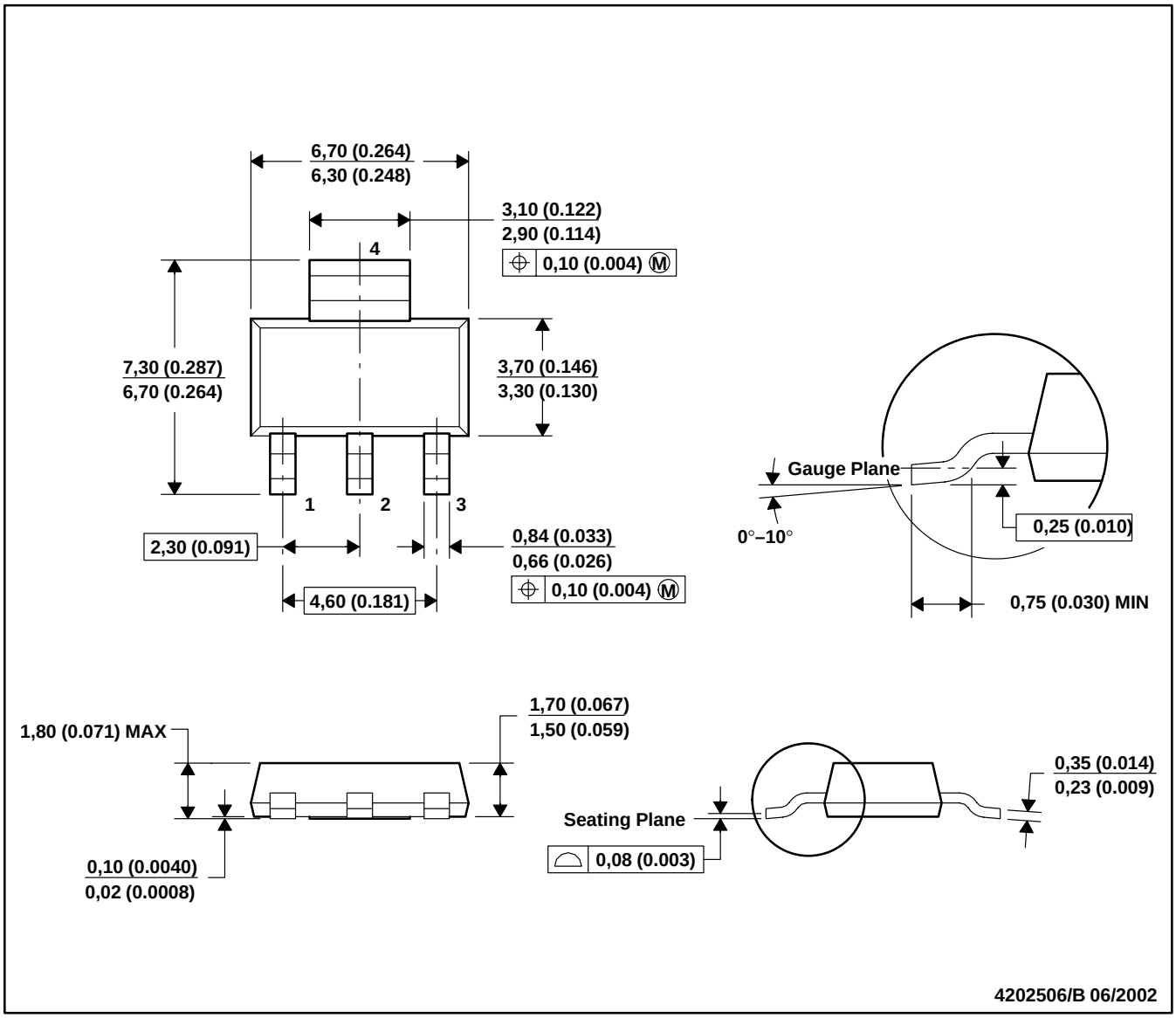
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MPDS094A – APRIL 2001 – REVISED JUNE 2002

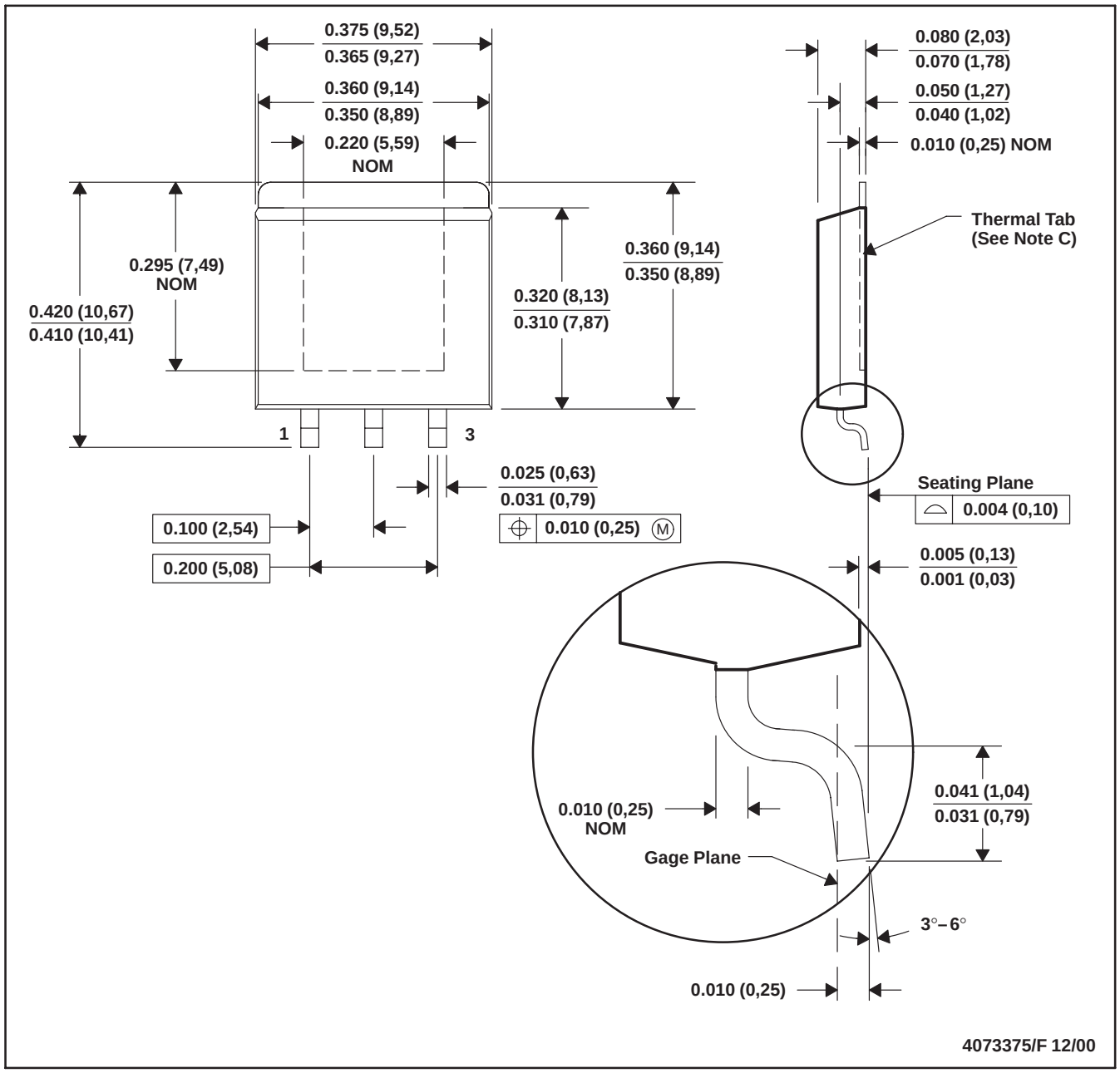
DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

KTE (R-PSFM-G3) **PowerFLEX™ PLASTIC FLANGE-MOUNT**

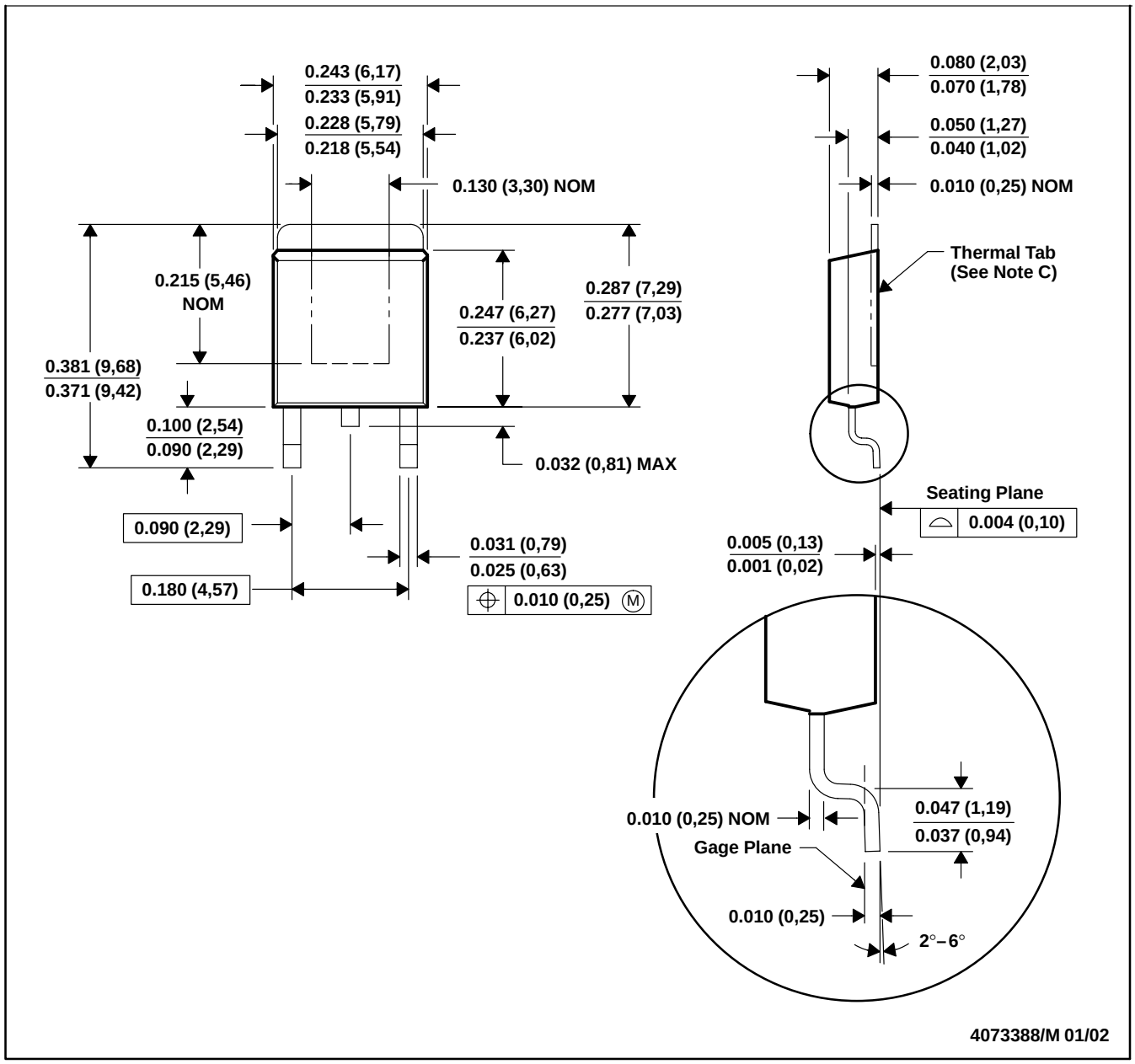


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC MO-169

PowerFLEX is a trademark of Texas Instruments.

MPSF001F – JANUARY 1996 – REVISED JANUARY 2002

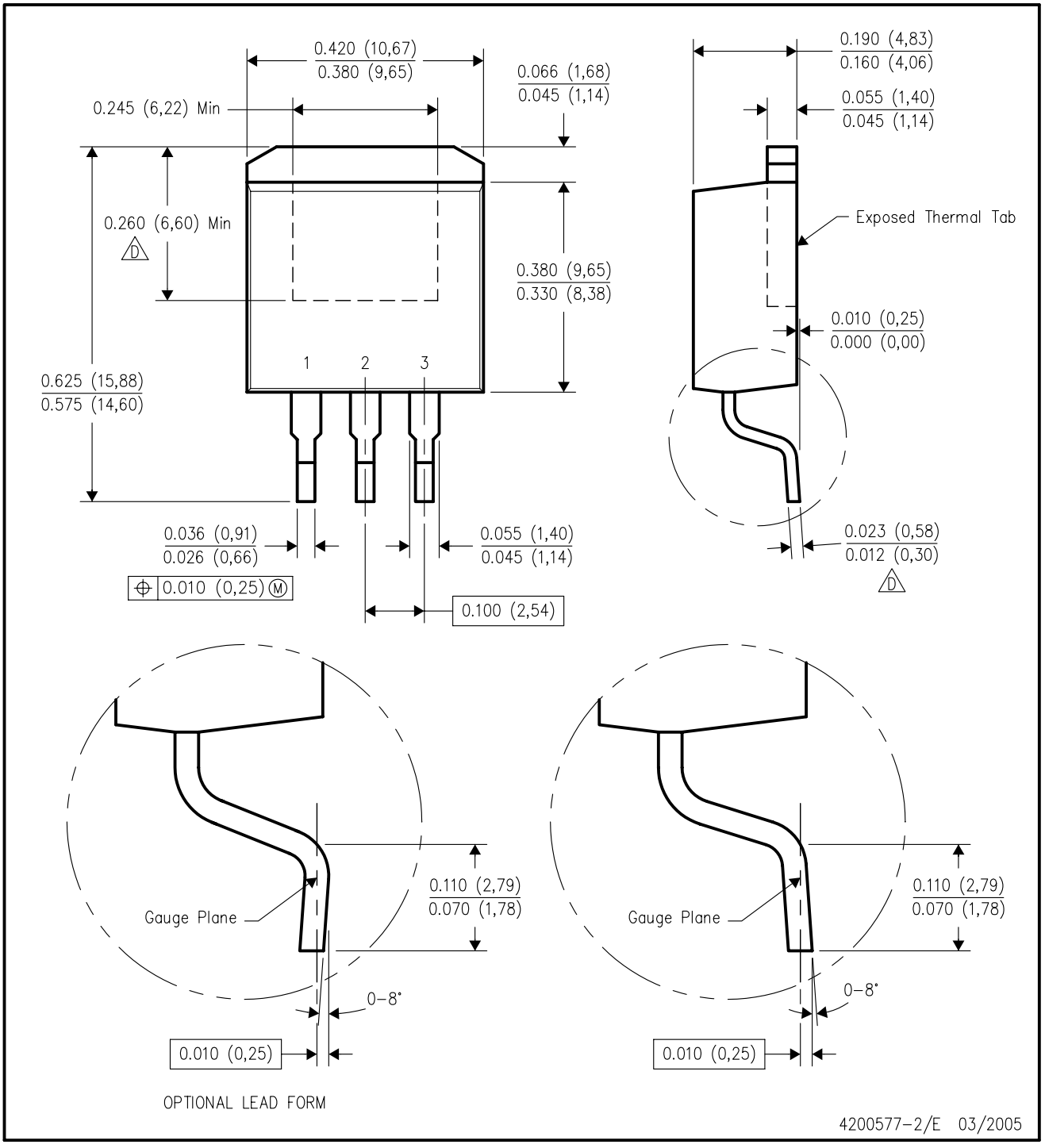
KTP (R-PSFM-G2) **PowerFLEX™ PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC TO-252 variation AC.

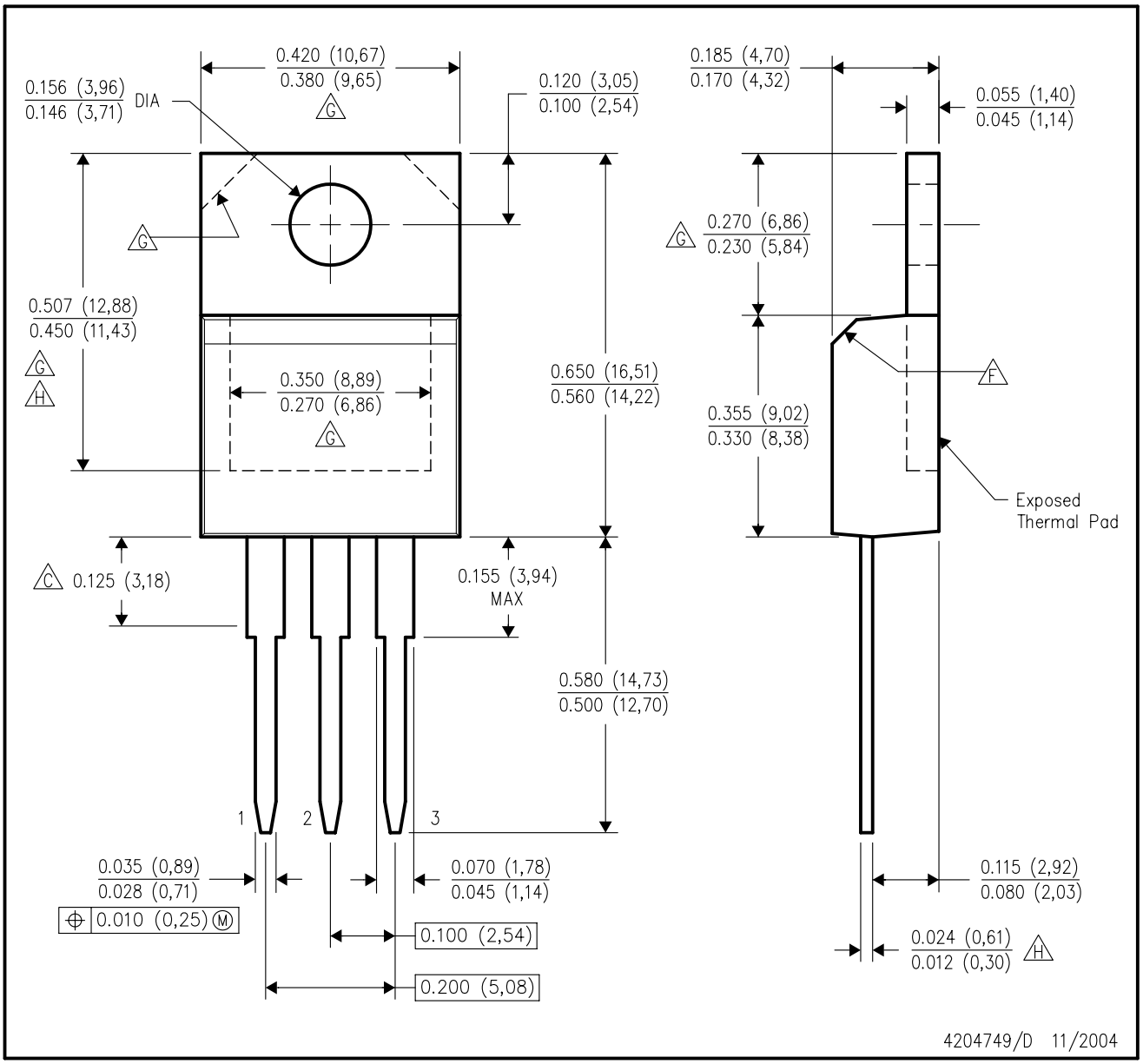
PowerFLEX is a trademark of Texas Instruments.

KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



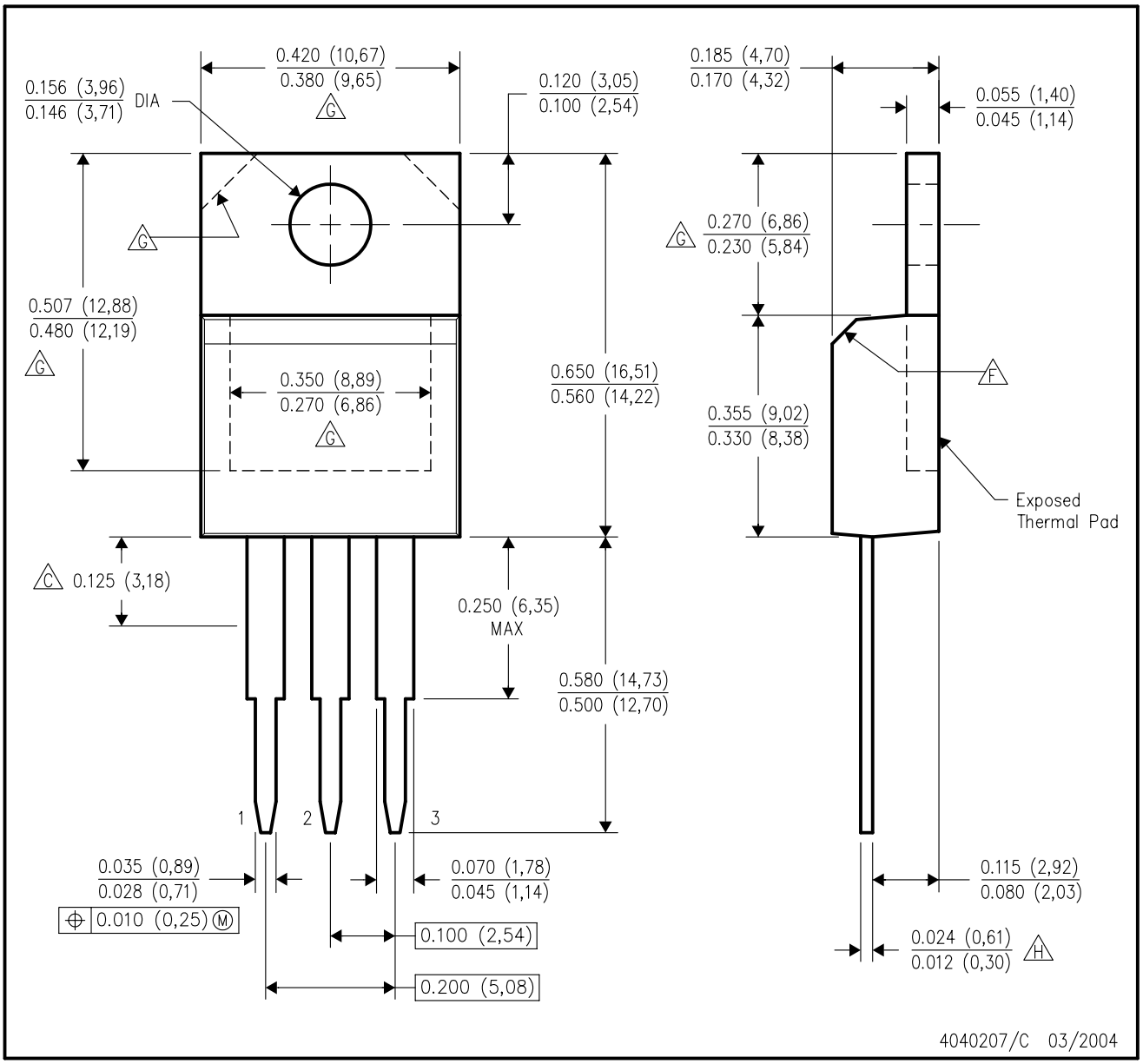
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.
F. The chamfer is optional.
G. Thermal pad contour optional within these dimensions.
H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness and minimum exposed pad length.

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

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