THS1230
3.3-V, 12-BIT, 30 MSPS, LOW-POWER ANALOG-TO-DIGITAL CONVERTER WITH POWER DOWN

SLAS291A – OCTOBER 2000 – REVISED NOVEMBER 2000

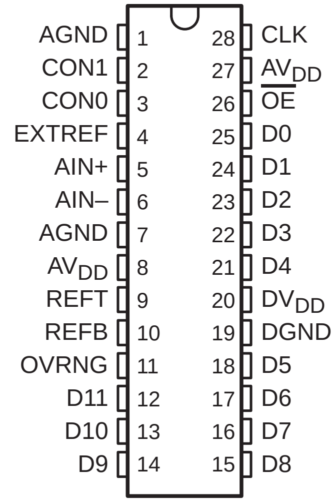
features

- **12-Bit Resolution, 30 MSPS Analog-to-Digital Converter**
- **Configurable Input Functions:**
  - **Single-Ended**
  - **Single-Ended With Offset**
  - **Differential**
- **3.3-V Supply Operation**
- **Internal Voltage Reference**
- **Out-of-Range Indicator**
- **Power-Down Mode**
- **IF Undersampling**

applications

- **Set Top Box (STB)**
- **Camcorders**
- **Digital Cameras**
- **Copiers**
- **Communications**
- **Test Instruments**
- **IF and Baseband Digitization**

DW OR PW PACKAGE
(TOP VIEW)



description

The THS1230 is a CMOS, low power, 12-bit, 30 MSPS analog-to-digital converter (ADC) that operates with a 3.3-V supply. The THS1230 gives circuit developers complete flexibility. The analog input to the THS1230 can be either single-ended, single-ended with offset, or differential. The THS1230 provides a wide selection of voltage references to match the user’s design requirements. For more design flexibility, the internal reference can be bypassed to use an external reference to suit the dc accuracy and temperature drift requirements of the application. The out-of-range output is used to monitor any out-of-range condition in the THS1230’s input range.

The speed, resolution, and single-supply operation of the THS1230 are suited for applications in set top box (STB), video, multimedia, high-speed acquisition, and communications. The speed and resolution ideally suit charge-couple device (CCD) input systems such as digital copiers, digital cameras, and camcorders. The wide input voltage range between V_{REFB} and V_{REFT} allows the THS1230 to be designed into multiple systems.

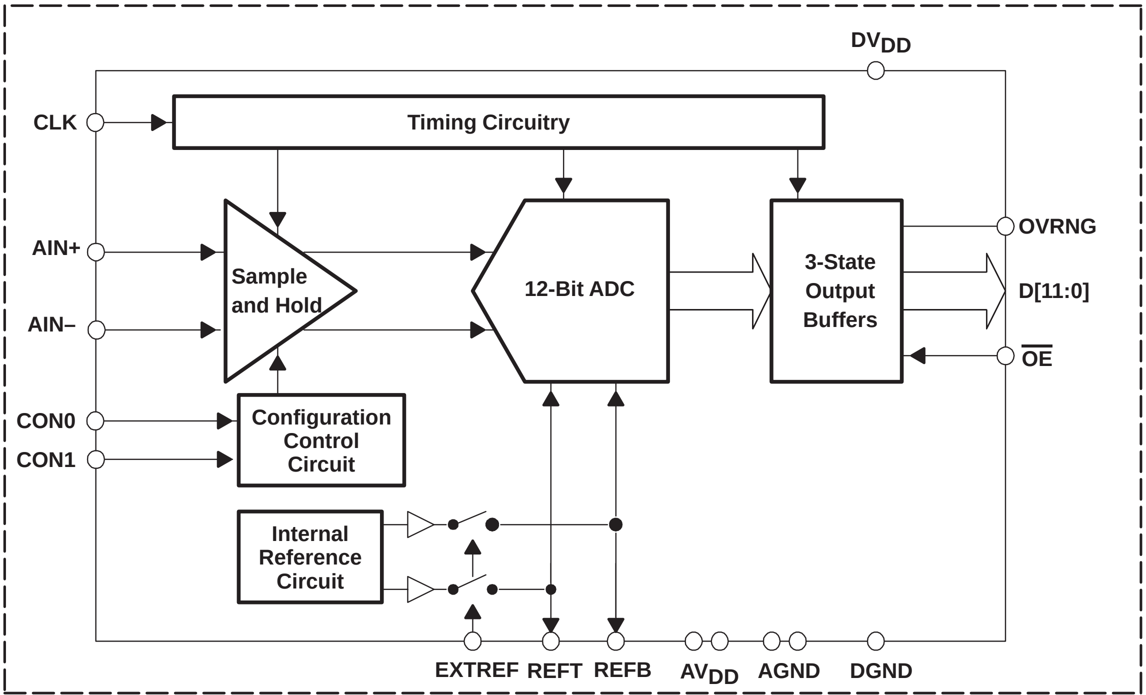
The THS1230C is characterized for operation from 0°C to 70°C. The THS1230I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	28-TSSOP (PW)	28-SOIC (DW)
0°C to 70°C	THS1230CPW	THS1230CDW
–40°C to 85°C	THS1230IPW	THS1230IDW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 7	I	Analog ground
AV_{DD}	8, 27	I	Analog supply
AIN+	5	I	Positive analog input
AIN–	6	I	Negative analog input
CLK	28	I	ADC conversion clock
CON1	2	I	Configuration Input 1
CON0	3	I	Configuration Input 0
DGND	19	I	Digital ground
DV_{DD}	20	I	Digital supply
D11	12	O	ADC data bit 11
D10	13	O	ADC data bit 10
D9	14	O	ADC data bit 9
D8	15	O	ADC data bit 8
D7	16	O	ADC data bit 7
D6	17	O	ADC data bit 6
D5	18	O	ADC data bit 5
D4	21	O	ADC data bit 4
D3	22	O	ADC data bit 3
D2	23	O	ADC data bit 2
D1	24	O	ADC data bit 1
D0	25	O	ADC data bit 0
EXTREF	4	I	Reference select input, high = external, low = internal
OVRNG	11	O	Out of range indicator
$\overline{OE}$	26	I	Output enable, high = disable, low = enable
REFT	9	I/O	Upper ADC reference voltage
REFB	10	I/O	Lower ADC reference voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range: AV_{DD} to AGND, DV_{DD} to DGND . . . . –0.3 to 4 V
AGND to DGND . . . . –0.3 to 0.3 V
Reference voltage input range, REFT, REFB to AGND . . . . –0.3 to AV_{DD} + 0.3 V
Analog input voltage range, AIN+, AIN– to AGND . . . . –0.3 to AV_{DD} + 0.3 V
Clock input voltage range, CLK to AGND . . . . –0.3 to AV_{DD} + 0.3 V
Digital input voltage range, digital input to DGND . . . . –0.3 to DV_{DD} + 0.3 V
Digital output voltage range, digital output to DGND . . . . –0.3 to DV_{DD} + 0.3 V
Operating junction temperature range, T_J . . . . –40°C to 150°C
Storage temperature range, T_{STG} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

electrical characteristics over recommended operating conditions (AV_{DD} = DV_{DD} = 3.3 V, f_S = 30 MHz/50% duty cycle, MODE = 1, 1-V input span, internal reference, T_{min} to T_{max}) (unless otherwise noted)

sampling rate and resolution

PARAMETER		MIN	NOM	MAX	UNIT
f_S	Sample frequency	5†		30	MSPS
	Resolution		12		Bits

analog inputs (all supplies = 3.3 V)

PARAMETER		MIN	TYP	MAX	UNIT
Positive analog input, AIN+		0		AV_{DD}	V
Negative analog input, AIN–		0		AV_{DD}	V
Analog input voltage difference for zero scale ADC out, (AIN+) – (AIN–)	MODE1		–1		V
	MODE2		–2		V
	MODE3		0		V
Analog input voltage difference for full scale ADC out, (AIN+) – (AIN–)	MODE1		1		V
	MODE2		2		V
	MODE3		1		V
Switched input capacitance, C_i			6		pF
Aperture delay time, $t_{d(ap)}$			2		ns
Aperture uncertainty (jitter)			2		ps
DC leakage current (input = ±FS)			10		µA

† The clock frequency may be extended to 5 MHz without degradation in specified performance.

electrical characteristics over recommended operating conditions ($AV_{DD} = DV_{DD} = 3.3$ V, $f_S = 30$ MHz/50% duty cycle, MODE = 1, 1-V input span, internal reference, T_{min} to T_{max}) (unless otherwise noted) (continued)

digital inputs and outputs (all supplies = 3.3 V)

PARAMETER			TEST CONDITION	MIN	TYP	MAX	UNIT
Digital Inputs							
V_{IH}	High level input voltage	All other inputs		$0.8 \times DV_{DD}$			V
		CLK		$0.8 \times AV_{DD}$			
V_{IL}	Low level input voltage	All other inputs				$0.2 \times DV_{DD}$	V
		CLK				$0.2 \times AV_{DD}$	
I_{IH}	High level input current					1	µA
I_{IL}	Low level input current					–1	µA
C_i	Input capacitance				5		pF
Digital Outputs							
V_{OH}	High level output voltage		I_{load} = 50 µA	DV_{DD}–0.4			V
V_{OL}	Low level output voltage		I_{load} = –50 µA			0.4	V
	High impedance output current					±1	µA
t_r/t_f	Rise/fall time		C_L = 10 pF		5.5		ns

power supply (CLK = 30 MHz)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
XV_{DD}	Supply voltage (all supplies)		3	3.3	3.6	V
I_{DD}	Supply current active – total			48	66	mA
$I_{(analog)}$	Supply current active – analog			35		mA
$I_{(digital)}$	Supply current active – digital			13		mA
$I_{I(standby)}$	Standby supply current	CLK = 0 MHz			10	µA
$t_{(PU)}$	Power-up time for references from standby			100		µs
P_D	Power dissipation	CLK = 30 MHz		168	220	mW
$P_{D(STBY)}$	Standby power dissipation	CLK = 0 MHz			36	µW
PSRR	Power supply rejection ratio			±0.1		%FS

electrical characteristics over recommended operating conditions (AV_{DD} = DV_{DD} = 3.3 V, f_S = 30 MHz/50% duty cycle, MODE = 1, 1-V input span, internal reference, T_{min} to T_{max}) (unless otherwise noted) (continued)

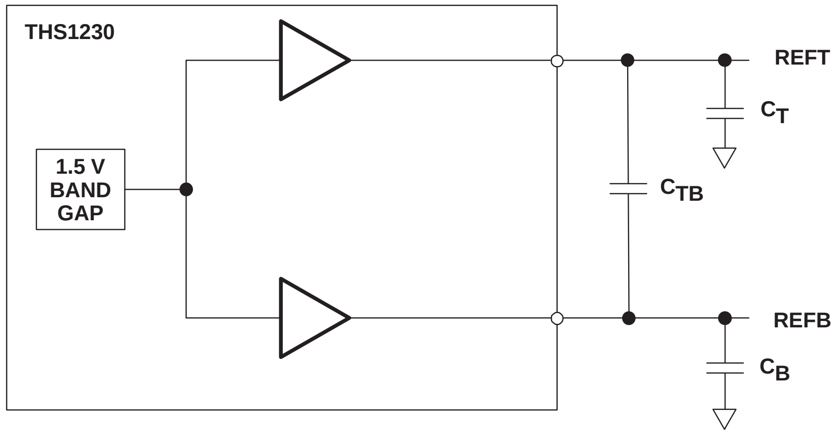


Figure 1. Reference Generation

REFT, REFB reference voltages (all supplies = 3.3 V)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Internal Reference						
V_{REFT}	Upper reference voltage			2.15		V
V_{REFB}	Lower reference voltage			1.15		V
V_{REF}	Differential reference voltage, V_{REFT}–V_{REFB}		0.95	1	1.05	V
	Differential reference voltage, V_{REFT}–V_{REFB} accuracy		–5%		5%	
External Reference						
	Externally applied V_{REFT} reference voltage range		2		2.5	V
	Externally applied V_{REFB} reference voltage range		1.05		1.3	V
	Externally applied (V_{REFT}–V_{REFB}) reference voltage range		0.75		1.05	V
	External mode V_{REFT} to V_{REFB} impedance			9		kΩ
Internal or External Reference						
C_T	V_{REFT} decoupling capacitor value			0.1		µF
C_B	V_{REFB} decoupling capacitor value			0.1		µF
C_{TB}	Decoupling capacitor V_{REFT} to V_{REFB}			10		µF

electrical characteristics over recommended operating conditions (AV_{DD} = DV_{DD} = 3.3 V, f_s = 30 MHz/50% duty cycle, MODE = 1, 1-V input span, internal reference, T_{min} to T_{max}) (unless otherwise noted) (continued)

dc accuracy (linearity)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Number of missing codes	All modes			0	codes
DNL	Differential nonlinearity	All modes		±0.4	±1	LSB
INL	Integral nonlinearity	All modes	–2.5	±1.2	2	LSB
	Offset error	All modes		0.5	1.2	%FSR
	Gain error	All modes		0.5	3.5	%FSR

dynamic performance (all supplies = 3.3 V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_i = 3.58 MHz		10.9		Bits
		f_i = 10 MHz	10.6	10.9		
		f_i = 15 MHz		10.8		
THD	Total harmonic distortion	f_i = 3.58 MHz		–76		dB
		f_i = 10 MHz		–74	–65	
		f_i = 15 MHz		–72.5		
SNR	Signal-to-noise ratio	f_i = 3.58 MHz		68		dB
		f_i = 10 MHz	66	68		
		f_i = 15 MHz		67.7		
SINAD	Signal-to-noise + distortion	f_i = 3.58 MHz		67.4		dB
		f_i = 10 MHz	65.6	67.4		
		f_i = 15 MHz		66.6		
SFDR	Spurious free dynamic range	f_i = 3.58 MHz		78.1		dB
		f_i = 10 MHz	67	76.4		
		f_i = 15 MHz		74.6		
	Analog input bandwidth			180		MHz
	Differential phase, DP			0.12		degree
$G_{(diff)}$	Differential gain			0.01%		

timing (all supplies = 3.3 V)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{CLK}	Clock frequency†		5		30	MHz
	Clock duty cycle		45%	50%	55%	
$t_{d(O)}$	Output delay time				19	ns
$t_{d(PZ)}$	Delay time, output disable to Hi-Z output			3.2		ns
$t_{d(EN)}$	Delay time, output enable to output valid			16	19	ns
	Latency				5	cycles

† The clock frequency may be extended to 5 MHz without degradation in specified performance.

PARAMETER MEASUREMENT INFORMATION

timing diagram

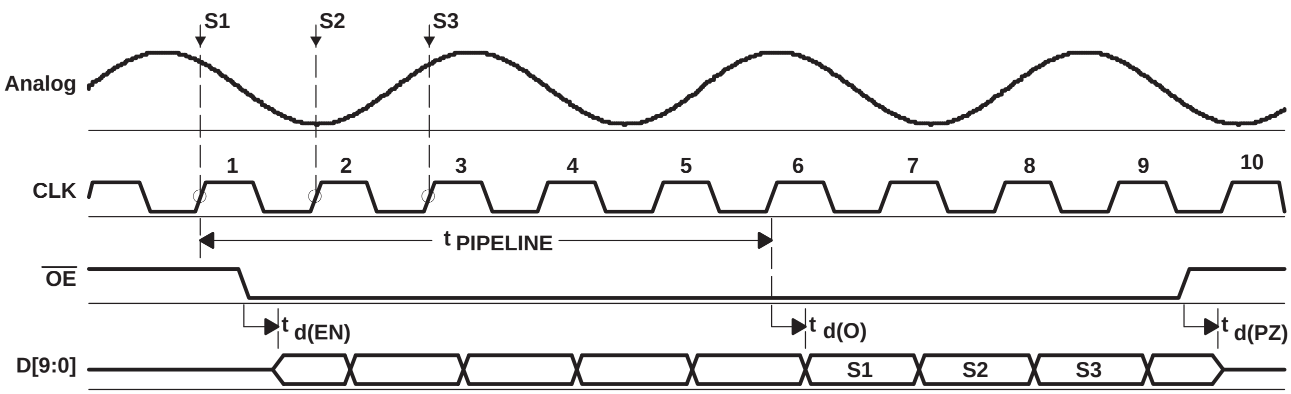


Figure 2. Input Timing

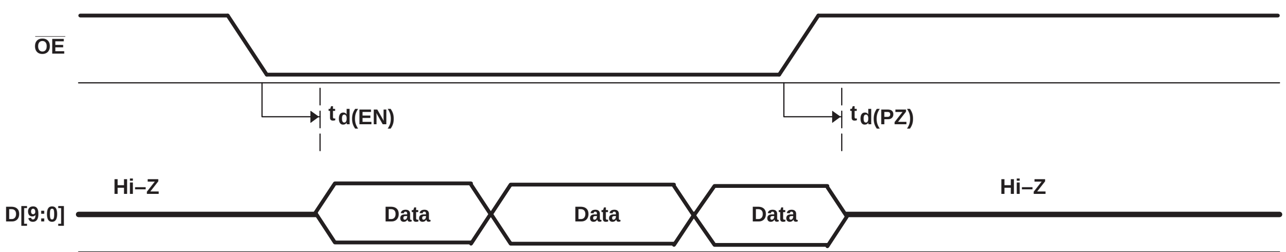


Figure 3. Output Timing

TYPICAL CHARACTERISTICS

POWER vs TEMPERATURE

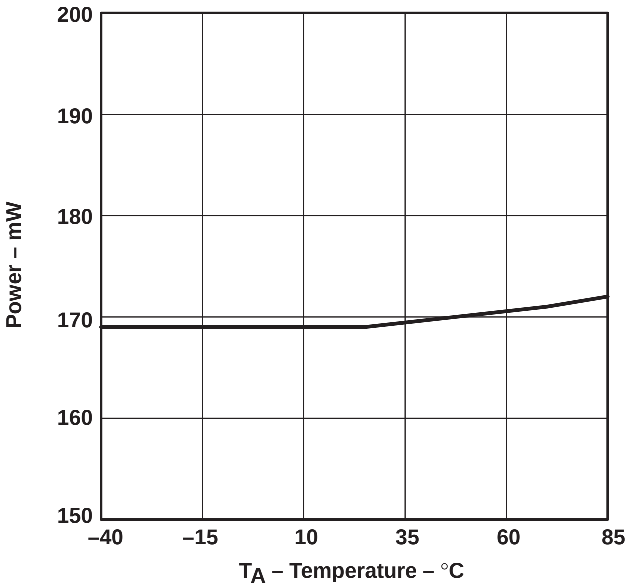


Figure 4

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

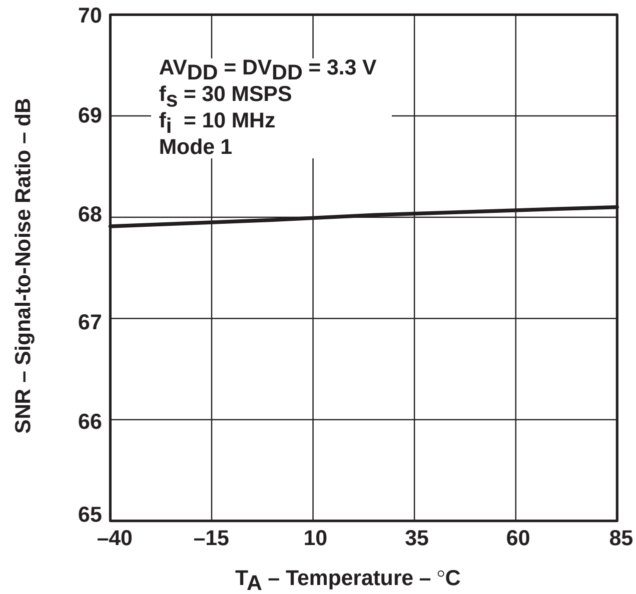


Figure 5

SPURIOUS FREE DYNAMIC RANGE vs TEMPERATURE

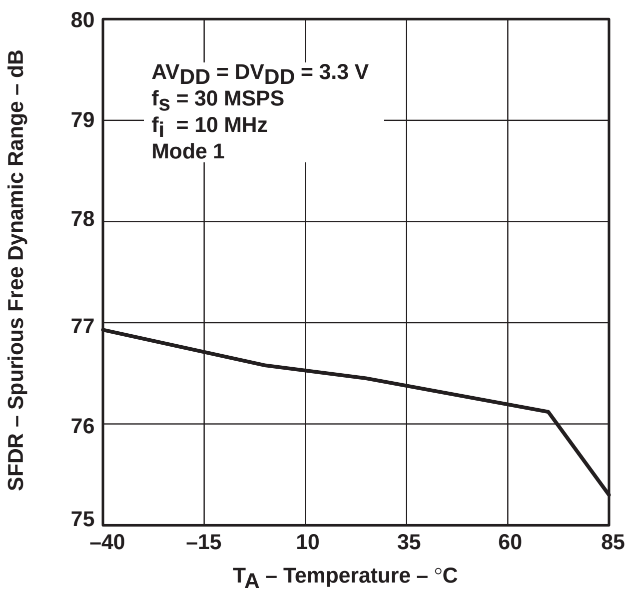


Figure 6

TOTAL HARMONIC DISTORTION vs TEMPERATURE

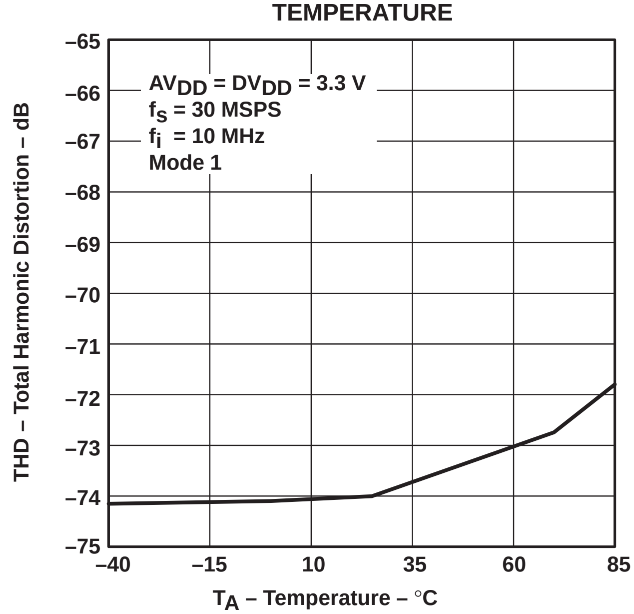


Figure 7

TYPICAL CHARACTERISTICS

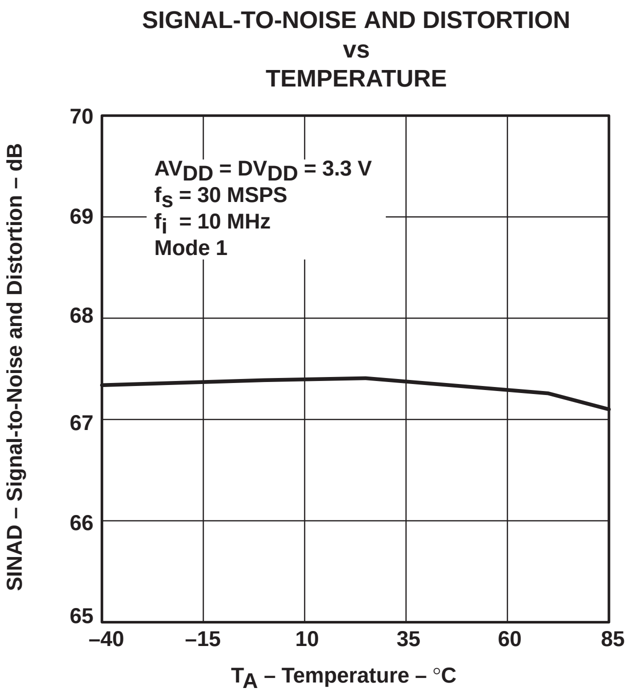


Figure 8

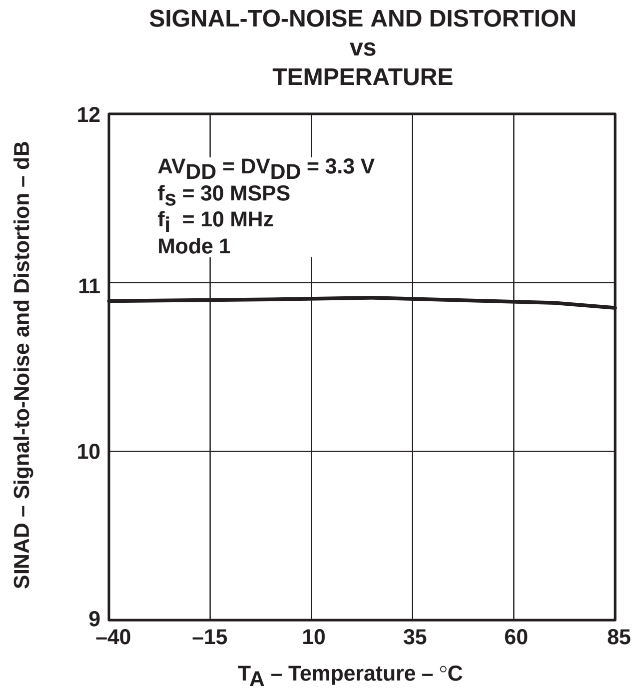


Figure 9

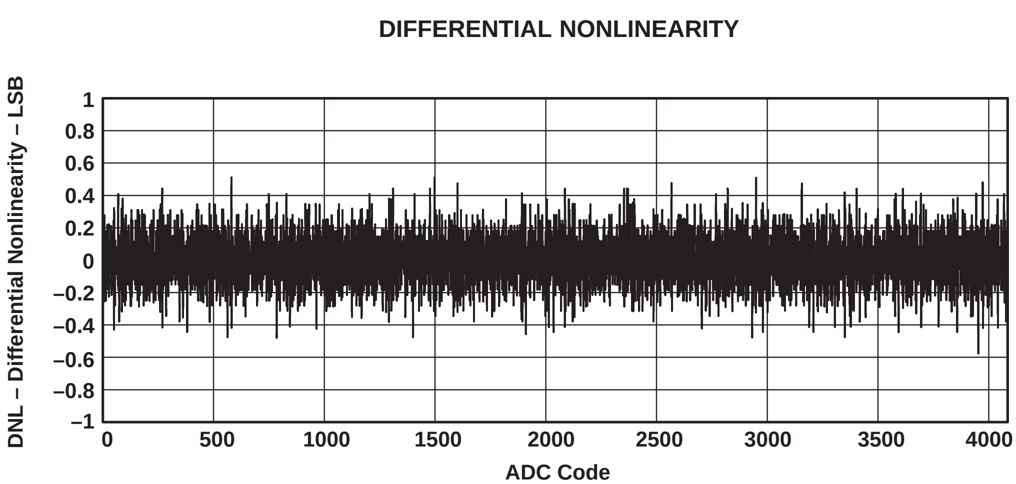


Figure 10

TYPICAL CHARACTERISTICS

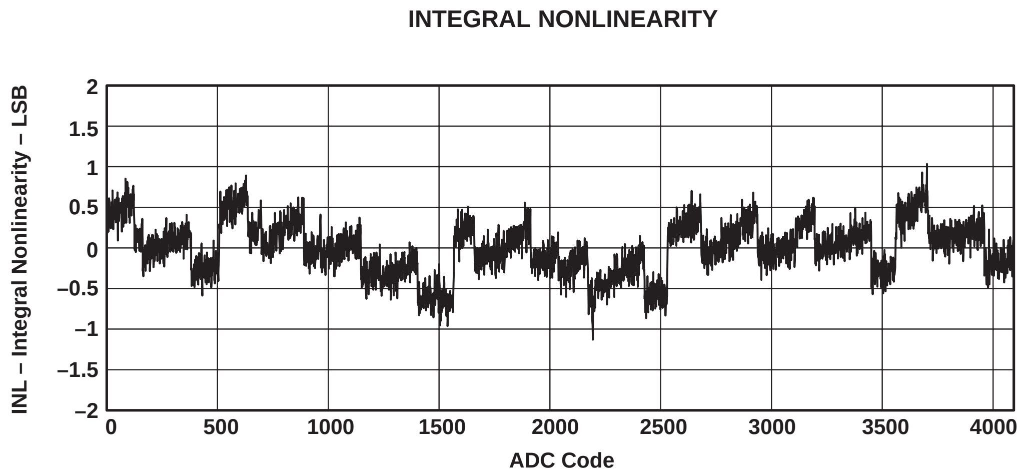


Figure 11

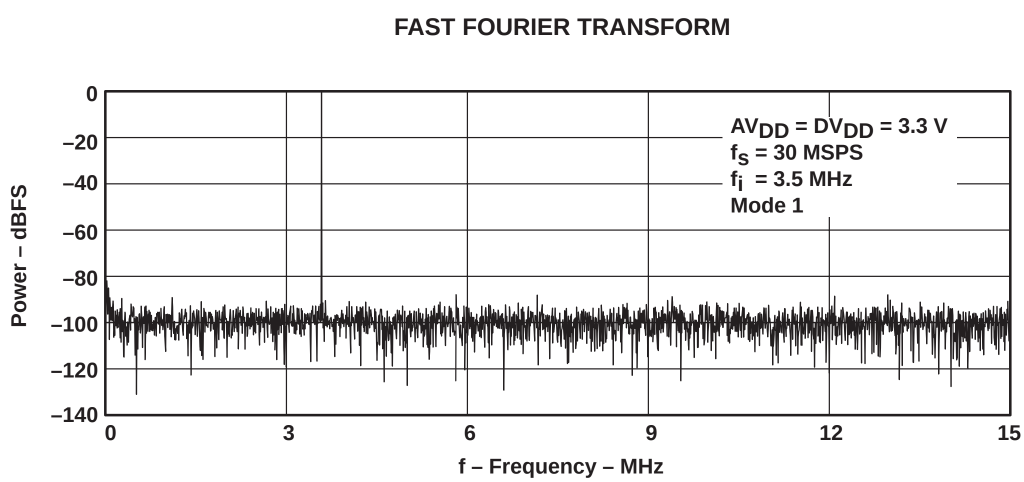


Figure 12

PRINCIPLES OF OPERATION

analog input

The analog input AIN is sampled in the sample and hold unit, the output of which feeds the ADC CORE, where the process of analog to digital conversion is performed against ADC reference voltages, V_{REFT} and V_{REFB}.

Connecting the EXTREF pin to one of two voltages, DGND or DV_{DD} selects one of the two configurations of ADC reference generation. The ADC reference voltages come from either the internal reference buffer or completely external sources. Connect EXTREF to DGND for internal reference generation or to DV_{DD} for external reference generation.

CON0 and CON1 as described below, select the input configuration mode or place the device in powerdown. The ADC core drives out through output buffers to the data pins D0 to D11. The output buffers can be disabled by the $\overline{OE}$ pin.

A single, sample-rate clock (30 MHz maximum) is required at pin CLK. The analog input signal is sampled on the rising edge of CLK, and corresponding data is output after the fifth following rising edge.

The THS1233 can operate in four input modes, controlled by the configuration pins CON0 and CON1 as shown in Table 1.

Table 1. Input Modes of Operation

MODE	CON1	CON0	MODE OF OPERATION
0	0	0	Device powered down
1	0	1	Single-ended mode/differential mode × 1
2	1	0	Differential mode × 0.5
3	1	1	Single-ended mode with offset

PRINCIPLES OF OPERATION

analog input (continued)

Modes 1, 2, and 3 are shown in Figure 13.

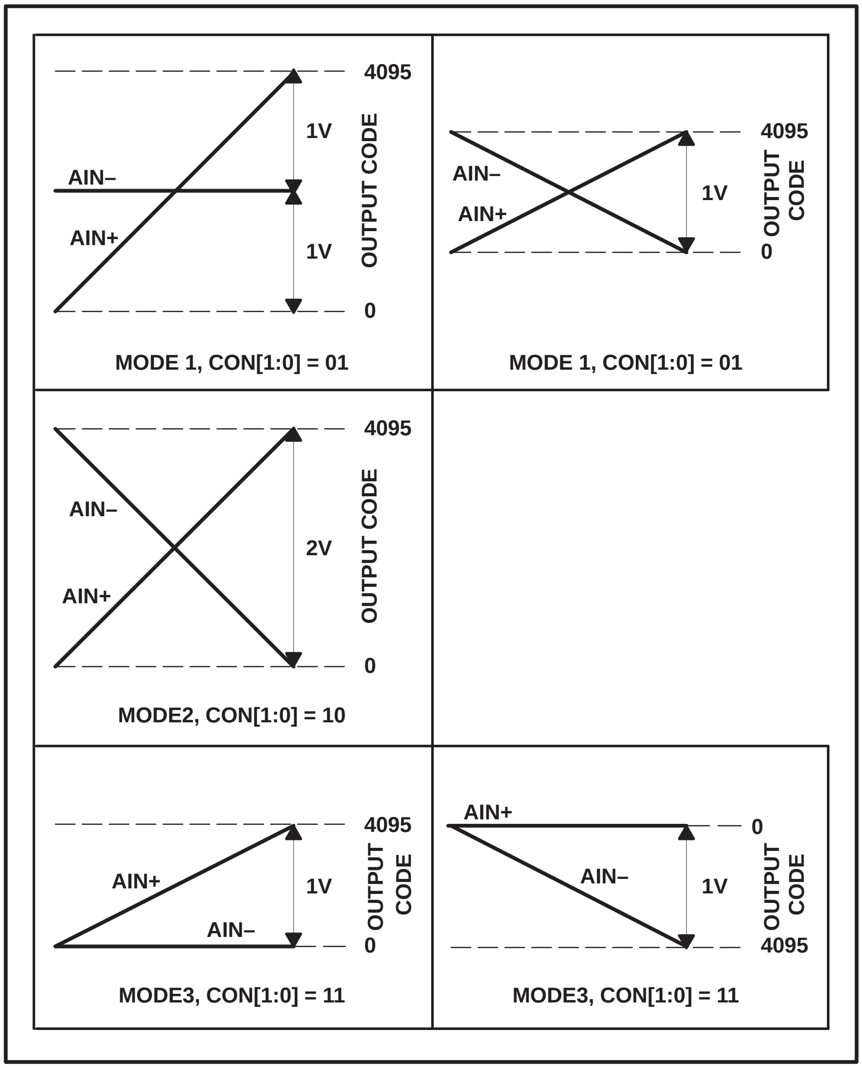


Figure 13. Input Mode Configurations

The difference between the AIN– and the AIN+ inputs is different in all three cases. The THS1230 automatically switches gain and offset in the S/H to accommodate for the input signals. This automatic switching is covered in Table 2.

Table 2. Input Mode Switching

MODE	CON1	CON0	(AIN+) – (AIN–) MIN	(AIN+) – (AIN–) MAX	S/H GAIN	S/H OFFSET
1	0	1	–1 V	1 V	×1	0 V
2	1	0	–2 V	2 V	×0.5	0 V
3	1	1	0 V	1 V	×1	–1 V

PRINCIPLES OF OPERATION

analog input (continued)

Table 2 assumes that the delta in ADC reference voltages V_{REFT} and V_{REFB} is set to 1 V, i.e., $V_{REFT} – V_{REFB}$ = 1 V. Note that V_{REFB} and V_{REFT} can be set externally, which will scale the numbers given in this table.

The user-chosen operating configuration and reference voltages determine what input signal voltage range the THS1230 can handle.

The following sections explain both the internal signal flow of the device and how the input signal span is related to the ADC reference voltages, as well as the ways in which the ADC reference voltages can be buffered internally or externally applied.

signal processing chain (sample and hold, ADC)

Figure 14 shows the signal flow through the sample and hold unit and the PGA to the ADC core.

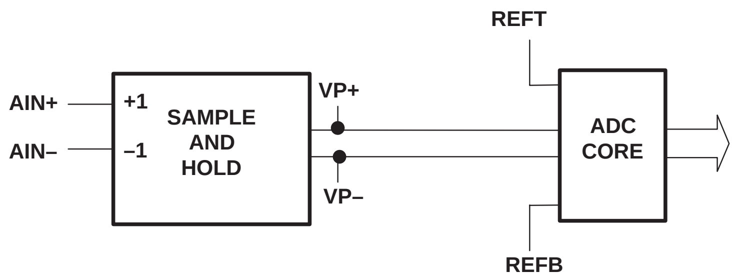


Figure 14. Analog Input Signal Flow

sample and hold

The differential sample and hold processes A_{IN} with respect to the voltages applied to the REFT and REFB pins, to give a differential output (VP+) – (VP–) = VP given by:

VP = (AIN+) – (AIN–)

For single-ended input signals, AIN– is a constant voltage; usually the AIN midscale input voltage. However if MODE = 3 (see Table 1) then AIN– or AIN+ can be used to create an offset for the other input in single-ended mode.

PRINCIPLES OF OPERATION

analog-to-digital converter

No matter what operating configuration is chosen, VP is digitized against ADC reference voltages V_{REFT} and V_{REFB}. The V_{REFT} and V_{REFB} voltages set the analog input span limits FS+ and FS– respectively. Any voltages at AIN greater than REFTS or less than V_{REFBS} will cause ADC over-range, which is signaled by OVR going high when the conversion result is output.

analog input

A first-order approximation for the equivalent analog input circuit of the THS1230 is shown in Figure 15. The equivalent input capacitance C_I is 5 pF typical. The input must charge/discharge this capacitance within the sample period of one half of a clock cycle. When a full-scale voltage step is applied, the input source provides the charging current through the switch resistance R_{SW} (200 Ω) of S1 and quickly settles. In this case the input impedance is low. Alternatively, when the source voltage equals the value previously stored on C_I, the hold capacitor requires no input current and the equivalent input impedance is very high.

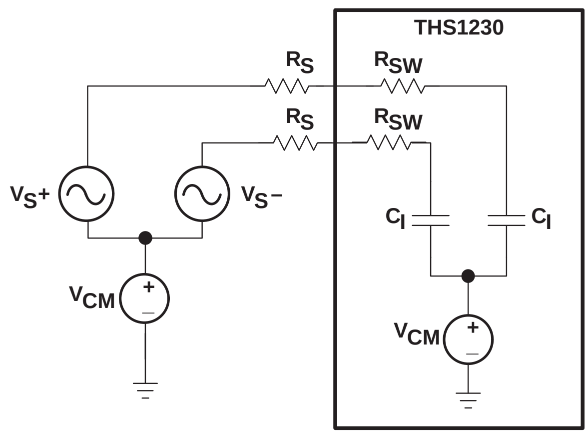


Figure 15. Simplified Equivalent Input Circuit

To maintain the frequency performance outlined in the specifications, the total source impedance should be limited to the following equation with f_{CLK} = 30 MHz, C_I = 5 pF, R_{SW} = 200 Ω:

$$R_S < \frac{1}{2f_{CLK} \times C_I \times \ln(256)} - R_{SW}$$

So, for applications running at a lower f_{CLK}, the total source resistance can increase proportionally.

The analog input of the THS1230 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (see Figure 16) will deliver the best performance from the converter.

PRINCIPLES OF OPERATION

analog input (continued)

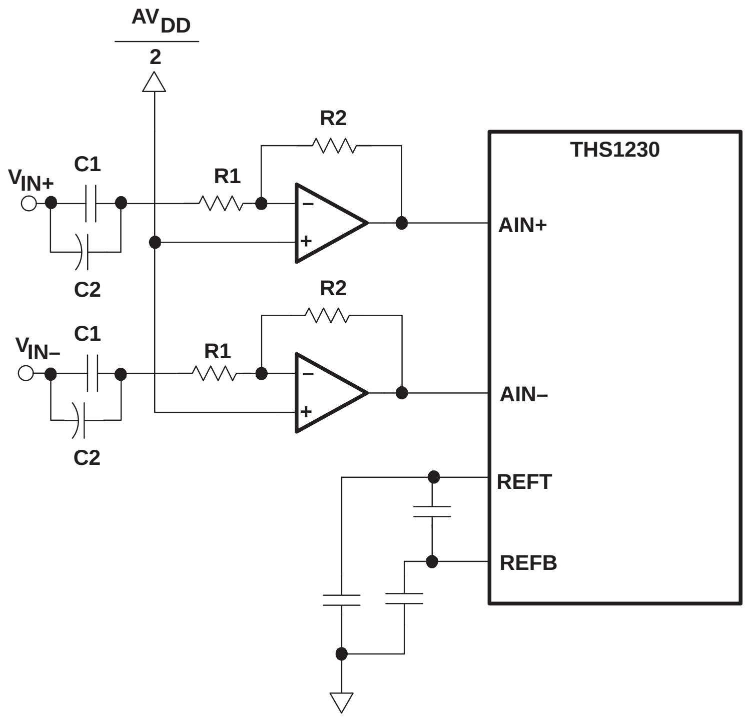


Figure 16. AC-Coupled Differential Input

The analog input can be dc-coupled (see Figure 17) as long as the inputs are within the analog input common mode voltage range. For example (see Figure 17), V+ and V– are signals centered on GND with a peak-to-peak voltage of 2 V, and the circuit in Figure 17 is used to interface it with the THS1230. Assume AV_{DD} of the converter is 3 V. Two problems have to be solved. The first is to shift CML from 0 V to 1.5 V (AV_{DD}/2). To do that, a V bias voltage and an adequate ratio of R1 and R2 have to be selected. For instance, if V bias = AV_{DD} = 3 V, then R1 = R2. The second is that the differential voltage has to be reduced from 4 V (2 x 2 V) to 1 V, and for that an attenuation of 4 to1 is needed. The attenuation is determined by the relation: (R3||2R2)/((R3||2R2) + 2R1). One possible solution is R1 = R2 = R3 = 150 Ω. In this case, moreover, the input impedance (2R1 + (R3||2R2)) will be 400 Ω. The values can be changed to match any other input impedance. A capacitor, C, connected from AIN+ to AIN– will help filter any high frequency noise on the inputs, also improving performance. Note that the chosen value of capacitor C must take into account the highest frequency component of the analog input signal.

PRINCIPLES OF OPERATION

analog input (continued)

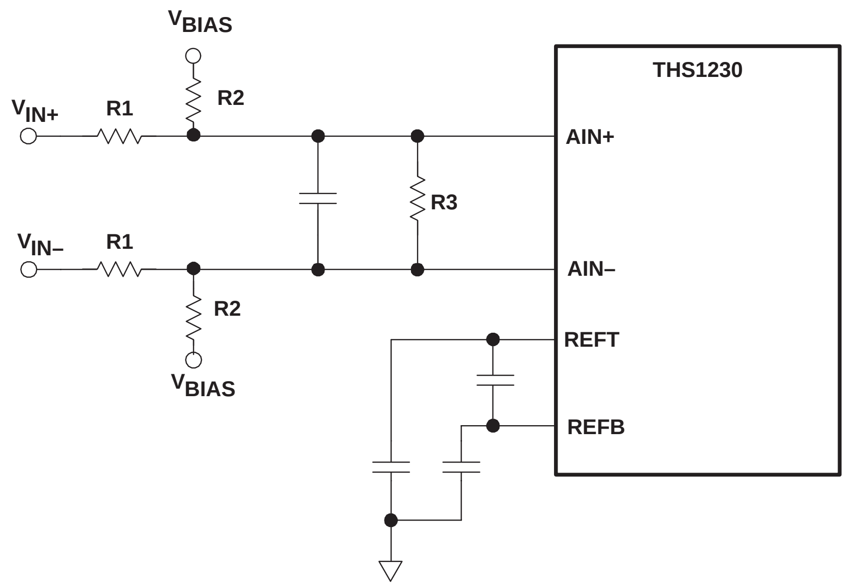


Figure 17. DC-Coupled Differential Input Circuit

The configuration shown in Figure 18 may be used with a single-ended ac-coupled input. If V_{IN} is a 1 V_{PP} sinewave, then AIN+ is a 1 V_{PP} sinewave riding on a positive voltage equal to $AV_{DD}/2$. The converter will be at positive full scale when AIN+ is at $AV_{DD}/2$ + 0.5 V and will be at negative full scale when AIN+ is equal to $AV_{DD}/2$ – 0.5 V. Sufficient headroom must be provided such that the input voltage never goes above 3.3 V or below AGND.

A single-ended source may give better overall system performance if it is first converted to differential before driving the THS1230.

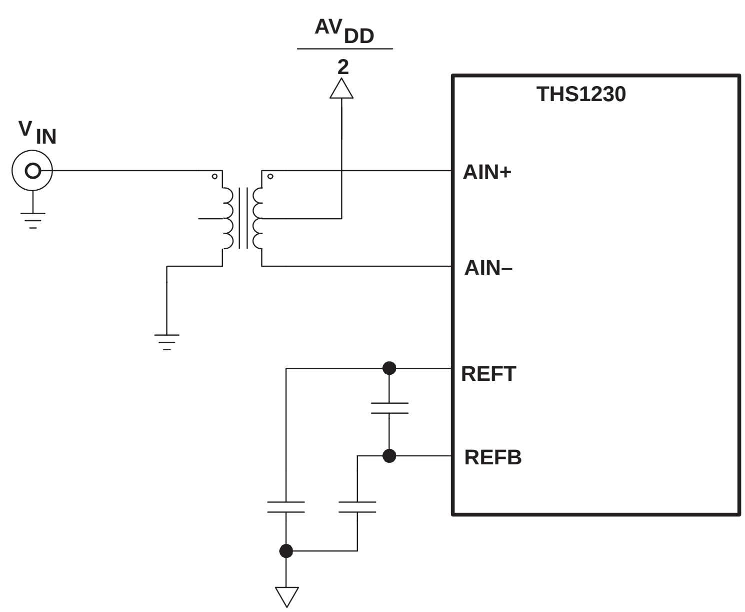


Figure 18. Transformer Coupled Single-Ended Input

PRINCIPLES OF OPERATION

digital outputs

The output of THS1230 is in unsigned binary code. The ADC input over-range indicator is output on pin OVRNG. Capacitive loading on the output should be kept as low as possible (a maximum loading of 10 pF is recommended) to ensure best performance. Higher output loading causes higher dynamic output currents and can therefore increase noise coupling into the part's analog front end. To drive higher loads the use of an output buffer is recommended.

When clocking output data from THS1230, it is important to observe its timing relation to CLK. The pipeline ADC delay is 5 clock cycles to which the maximum output propagation delay needs to be added.

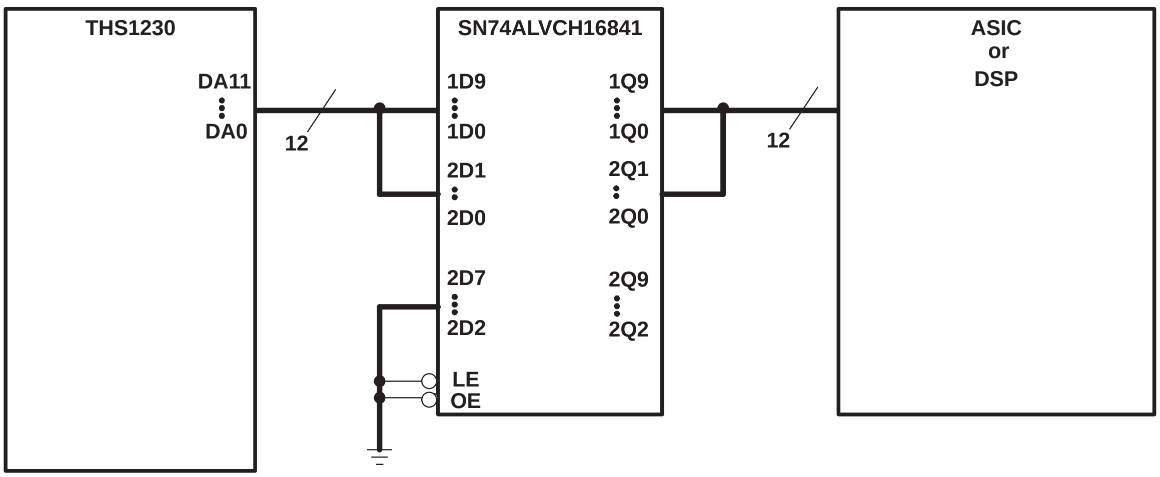


Figure 19. Buffered Output Connection

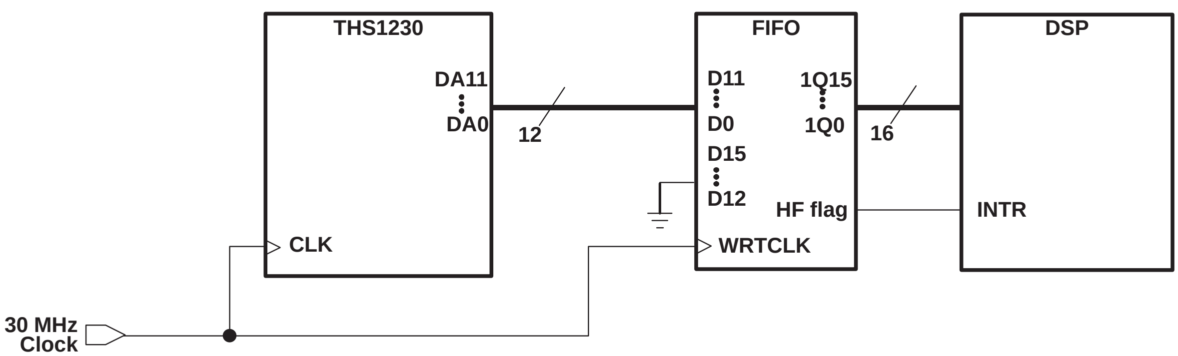


Figure 20. FIFO Connection

layout, decoupling and grounding rules

Proper grounding and layout of the PCB on which THS1230 is populated is essential to achieve the stated performance. It is advised to use separate analog and digital ground planes that are spliced underneath the IC. THS1230 has digital and analog pins on opposite sides of the package to make this easier. Since there is no connection internally between analog and digital grounds, they have to be joined on the PCB. It is advised to do this at one point in close proximity to THS1230.

Because of the high sampling rate and switched-capacitor architecture, THS1230 generates transients on the supply and reference lines. Proper decoupling of these lines is therefore essential. Decoupling is recommended as shown in the schematic of the THS1230 evaluation module in this data sheet.

PRINCIPLES OF OPERATION

definitions of specifications and terminology

integral nonlinearity (INL)

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs 1/2 LSB before the first code transition. The full-scale point is defined as level 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two end points.

differential nonlinearity (DNL)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, this measure indicates how uniform the transfer function step sizes are. The ideal step size is defined here as the step size for the device under test, i.e. (last transition level – first transition level)/(2n –2). Using this definition for DNL separates the effects of gain and offset error. A minimum DNL better than –1 LSB ensures no missing codes.

offset and gain error

Offset error (in LSBs) is defined as the average offset for all inputs, and gain error is defined as the maximum error (in LSBs) caused by the angular deviation from the offset corrected straight line.

analog input bandwidth

The analog input bandwidth is defined as the maximum frequency of a 1 –dBFS input sine wave that can be applied to the device for which an extra 3 –dB attenuation is observed in the reconstructed output signal.

output timing

Output timing td(O) is measured from the 50% level of the CLK input falling edge to the 10%/90% level of the digital output. The digital output load is not higher than 10 pF.

Output hold time $t_{h(O)}$ is measured from the 50% level of the CLK input falling edge to the10%/90% level of the digital output. The digital output load is not less than 2 pF.

Aperture delay $t_{d(A)}$ is measured from the 50% level of the CLK input to the actual sampling instant.

The OE signal is asynchronous.

OE timing $t_{d(PZ)}$ is measured from the $V_{IH(min)}$ level of OE to the high-impedance state of the output data. The digital output load is not higher than 10 pF.

OE timing $t_{d(EN)}$ is measured from the $V_{IL(max)}$ level of OE to the instant when the output data reaches $V_{OH(min)}$ or $V_{OL(max)}$ output levels. The digital output load is not higher than 10 pF.

signal-to-noise ratio + distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

PRINCIPLES OF OPERATION

definitions of specifications and terminology (continued)

effective number of bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

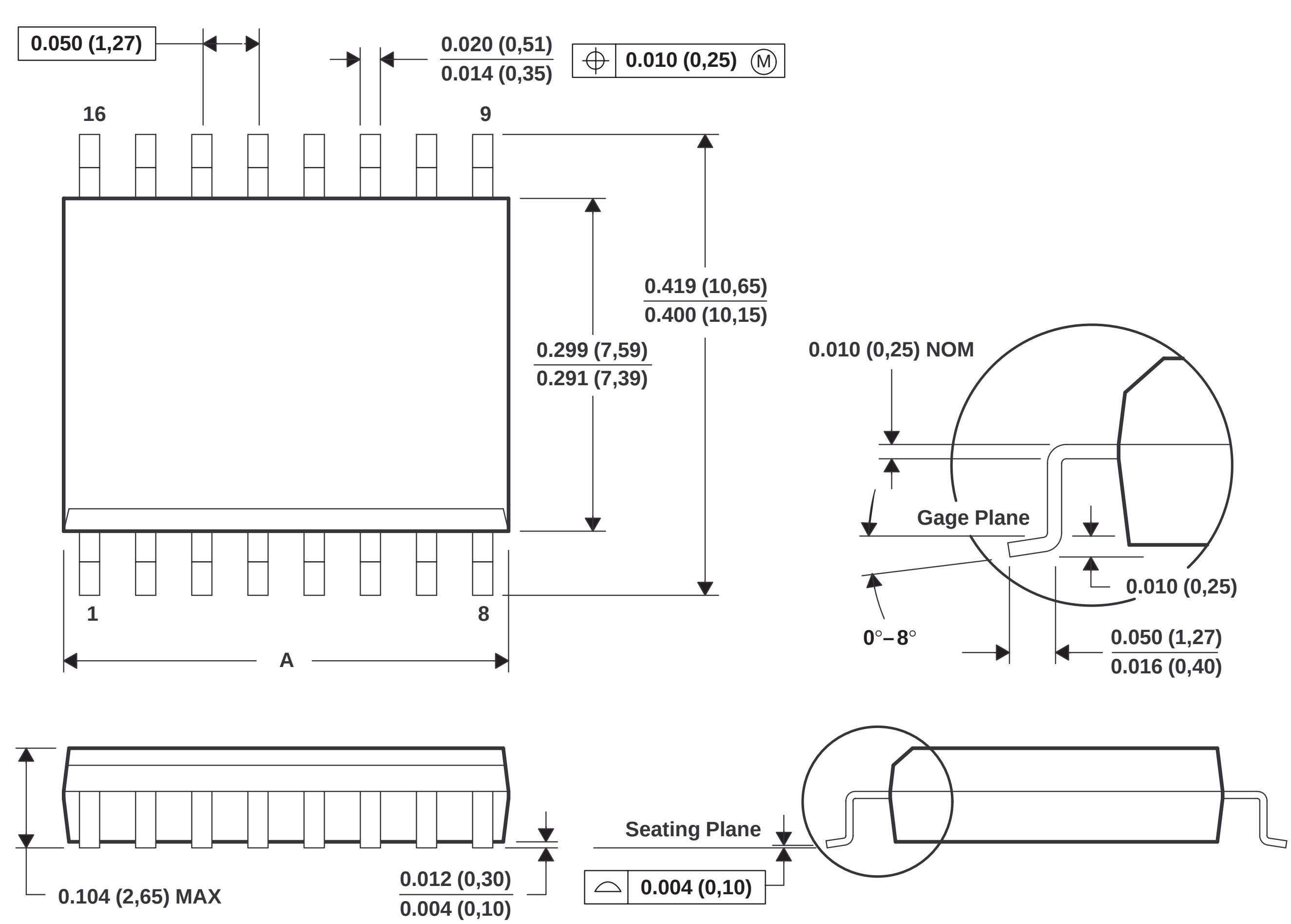
spurious free dynamic range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

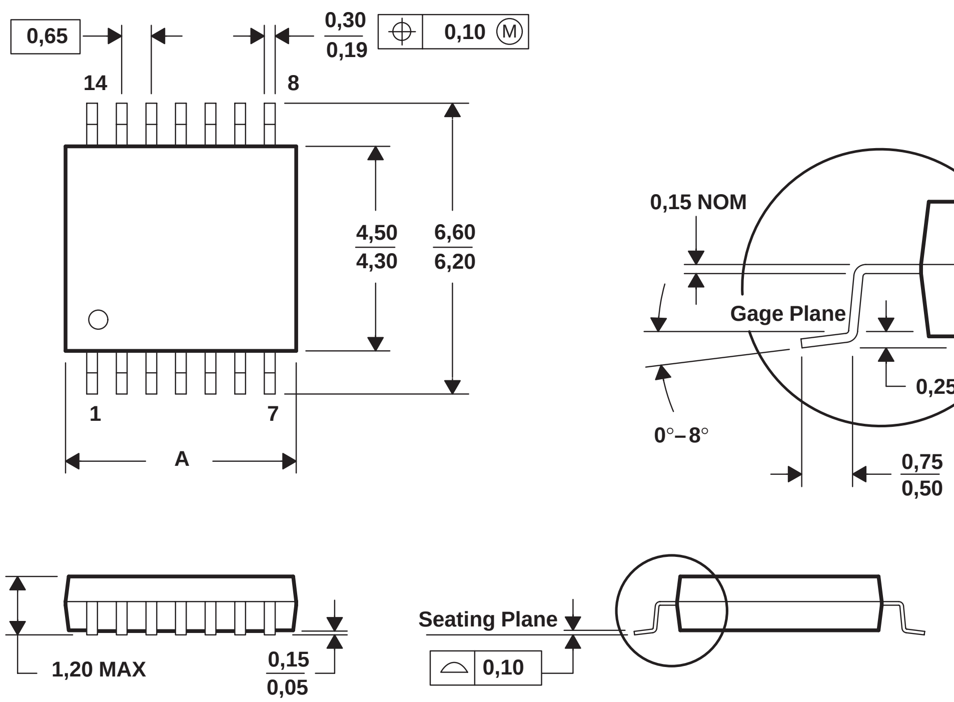
4040000/D 01/00

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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