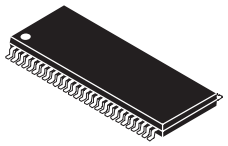


DIGITAL AMPLIFIER POWER STAGE

TM

FEATURES

- 50 W per Channel (BTL) Into 6 Ω (Stereo)
- 95-dB Dynamic Range With TAS5026
- Less Than 0.1% THD+N (1 W RMS Into 6 Ω)
- Less Than 0.2% THD+N (50 W RMS into 6 Ω)
- Power Efficiency Typically 90% Into 6-Ω Load
- Self-Protecting Design (Undervoltage, Overtemperature and Short Conditions) With Error Reporting
- Internal Gate Drive Supply Voltage Regulator
- EMI Compliant When Used With Recommended System Design

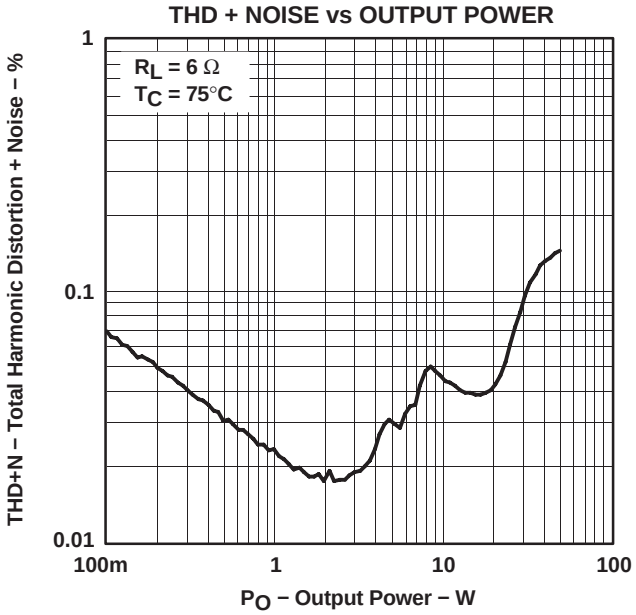
APPLICATIONS

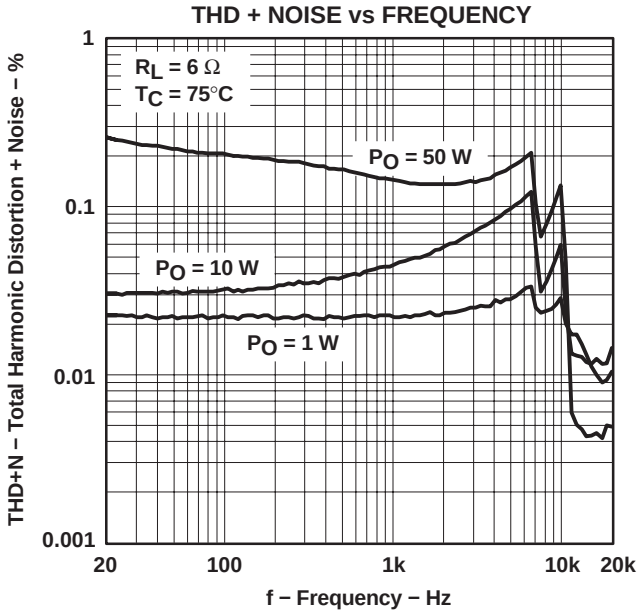
- DVD Receiver
- Home Theatre
- Mini/Micro Component Systems
- Internet Music Appliance

DESCRIPTION

The TAS5112 is a high-performance, integrated stereo digital amplifier power stage designed to drive 6-Ω speakers at up to 50 W per channel. The device incorporates TI's PurePath Digital™ technology and is used with a digital audio PWM processor (TAS50XX) and a simple passive demodulation filter to deliver high-quality, high-efficiency, true-digital audio amplification.

The efficiency of this digital amplifier is typically 90%, reducing the size of both the power supplies and heatsinks needed. Overcurrent protection, overtemperature protection, and undervoltage protection are built into the TAS5112, safeguarding the device and speakers against fault conditions that could damage the system.





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Other trademarks are the property of their respective owners.

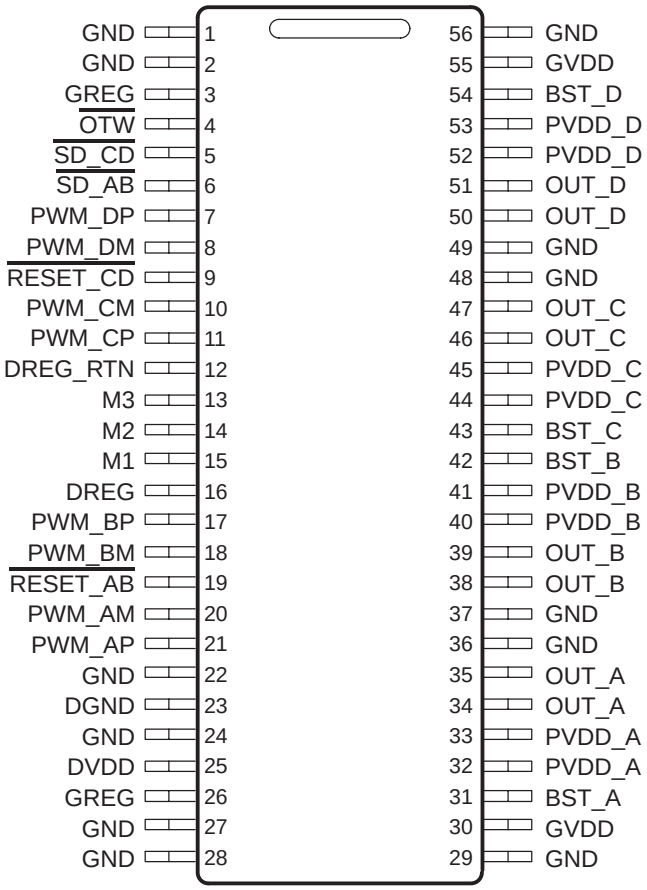
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

GENERAL INFORMATION

Terminal Assignment

The TAS5112 is offered in a thermally enhanced 56-pin TSSOP DFD (thermal pad is on the top), shown as follows.

DFD PACKAGE
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

TAS5112	UNITS
DVDD TO DGND	–0.3 V to 4.2 V
GVDD TO GND	33.5 V
PVDD_X TO GND (dc voltage)	33.5 V
PVDD_X TO GND (spike voltage(2))	48 V
OUT_X TO GND (dc voltage)	33.5 V
OUT_X TO GND (spike voltage(2))	48 V
BST_X TO GND (dc voltage)	48 V
BST_X TO GND (spike voltage(2))	53 V
GREG TO GND (3)	14.2 V
PWM_XP, $\overline{\text{RESET}}$, M1, M2, M3, $\overline{\text{SD}}$, $\overline{\text{OTW}}$	–0.3 V to DVDD + 0.3 V
Maximum operating junction temperature, T_J	–40°C to 150°C
Storage temperature	–40°C to 125°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The duration of voltage spike should be less than 100 ns.
(3) GREG is treated as an input when the GREG pin is overdriven by GVDD of 12 V.

ORDERING INFORMATION

T_A	PACKAGE	DESCRIPTION
0°C to 70°C	TAS5112DFD	56-pin small TSSOP

(1) For the most current specification and package information, refer to our Web site at www.ti.com.

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)
56-pin DAD TSSOP	1.14	See Note 1

(1) The TAS5112 package is thermally enhanced for conductive cooling using an exposed metal pad area. It is impractical to use the device with the pad exposed to ambient air as the only heat sinking of the device.

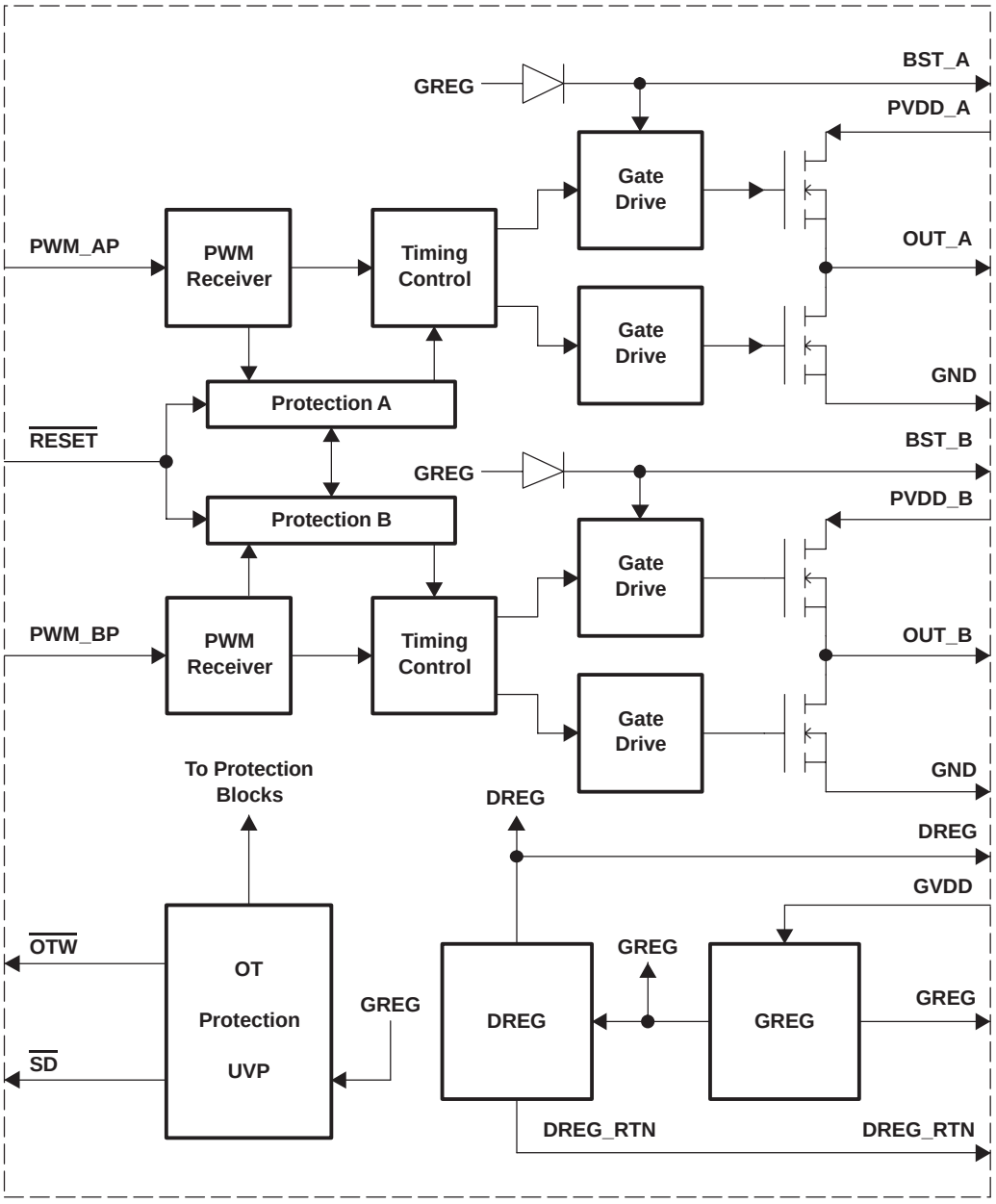
For this reason, $R_{\theta JA}$, a system parameter that characterizes the thermal treatment, is provided in the *Application Information* section of the data sheet. An example and discussion of typical system $R_{\theta JA}$ values are provided in the *Thermal Information* section. This example provides additional information regarding the power dissipation ratings. This example should be used as a reference to calculate the heat dissipation ratings for a specific application. TI application engineering provides technical support to design heatsinks if needed.

Terminal Functions

TERMINAL		FUNCTION(1)	DESCRIPTION
NAME	NO.		
BST_A	31	P	High-side bootstrap supply (BST), external capacitor to OUT_A required
BST_B	42	P	High-side bootstrap supply (BST), external capacitor to OUT_B required
BST_C	43	P	HS bootstrap supply (BST), external capacitor to OUT_C required
BST_D	54	P	HS bootstrap supply (BST), external capacitor to OUT_D required
DGND	23	P	Digital I/O reference ground
DREG	16	P	Digital supply voltage regulator decoupling pin, capacitor connected to GND
DREG_RTN	12	P	Digital supply voltage regulator decoupling return pin
DVDD	25	P	I/O reference supply input (3.3 V)
GND	1, 2, 22, 24, 27, 28, 29, 36, 37, 48, 49, 56	P	Power ground
GREG	3, 26	P	Gate drive voltage regulator decoupling pin, capacitor to REG_GND
GVDD	30, 55	P	Voltage supply to on-chip gate drive and digital supply voltage regulators
M1 (TST0)	15	I	Mode selection pin
M2	14	I	Mode selection pin
M3	13	I	Mode selection pin
$\overline{\text{OTW}}$	4	O	Overtemperature warning output, open drain with internal pullup resistor
OUT_A	34, 35	O	Output, half-bridge A
OUT_B	38, 39	O	Output, half-bridge B
OUT_C	46, 47	O	Output, half-bridge C
OUT_D	50, 51	O	Output, half-bridge D
PVDD_A	32, 33	P	Power supply input for half-bridge A
PVDD_B	40, 41	P	Power supply input for half-bridge B
PVDD_C	44, 45	P	Power supply input for half-bridge C
PVDD_D	52, 53	P	Power supply input for half-bridge D
PWM_AM	20	I	Input signal (negative), half-bridge A
PWM_AP	21	I	Input signal (positive), half-bridge A
PWM_BM	18	I	Input signal (negative), half-bridge B
PWM_BP	17	I	Input signal (positive), half-bridge B
PWM_CM	10	I	Input signal (negative), half-bridge C
PWM_CP	11	I	Input signal (positive), half-bridge C
PWM_DM	8	I	Input signal (negative), half-bridge D
PWM_DP	7	I	Input signal (positive), half-bridge D
$\overline{\text{RESET\_AB}}$	19	I	Reset signal, active low
$\overline{\text{RESET\_CD}}$	9	I	Reset signal, active low
$\overline{\text{SD\_AB}}$	6	O	Shutdown signal for half-bridges A and B, active-low
$\overline{\text{SD\_CD}}$	5	O	Shutdown signal for half-bridges C and D, active-low

(1) I = input, O = Output, P = Power

FUNCTIONAL BLOCK DIAGRAM



This diagram shows one channel.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
DVDD	Digital supply (1)	Relative to DGND	3	3.3	3.6	V
GVDD	Supply for internal gate drive and logic regulators	Relative to GND	16	29.5	30.5	V
PVDD_x	Half-bridge supply	Relative to GND, R_L = 6 Ω to 8 Ω	0	29.5	30.5	V
T_J	Junction temperature		0		125	°C

(1) It is recommended for DVDD to be connected to DREG via a 100-Ω resistor.

ELECTRICAL CHARACTERISTICS

PVDD_X = 29.5 V, GVDD = 29.5 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 6 Ω, 8X f_S = 384 kHz, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE				
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	T_A=40°C TO 85°C	UNITS	MIN/TYP/ MAX
AC PERFORMANCE, BTL Mode, 1 kHz								
Po	Output power	R_L = 8 Ω, THD = 0.2%, AES17 filter, 1 kHz			40		W	Typ
		R_L = 8 Ω, THD = 10%, AES17 filter, 1 kHz			50		W	Typ
		R_L = 6 Ω, THD = 0.2%, AES17 filter, 1 kHz			50		W	Typ
		R_L = 6 Ω, THD = 10%, AES17 filter, 1 kHz			62		W	Typ
THD+N	Total harmonic distortion + noise	Po = 1 W/ channel, R_L = 6 Ω, AES17 filter			0.03%			Typ
		Po = 10 W/channel, R_L = 6 Ω, AES17 filter			0.04%			Typ
		Po = 50 W/channel, R_L = 6 Ω, AES17 filter			0.2%			Typ
V_n	Output integrated voltage noise	A-weighted, mute, R_L = 6 Ω,, 20 Hz to 20 kHz, AES17 filter			260		μV	Max
SNR	Signal-to-noise ratio	A-weighted, AES17 filter			96		dB	Typ
DR	Dynamic range	f = 1 kHz, A-weighted, AES17 filter			96		dB	Typ
INTERNAL VOLTAGE REGULATOR								
DREG	Voltage regulator	I_O = 1 mA, PVDD = 18 V−30.5 V	3.1				V	Typ
GREG	Voltage regulator	I_O = 1.2 mA, PVDD = 18 V−30.5 V	13.4				V	Typ
IVGDD	GVDD supply current, operating	f_S = 384 kHz, no load, 50% duty cycle		24			mA	Max
IDVDD	DVDD supply current, operating	f_S = 384 kHz, no load	1	5			mA	Max
OUTPUT STAGE MOSFETs								
$R_{on,LS}$	Forward on-resistance, low side	T_J = 25°C	155				mΩ	Typ
$R_{on,HS}$	Forward on-resistance, high side	T_J = 25°C	155				mΩ	Typ

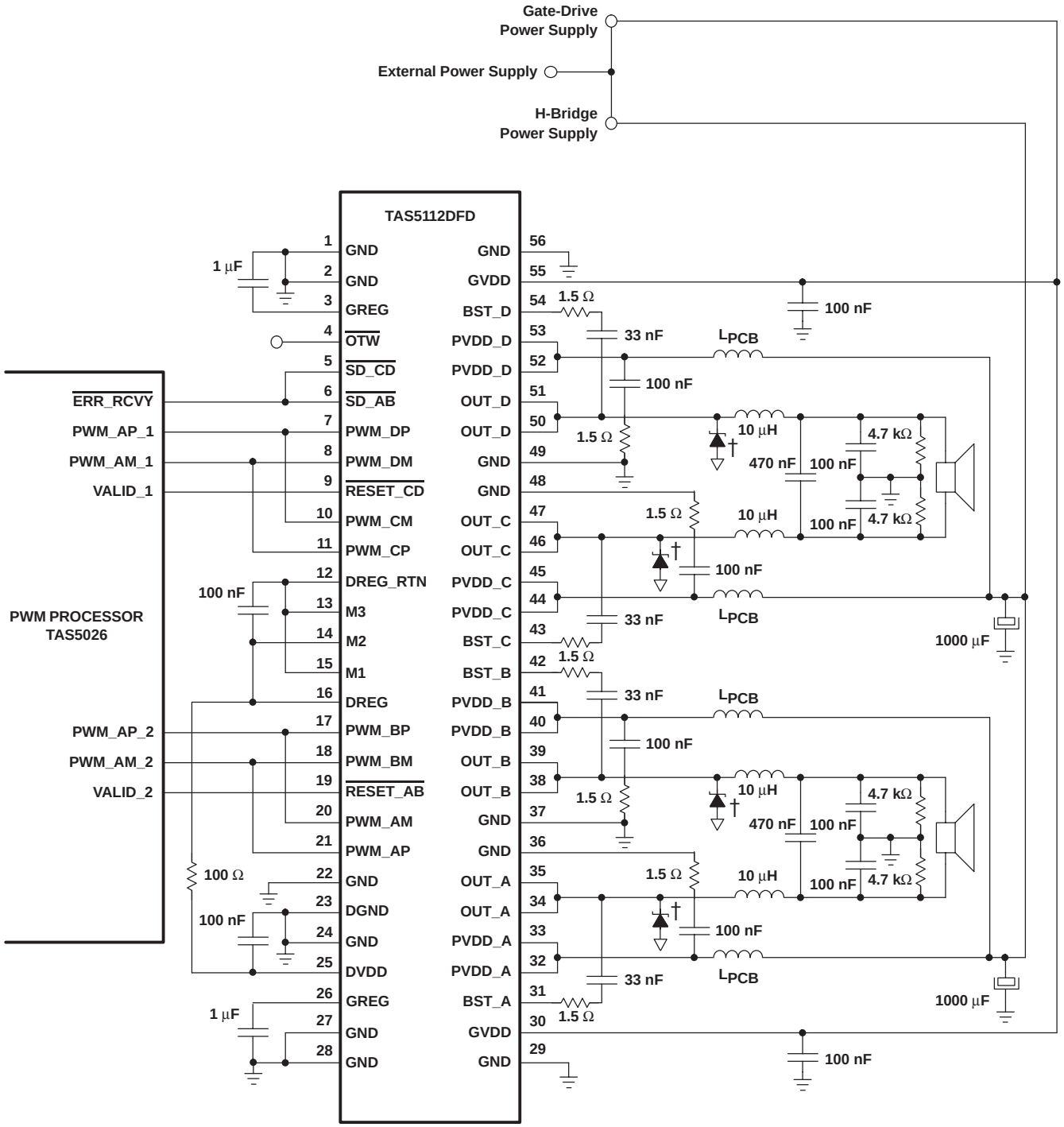
ELECTRICAL CHARACTERISTICS

PVDD_x = 29.5 V, GVDD = 29.5 V, DVDD connected to DREG via a 100-Ω resistor, R_L = 6 Ω, 8X f_S = 384 kHz, unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS	TYPICAL	OVER TEMPERATURE				
			T_A=25°C	T_A=25°C	T_{Case}= 75°C	T_A=40°C TO 85°C	UNITS	MIN/TYP/ MAX
INPUT/OUTPUT PROTECTION								
$V_{uvp,G}$	Undervoltage protection limit, GVDD	Set the DUT in normal operation mode with all the protections enabled. Sweep GVDD up and down. Monitor $\overline{SD}$ output. Record the GREG reading when $\overline{SD}$ is triggered.	7.4	6.9			V	Min
				7.9			V	Max
OTW	Overtemperature warning, junction temperature		125				°C	Typ
OTE	Overtemperature error, junction temperature		150				°C	Typ
OC	Overcurrent protection	See Note 1.	5.8				A	Typ
STATIC DIGITAL SPECIFICATION								
	PWM_AP, PWM_BP, M1, M2, M3, $\overline{SD}$, $\overline{OTW}$							
V_{IH}	High-level input voltage			2			V	Min
				DVDD			V	Max
V_{IL}	Low-level input voltage			0.8			V	Max
Leakage	Input leakage current			−10			µA	Min
				10			µA	Max
OTW/SHUTDOWN (SD)								
	Internally pull up R from $\overline{OTW}$/$\overline{SD}$ to DVDD		30	22.5			kΩ	Min
V_{OL}	Low-level output voltage	I_O = 4 mA		0.4			V	Max

(1) To optimize device performance and prevent overcurrent (OC) protection tripping, the demodulation filter must be designed with special care. See *Demodulation Filter Design* in the *Application Information* section of the data sheet and consider the recommended inductors and capacitors for optimal performance. It is also important to consider PCB design and layout for optimum performance of the TAS5112. It is recommended to follow the TAS5112F2EVM (S/N 112) design and layout guidelines for best performance.

SYSTEM CONFIGURATION USED FOR CHARACTERIZATION



L_{PCB} : TRACK IN THE PCB (1,0 mm wide and 50 mm long)

†Voltage Suppressor Diode: 1SMA33CAT

TYPICAL CHARACTERISTICS AND SYSTEM PERFORMANCE OF TAS5112 EVM WITH TAS5026 PWM PROCESSOR

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

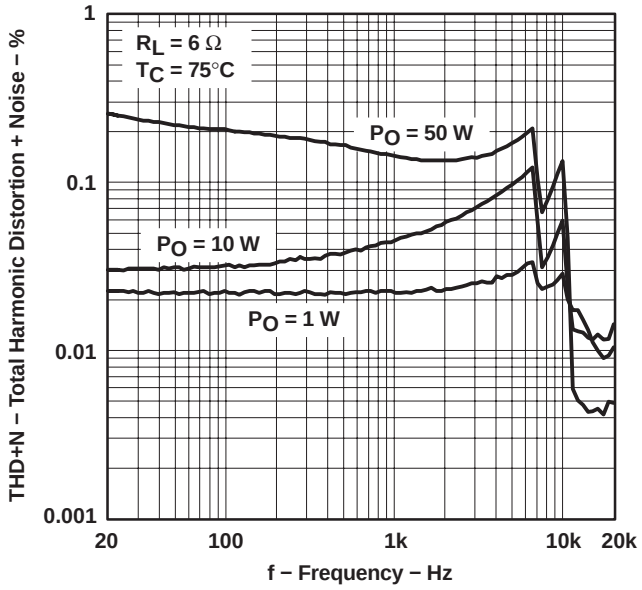


Figure 1

NOISE AMPLITUDE vs FREQUENCY

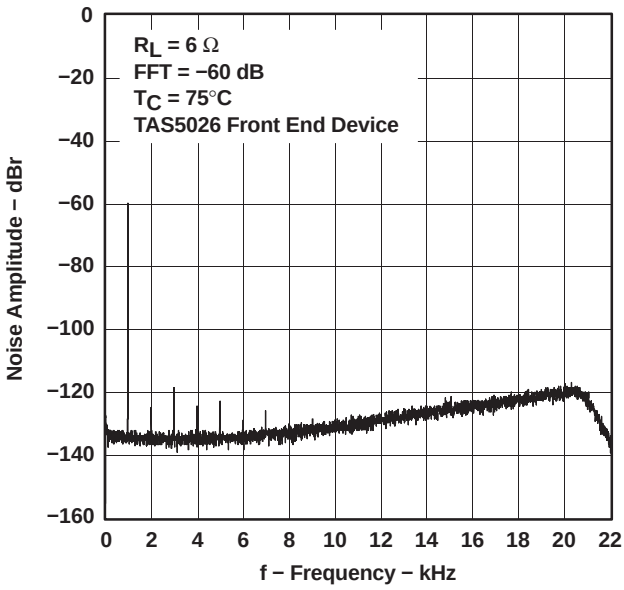


Figure 2

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

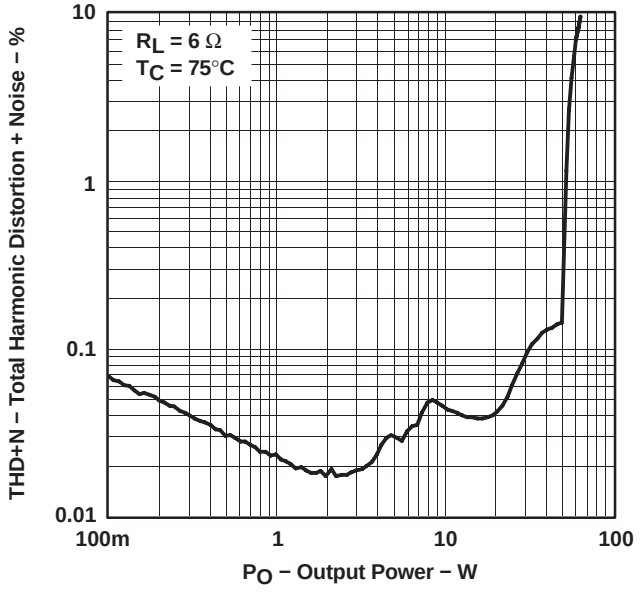


Figure 3

OUTPUT POWER vs H-BRIDGE VOLTAGE

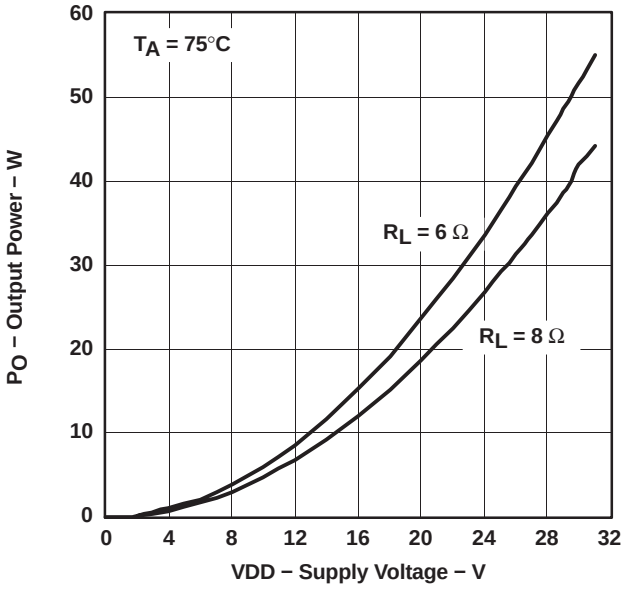


Figure 4

SYSTEM OUTPUT STAGE EFFICIENCY vs OUTPUT POWER

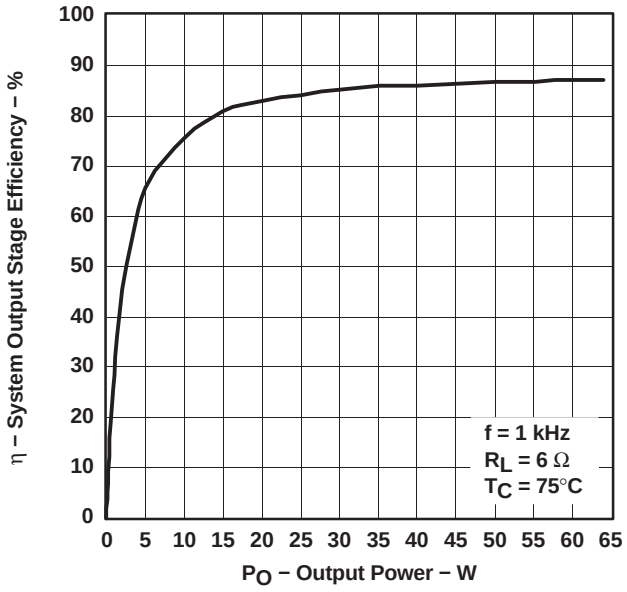


Figure 5

POWER LOSS vs OUTPUT POWER

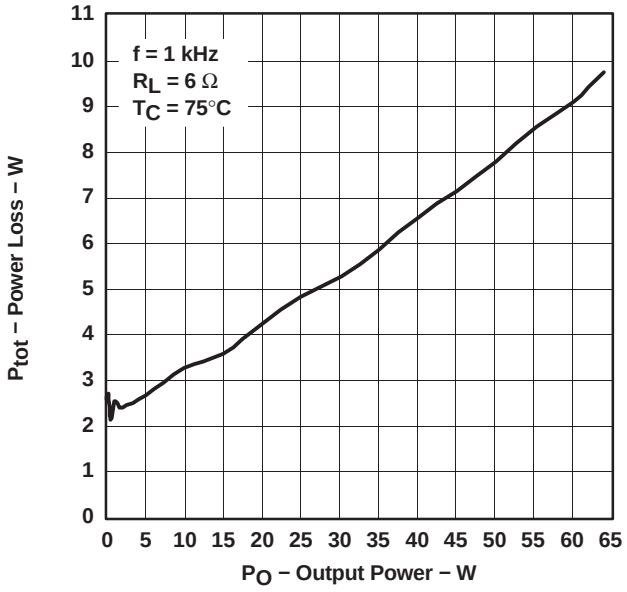


Figure 6

OUTPUT POWER vs CASE TEMPERATURE

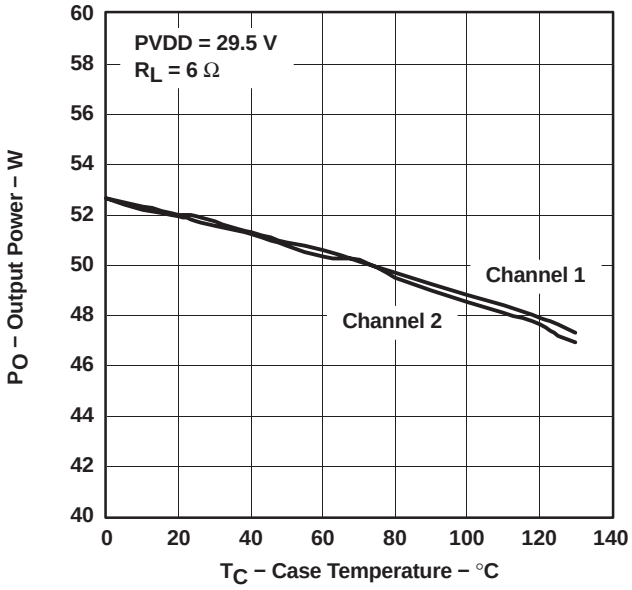


Figure 7

AMPLITUDE vs FREQUENCY

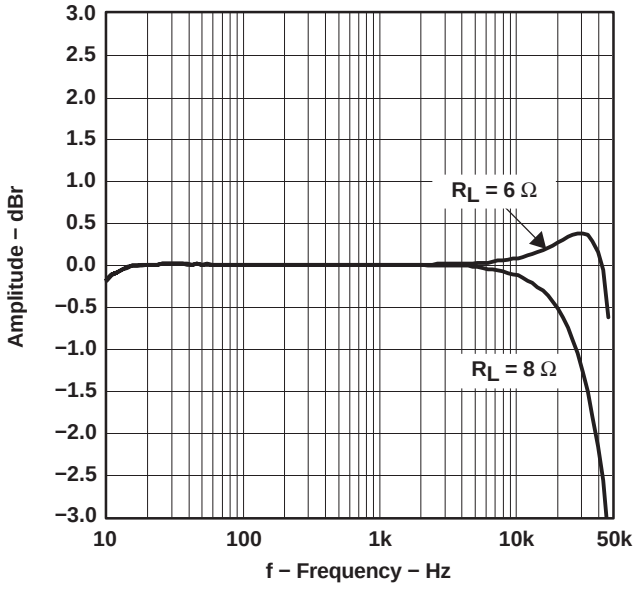


Figure 8

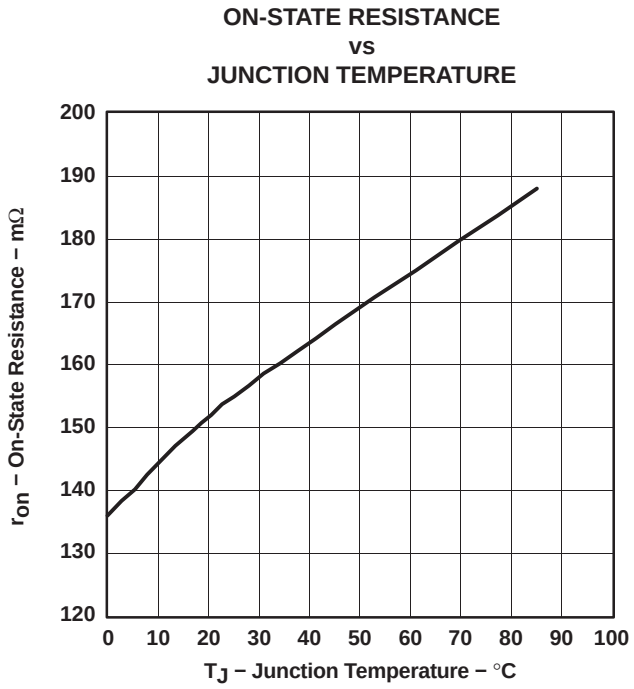

ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE
200
190
180
170
160
150
140
130
120
0
10
20
30
40
50
60
70
80
90
100
rON − On-State Resistance − mΩ
TJ − Junction Temperature − °C

Figure 9

THEORY OF OPERATION

POWER SUPPLIES

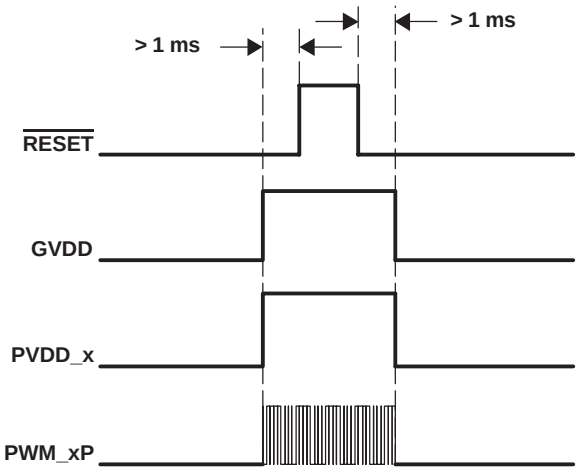
The power device only requires two supply voltages, GVDD and PVDD_X.

GVDD is the gate drive supply for the device, regulated internally down to approximately 12 V, and decoupled with regards to board GND on the GREG pins through an external capacitor. GREG powers both the low side and high side via a bootstrap step-up conversion. The bootstrap supply is charged after the first low-side turn-on pulse. Internal digital core voltage DREG is also derived from GVDD and regulated down by internal circuitry to 3.3 V.

The gate-driver regulator can be bypassed for reducing idle loss in the device by shorting GREG to GVDD and directly feeding in 12.0 V. This can be useful in an application where thermal conduction of heat from the device is difficult.

PVDD_X is the H-bridge power supply pin. Two power pins exists for each half-bridge to handle the current density. It is important that the circuitry recommendations around the PVDD_X pins are followed carefully both topology- and layout-wise. For topology recommendations, see the *Typical System Configuration* section. Following these recommendations is important for parameters like EMI, reliability, and performance.

POWERING UP



NOTE: PVDD should not be powered up before GVDD.

During power up when $\overline{\text{RESET}}$ is asserted LOW, all MOSFETs are turned off and the two internal half-bridges are in the high-impedance state (Hi-Z). The bootstrap capacitors supplying high-side gate drive are not charged at this point. To comply with the click and pop scheme and use of non-TI modulators it is recommended to use a 4-kΩ pulldown resistor on each PWM output node to ground. This precharges the bootstrap supply capacitors and discharges the output filter capacitor (see the *Typical TAS5112 Application Configuration* section).

After GVDD has been applied, it takes approximately 800 µs to fully charge the BST capacitor. Within this time, $\overline{\text{RESET}}$ must be kept low. After approximately 1 ms, the back-end bootstrap capacitor is charged.

$\overline{\text{RESET}}$ can now be released if the modulator is powered up and streaming valid PWM signals to the back-end PWM_xP. Valid means a switching PWM signal which complies with the frequency and duty cycle ranges stated in the *Recommended Operating Conditions*.

A constant HIGH dc level on the PWM_xP is not permitted, because it would force the high-side MOSFET ON until it eventually ran out of BST capacitor energy and might damage the device.

An unknown state of the PWM output signals from the modulator is illegal and should be avoided, which in practice means that the PWM processor must be powered up and initialized before $\overline{\text{RESET}}$ is de-asserted HIGH to the back end.

POWERING DOWN

For power down of the back end, an opposite approach is necessary. The $\overline{\text{RESET}}$ must be asserted LOW before the valid PWM signal is removed.

When PWM processors are used with TI PurePath Digital amplifiers, the correct timing control of $\overline{\text{RESET}}$ and PWM_xP is performed by the modulator.

PRECAUTION

The TAS5112 must always start up in the high-impedance (Hi-Z) state. In this state, the bootstrap (BST) capacitor is precharged by a resistor on each PWM output node to ground. See the system configuration. This ensures that the back end is ready for receiving PWM pulses, indicating either HIGH- or LOW-side turnon after $\overline{\text{RESET}}$ is de-asserted to the back end.

With the following pulldown resistor and BST capacitor size, the charge time is:

C = 33 nF, R = 4.7 kΩ
$R \times C \times 5 = 775.5$ µs

After GVDD has been applied, it takes approximately 800 µs to fully charge the BST capacitor. During this time, $\overline{\text{RESET}}$ must be kept low. After approximately 1 ms the back end BST is charged and ready. $\overline{\text{RESET}}$ can now be released if the PWM modulator is ready and is streaming valid PWM signals to the back end. Valid PWM signals are switching PWM signals with a frequency between 350−400 kHz. A constant HIGH level on the PWM+ would force the high-side MOSFET ON until it eventually ran out of BST capacitor energy. Putting the device in this condition should be avoided.

In practice this means that the DVDD-to-PWM processor (front-end) should be stable and initialization should be completed before $\overline{\text{RESET}}$ is de-asserted to the back end.

CONTROL I/O

Shutdown Pin: $\overline{\text{SD}}$

The $\overline{\text{SD}}$ pin functions as an output pin and is intended for protection-mode signaling to, for example, a controller or other front-end device. The pin is open-drain with an internal pullup resistor to DVDD.

The logic output is, as shown in the following table, a combination of the device state and $\overline{\text{RESET}}$ input:

$\overline{\text{SD}}$	$\overline{\text{RESET}}$	DESCRIPTION
0	0	Not used
0	1	Device in protection mode, i.e., UVP and/or OC and/or OT error
1(1)	0	Device set high-impedance (Hi-Z), $\overline{\text{SD}}$ forced high
1	1	Normal operation

(1) $\overline{\text{SD}}$ is pulled high when $\overline{\text{RESET}}$ is asserted low independent of chip state (i.e., protection mode). This is desirable to maintain compatibility with some TI PWM front ends.

Temperature Warning Pin: $\overline{\text{OTW}}$

The $\overline{\text{OTW}}$ pin gives a temperature warning signal when temperature exceeds the set limit. The pin is of the open-drain type with an internal pullup resistor to DVDD.

$\overline{\text{OTW}}$	DESCRIPTION
0	Junction temperature higher than 125°C
1	Junction temperature lower than 125°C

Overall Reporting

The $\overline{\text{SD}}$ pin, together with the $\overline{\text{OTW}}$ pin, gives chip state information as described in Table 1.

Table 1. Error Signal Decoding

$\overline{\text{OTW}}$	$\overline{\text{SD}}$	DESCRIPTION
0	0	Overtemperature error (OTE)
0	1	Overtemperature warning (OTW)
1	0	Overcurrent (OC) or undervoltage (UVP) error
1	1	Normal operation, no errors/warnings

Chip Protection

The TAS5112 protection function is implemented in a closed loop with, for example, a system controller and TI PWM processor. The TAS5112 contains three individual systems protecting the device against error conditions. All of the error events covered result in the output stage being set in a high-impedance state (Hi-Z) for maximum protection of the device and connected equipment.

The device can be recovered by toggling $\overline{\text{RESET}}$ low and then high, after all errors are cleared.

Overcurrent (OC) Protection

The device has individual forward current protection on both high-side and low-side power stage FETs. The OC protection works only with the demodulation filter present at the output. See *Demodulation Filter Design* in the *Application Information* section of the data sheet for design constraints.

Overtemperature (OT) Protection

A dual temperature protection system asserts a warning signal when the device junction temperature exceeds 125°C. The OT protection circuit is shared by all half-bridges.

Undervoltage (UV) Protection

Undervoltage lockout occurs when GVDD is insufficient for proper device operation. The UV protection system protects the device under power-up and power-down situations. The UV protection circuits are shared by all half-bridges.

Reset Function

The function of the reset input is twofold:

- Reset is used for re-enabling operation after a latching error event.
- Reset is used for disabling output stage switching (mute function).

The error latch is cleared on the falling edge of reset and normal operation is resumed when reset goes high.

PROTECTION MODE

Autorecovery (AR) After Errors (PMODE0)

In autorecovery mode (PMODE0) the TAS5112 is self-supported in handling of error situations. All protection systems are active, setting the output stage in the high-impedance state to protect the output stage and connected equipment. However, after a short time the device autorecovers, i.e., operation is automatically resumed provided that the system is fully operational.

The autorecovery timing is set by counting PWM input cycles, i.e., the timing is relative to the switching frequency.

The AR system is common to both half-bridges.

Timing and Function

The function of the autorecovery circuit is as follows:

1. An error event occurs and sets the protection latch (output stage goes Hi-Z).
2. The counter is started.
3. After n/2 cycles, the protection latch is cleared but the output stage remains Hi-Z (identical to pulling $\overline{\text{RESET}}$ low).
4. After n cycles, operation is resumed (identical to pulling $\overline{\text{RESET}}$ high) (n = 512).

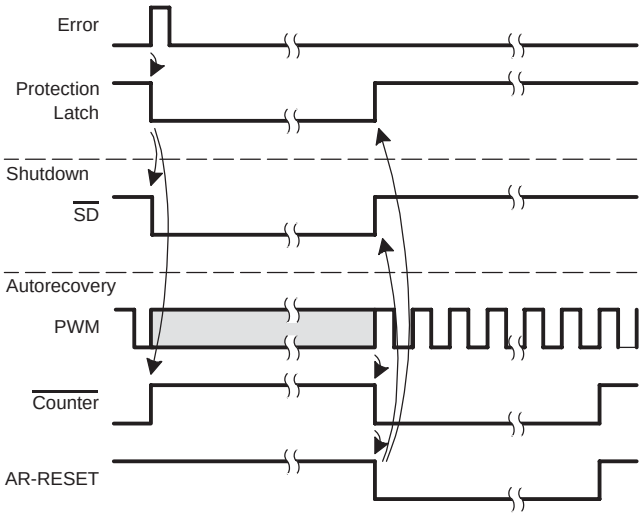


Figure 10. Autorecovery Function

Latching Shutdown on All Errors (PMODE1)

In latching shutdown mode, all error situations result in a power down (output stage Hi-Z). Re-enabling can be done by toggling the $\overline{\text{RESET}}$ pin.

All Protection Systems Disabled (PMODE2)

In PMODE2, all protection systems are disabled. This mode is purely intended for testing and characterization purposes and thus not recommended for normal device operation.

MODE Pins Selection

The protection mode is selected by shorting M1/M2 to DREG or DGND according to Table 2.

Table 2. Protection Mode Selection

M1	M2	PROTECTION MODE
0	0	Autorecovery after errors (PMODE 0)
0	1	Latching shutdown on all errors (PMODE 1)
1	0	All protection systems disabled (PMODE 2)
1	1	Reserved

The output configuration mode is selected by shorting the M3 pin to DREG or DGND according to Table 3.

Table 3. Output Mode Selection

M3	OUTPUT MODE
0	Bridge-tied load output stage (BTL)
1	Reserved

APPLICATION INFORMATION

DEMODULATION FILTER DESIGN

The PurePath Digital amplifier outputs are driven by heavy-duty DMOS transistors in an H-bridge configuration. These transistors are either off or fully on, which reduces the DMOS transistor on-state resistance, R(DMOSon), and the power dissipated in the device, thereby increasing efficiency.

The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. For this application, EMI is considered important; therefore, the selected filter is the full-output type shown in Figure 11.

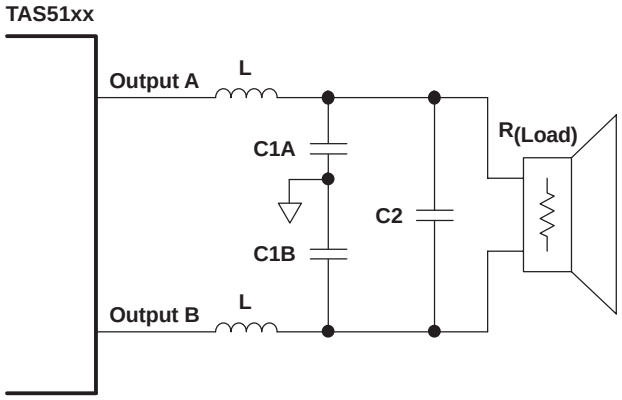


Figure 11. Demodulation Filter

The main purpose of the output filter is to attenuate the high-frequency switching component of the PurePath Digital amplifier while preserving the signals in the audio band.

Design of the demodulation filter affects the performance of the power amplifier significantly. As a result, to ensure proper operation of the overcurrent (OC) protection circuit and meet the device THD+N specifications, the selection of the inductors used in the output filter must be considered according to the following. The rule is that the inductance should remain stable within the range of peak current seen at maximum output power and deliver at least 5 μH of inductance at 15 A.

If this rule is observed, the TAS5112 does not have distortion issues due to the output inductors and overcurrent conditions do not occur due to inductor saturation in the output filter.

Another parameter to be considered is the idle current loss in the inductor. This can be measured or specified as inductor dissipation (D). The target specification for dissipation is less than 0.05.

In general, 10-μH inductors suffice for most applications. The frequency response of the amplifier is slightly altered by the change in output load resistance; however, unless tight control of frequency response is necessary (better than 0.5 dB), it is not necessary to deviate from 10 μH.

The graphs in Figure 12 display the inductance vs current characteristics of two inductors that are recommended for use with the TAS5112.

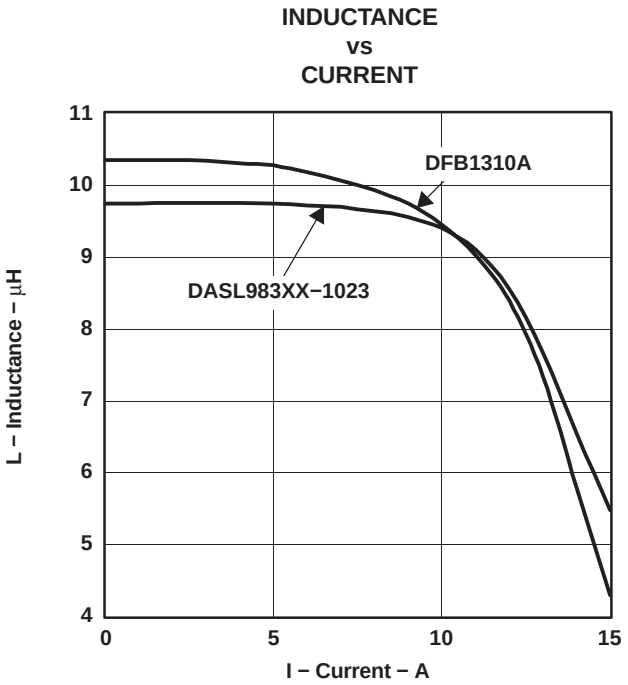


Figure 12. Inductance Saturation

The selection of the capacitor that is placed across the output of each inductor (C2 in Figure 11) is simple. To complete the output filter, use a 0.47-μF capacitor with a voltage rating at least twice the voltage applied to the output stage (PVDD).

This capacitor should be a good quality polyester dielectric such as a Wima MKS2-047ufd/100/10 or equivalent.

In order to minimize the EMI effect of unbalanced ripple loss in the inductors, 0.1-μF 50-V SMD capacitors (X7R or better) (C1A and C1B in Figure 11) should be added from the output of each inductor to ground.

THERMAL INFORMATION

The thermally augmented package provided with the TAS5112 is designed to be interfaced directly to heatsinks using a thermal interface compound (for example, Wakefield Engineering type 126 thermal grease.) The heatsink then absorbs heat from the ICs and couples it to the local air. If the heatsink is carefully designed, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the TAS5112, heatsinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with roughly the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the metal pad)
- Thermal grease thermal resistance
- Heatsink thermal resistance

$R_{\theta JC}$ has been provided in the *General Information* section.

The thermal grease thermal resistance can be calculated from the exposed pad area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W). The area thermal resistance of the example thermal grease with a 0.002-inch thick layer is about 0.1 °C-in^2/W. The approximate exposed pad area is as follows:

56-pin HTSSOP	0.045 in^2

Dividing the example thermal grease area resistance by the surface area gives the actual resistance through the thermal grease for both ICs inside the package:

56-pin HTSSOP	2.27 °C/W

The thermal resistance of thermal pads is generally considerably higher than a thin thermal grease layer. Thermal tape has an even higher thermal resistance. Neither pads nor tape should be used with either of these two packages. A thin layer of thermal grease with careful clamping of the heatsink is recommended. It may be difficult to achieve a layer 0.001-inch thick or less, so the modeling below is done with a 0.002-inch thick layer, which may be more representative of production thermal grease thickness.

Heatsink thermal resistance is generally predicted by the heatsink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal-grease resistance + heatsink resistance.

Table 4, Table 5, and Table 6 indicate modeled parameters for one or two TAS5112 ICs on a single heatsink. The final junction temperature is set at 110°C in

all cases. It is assumed that the thermal grease is 0.002 inch thick and that it is similar in performance to Wakefield Type 126 thermal grease. It is important that the thermal grease layer is ≤0.002 inches thick and that thermal pads or tape are not used in the pad-to-heatsink interface due to the high power density that results in these extreme power cases.

Table 4. Case 1 (2 × 50 W Unclipped Into 6 Ω, Both Channels in Same IC) (1)

	56-Pin HTSSOP
Ambient temperature	25°C
Power to load (per channel)	50 W (unclipped)
Power dissipation	4.5 W
Delta T inside package	10.2°C, note 2 × channel dissipation
Delta T through thermal grease	37.1°C, note 2 × channel dissipation
Required heatsink thermal resistance	4.2°C/W
Junction temperature	110°C
System $R_{\theta JA}$	19°C/W
$R_{\theta JA}$ * power dissipation	85°C
Junction temperature	85°C + 25°C = 110°C

(1) This case represents a stereo system with only one package. See Case 2 and Case 2A if doing a full-power, 2-channel test in a multichannel system.

Table 5. Case 2 (2 × 50 W Unclipped Into 6 Ω, Channels in Separate Packages) (1)

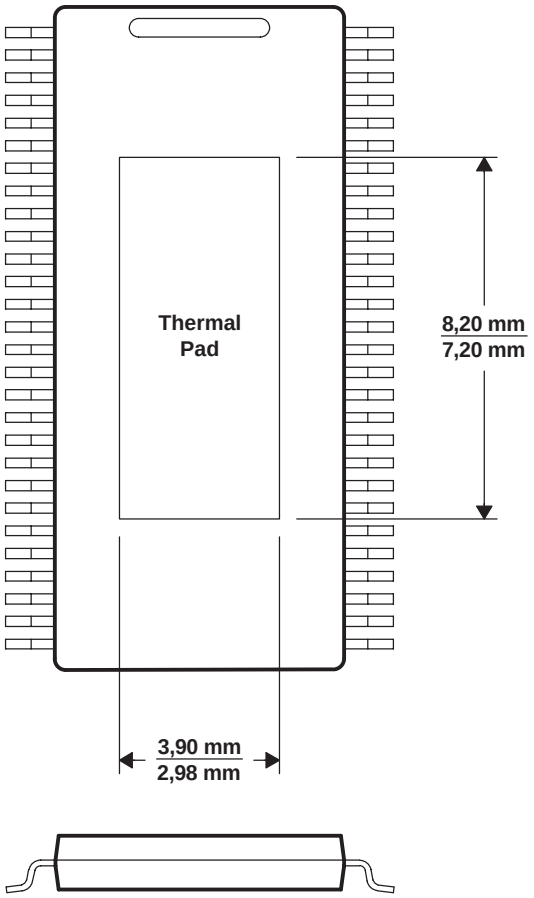
	56-Pin HTSSOP
Ambient temperature	25°C
Power to load (per channel)	50 W (unclipped)
Power dissipation	4.5 W
Delta T inside package	5.1°C
Delta T through thermal grease	18.6°C
Required heatsink thermal resistance	6.9°C/W
Junction temperature	110°C
System $R_{\theta JA}$	19°C/W
$R_{\theta JA}$ * power dissipation	85°C
Junction temperature	85°C + 25°C = 110°C

(1) In this case, the power is separated into two packages. Note that this allows a considerably smaller heatsink because twice as much area is available for heat transfer through the thermal grease. For this reason, separating the stereo channels into two ICs is recommended in full-power stereo tests made on multichannel systems.

Table 6. Case 2A (2 × 60 W Unclipped Into 6 Ω, Channels in Separate IC Packages) (1)

	56-Pin HTSSOP
Ambient temperature	25°C
Power to load (per channel)	60 W (10% THD)
Power dissipation per channel	5.4 W
Delta T inside package	6.1°C, note 2 × channel dissipation
Delta T through thermal grease	22.3°C, note 2 × channel dissipation
Required heatsink thermal resistance	5.3°C/W
Junction temperature	110°C
System $R_{\theta JA}$	15.9°C/W
$R_{\theta JA}$ * power dissipation	85°C
Junction temperature	85°C + 25°C = 110°C

(1) In this case, the power is also separated into two packages, but overdriving causes clipping to 10% THD. In this case, the high power requires extreme care in attachment of the heatsink to ensure that the thermal grease layer is ≤ 0.002 inches thick. Note that this power level should not be attempted with both channels in a single IC because of the high power density through the thermal grease layer.



CLICK AND POP REDUCTION

TI modulators feature a pop and click reduction system that controls the timing when switching starts and stops.

Going from nonswitching to switching operation causes a spectral energy burst to occur within the audio bandwidth, which is heard in the speaker as an audible click, for instance, after having asserted $\overline{\text{RESET}}$ LH during a system start-up.

To make this system work properly, the following design rules must be followed when using the TAS5112 back end:

- The relative timing between the PWM_AP/M_x signals and their corresponding VALID_x signal should not be skewed by inserting delays, because this increases the audible amplitude level of the click.
- The output stage must start switching from a fully discharged output filter capacitor. Because the output stage prior to operation is in the high-impedance state, this is done by having a passive pulldown resistor on each speaker output to GND (see *Typical System Configuration*).

Other things that can affect the audible click level:

- The spectrum of the click seems to follow the speaker impedance vs. frequency curve—the higher the impedance, the higher the click energy.
- Crossover filters used between woofer and tweeter in a speaker can have high impedance in the audio band, which should be avoided if possible.

Another way to look at it is that the speaker impulse response is a major contributor to how the click energy is shaped in the audio band and how audible the click will be.

The following mode transitions feature click and pop reduction.

STATE			CLICK AND POP REDUCED
Normal(1)	→	Mute	Yes
Mute	→	Normal(1)	Yes
Normal(1)	→	Error recovery (ERRCVY)	Yes
Error recovery	→	Normal(1)	Yes
Normal(1)	→	Hard Reset	No
Hard Reset	→	Normal(1)	Yes

(1) Normal = switching

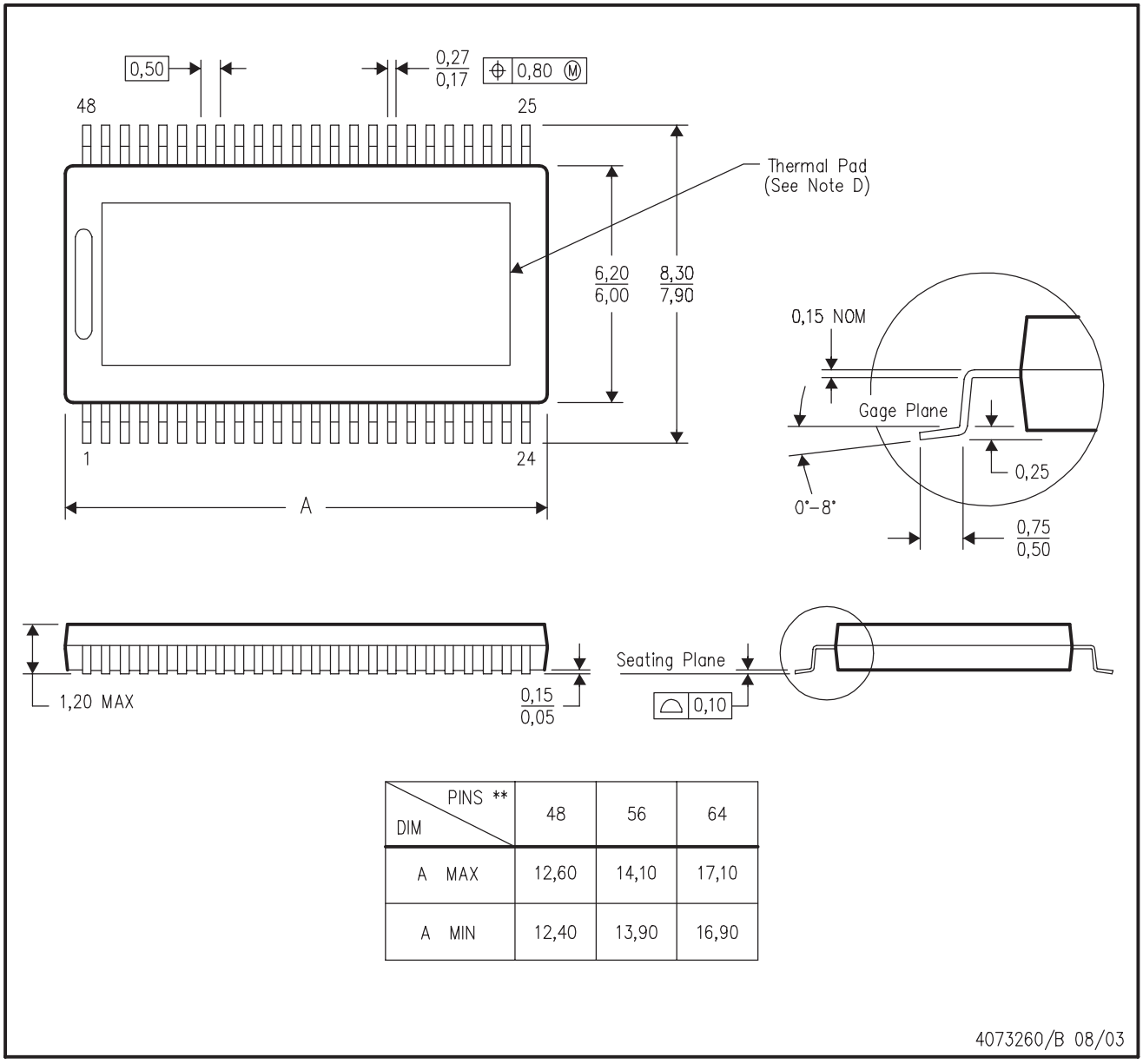
REFERENCES

1. *TAS5000 Digital Audio PWM Processor* data manual—TI (SLAS270)
2. *True Digital Audio Amplifier TAS5001 Digital Audio PWM Processor* data sheet—TI (SLES009)
3. *True Digital Audio Amplifier TAS5010 Digital Audio PWM Processor* data sheet—TI (SLAS328)
4. *True Digital Audio Amplifier TAS5012 Digital Audio PWM Processor* data sheet—TI (SLES006)
5. *TAS5026 Six-Channel Digital Audio PWM Processor* data manual—TI (SLES041)
6. *TAS5036A Six-Channel Digital Audio PWM Processor* data manual—TI (SLES061)
7. *TAS3103 Digital Audio Processor With 3D Effects* data manual—TI (SLES038)
8. *Digital Audio Measurements* application report—TI (SLAA114)
9. *PowerPAD™ Thermally Enhanced Package* technical brief—TI (SLMA002)
10. *System Design Considerations for True Digital Audio Power Amplifiers* application report—TI (SLAA117)

MECHANICAL DATA

DFD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

48 PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.
D. The package thermal performance may be enhanced by attaching an external heatsink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO–153

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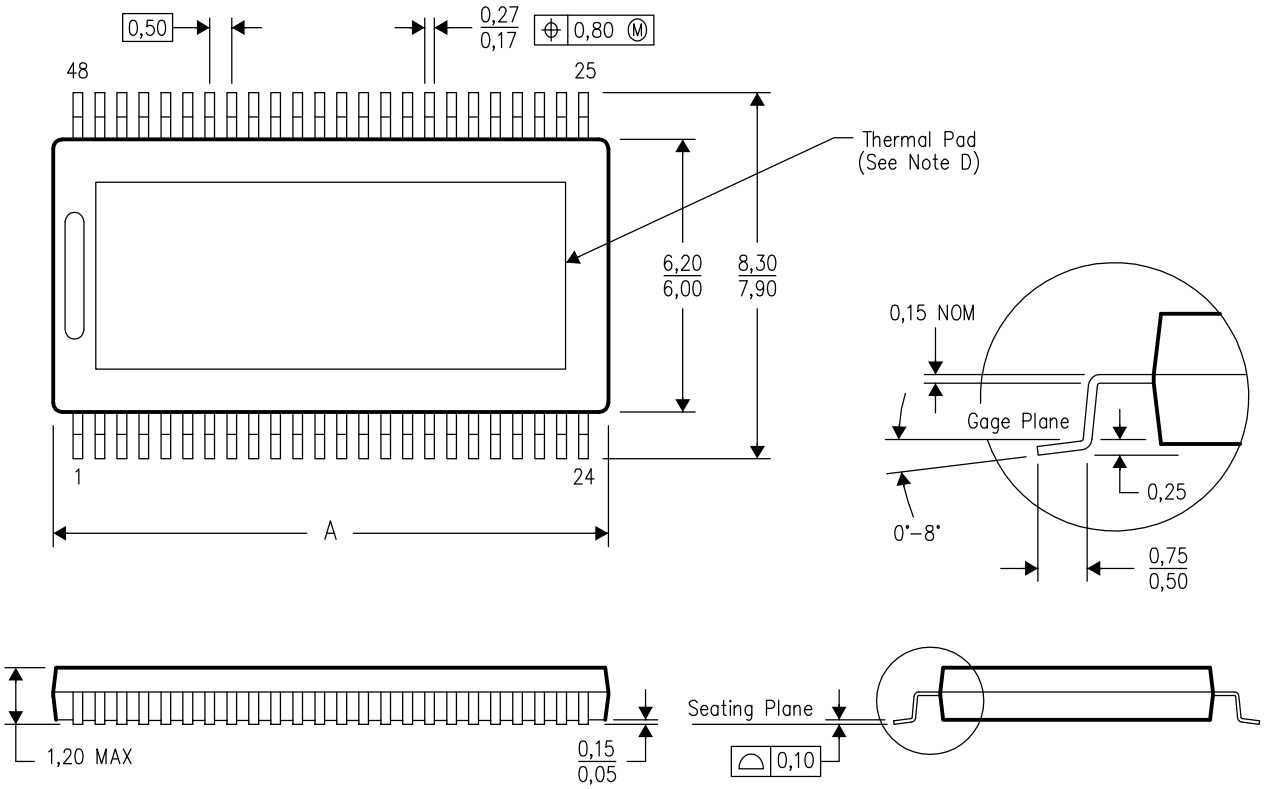
DFD (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)

48 PIN SHOWN



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4073260/B 08/03

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