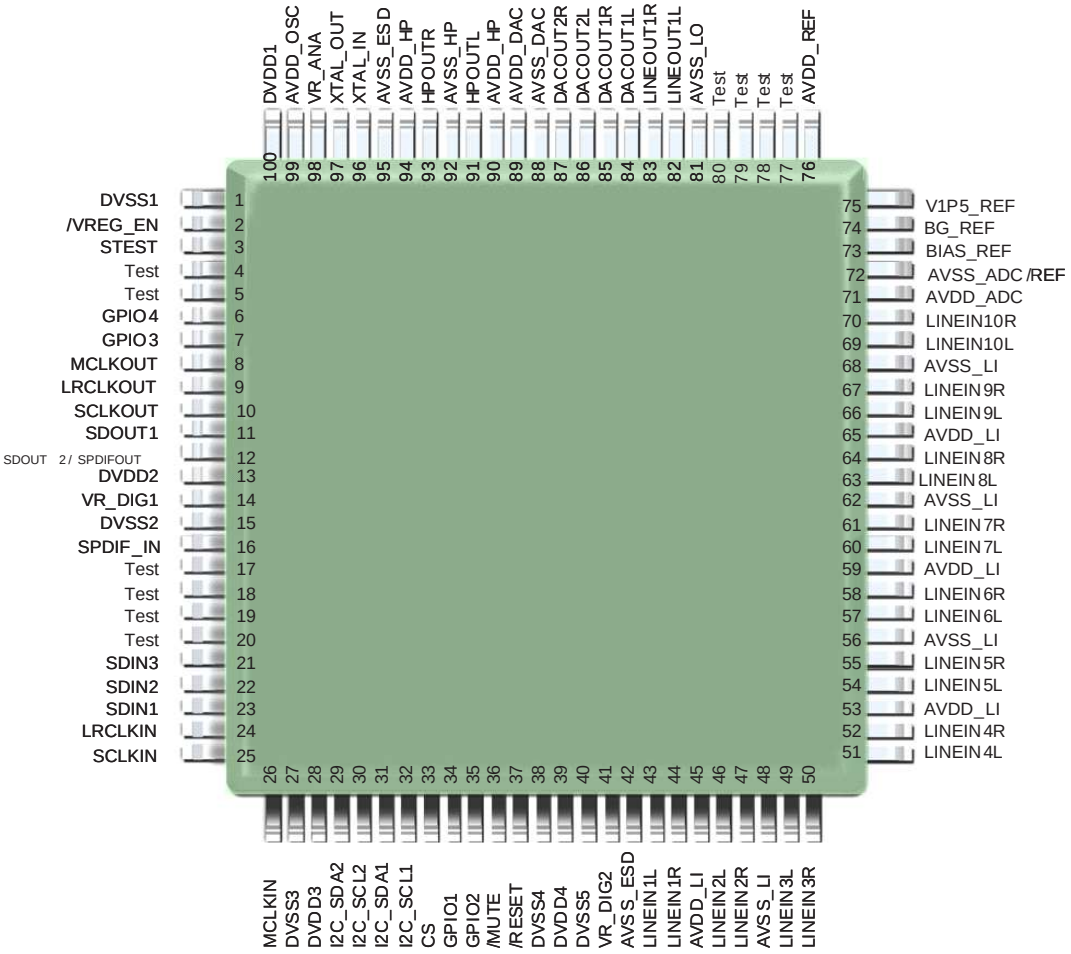
FEATURES

- Audio Input/Output
  - Three Synchronous Serial Audio Inputs (Six Channels)
  - Two Synchronous Serial Audio Outputs (Four Channels)
  - Input and Output Data Formats: 16-, 20-, or 24-Bit Data Left, Right, and I^2S
  - SPDIF Transmitter
  - 64 × Fs Bit Clock Rate
  - 512 × Fs XTAL Input for Master-Mode Clock Rates
  - 256 × Fs MCLKIN for Slave-Mode Clock Rates
  - Ten Multiplexed Stereo Analog Inputs Selectable Into One Stereo ADC and Three Stereo Line Outputs
    - High-Quality 93 dB DNR (Typical) ADC Channel Performance (Two Channels)
    - A Single Ended Analog Stereo Line Driver Output With 1 of 11 Selectable Inputs, 10-kΩ, 100-pF Drive Capability (Typical Output Level: 1-V RMS)
  - Three Stereo Audio DACs
    - High-Quality 96-dB DNR (Typical) DAC Channel Performance (Six Channels)
    - Stereo Headphone Amplifier – 24 mW Power Output Into 16 Ω, 100 pF
- Audio Digital Signal Processor
  - Programmable Functionality
  - 135-MHz Operation
  - 48-Bit Data Path With 76-Bit Accumulator
  - Hardware Single Cycle Multiplier (28 × 48)
  - Two Memory Loads and One Memory Store Per Cycle
  - Usable 768 Data RAM Words (48 Bit), Usable 1K Coefficient RAM (28 Bit)
  - Usable 2.5K Program RAM
  - 360 mS @ 48KHz, 17280 Words 24-Bit Delay Memory for Video Sync
- System Control Processor
  - Embedded 8051 WARP Microprocessor
  - Programmable Using Standard 8051 C Compilers
  - 16K Words of Program RAM (8 Bit)
  - Programmable Using Standard 8051 C Compilers
  - 2048 Words of Data RAM (8 Bit)
  - 256 Words of Internal RAM (8 Bit)
  - Programmable Functionality
- General Features
  - Easy to Use Control Interface
  - I^2C Serial Control Master and Slave Interface
  - Control Interface Operational Without External MCLK Input
  - Single 3.3-V Power Supply
  - Integrated Regulators
  - 100-Pin TQFP Package

TQFP PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The TAS3208 is an audio SOC designed for digital TV Audio Systems and Mini/Micro Component applications. TAS3208 has a programmable audio DSP that preserves high-quality audio by using a 48-bit data path, 28-bit filter coefficients, and a single-cycle 28 times 48-bit multiplier. The programmability feature allows users to customize features in the DSP RAM.

The TAS3208 is composed of seven functional blocks.

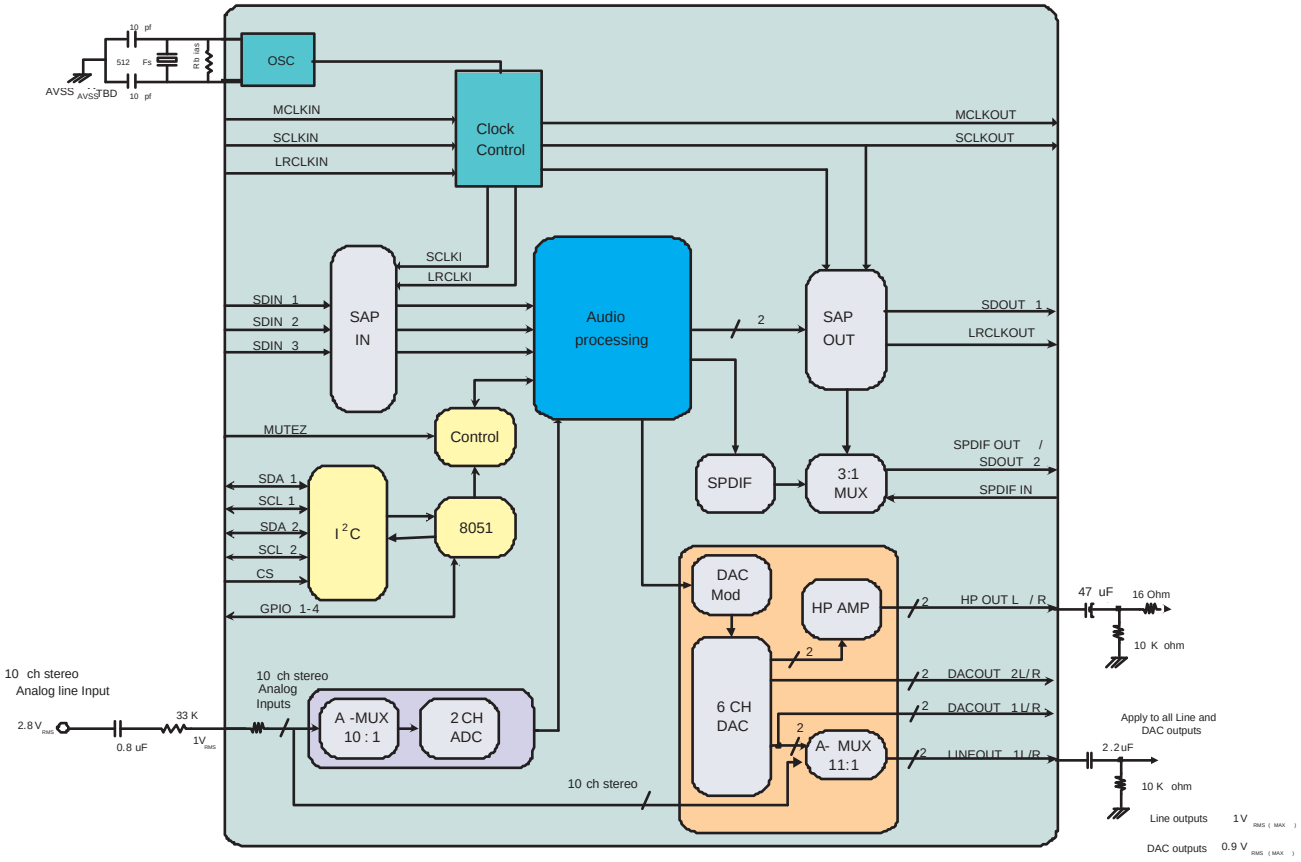
- Clock and Serial Data Interface
- Analog Input and Output
- 8051 WARP Controller, Serial Control Interface and Device Control
- Audio DSP – Digital Audio Processing
- Power Supply
- Internal References

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TQFP – YZP	TBD	TAS3208YZPR	TBD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The TAS3208 may be used with an external Asynchronous Sample Rate Converter (ASRC) to accommodate asynchronous serial inputs at different sampling rates. An example of this is shown in the block diagram of Figure 2.2.

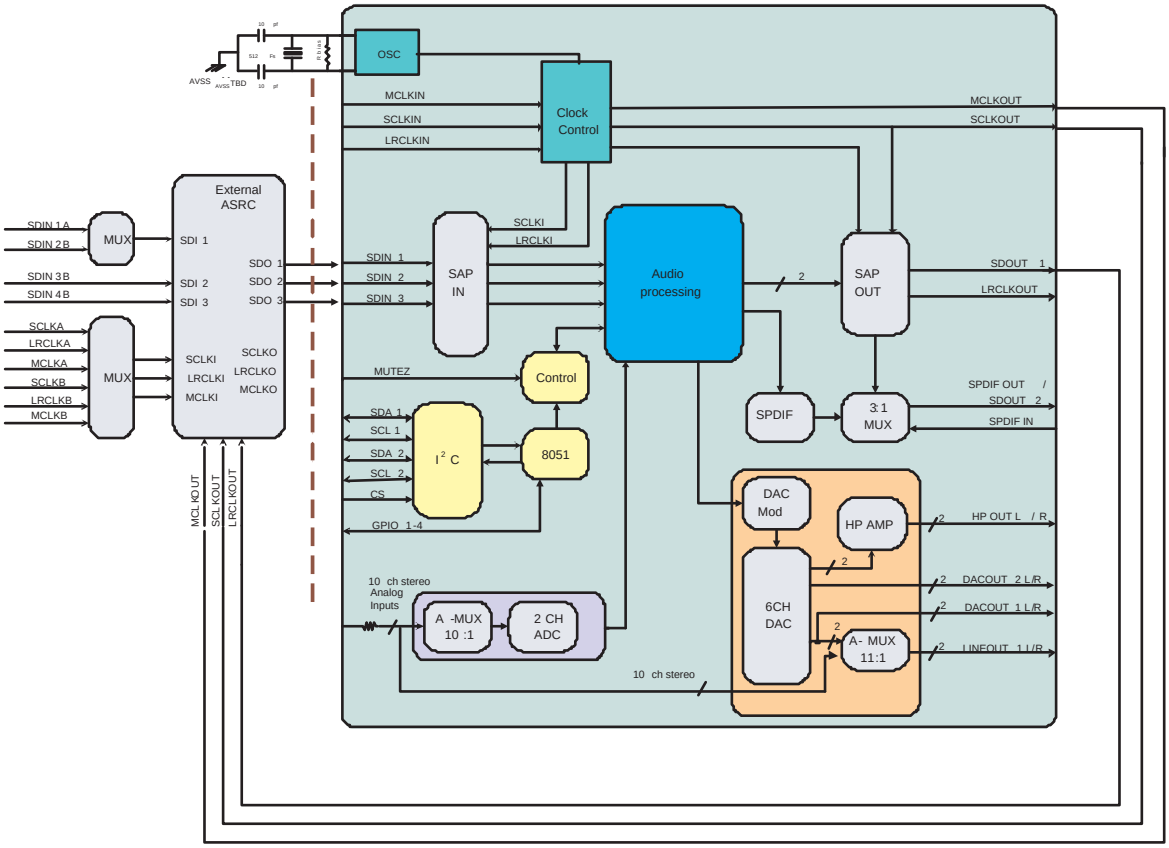


Figure 1. TAS3208 and interface to external ASRC

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
D_{VDD}	Supply voltage range		–0.5	3.8	V
A_{VDD}	Supply voltage range		–0.5	3.8	V
V_I	Input voltage range	3.3-V TTL	–0.5	V_{DDS} + 0.5	V
		3.3-V analog	–0.5	A_{VDDS} + 0.5	
		1.8-V LVCMOS	–0.5	A_{VDD} + 0.5(2)	
V_O	Voltage range applied to any output in the high-impedance or power-off state	3.3-V TTL	–0.5	V_{DDS} + 0.5	V
		3.3-V analog	–0.5	A_{VDDS} + 0.5	
		1.8-V LVCMOS	–0.5	D_{VDD} + 0.5(3)	
		1.8-V LVCMOS	–0.5	A_{VDD} + 0.5(4)	
I_{IK}	Input clamp current	V_I < 0 or V_I > D_{VDD}		±20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > D_{VDD}		±20	mA
T_{stg}	Storage temperature range		–65	150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) A_{VDD} is an internal 1.8-V supply derived from a regulator in the CXD9890Q chip. Pin XTALI is the only CXD9890Q input that is referenced to this 1.8-V logic supply. The absolute maximum rating listed is for reference; only a crystal should be connected to XTALI.
(3) D_{VDD} is an internal 1.8-V supply derived from regulators in the CXD9890Q chip. D_{VDD} is routed to– DVDD_BYPASS_CAP – to provide access to external filter capacitors, but should not be used to source power to external devices.
(4) Pin XTALO is the only CXD9890Q output that is derived from the internal 1.8-V logic supply A_{VDD}. The absolute maximum rating listed is for reference; only a crystal should be connected to XTALO. A_{VDD} is also routed to – AVDD_BYPASS_CAP – to provide access to external filter capacitors, but should not be used to source power to external devices.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
D_{VDD}	Digital supply voltage		3.0	3.3	3.6	V
A_{VDD}	Analog supply voltage	3.3-V analog	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	3.3-V TTL	2.0			V
		1.8-V LVCMOS (XTL_IN)	1.26		1.95	
V_{IL}	Low-level input voltage	3.3-V TTL			0.8	V
		1.8-V LVCMOS (XTL_IN)			0.54	
T_A	Operating ambient air temperature (ensuring Parametric)		–20	25	70	°C
T_J	Operating junction temperature		–20		105	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	3.3-V TTL	I_{OH} = –4 mA	2.4		V
		1.8-V LVCMOS (XTL_OUT)	I_{OH} = –0.55 mA	1.44		
V_{OL}	Low-level output voltage	3.3-V TTL	I_{OL} = 4 mA		0.5	V
		1.8-V LVCMOS (XTL_OUT)	I_{OL} = 0.75 mA		0.396	
I_{OZ}	High-impedance output current	3.3-V TTL			±20	µA
I_{IL} (1)	Low-level input current	1.8-V LVCMOS (XTL_IN)	$V_I = V_{IL}$		±1	µA
		3.3-V TTL	$V_I = V_{IL}$		±1	
I_{IH} (2)	High-level input current	1.8-V LVCMOS (XTL_IN)	$V_I = V_{IH}$		±1	µA
		3.3-V TTL	$V_I = V_{IH}$		±1	
I_{DVDD}	Digital supply current		DSP clock = 135-MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.288 MHz		200	mA
I_{AVDD}	Analog supply current		DSP clock = 135-MHz LRCLKIN/LRCLKOUT = 48 KHz, XTALI = 24.288 MHz		28	mA
I_{DVDD}	Digital supply current		$\overline{\text{RESET}}$ = Low		0.1	mA
I_{AVDD}	Analog supply current		$\overline{\text{RESET}}$ = Low		5	mA

(1) Value given is for those input pins that connect to an internal pull-up resistor as well as an input buffer. For inputs that have a pull-down resistor or no resistor, I_{IL} is ± 1 µa.
(2) Value given is for those input pins that connect to an internal pull-down resistor as well as an input buffer. For inputs that have a pull-up resistor or no resistor, I_{IH} is ± 1 µa.

PACKAGING INFORMATION

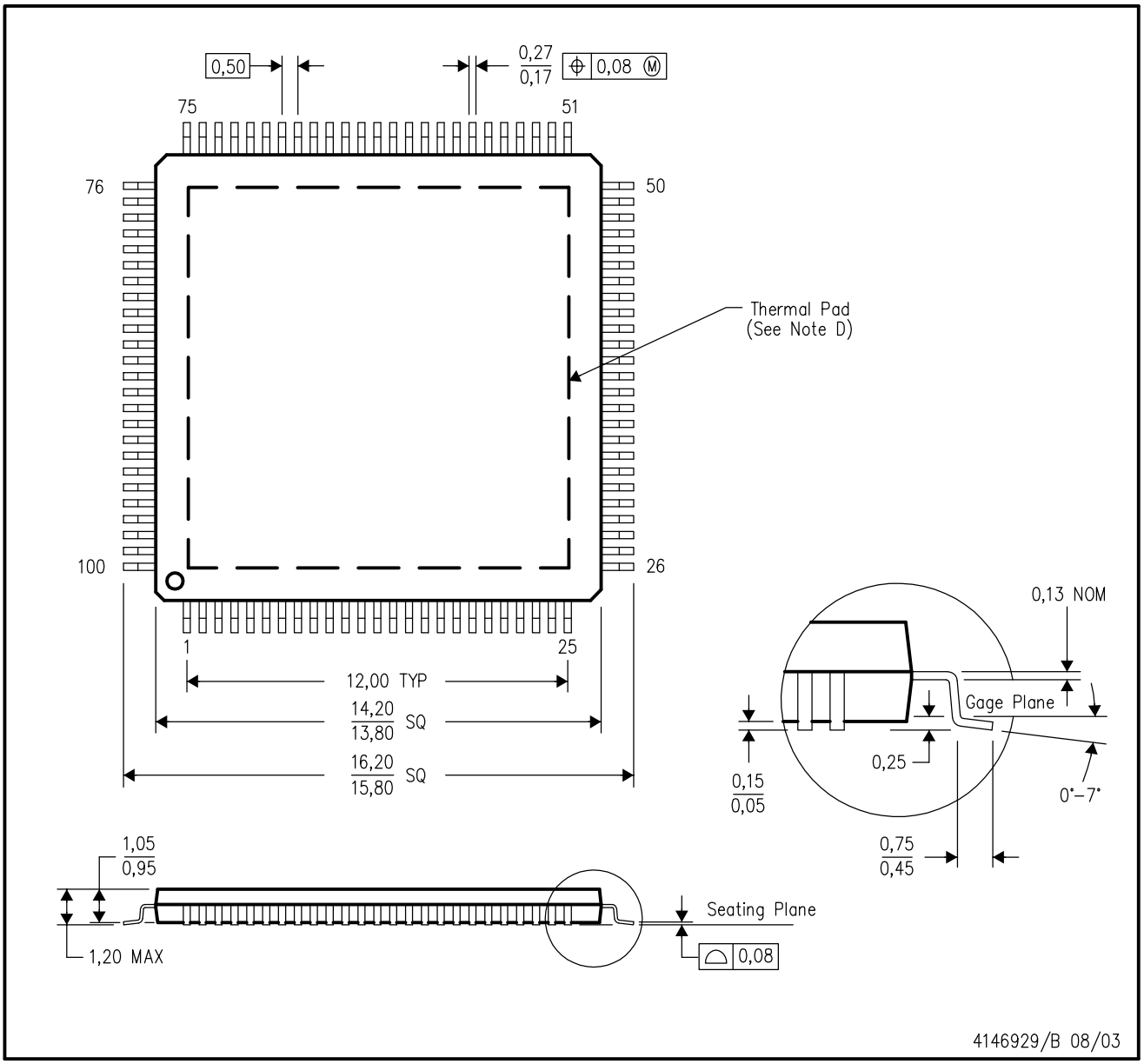
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS3208PZP	ACTIVE	HTQFP	PZP	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TAS3208PZPR	ACTIVE	HTQFP	PZP	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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