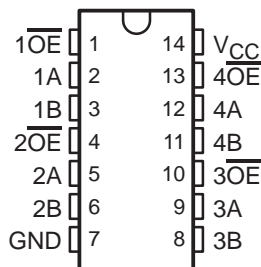
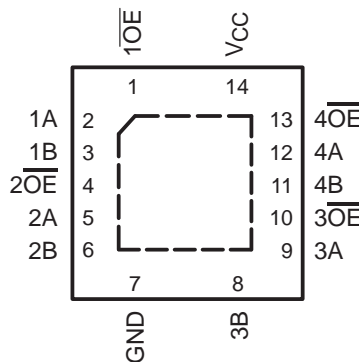


- Undershoot Protection for Off-Isolation on A and B Ports Up To –2 V
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance ( $r_{on}$ ) Characteristics ( $r_{on} = 3\ \Omega$  Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ( $C_{io(OFF)} = 5\text{ pF}$  Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- Low Power Consumption ( $I_{CC} = 3\ \mu\text{A}$  Max)
- $V_{CC}$  Operating Range From 4 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can Be Driven by TTL or 5-V/3.3-V CMOS Outputs
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: USB Interface, Bus Isolation, Low-Distortion Signal Gating

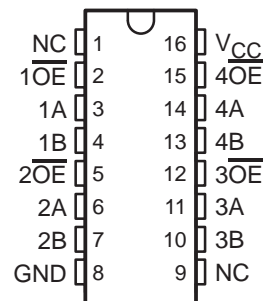
D, DB, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



DBQ PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74CBT3125C is a high-speed TTL-compatible FET bus switch with low ON-state resistance ( $r_{on}$ ), allowing for minimal propagation delay. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBT3125C provides protection for undershoot up to –2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBT3125C is organized as four 1-bit bus switches with separate output-enable ( $1\overline{OE}$ ,  $2\overline{OE}$ ,  $3\overline{OE}$ ,  $4\overline{OE}$ ) inputs. It can be used as four 1-bit bus switches or as one 4-bit bus switch. When  $\overline{OE}$  is low, the associated 1-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When  $\overline{OE}$  is high, the associated 1-bit bus switch is OFF, and the high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN74CBT3125C  
QUADRUPLE FET BUS SWITCH  
5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS122A – JULY 2003 – REVISED OCTOBER 2003

description/ordering information (continued)

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

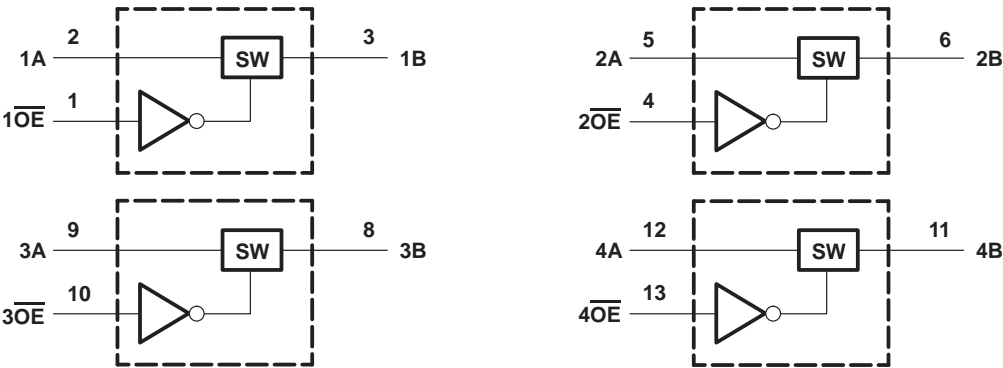
T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3125CRGYR	CU125C
	SOIC – D	Tube	SN74CBT3125CD	CBT3125C
		Tape and reel	SN74CBT3125CDR	
	SSOP – DB	Tube	SN74CBT3125CDB	CU125C
		Tape and reel	SN74CBT3125CDBR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3125CDBQR	CU125C
	TSSOP – PW	Tube	SN74CBT3125CPW	CU125C
		Tape and reel	SN74CBT3125CPWR	
	TVSOP – DGV	Tape and reel	SN74CBT3125CDGVR	CU125C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each bus switch)

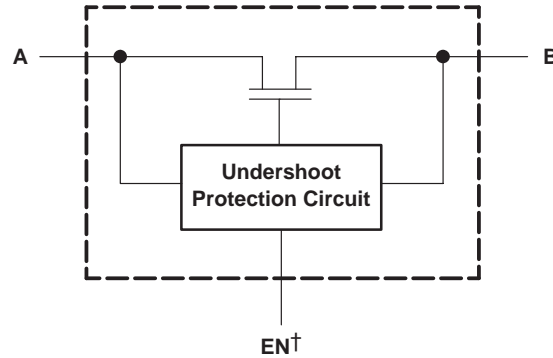
INPUT $\overline{OE}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



Pin numbers shown are for the D, DB, DGV, PW, and RGY packages.

**simplified schematic, each FET switch (SW)**



† EN is the internal enable signal applied to the switch.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, $I_{IK}$ ( $V_{IN} < 0$ )	–50 mA
I/O port clamp current, $I_{I/OK}$ ( $V_{I/O} < 0$ )	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through $V_{CC}$ or GND terminals	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package	86°C/W
(see Note 5): DB package	96°C/W
(see Note 5): DBQ package	90°C/W
(see Note 5): DGV package	127°C/W
(see Note 5): PW package	113°C/W
(see Note 6): RGY package	47°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
  2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  3.  $V_I$  and  $V_O$  are used to denote specific conditions for  $V_{I/O}$ .
  4.  $I_I$  and  $I_O$  are used to denote specific conditions for  $I_{I/O}$ .
  5. The package thermal impedance is calculated in accordance with JESD 51-7.
  6. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 7)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2	5.5	V
$V_{IL}$ Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 7: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74CBT3125C

## QUADRUPLE FET BUS SWITCH

### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS122A – JULY 2003 – REVISED OCTOBER 2003

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Control inputs	$V_{CC} = 4.5\text{ V}$ ,	$I_{IN} = -18\text{ mA}$			-1.8	V
$V_{IKU}$	Data inputs	$V_{CC} = 5\text{ V}$ ,	$0\text{ mA} > I_I \geq -50\text{ mA}$ , $V_{IN} = V_{CC}$ or GND, Switch OFF			-2	V
$I_{IN}$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	$V_{IN} = V_{CC}$ or GND			$\pm 1$	$\mu\text{A}$
$I_{OZ}^\ddagger$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$ , Switch OFF, $V_{IN} = V_{CC}$ or GND			$\pm 10$	$\mu\text{A}$
$I_{off}$		$V_{CC} = 0$ ,	$V_O = 0$ to $5.5\text{ V}$ , $V_I = 0$			10	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$I_{I/O} = 0$ , $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			3	$\mu\text{A}$
$\Delta I_{CC}^\S$	Control inputs	$V_{CC} = 5.5\text{ V}$ ,	One input at $3.4\text{ V}$ , Other inputs at $V_{CC}$ or GND			2.5	mA
$C_{in}$	Control inputs	$V_{IN} = 3\text{ V}$ or 0			3		pF
$C_{io}(\text{OFF})$		$V_{I/O} = 3\text{ V}$ or 0, Switch OFF,	$V_{IN} = V_{CC}$ or GND		5		pF
$C_{io}(\text{ON})$		$V_{I/O} = 3\text{ V}$ or 0, Switch ON,	$V_{IN} = V_{CC}$ or GND		12.5		pF
$r_{on}^\P$		$V_{CC} = 4\text{ V}$ , TYP at $V_{CC} = 4\text{ V}$	$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$		8	12	$\Omega$
		$V_{CC} = 4.5\text{ V}$	$V_I = 0$ , $I_O = 64\text{ mA}$		3	6	
			$I_O = 30\text{ mA}$		3	6	
			$V_I = 2.4\text{ V}$ , $I_O = -15\text{ mA}$		5	10	

$V_{IN}$  and  $I_{IN}$  refer to control inputs.  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to data pins.

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ For I/O ports, the parameter  $I_{OZ}$  includes the input leakage current.

§ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\#$	A or B	B or A		0.24		0.15	ns
$t_{en}$	$\overline{OE}$	A or B		4.4	1.5	4	ns
$t_{dis}$	$\overline{OE}$	A or B		4.4	1.5	4.4	ns

# The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**SN74CBT3125C**  
**QUADRUPLE FET BUS SWITCH**  
**5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION**  
 SCDS122A – JULY 2003 – REVISED OCTOBER 2003

undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{OUTU}$	$V_{CC} = 5.5\text{ V}$ , Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

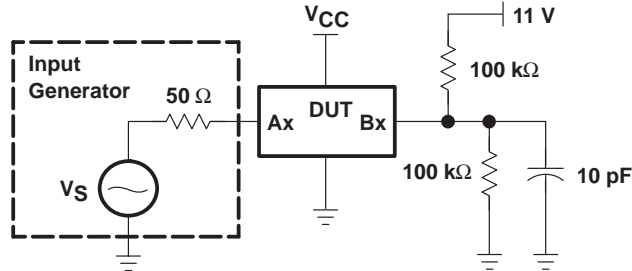


Figure 1. Device Test Setup



Figure 2. Transient Input Voltage ( $V_I$ ) and Output Voltage ( $V_{OUTU}$ ) Waveforms (Switch OFF)

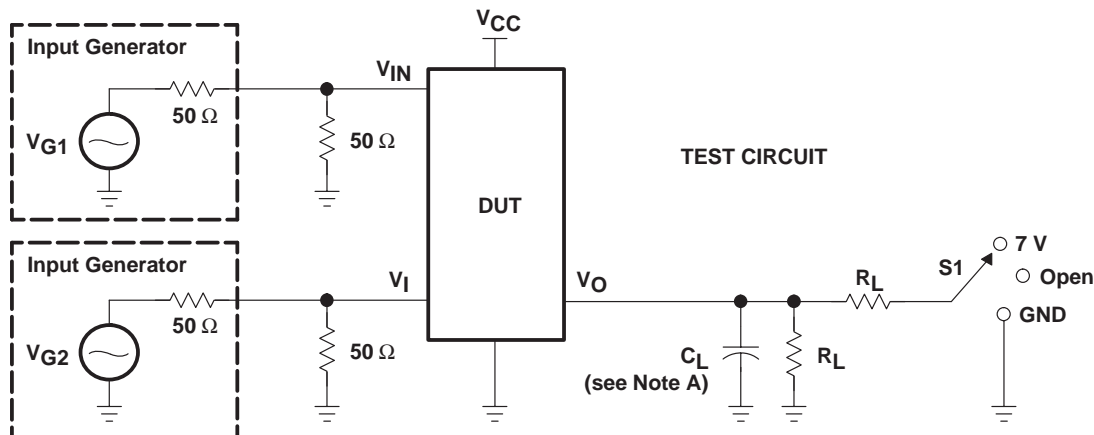
# SN74CBT3125C

## QUADRUPLE FET BUS SWITCH

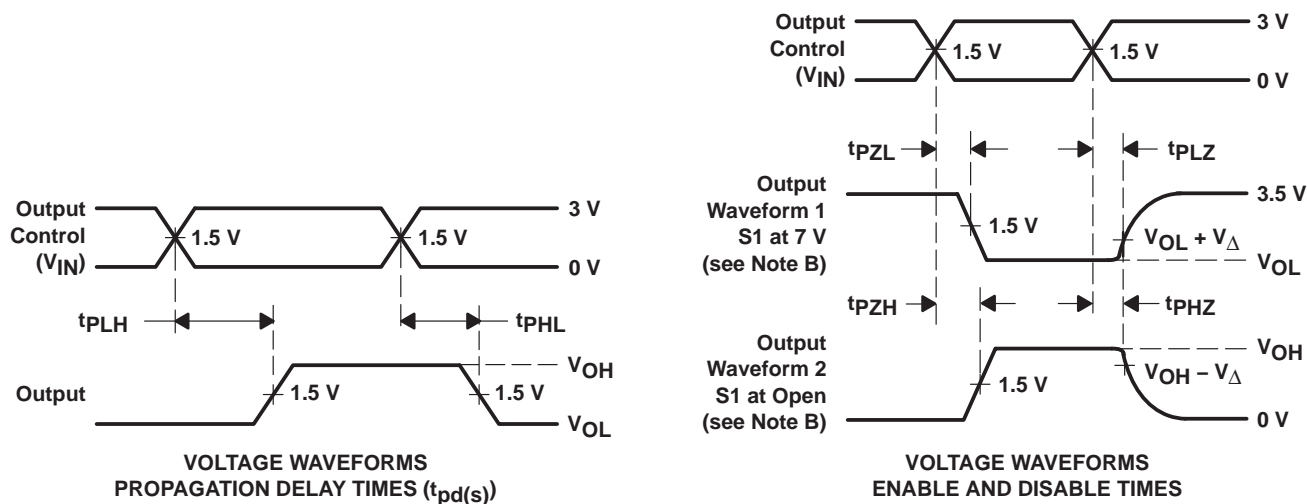
### 5-V BUS SWITCH WITH -2-V UNDERSHOOT PROTECTION

SCDS122A – JULY 2003 – REVISED OCTOBER 2003

#### PARAMETER MEASUREMENT INFORMATION



TEST	V <sub>CC</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>pd</sub> (s)	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V <sub>CC</sub> or GND V <sub>CC</sub> or GND	50 pF 50 pF	
t <sub>PLZ</sub> /t <sub>PZL</sub>	5 V ± 0.5 V 4 V	7 V 7 V	500 Ω 500 Ω	GND GND	50 pF 50 pF	0.3 V 0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	5 V ± 0.5 V 4 V	Open Open	500 Ω 500 Ω	V <sub>CC</sub> V <sub>CC</sub>	50 pF 50 pF	0.3 V 0.3 V



- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>(s). The t<sub>pd</sub> propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74CBT3125CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDB	PREVIEW	SSOP	DB	14	80	TBD	Call TI	Call TI
SN74CBT3125CDBQR	ACTIVE	SSOP/QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3125CDBQRE4	ACTIVE	SSOP/QSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3125CDBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBT3125CRGYR	ACTIVE	QFN	RGY	14	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN74CBT3125CRGYRG4	ACTIVE	QFN	RGY	14	1000	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## D (R-PDSO-G14)

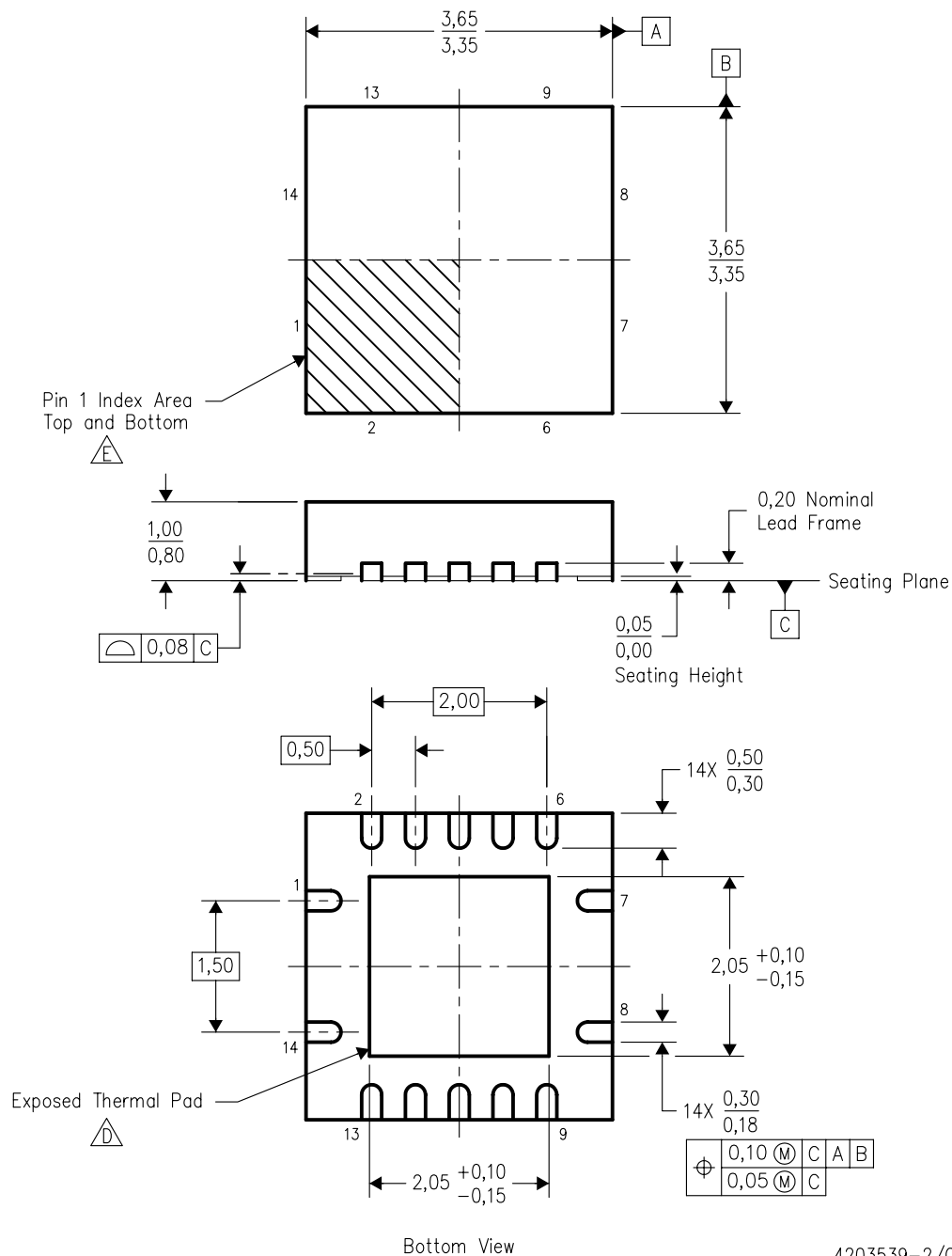
## PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



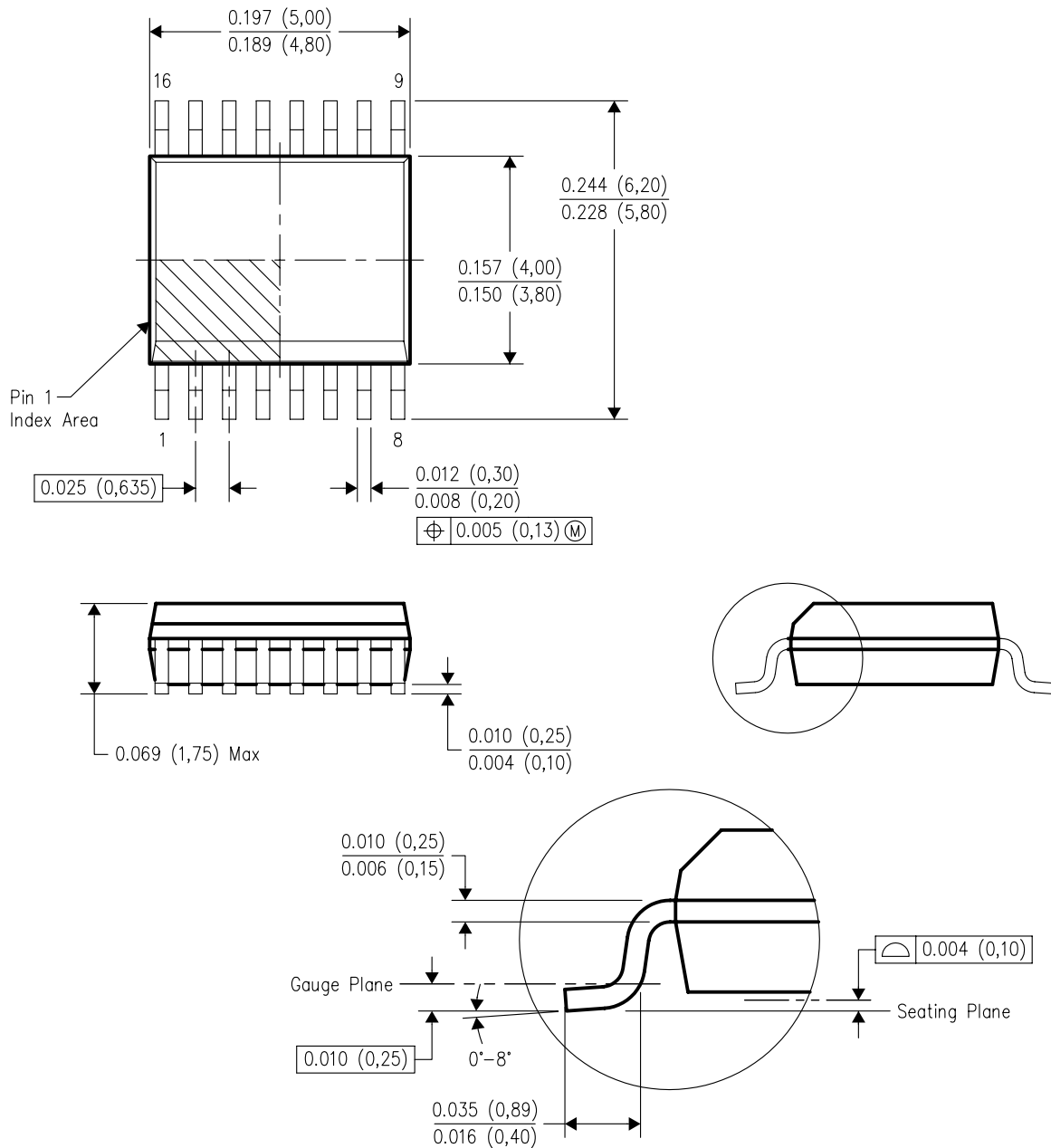
Bottom View

4203539-2/G 04/2005

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

## DBQ (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4073301-2/G 02/2005

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AB.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated