

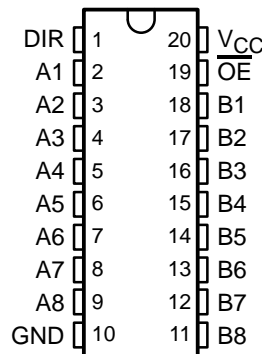
SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce dc Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

TYPE	I _{OL} (SINK CURRENT)	I _{OH} (SOURCE CURRENT)
SN54LS245	12 mA	–12 mA
SN74LS245	24 mA	–15 mA

SN54LS245 . . . J OR W PACKAGE
SN74LS245 . . . DB, DW, N, OR NS PACKAGE
(TOP VIEW)

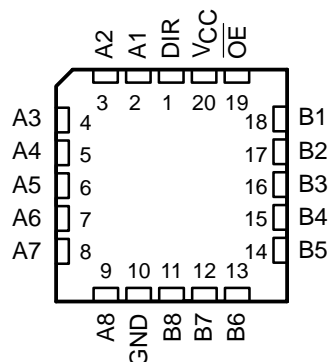


description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that the buses are effectively isolated.

SN54LS245 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS245N	SN74LS245N
	SOIC – DW	Tube	SN74LS245DW	LS245
		Tape and reel	SN74LS245DWR	
	SOP – NS	Tape and reel	SN74LS245NSR	74LS245
–55°C to 125°C	SSOP – DB	Tape and reel	SN74LS245DBR	LS245
	CDIP – J	Tube	SN54LS245J	SN54LS245J
		Tube	SNJ54LS245J	SNJ54LS245J
	CFP – W	Tube	SNJ54LS245W	SNJ54LS245W
	LCCC – FK	Tube	SN54LS245FK	SN54LS245FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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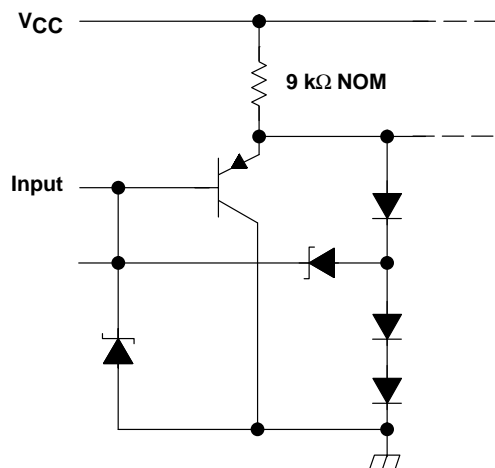
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FUNCTION TABLE

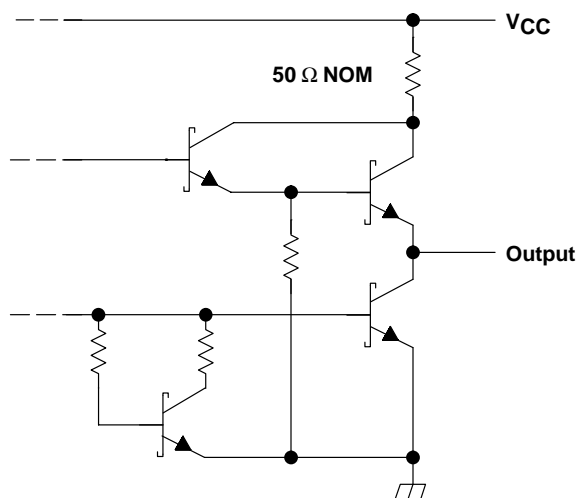
INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

schematics of inputs and outputs

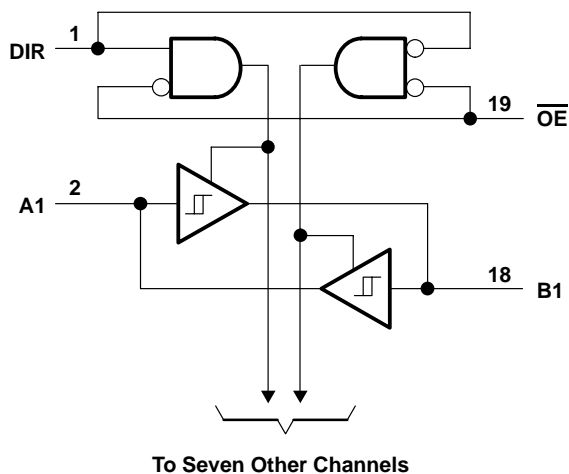
EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



logic diagram (positive logic)



SN54LS245, SN74LS245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I (see Note 1)	7 V
Package thermal impedance, θ_{JA} (see Note 2): DB package	70°C/W
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54LS245			SN74LS245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C



SN54LS245, SN74LS245

OCTAL BUS TRANSCEIVERS

WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS245			SN74LS245			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IH}	High-level input voltage				2			2			V
V _{IL}	Low-level input voltage				0.7			0.8			V
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = −18 mA		−1.5			−1.5			V
Hysteresis (V _{T+} − V _{T−})		A or B	V _{CC} = MIN		0.2	0.4		0.2	0.4		V
V _{OH}	High-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL(max)}	I _{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I _{OH} = MAX	2		2				
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL(max)}	I _{OL} = 12 mA	0.4			0.4			V
				I _{OL} = 24 mA				0.5			
I _{OZH}	Off-state output current, high-level voltage applied		V _{CC} = MAX, $\overline{\text{OE}}$ at 2 V	V _O = 2.7 V	20			20			μA
I _{OZL}	Off-state output current, low-level voltage applied		V _{CC} = MAX, $\overline{\text{OE}}$ at 2 V	V _O = 0.4 V	−200			−200			μA
I _I	Input current at maximum input voltage	A or B	V _{CC} = MAX	V _I = 5.5 V	0.1			0.1			mA
		DIR or $\overline{\text{OE}}$		V _I = 7 V	0.1			0.1			
I _{IH}	High-level input current		V _{CC} = MAX, V _{IH} = 2.7 V	20			20			μA	
I _{IL}	Low-level input current		V _{CC} = MAX, V _{IL} = 0.4 V	−0.2			−0.2			mA	
I _{OS}	Short-circuit output current§		V _{CC} = MAX	−40	−225		40	−225		mA	
I _{CC}	Supply current	Total, outputs high	V _{CC} = MAX	Outputs open	48	70	48	70		mA	
		Total, outputs low			62	90	62	90			
		Outputs at high Z			64	95	64	95			

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

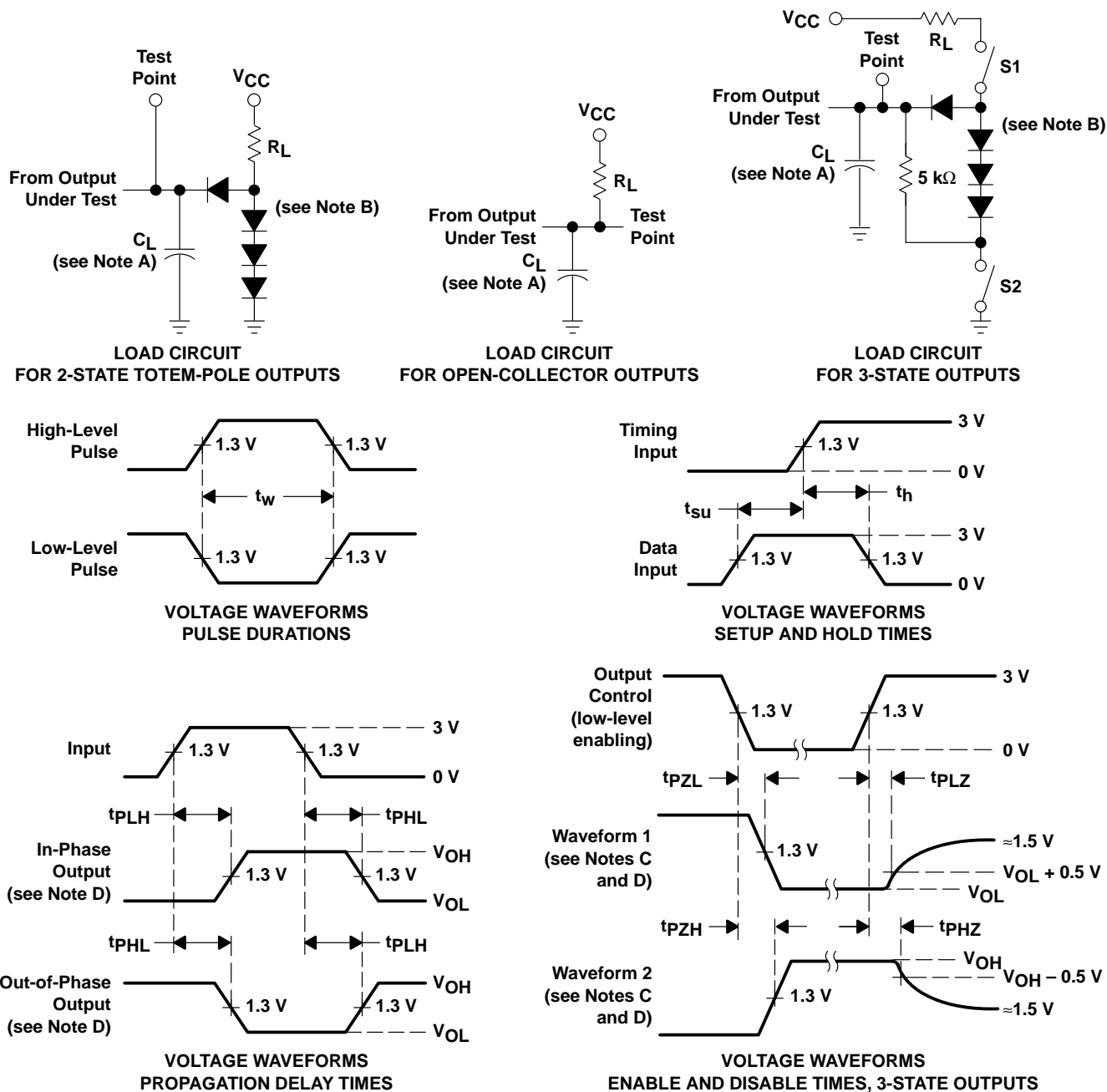
switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		8	12	ns
t_{PHL}	Propagation delay time, high- to low-level output		8	12	
t_{PZL}	Output enable time to low level		27	40	ns
t_{PZH}	Output enable time to high level		25	40	
t_{PLZ}	Output disable time from low level		15	25	ns
t_{PHZ}	Output disable time from high level		15	28	



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PARAMETER MEASUREMENT INFORMATION
SERIES 54LS/74LS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{PZH} ; S1 is closed and S2 is open for t_{PZL} .
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
G. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-8002101VRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
5962-8002101VSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
80021012A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
8002101SA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
JM38510/32803B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/32803BRA	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
JM38510/32803BSA	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC
SN54LS245J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SN74LS245DBR	ACTIVE	SSOP	DB	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS245DW	ACTIVE	SOIC	DW	20	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS245DWR	ACTIVE	SOIC	DW	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74LS245J	OBSOLETE	CDIP	J	20		None	Call TI	Call TI
SN74LS245N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS245N3	OBSOLETE	PDIP	N	20		None	Call TI	Call TI
SN74LS245NSR	ACTIVE	SO	NS	20	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54LS245FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS245J	ACTIVE	CDIP	J	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS245W	ACTIVE	CFP	W	20	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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