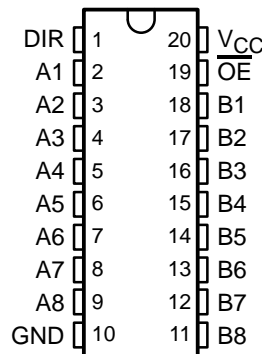# SN54LS245, SN74LS245
# OCTAL BUS TRANSCEIVERS
# WITH 3-STATE OUTPUTS

SDLS146A – OCTOBER 1976 – REVISED FEBRUARY 2002

- **3-State Outputs Drive Bus Lines Directly**
- **PNP Inputs Reduce dc Loading on Bus Lines**
- **Hysteresis at Bus Inputs Improves Noise Margins**
- **Typical Propagation Delay Times Port to Port, 8 ns**

| TYPE | $I_{OL}$ (SINK CURRENT) | $I_{OH}$ (SOURCE CURRENT) |
|---|---|---|
| SN54LS245 | 12 mA | −12 mA |
| SN74LS245 | 24 mA | −15 mA |

**SN54LS245 . . . J OR W PACKAGE**
**SN74LS245 . . . DB, DW, N, OR NS PACKAGE**
**(TOP VIEW)**

```
      DIR [ 1    20 ] V_CC
       A1 [ 2    19 ] OE
       A2 [ 3    18 ] B1
       A3 [ 4    17 ] B2
       A4 [ 5    16 ] B3
       A5 [ 6    15 ] B4
       A6 [ 7    14 ] B5
       A7 [ 8    13 ] B6
       A8 [ 9    12 ] B7
      GND [ 10   11 ] B8
```

**SN54LS245 . . . FK PACKAGE**
**(TOP VIEW)**

```
         A2  A1  DIR V_CC OE
          3   2   1  20  19
     A3 [ 4             18 ] B1
     A4 [ 5             17 ] B2
     A5 [ 6             16 ] B3
     A6 [ 7             15 ] B4
     A7 [ 8             14 ] B5
          9  10  11  12  13
         A8 GND B8  B7  B6
```
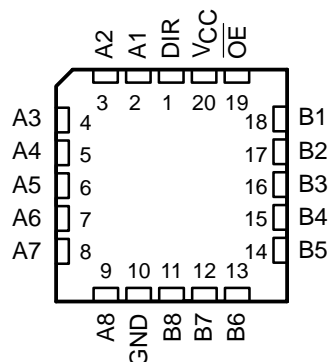
## description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN74LS245N | SN74LS245N |
| | SOIC – DW | Tube | SN74LS245DW | LS245 |
| | | Tape and reel | SN74LS245DWR | |
| | SOP – NS | Tape and reel | SN74LS245NSR | 74LS245 |
| | SSOP – DB | Tape and reel | SN74LS245DBR | LS245 |
| −55°C to 125°C | CDIP – J | Tube | SN54LS245J | SN54LS245J |
| | | Tube | SNJ54LS245J | SNJ54LS245J |
| | CFP – W | Tube | SNJ54LS245W | SNJ54LS245W |
| | LCCC – FK | Tube | SN54LS245FK | SN54LS245FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**TEXAS INSTRUMENTS**

**FUNCTION TABLE**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{\text{OE}}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

## schematics of inputs and outputs

**EQUIVALENT OF EACH INPUT**
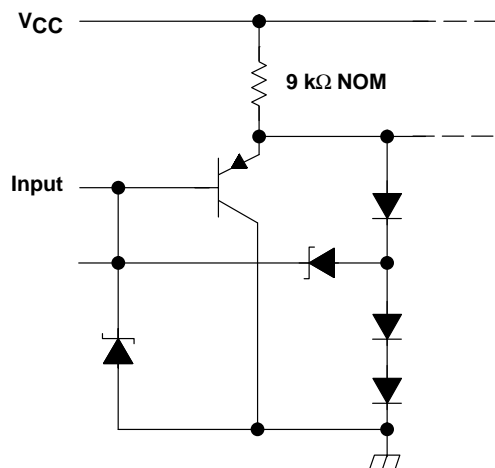
**TYPICAL OF ALL OUTPUTS**
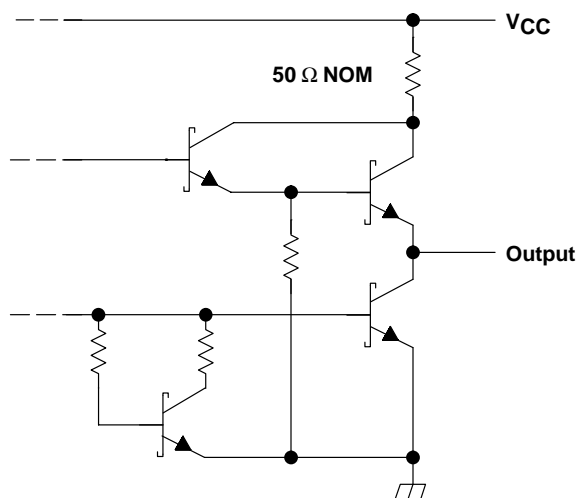


## logic diagram (positive logic)
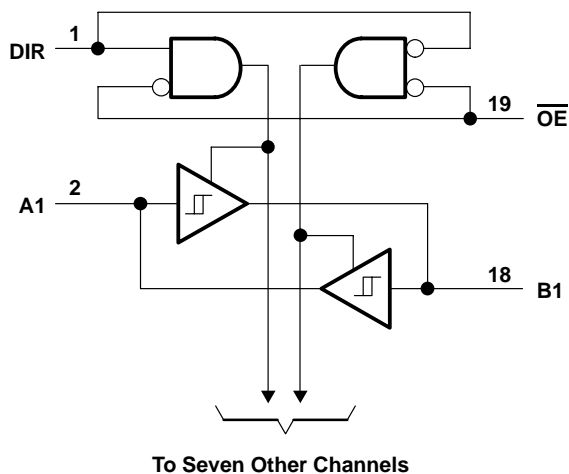


**To Seven Other Channels**

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Input voltage, $V_I$ (see Note 1) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 70°C/W
DW package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 58°C/W
N package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 69°C/W
NS package . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 60°C/W
Storage temperature range, $T_{stg}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to GND.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions

| | | SN54LS245 | | | SN74LS245 | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $I_{OH}$ | High-level output current | | | –12 | | | –15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | | | 24 | mA |
| $T_A$ | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS245 MIN | SN54LS245 TYP‡ | SN54LS245 MAX | SN74LS245 MIN | SN74LS245 TYP‡ | SN74LS245 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| | Hysteresis ($V_{T+} - V_{T-}$)   A or B | $V_{CC}$ = MIN | | 0.2 | 0.4 | | 0.2 | 0.4 | | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL} = V_{IL(max)}$ | $I_{OH}$ = −3 mA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| | | | $I_{OH}$ = MAX | 2 | | | 2 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL} = V_{IL(max)}$ | $I_{OL}$ = 12 mA | | | 0.4 | | | 0.4 | V |
| | | | $I_{OL}$ = 24 mA | | | | | | 0.5 | |
| $I_{OZH}$ | Off-state output current, high-level voltage applied | $V_{CC}$ = MAX, $\overline{OE}$ at 2 V | $V_O$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{OZL}$ | Off-state output current, low-level voltage applied | $V_{CC}$ = MAX, $\overline{OE}$ at 2 V | $V_O$ = 0.4 V | | | −200 | | | −200 | µA |
| $I_I$ | Input current at maximum input voltage | A or B | $V_{CC}$ = MAX | $V_I$ = 5.5 V | | | 0.1 | | | 0.1 | mA |
| | | DIR or $\overline{OE}$ | | $V_I$ = 7 V | | | 0.1 | | | 0.1 | |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, | $V_{IH}$ = 2.7 V | | | 20 | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, | $V_{IL}$ = 0.4 V | | | −0.2 | | | −0.2 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −40 | | −225 | 40 | | −225 | mA |
| $I_{CC}$ | Supply current   Total, outputs high | $V_{CC}$ = MAX | Outputs open | | 48 | 70 | | 48 | 70 | mA |
| | Total, outputs low | | | | 62 | 90 | | 62 | 90 | |
| | Outputs at high Z | | | | 64 | 95 | | 64 | 95 | |

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
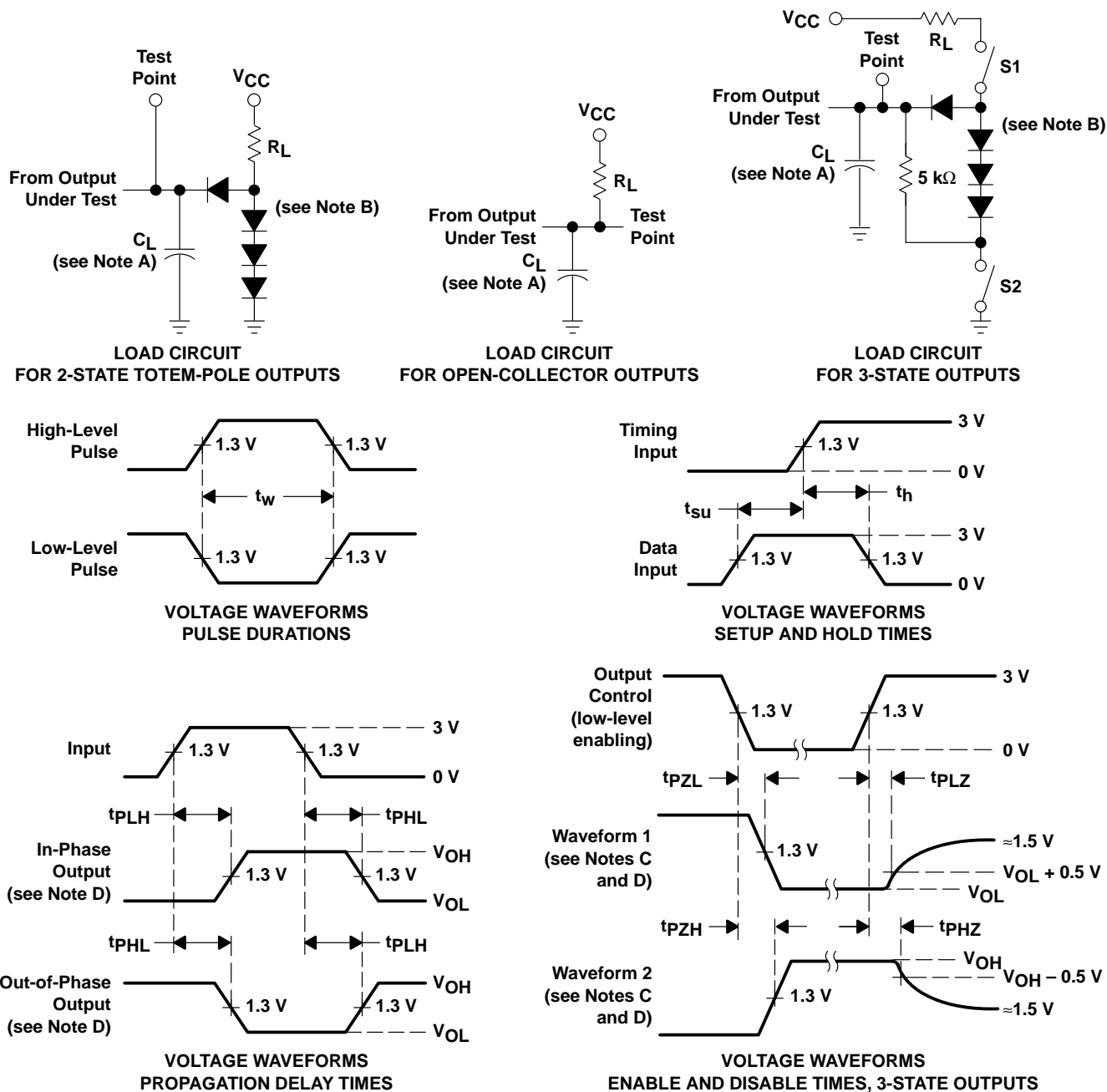
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see Figure 1)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $C_L$ = 45 pF, | $R_L$ = 667 Ω | | 8 | 12 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 8 | 12 | |
| $t_{PZL}$ | Output enable time to low level | $C_L$ = 45 pF, | $R_L$ = 667 Ω | | 27 | 40 | ns |
| $t_{PZH}$ | Output enable time to high level | | | | 25 | 40 | |
| $t_{PLZ}$ | Output disable time from low level | $C_L$ = 5 pF, | $R_L$ = 667 Ω | | 15 | 25 | ns |
| $t_{PHZ}$ | Output disable time from high level | | | | 15 | 28 | |

**TEXAS INSTRUMENTS**

## PARAMETER MEASUREMENT INFORMATION
## SERIES 54LS/74LS DEVICES



**LOAD CIRCUIT**
**FOR 2-STATE TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT**
**FOR OPEN-COLLECTOR OUTPUTS**

**LOAD CIRCUIT**
**FOR 3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS**
**PULSE DURATIONS**

**VOLTAGE WAVEFORMS**
**SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. $C_L$ includes probe and jig capacitance.
   B. All diodes are 1N3064 or equivalent.
   C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   D. S1 and S2 are closed for $t_{PLH}$, $t_{PHL}$, $t_{PHZ}$, and $t_{PLZ}$; S1 is open and S2 is closed for $t_{PZH}$; S1 is closed and S2 is open for $t_{PZL}$.
   E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
   F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ ≈ 50 Ω, $t_r$ ≤ 1.5 ns, $t_f$ ≤ 2.6 ns.
   G. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuits and Voltage Waveforms**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| 5962-8002101VRA | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 5962-8002101VSA | ACTIVE | CFP | W | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 80021012A | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| 8002101SA | ACTIVE | CFP | W | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/32803B2A | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/32803BRA | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| JM38510/32803BSA | ACTIVE | CFP | W | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SN54LS245J | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SN74LS245DBR | ACTIVE | SSOP | DB | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS245DW | ACTIVE | SOIC | DW | 20 | 25 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS245DWR | ACTIVE | SOIC | DW | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-250C-1 YEAR/ Level-1-235C-UNLIM |
| SN74LS245J | OBSOLETE | CDIP | J | 20 | | None | Call TI | Call TI |
| SN74LS245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |
| SN74LS245N3 | OBSOLETE | PDIP | N | 20 | | None | Call TI | Call TI |
| SN74LS245NSR | ACTIVE | SO | NS | 20 | 2000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR/ Level-1-235C-UNLIM |
| SNJ54LS245FK | ACTIVE | LCCC | FK | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54LS245J | ACTIVE | CDIP | J | 20 | 1 | None | Call TI | Level-NC-NC-NC |
| SNJ54LS245W | ACTIVE | CFP | W | 20 | 1 | None | Call TI | Level-NC-NC-NC |

**[1]** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**[2]** Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

**[3]** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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