# Voltage Output
# PROGRAMMABLE SENSOR CONDITIONER

## FEATURES

- **COMPLETE BRIDGE SENSOR CONDITIONER**
- **VOLTAGE OUTPUT: Ratiometric or Absolute**
- **DIGITAL CAL: No Potentiometers/Sensor Trims**
- **SENSOR ERROR COMPENSATION**
  - **Span, Offset, and Temperature Drifts**
- **LOW ERROR, TIME-STABLE**
- **SENSOR LINEARIZATION CIRCUITRY**
- **TEMPERATURE SENSE: Internal or External**
- **CALIBRATION LOOKUP TABLE LOGIC**
  - **Uses External EEPROM (SOT23-5)**
- **OVER/UNDER-SCALE LIMITING**
- **SENSOR FAULT DETECTION**
- **+2.7V TO +5.5V OPERATION**
- **−40°C to +125°C OPERATION**
- **SMALL TSSOP-16 PACKAGE**

## APPLICATIONS

- **BRIDGE SENSORS**
- **REMOTE 4-20mA TRANSMITTERS**
- **STRAIN, LOAD, AND WEIGH SCALES**
- **AUTOMOTIVE SENSORS**

## EVALUATION TOOLS

- **HARDWARE DESIGNER'S KIT (PGA309EVM)**
  - **Temperature Eval of PGA309 + Sensor**
  - **Full Programming of PGA309**
  - **Sensor Compensation Analysis Tool**

## DESCRIPTION

The PGA309 is a programmable analog signal conditioner designed for bridge sensors. The analog signal path amplifies the sensor signal and provides digital calibration for zero, span, zero drift, span drift, and sensor linearization errors with applied stress (pressure, strain, etc.). The calibration is done via a One-Wire digital serial interface or through a Two-Wire industry-standard connection. The calibration parameters are stored in external nonvolatile memory (typically SOT23-5) to eliminate manual trimming and achieve long-term stability.

The all-analog signal path contains a 2x2 input multiplexer (mux), auto-zero programmable-gain instrumentation amplifier, linearization circuit, voltage reference, internal oscillator, control logic, and an output amplifier. Programmable level shifting compensates for sensor DC offsets.

The core of the PGA309 is the precision, low-drift, no 1/f noise Front-End PGA (Programmable Gain Amplifier). The overall gain of the Front-End PGA + Output Amplifier can be adjusted from 2.7V/V to 1152V/V. The polarity of the inputs can be switched through the input mux to accommodate sensors with unknown polarity output. The Fault Monitor circuit detects and signals sensor burnout, overload, and system fault conditions.

**For detailed application information, see the PGA309 User's Guide (SBOU024), available for download at www.ti.com.**
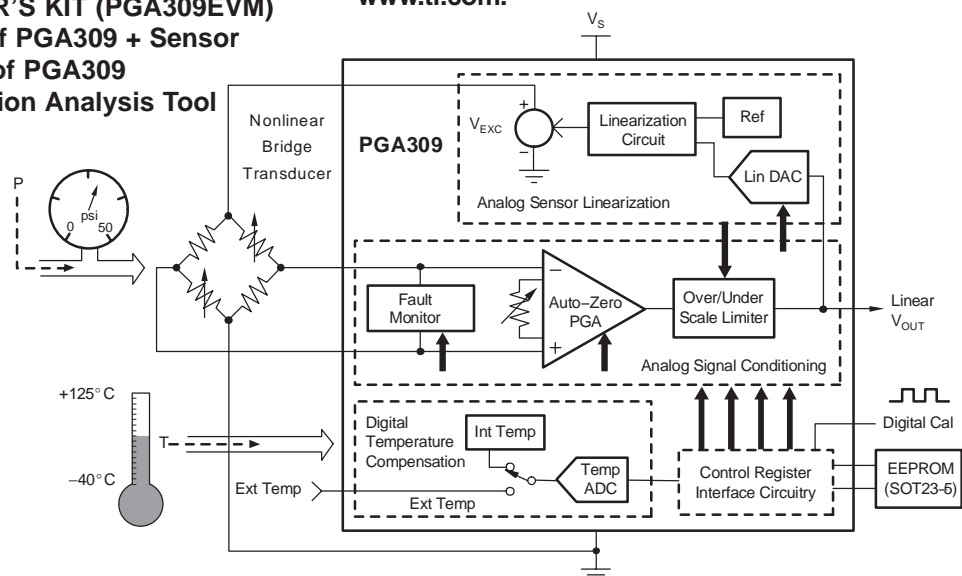
**TEXAS INSTRUMENTS**
www.ti.com

## PACKAGE/ORDERING INFORMATION[1]

| PRODUCT | PACKAGE–LEAD | PACKAGE DRAWING | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| PGA309 | TSSOP-16 | PW | −40°C to +125°C | PGA309 | PGA309AIPWR | Tape and Reel, 2500 |
|  |  |  |  |  | PGA309AIPWT | Tape and Reel, 250 |

[1] For the most current package and ordering information, refer to our web site at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range unless otherwise noted.

| | |
|---|---|
| Supply Voltage, $V_{SD}$, $V_{SD}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . | +7.0V |
| Input Voltage, $V_{IN1}$, $V_{IN2}$[2] . . . . . . . . . . . . . . . . . . . . . | −0.3V to $V_{SA}$ +0.3V |
| Input Current, $V_{FB}$, $V_{OUT}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . | ±150mA |
| Input Current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . | ±10mA |
| Output Current Limit . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . | 50mA |
| Storage Temperature Range . . . . . . . . . . . . . . . . . . . . . . . . | −60°C to +150°C |
| Operating Temperature Range . . . . . . . . . . . . . . . . . . . . . . | −55°C to +150°C |
| Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . | +150°C |
| Lead Temperature (soldering, 10s) . . . . . . . . . . . . . . . . . . . . . . . . | +300°C |
| ESD Protection (Human Body Model) . . . . . . . . . . . . . . . . . . . . . . . . | 4kV |

[1] Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# ELECTRICAL CHARACTERISTICS

**BOLDFACE** limits apply over the specified temperature range: $T_A = -40°C$ to $+125°C$

$T_A = +25°C$, $V_{SA} = V_{SD} = +5V$ ($V_{SA} = V_{SUPPLY\ ANALOG}$, $V_{SD} = V_{SUPPLY\ DIGITAL}$; $V_{SA}$ must equal $V_{SD}$), $GND_D = GND_A = 0$, and $V_{REF} = REF_{IN}/REF_{OUT} = +5V$, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA309 | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **FRONT-END PGA + OUTPUT AMPLIFIER** | | | | | |
| $V_{OUT}/V_{IN}$ Differential Signal Gain Range[1] | Fine Gain Adjust = 1<br>Front-End PGA Gains: 4, 8, 16, 23.27, 32, 42.67, 64, 128<br>Output Amplifier Gains: 2, 2.4, 3, 3.6, 4.5, 6, 9 | | 8 to 1152 | | V/V |
| $V_{OUT}$ Slew Rate | | | 0.5 | | V/µs |
| $V_{OUT}$ Settling Time (0.01%) | $V_{OUT}/V_{IN}$ Differential Gain = 8, $R_L = 5k\Omega \parallel 200pF$ | | 6 | | µs |
| $V_{OUT}$ Settling Time (0.01%) | $V_{OUT}/V_{IN}$ Differential Gain = 191, $R_L = 5k\Omega \parallel 200pF$ | | 4.1 | | µs |
| $V_{OUT}$ Nonlinearity | | | 0.002 | | %FSR |
| External Sensor Output Sensitivity | $V_{SA} = V_{SD} = V_{EXC} = +5V$ | | 1 to 245 | | mV/V |
| **FRONT-END PGA** | | | | | |
| Auto-Zero Internal Frequency | | | 7 | | kHz |
| Offset Voltage (RTI)[2] | Coarse Offset Adjust Disabled | | ±3 | ±50 | µV |
| **vs Temperature** | | | **±0.2** | | **µV/°C** |
| vs Supply Voltage, $V_{SA}$ | | | ±2 | | µV/V |
| vs Common-Mode Voltage | $G_F$ = Front-End PGA Gain | | $1500/G_F$ | $6000/G_F$ | µV/V |
| Linear Input Voltage Range[3] | | 0.2 | | $V_{SA}-1.5$ | **V** |
| Input Bias Current | | | 0.1 | 1.5 | nA |
| Input Impedance: Differential | | | 30 ‖ 6 | | $G\Omega \parallel pF$ |
| Input Impedance: Common-Mode | | | 50 ‖ 20 | | $G\Omega \parallel pF$ |
| Input Voltage Noise | 0.1Hz to 10Hz, $G_F$ = 128 | | 4 | | µV$_{PP}$ |
| PGA Gain | | | | | |
| Gain Range Steps | 4, 8, 16, 23.27, 32, 42.67, 64, 128 | | 4 to 128 | | V/V |
| Initial Gain Error | $G_F$ = 4 to 42 | | 0.2 | ±1 | % |
| | $G_F$ = 64 | | 0.25 | ±1.2 | % |
| | $G_F$ = 128 | | 0.3 | ±1.6 | % |
| **vs Temperature** | | | **10** | | **ppm/°C** |
| **Output Voltage Range** | | | **0.05 to $V_{SA} - 0.1$** | | **V** |
| Bandwidth | Gain = 4 | | 400 | | kHz |
| | Gain = 128 | | 60 | | kHz |
| **COARSE OFFSET ADJUST**<br>**(RTI OF FRONT-END PGA)** | | | | | |
| Range | $\pm(14)(V_{REF})(0.00085)$ | ±56 | ±59.5 | ±64 | mV |
| **vs Temperature** | | | **0.004** | | **%/°C** |
| Resolution | ±14 steps, 4-Bit + Sign | | 4 | | mV |
| **FINE OFFSET ADJUST (ZERO DAC)**<br>**(RTO of the Front-End PGA)[2]** | | | | | |
| Programming Range | | 0 | | $V_{REF}$ | V |
| Output Range | | 0.1 | | $V_{SA}-0.1$ | V |
| Resolution | 65,536 steps, 16-Bit DAC | | 73 | | µV |
| Integral Nonlinearity | | | 20 | | LSB |
| Differential Nonlinearity | | | 0.5 | | LSB |
| Gain Error | | | 0.1 | | % |
| Gain Error Drift | | | 10 | | ppm/°C |
| Offset | | | 5 | | mV |
| Offset Drift | | | 10 | | µV/°C |
| **OUTPUT FINE GAIN ADJUST (GAIN DAC)** | | | | | |
| Range | | | 0.33 to 1 | | V/V |
| Resolution | 65,536 steps, 16-Bit DAC | | 10 | | µV/V |
| Integral NonLinearity | | | 20 | | LSB |
| Differential NonLinearity | | | 0.5 | | LSB |

# ELECTRICAL CHARACTERISTICS (continued)

**BOLDFACE** limits apply over the specified temperature range: $T_A$ = **–40°C to +125°C**

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY\ ANALOG}$, $V_{SD}$ = $V_{SUPPLY\ DIGITAL}$; $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}/REF_{OUT}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA309 | | | UNITS |
| --- | --- | --- | --- | --- | --- |
| | | MIN | TYP | MAX | |
| **OUTPUT AMPLIFIER** | | | | | |
| Offset Voltage (RTI of Output Amplifier)[2] | | | 3 | | mV |
| **vs Temperature** | | | **5** | | **μV/°C** |
| vs Supply Voltage, $V_{SA}$ | | | 30 | | μV/V |
| **Common-Mode Input Range** | | **0** | | **$V_{SA}$–1.5** | **V** |
| Input Bias Current | | | 100 | | pA |
| Amplifier Internal Gain | | | | | |
| Gain Range Steps | 2, 2.4, 3, 3.6, 4.5, 6, 9 | | 2 to 9 | | V/V |
| Initial Gain Error | 2, 2.4, 3.6 | | 0.25 | **±1** | **%** |
| | 4.5 | | 0.3 | ±1.2 | **%** |
| | 6 | | 0.4 | ±1.5 | **%** |
| | 9 | | 0.6 | ±2.0 | **%** |
| **vs Temperature** | **2, 2.4, 3.6** | | **5** | | **ppm/°C** |
| | **4.5** | | **5** | | **ppm/°C** |
| | **6** | | **15** | | **ppm/°C** |
| | **9** | | **30** | | **ppm/°C** |
| **Output Voltage Range**[4] | **$R_L$ = 10kΩ** | **0.1** | | **4.9** | **V** |
| Open Loop Gain | | | 115 | | dB |
| Gain-Bandwidth Product | | | 2 | | MHz |
| Phase Margin | Gain = 2, $C_L$ = 200pF | | 45 | | Degrees |
| Output Resistance | AC Small-Signal, Open-Loop, f = 1MHz, $I_O$ = 0 | | 675 | | Ω |
| **OVER- AND UNDER-SCALE LIMITS** | ($V_{REF}$ = 4.096) | | | | |
| Over-Scale Thresholds | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '000' | | 0.9708 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '001' | | 0.9610 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '010' | | 0.9394 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '011' | | 0.9160 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '100' | | 0.9102 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '101' | | 0.7324 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D5, D4, D3 = '110' | | 0.5528 | | |
| Over-Scale Comparator Offset | | +6 | +60 | +114 | mV |
| Over-Scale Comparator Offset Drift | | | +0.37 | | mV/°C |
| Under-Scale Thresholds | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '111' | | 0.0605 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '110' | | 0.0547 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '101' | | 0.0507 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '100' | | 0.0449 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '011' | | 0.0391 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '010' | | 0.0352 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '001' | | 0.0293 | | |
| | Ratio of $V_{REF}$, Register 5—Bits D2, D1, D0 = '000' | | 0.0254 | | |
| Under-Scale Comparator Offset | | –7 | –50 | +93 | mV |
| Under-Scale Comparator Offset Drift | | | –0.15 | | mV/°C |
| **FAULT MONITOR CIRCUIT** | | | | | |
| INP_HI, INN_HI Comparator Threshold | See Note 5 | | $V_{SA}$–1.2 or $V_{EXC}$–0.1 | | V |
| INP_LO, INN_LO Comparator Threshold | | 40 | 100 | | mV |
| A1SAT_HI, A2SAT_HI Comparator Threshold | | | $V_{SA}$–0.12 | | V |
| A1SAT_LO, A2SAT_LO Comparator Threshold | | | $V_{SA}$–0.12 | | V |
| A3_VCM Comparator Threshold | | | $V_{SA}$–1.2 | | V |
| Comparator Hysteresis | | | 20 | | mV |

## ELECTRICAL CHARACTERISTICS (continued)

**BOLDFACE** limits apply over the specified temperature range: **$T_A$ = −40°C to +125°C**

$T_A$ = +25°C, $V_{SA} = V_{SD}$ = +5V ($V_{SA} = V_{SUPPLY\ ANALOG}$, $V_{SD} = V_{SUPPLY\ DIGITAL}$; $V_{SA}$ must equal $V_{SD}$), $GND_D = GND_A$ = 0, and $V_{REF} = REF_{IN}/REF_{OUT}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA309 | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **INTERNAL VOLTAGE REFERENCE** | | | | | |
| $V_{REF1}$ | Register 3, Bit D9 = 1 | 2.46 | 2.5 | 2.53 | V |
| **$V_{REF1}$ Drift vs Temperature** | | | **+10** | | **ppm/°C** |
| $V_{REF2}$ | Register 3, Bit D9 = 0 | 4.0 | 4.096 | 4.14 | V |
| **$V_{REF2}$ Drift vs Temperature** | | | **+10** | | **ppm/°C** |
| Input Current $REF_{IN}/REF_{OUT}$ | Internal $V_{REF}$ Disabled | | 100 | | µA |
| Output Current $REF_{IN}/REF_{OUT}$ | $V_{SA} > $ 2.7V for $V_{REF}$ = 2.5V | | 1 | | mA |
| | $V_{SA} > $ 4.3V for $V_{REF}$ = 4.096V | | 1 | | mA |
| **TEMPERATURE SENSE CIRCUITRY (ADC)** | | | | | |
| Internal Temperature Measurement | Register 6, Bit D9 = 1 | | | | |
|   Accuracy | | | ±2 | | °C |
|   Resolution | 12-Bit + Sign, Two's Complement Data Format | | ±0.0625 | | °C |
|   Temperature Measurement Range | | −55 | | +150 | °C |
|   Conversion Rate | $R_1$, $R_0$ = '11', 12-Bit + Sign Resolution | | 24 | | ms |
| **TEMPERATURE ADC** | | | | | |
| External Temperature Mode | Temp PGA + Temp ADC | | | | |
|   Gain Range Steps | $G_{PGA}$ = 1, 2, 4, 8 | | 1 to 8 | | V/V |
|   Analog Input Voltage Range | | GND–0.2 | | $V_{SA}$+0.2 | V |
| Temperature ADC Internal REF (2.048V) | Register 6, Bit D8 = 1 | | | | V |
|   Full-Scale Input Voltage | (+Input) – (–Input) | | ±2.048/$G_{PGA}$ | | V |
|   Differential Input Impedance | | | 2.8/$G_{PGA}$ | | MΩ |
|   Common-Mode Input Impedance | $G_{PGA}$ = 1 | | 3.5 | | MΩ |
| | $G_{PGA}$ = 2 | | 3.5 | | MΩ |
| | $G_{PGA}$ = 4 | | 1.8 | | MΩ |
| | $G_{PGA}$ = 8 | | 0.9 | | MΩ |
|   Resolution | R1, R0 = '00', ADC2X = '0', Conversion Time = 8ms | | 11 | | Bits + Sign |
| | R1, R0 = '01', ADC2X = '0', Conversion Time = 32ms | | 13 | | Bits + Sign |
| | R1, R0 = '10', ADC2X = '0', Conversion Time = 64ms | | 14 | | Bits + Sign |
| | R1, R0 = '11', ADC2X = '0', Conversion Time = 128ms | | 15 | | Bits + Sign |
|   Integral Nonlinearity | | | 0.004 | | % |
|   Offset Error | $G_{PGA}$ = 1 | | 1.2 | | mV |
| | $G_{PGA}$ = 2 | | 0.7 | | mV |
| | $G_{PGA}$ = 4 | | 0.5 | | mV |
| | $G_{PGA}$ = 8 | | 0.4 | | mV |
|   Offset Drift | $G_{PGA}$ = 1 | | 1.2 | | µV/°C |
| | $G_{PGA}$ = 2 | | 0.6 | | µV/°C |
| | $G_{PGA}$ = 4 | | 0.3 | | µV/°C |
| | $G_{PGA}$ = 8 | | 0.3 | | µV/°C |
|   Offset vs $V_{SA}$ | $G_{PGA}$ = 1 | | 800 | | µV/V |
| | $G_{PGA}$ = 2 | | 400 | | µV/V |
| | $G_{PGA}$ = 4 | | 200 | | µV/V |
| | $G_{PGA}$ = 8 | | 150 | | µV/V |
|   Gain Error | | | 0.05 | 0.50 | % |
|   Gain Error Drift | | | 5 | 50 | ppm/°C |
|   Noise | All Gains | | < 1 | | LSB |
|   Gain vs $V_{SA}$ | | | 80 | | ppm/V |
|   Common-Mode Rejection | At DC and $G_{PGA}$ = 8 | | 105 | | dB |
| | At DC and $G_{PGA}$ = 1 | | 100 | | dB |

# ELECTRICAL CHARACTERISTICS (continued)

**BOLDFACE** limits apply over the specified temperature range: $T_A$ = –40°C to +125°C

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY ANALOG}$, $V_{SD}$ = $V_{SUPPLY DIGITAL}$; $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}/REF_{OUT}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA309 MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **TEMPERATURE ADC (CONTINUED)** | | | | | |
| Temp ADC Ext. REF ($V_{REFT}$ = $V_{REF}$, $V_{EXC}$, or $V_{SA}$) | Register 6, Bit D8 = 0 | | | | |
| Full-Scale Input Voltage | (+Input) – (–Input) | | $\pm V_{REFT}/G_{PGA}$ | | V |
| Differential Input Impedance | | | $2.4/G_{PGA}$ | | MΩ |
| Common-Mode Input Impedance | $G_{PGA}$ = 1 | | 8 | | MΩ |
| | $G_{PGA}$ = 2 | | 8 | | MΩ |
| | $G_{PGA}$ = 4 | | 8 | | MΩ |
| | $G_{PGA}$ = 8 | | 8 | | MΩ |
| Resolution | R1, R0 = '00', ADC2X = '0', Conversion Time = 6ms | | 11 | | Bits + Sign |
| | R1, R0 = '01', ADC2X = '0', Conversion Time = 24ms | | 13 | | Bits + Sign |
| | R1, R0 = '10', ADC2X = '0', Conversion Time = 50ms | | 14 | | Bits + Sign |
| | R1, R0 = '11', ADC2X = '0', Conversion Time = 100ms | | 15 | | Bits + Sign |
| Integral Nonlinearity | | | 0.01 | | % |
| Offset Error | $G_{PGA}$ = 1 | | 2.5 | | mV |
| | $G_{PGA}$ = 2 | | 1.25 | | mV |
| | $G_{PGA}$ = 4 | | 0.7 | | mV |
| | $G_{PGA}$ = 8 | | 0.3 | | mV |
| Offset Drift | $G_{PGA}$ = 1 | | 1.5 | | µV/°C |
| | $G_{PGA}$ = 2 | | 1.0 | | µV/°C |
| | $G_{PGA}$ = 4 | | 0.7 | | µV/°C |
| | $G_{PGA}$ = 8 | | 0.6 | | µV/°C |
| Gain Error | | | –0.2 | | % |
| Gain Error Drift | | | 2 | | ppm/°C |
| Gain vs $V_{SA}$ | | | 80 | | ppm/V |
| Common-Mode Rejection | At DC and $G_{PGA}$ = 8 | | 100 | | dB |
| | At DC and $G_{PGA}$ = 1 | | 85 | | dB |
| External Temperature Current Excitation    $I_{TEMP}$ | Register 6, Bit D11 = 1 | | | | |
| Current Excitation | | 5.8 | 7 | 8 | µA |
| Temperature Drift | | | 5 | | nA/°C |
| Voltage Compliance | | | $V_{SA}$–1.2 | | V |
| **LINEARIZATION ADJUST AND EXCITATION VOLTAGE ($V_{EXC}$)** | | | | | |
| Range 0 | Register 3, Bit D11 = 0 | | | | |
| Linearization DAC Range | With Respect to $V_{FB}$ | | –0.166 to +0.166 | | V/V |
| Linearization DAC Resolution | ±127 Steps, 7-Bit + Sign | | 1.307 | | mV/V |
| $V_{EXC}$ Gain | With Respect to $V_{REF}$ | | 0.83 | | V/V |
| Gain Error Drift | | | 25 | | ppm/°C |
| Range 1 | Register 3, Bit D11 = 1 | | | | |
| Linearization DAC Range | With Respect to $V_{FB}$ | | –0.124 to +0.124 | | V/V |
| Linearization DAC Resolution | ±127 Steps, 7-Bit + Sign | | 0.9764 | | mV/V |
| $V_{EXC}$ Gain | With Respect to $V_{REF}$ | | 0.52 | | V/V |
| Gain Error Drift | | | 25 | | ppm/°C |
| $V_{EXC}$ Range Upper Limit | $I_{EXC}$ = 5mA | | $V_{SA}$ – 0.5 | | V |
| $I_{EXC SHORT}$ | Short-Circuit $V_{EXC}$ Output Current | | 50 | | mA |
| **DIGITAL INTERFACE** | | | | | |
| Two-Wire Compatible | Bus Speed | 1 | | 400 | kHz |
| One-Wire | Serial Speed Baud Rate | 4.8K | | 38.4K | Bits/s |
| Maximum Lookup Table Size[6] | | | 17 x 3 x 16 | | Bits |
| Two-Wire Data Rate | PGA309 to EEPROM (SCL frequency) | | 65 | | kHz |
| **LOGIC LEVELS** | | | | | |
| Input Levels (SDA, SCL, PRG, TEST) | Low | | | $0.2 \cdot V_{SD}$ | V |
| (SDA, SCL, PRG, TEST) | High | $0.7 \cdot V_{SD}$ | | | V |
| (SDA, SCL) | Hysteresis | | $0.1 \cdot V_{SD}$ | | V |
| Pull-Up Current Source (SDA, SCL) | | 55 | 85 | 125 | µA |
| Pull-Down Current Source (TEST) | | 15 | 25 | 40 | µA |
| Output LOW Level (SDA, SCL, PRG) | Open Drain, $I_{SINK}$ = 5mA | | | 0.4 | V |

## ELECTRICAL CHARACTERISTICS (continued)

**BOLDFACE** limits apply over the specified temperature range: $T_A$ = **–40°C to +125°C**

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY\ ANALOG}$, $V_{SD}$ = $V_{SUPPLY\ DIGITAL}$; $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}/REF_{OUT}$ = +5V, unless otherwise noted.

| PARAMETER | CONDITIONS | PGA309 | | | UNITS |
|---|---|---|---|---|---|
| | | **MIN** | **TYP** | **MAX** | |
| **POWER SUPPLY** | | | | | |
| $V_{SA}$, $V_{SD}$ | | 2.7 | | 5.5 | V |
| $I_{SA}$ + $I_{SD}$, Quiescent Current | $V_{SA}$ = $V_{SD}$ = +5V, without Bridge Load | | 1.2 | 1.6 | mA |
| **POWER-ON RESET** | | | | | |
| **Power-Up Threshold** | **$V_{SA}$ Rising** | | **2.2** | **2.7** | **V** |
| Power-Down Threshold | $V_{SA}$ Falling | | 1.7 | | V |
| **TEMPERATURE RANGE** | | | | | |
| Specified Performance | | –40 | | +125 | °C |
| Operational – Degraded Performance | | –55 | | +150 | °C |

(1) PGA309 total differential gain from input ($V_{IN1}$–$V_{IN2}$) to output ($V_{OUT}$). $V_{OUT}$ / ($V_{IN1}$–$V_{IN2}$) = (Front-End PGA gain) (Output Amplifier gain) (Gain DAC).

(2) RTI = referred to input. RTO = referred to output.

(3) Linear input range is the allowed min/max voltage on the $V_{IN1}$ and $V_{IN2}$ pins for the input PGA to continue to operate in a linear region. The allowed common-mode and differential voltage is dependent upon gain and offset settings. Refer to the Gain Scaling section for more information.

(4) Unless limited by over/under-scale setting.

(5) When $V_{EXC}$ is enabled, a minimum reference selector circuit becomes the reference for the comparator threshold. This minimum reference selector circuit uses $V_{EXC}$ – 100mV and $V_{SA}$ – 1.2V and compares the $V_{INX}$ pin to the lower of the two references. This ensures accurate fault monitoring in conditions where $V_{EXC}$ might be higher or lower than the input CMR of the PGA input amplifier relative to $V_{SA}$.

(6) Lookup Table allows multislope compensation over temperature. Lookup Table has access to 17 calibration points consisting of 3 adjustment values (Tx, Temperature, ZMx, Zero DAC, GMx, Gain DAC) that are stored in 16-bit data format (17x3x16 = Lookup Table size).
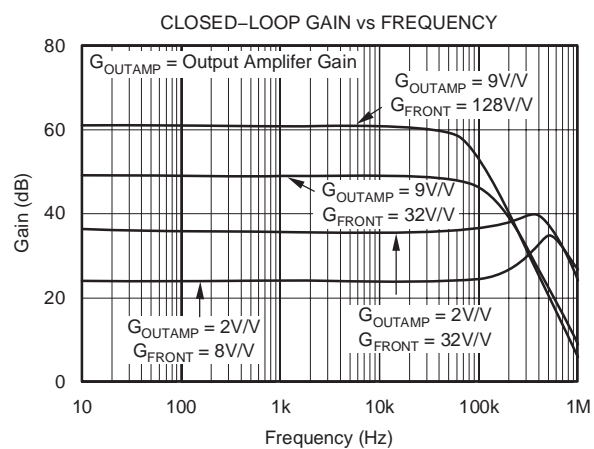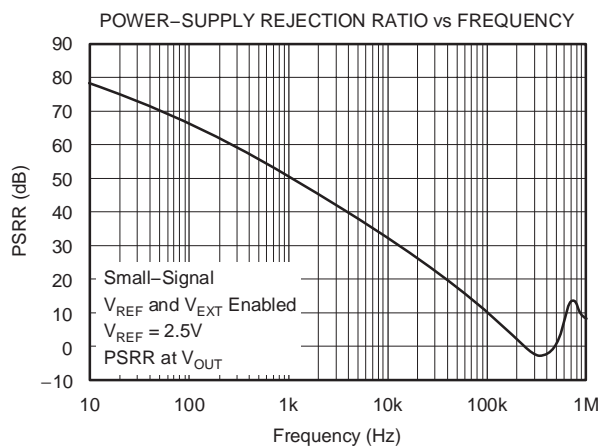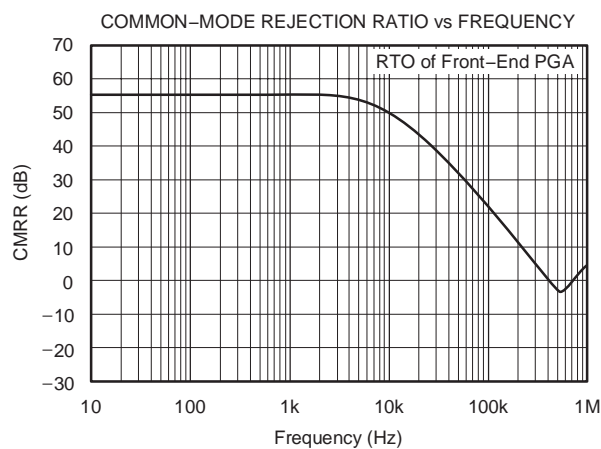
# PGA309

## PIN CONFIGURATION

**Top View**                                                                 **TSSOP**

| | | |
|---|---|---|
| $V_{EXC}$ | 1 | 16 | $REF_{IN}/REF_{OUT}$ |
| $GND_A$ | 2 | 15 | $TEMP_{IN}$ |
| $V_{SA}$ | 3 | 14 | SDA |
| $V_{IN1}$ | 4 | 13 | SCL |
| $V_{IN2}$ | 5 | 12 | PRG |
| $V_{FB}$ | 6 | 11 | $GND_D$ |
| $V_{OUT}$ | 7 | 10 | $V_{SD}$ |
| $V_{SJ}$ | 8 | 9 | TEST |

PGA309
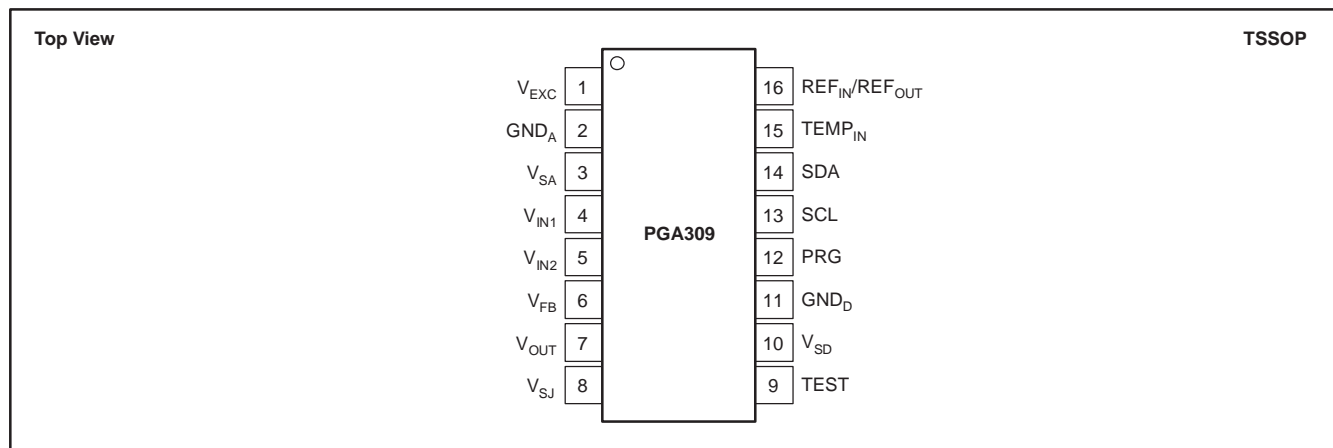
## PIN DESCRIPTION

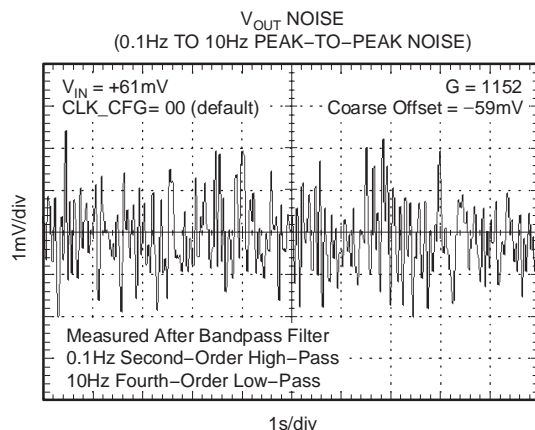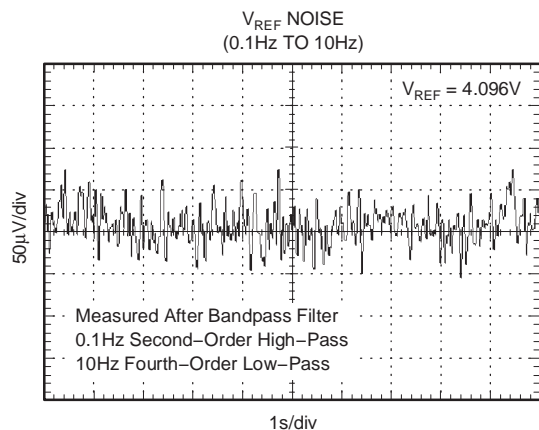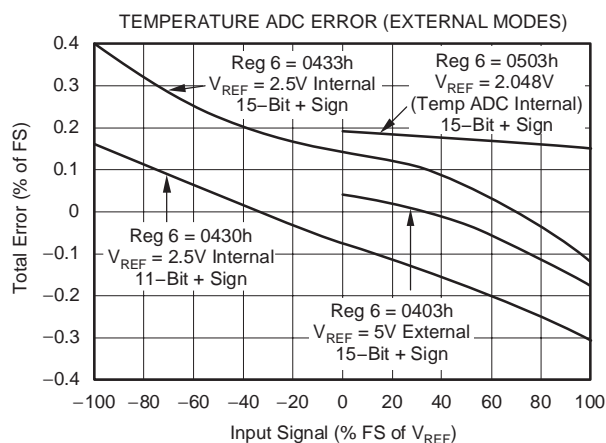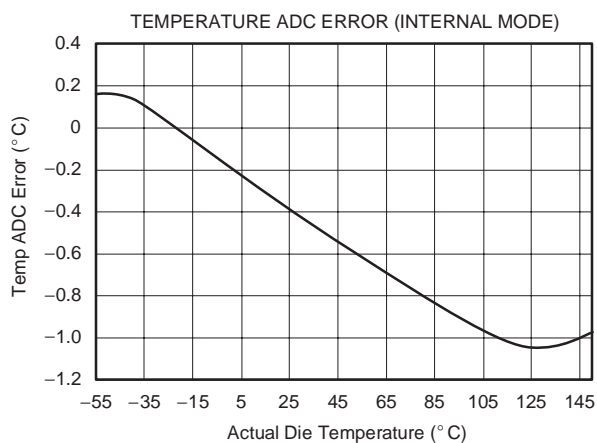| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{EXC}$ | Bridge sensor excitation. Connect to bridge if linearization and/or internal reference for bridge excitation is to be used. |
| 2 | $GND_A$ | Analog ground. Connect to analog ground return path for $V_{SA}$. Should be same as $GND_D$. |
| 3 | $V_{SA}$ | Analog voltage supply. Connect to analog voltage supply. To be within 200mV of $V_{SD}$. |
| 4 | $V_{IN1}$ | Signal input voltage 1. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA. |
| 5 | $V_{IN2}$ | Signal input voltage 2. Connect to + or – output of sensor bridge. Internal multiplexer can change connection internally to Front-End PGA. |
| 6 | $V_{FB}$ | $V_{OUT}$ feedback pin. Voltage feedback sense point for over/under-scale limit circuitry. When internal gain set resistors for the output amplifier are used, this is also the voltage feedback sense point for the output amplifier. $V_{FB}$ in combination with $V_{SJ}$ allows for ease of external filter and protection circuits without degrading the PGA309 $V_{OUT}$ accuracy. $V_{FB}$ must always be connected to either $V_{OUT}$ or the point of feedback for $V_{OUT}$, if external protection is used. |
| 7 | $V_{OUT}$ | Analog output voltage of conditioned sensor. |
| 8 | $V_{SJ}$ | Output amplifier summing junction. Use for output amplifier compensation when driving large capacitive loads (> 100pF) and/or for using external gain setting resistors for the output amplifier. |
| 9 | TEST | Test/External Controller Mode pin. Pull to $GND_D$ in normal mode. |
| 10 | $V_{SD}$ | Digital voltage supply. Connect to digital voltage supply. To be within 200mV of $V_{SA}$. |
| 11 | $GND_D$ | Digital ground. Connect to digital ground return path for $V_{SD}$. Should be same as $GND_A$. |
| 12 | PRG | Single-wire interface program pin. UART-type interface for digital calibration of the PGA309 over a single wire. Can be connected to $V_{OUT}$ for a three-lead ($V_S$, GND, $V_{OUT}$) digitally-programmable sensor assembly. |
| 13 | SCL | Clock input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface. |
| 14 | SDA | Data input/output for Two-Wire, industry-standard compatible interface for reading and writing digital calibration and configuration from external EEPROM. Can also communicate directly to the registers in the PGA309 through the Two-Wire, industry-standard compatible interface. |
| 15 | $TEMP_{IN}$ | External temperature signal input. PGA309 can be configured to read a bridge current sense resistor as an indicator of bridge temperature, or an external temperature sensing device such as diode junction, RTD, or thermistor. This input can be internally gained by 1, 2, 4, or 8. In addition, this input can be read differentially with respect to $V_{GNDA}$, $V_{EXC}$, or the internal/external $V_{REF}$. There is also an internal, register-selectable, $7\mu A$ current source ($I_{TEMP}$) that can be connected to $TEMP_{IN}$ as an RTD, thermistor, or diode excitation source. |
| 16 | $REF_{IN}/REF_{OUT}$ | Reference input/output pin. As an output, the internal reference (selectable as 2.5V or 4.096V) is available for system use on this pin. As an input, the internal reference may be disabled and an external reference can then be applied as the reference for the PGA309. |

# TYPICAL CHARACTERISTICS

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY\ ANALOG}$, $V_{SD}$ = $V_{SUPPLY\ DIGITAL}$, $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}$/$REF_{OUT}$ = +5V, unless otherwise noted.



$V_{REF}$ vs TEMPERATURE



$I_B$ CURRENT vs TEMPERATURE



$I_{TEMP}$ CURRENT vs TEMPERATURE



COMMON–MODE REJECTION RATIO vs FREQUENCY



POWER–SUPPLY REJECTION RATIO vs FREQUENCY



CLOSED–LOOP GAIN vs FREQUENCY

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# TYPICAL CHARACTERISTICS (Cont.)

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY\ ANALOG}$, $V_{SD}$ = $V_{SUPPLY\ DIGITAL}$, $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}/REF_{OUT}$ = +5V, unless otherwise noted.

$V_{OUT}$ SWING TO RAIL vs $I_{LOAD}$

$V_S$ = 2.7V
$V_S$ = 5V
$V_S$ = 5V
$V_S$ = 2.7V

$I_{LOAD}$ (mA)

$I_Q$ vs TEMPERATURE

All Blocks Enabled

Ref, Exc, and ADC Disabled

$I_Q$ (mA)

Temperature (°C)

TEMPERATURE ADC ERROR (INTERNAL MODE)

Temp ADC Error (°C)

Actual Die Temperature (°C)

TEMPERATURE ADC ERROR (EXTERNAL MODES)

Reg 6 = 0433h
$V_{REF}$ = 2.5V Internal
15–Bit + Sign

Reg 6 = 0503h
$V_{REF}$ = 2.048V
(Temp ADC Internal)
15–Bit + Sign

Reg 6 = 0430h
$V_{REF}$ = 2.5V Internal
11–Bit + Sign

Reg 6 = 0403h
$V_{REF}$ = 5V External
15–Bit + Sign

Total Error (% of FS)

Input Signal (% FS of $V_{REF}$)

$V_{REF}$ NOISE
(0.1Hz TO 10Hz)

$V_{REF}$ = 4.096V

50μV/div

Measured After Bandpass Filter
0.1Hz Second–Order High–Pass
10Hz Fourth–Order Low–Pass

1s/div

$V_{OUT}$ NOISE
(0.1Hz TO 10Hz PEAK–TO–PEAK NOISE)

$V_{IN}$ = +61mV
CLK_CFG = 00 (default)

G = 1152
Coarse Offset = –59mV

1mV/div

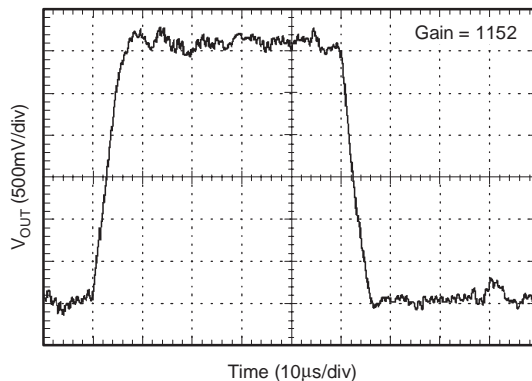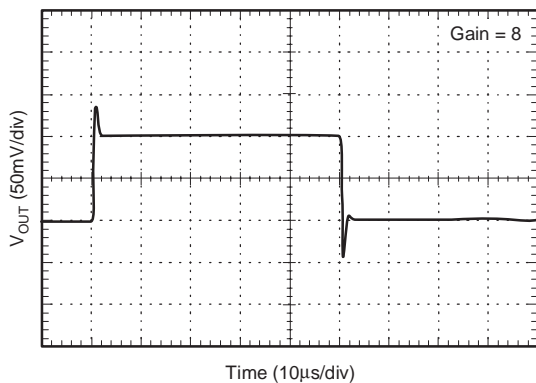Measured After Bandpass Filter
0.1Hz Second–Order High–Pass
10Hz Fourth–Order Low–Pass

1s/div

# TYPICAL CHARACTERISTICS (Cont.)

$T_A = +25°C$, $V_{SA} = V_{SD} = +5V$ ($V_{SA} = V_{SUPPLY\ ANALOG}$, $V_{SD} = V_{SUPPLY\ DIGITAL}$, $V_{SA}$ must equal $V_{SD}$), $GND_D = GND_A = 0$, and $V_{REF} = REF_{IN}/REF_{OUT} = +5V$, unless otherwise noted.
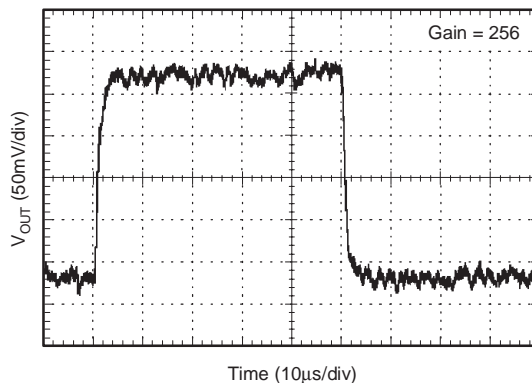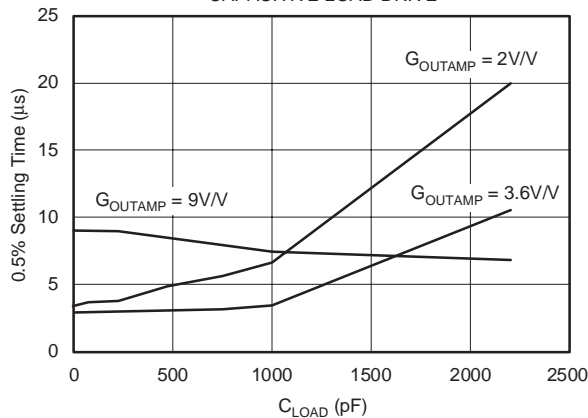
LARGE–SIGNAL STEP RESPONSE
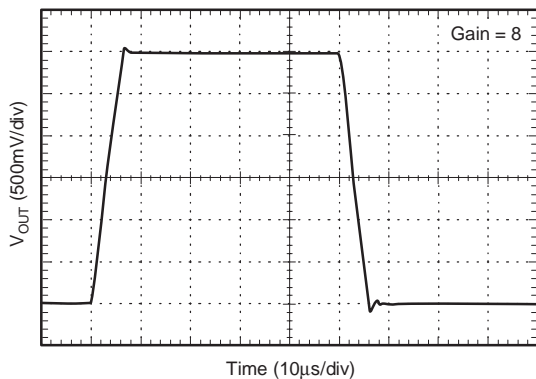
Gain = 8

$V_{OUT}$ (500mV/div)

Time (10µs/div)

LARGE–SIGNAL STEP RESPONSE

Gain = 1152

$V_{OUT}$ (500mV/div)

Time (10µs/div)

SMALL–SIGNAL STEP RESPONSE

Gain = 8

$V_{OUT}$ (50mV/div)

Time (10µs/div)

SMALL–SIGNAL STEP RESPONSE

Gain = 256

$V_{OUT}$ (50mV/div)

Time (10µs/div)

CAPACITIVE LOAD DRIVE

0.5% Settling Time (µs)

$G_{OUTAMP} = 2V/V$

$G_{OUTAMP} = 9V/V$

$G_{OUTAMP} = 3.6V/V$

$C_{LOAD}$ (pF)

OVERVOLTAGE RECOVERY

$V_{OUT}$

$V_{IN}$

$V_{IN}$ (200mV/div), $V_{OUT}$ (1V/div)

Time (100µs/div)

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# TYPICAL CHARACTERISTICS (Cont.)

$T_A$ = +25°C, $V_{SA}$ = $V_{SD}$ = +5V ($V_{SA}$ = $V_{SUPPLY\ ANALOG}$, $V_{SD}$ = $V_{SUPPLY\ DIGITAL}$, $V_{SA}$ must equal $V_{SD}$), $GND_D$ = $GND_A$ = 0, and $V_{REF}$ = $REF_{IN}$/$REF_{OUT}$ = +5V, unless otherwise noted.

OUTPUT AMPLIFIER
OPEN–LOOP GAIN/PHASE vs FREQUENCY

ZERO DAC TYPICAL ERROR vs CODE

GAIN DAC TYPICAL ERROR vs CODE
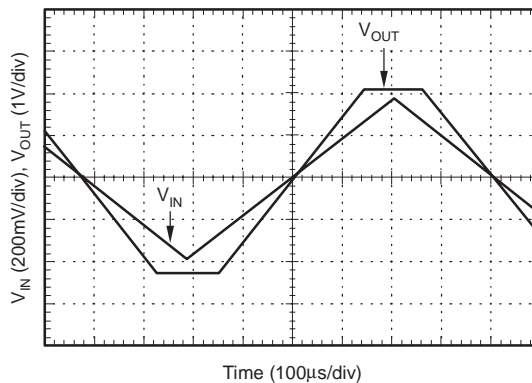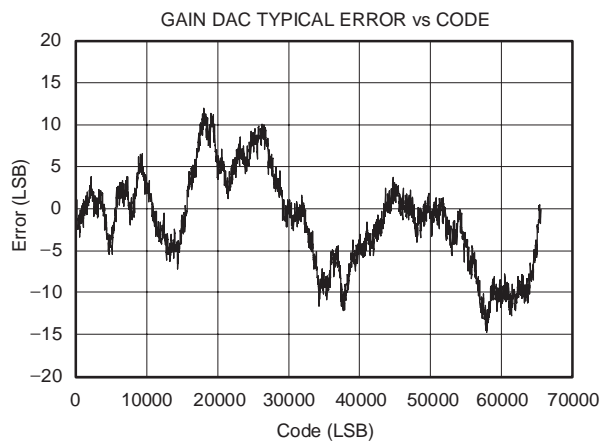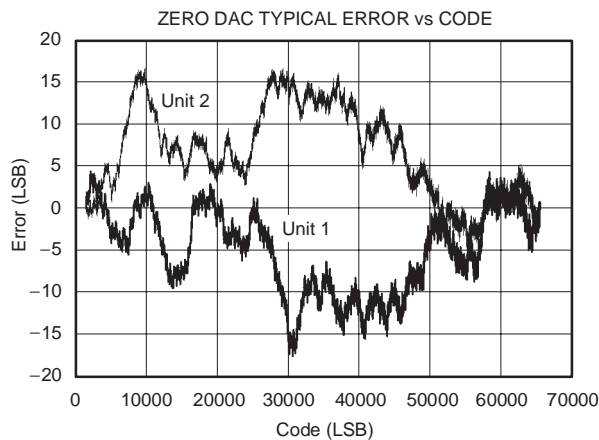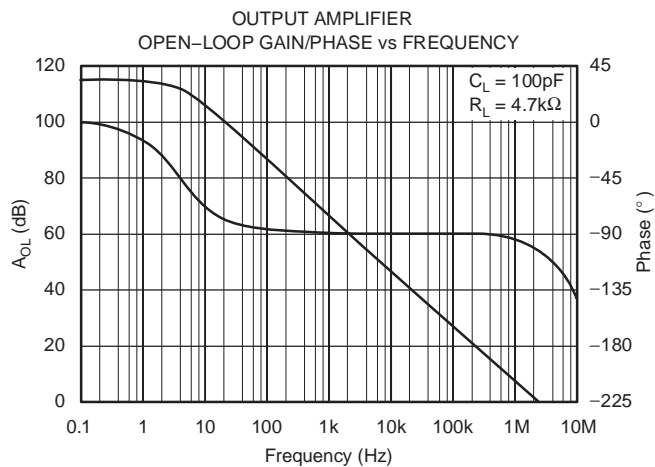
# FUNCTIONAL DESCRIPTION

The PGA309 is a programmable analog signal conditioner designed for resistive bridge sensor applications. It is a complete signal conditioner with bridge excitation, initial span and offset adjustment, temperature adjustment of span and offset, internal/external temperature measurement capability, output over-scale and under-scale limiting, fault detection, and digital calibration. The PGA309, in a calibrated sensor module, can reduce errors to the level approaching the bridge sensor repeatability. Figure 1 shows a block diagram of the PGA309. Following is a brief overview of each major function.

## SENSOR ERROR ADJUSTMENT RANGE

The adjustment capability of the PGA309 is summarized in Table 1.

| FSS (full-scale sensitivity) | 1mV/V to 245mV/V |
|---|---|
| Span TC | Over ±3300ppmFS/°C[1] |
| Span TC nonlinearity | $\geq$ 10% |
| Zero offset | ±200%FS[2] |
| Zero offset TC | Over ±3000ppmFS/°C[2] |
| Zero offset TC nonlinearity | $\geq$ 10% |
| Sensor impedance | Down to 200Ω[3] |

[1] Depends on the temperature sensing scheme
[2] Combined coarse and fine offset adjust
[3] Lower impedance possible by using a dropping resistor in series with the bridge

Table 1. PGA309 Adjustment Capability

## GAIN SCALING

The core of the PGA309 is the precision low-drift and no 1/f noise Front-End PGA. The overall gain of the Front-End PGA + Output Amplifier can be adjusted from 2.7V/V to 1152V/V. The polarity of the inputs can be switched through the 2x2 input mux to accommodate sensors with unknown polarity output.

The Front-End PGA provides initial coarse signal gain using a no 1/f noise, auto-zero instrumentation amplifier. The fine gain adjust is accomplished by the 16-bit attenuating Gain Digital-to-Analog Converter (Gain DAC). This Gain DAC is controlled by the data in the Temperature Compensation Lookup Table driven by the Temperature Analog-to-Digital Converter (Temp ADC). In order to compensate for second-order and higher drift nonlinearity, the span drift can be fitted to piecewise linear curves during calibration with the coefficients stored in an external nonvolatile EEPROM lookup table.

Following the fine gain adjust stage is the Output Amplifier that provides additional programmable gain. Two key output amplifier connections, $V_{FB}$ and $V_{SJ}$, are brought out on the PGA309 for application flexibility. These connections allow for an accurate conditioned signal voltage while also providing a means for PGA309 output overvoltage and large capacitive loading for RFI/EMI filtering required in many end applications.

## OFFSET ADJUSTMENT

The sensor offset adjustment is performed in two stages. The input-referred Coarse Offset Adjust DAC has approximately a ±60mV offset adjustment range for a selected $V_{REF}$ of 5V. The fine offset and the offset drift are canceled by the 16-bit Zero DAC that sums the signal with the output of the front-end instrumentation amplifier. Similar to the Gain DAC, the input digital values of the Zero DAC are controlled by the data in the Temperature Compensation Lookup Table, stored in external EEPROM, driven by the Temp ADC. The programming range of the Zero DAC is 0V to $V_{REF}$ with an output range of 0.1V to $V_{SA} - 0.1V$.

## VOLTAGE REFERENCE

The PGA309 contains a precision low-drift voltage reference (selectable for 2.5V or 4.096V) that can be used for external circuitry through the $REF_{IN}/REF_{OUT}$ pin. This same reference is used for the Coarse Offset Adjust DAC, Zero DAC, Over/Under-Scale Limits and sensor excitation/linearization through the $V_{EXC}$ pin. When the internal reference is disabled, the $REF_{IN}/REF_{OUT}$ pin should be connected to an external reference or to $V_{SA}$ for ratiometric-scaled systems.

## SENSOR EXCITATION AND LINEARIZATION

A dedicated circuit with a 7-bit + sign DAC for sensor voltage excitation and linearization is provided on the PGA309. This block scales the reference voltage and sums it with a portion of the PGA309 output to compensate the positive or negative bow-shaped nonlinearity exhibited by many sensors over their applied pressure range. Sensors not requiring linearization can be connected directly to the supply ($V_{SA}$) or to the $V_{EXC}$ pin with the Linearization DAC (Lin DAC) set to zero.
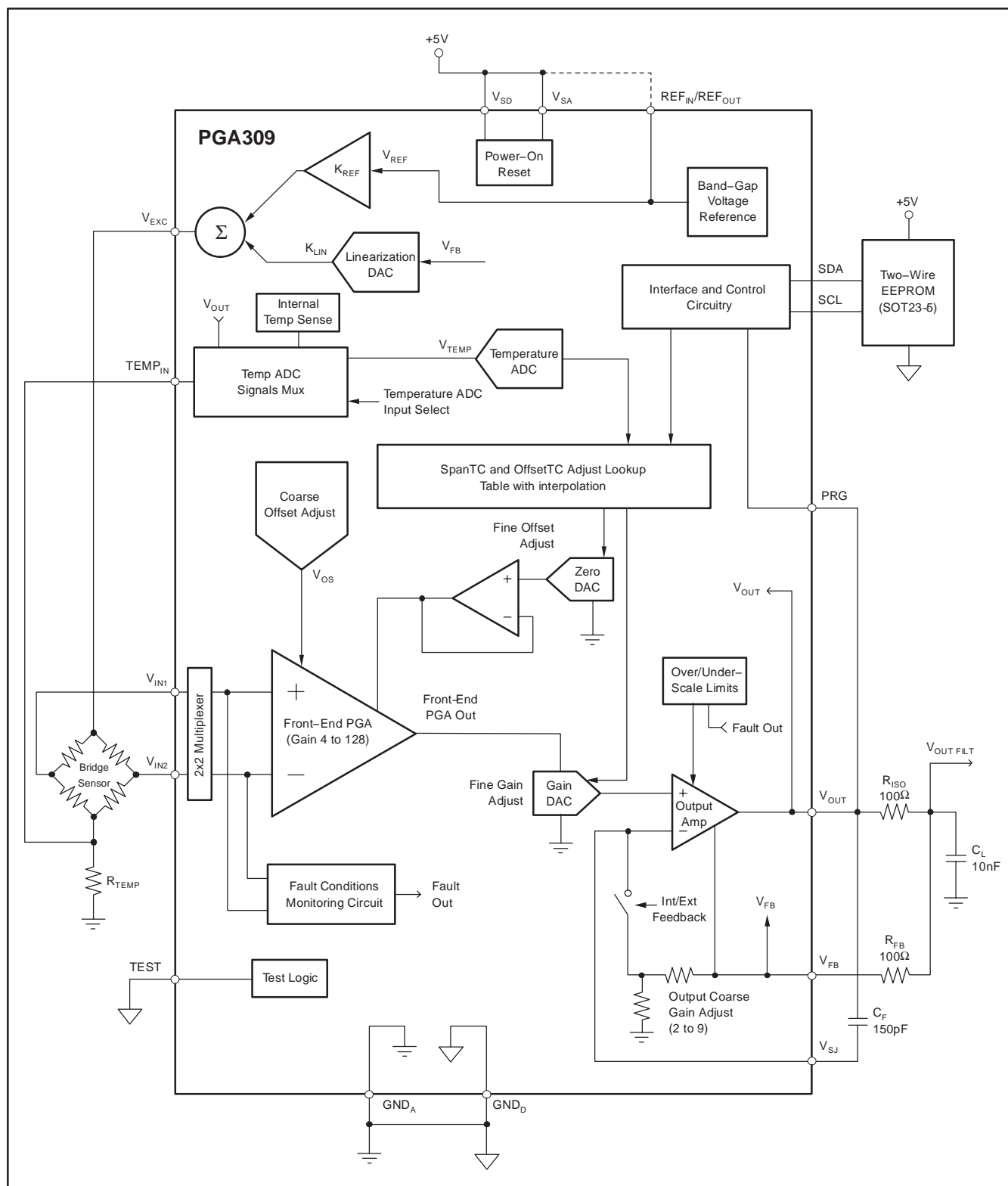
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Figure 1. Simplified Diagram of the PGA309 in a Typical Configuration.

**ADC FOR TEMPERATURE SENSING**

The temperature sense circuitry drives the compensation for the sensor span and offset drift. Either internal or external temperature sensing is possible. The temperature can be sensed in one of the following ways:

- Bridge impedance change (excitation current sense, in the positive or negative part of the bridge), for sensors with large temperature coefficient of resistance (TCR > 0.1%/°C).
- On-chip PGA309 temperature, when the chip is located sufficiently close to the sensor.
- External diode, thermistor, or RTD placed on the sensor membrane. An internal 7µA current source may be enabled to excite these types of temperature sensors.

The temperature signal is digitized by the onboard Temp ADC. The output of the Temp ADC is used by the control digital circuit to read the data from the Lookup Table in an external EEPROM, and set the output of the Gain DAC and the Zero DAC to the calibrated values as temperature changes.

An additional function provided through the Temp ADC is the ability to read the $V_{OUT}$ pin back through the Temp ADC input mux. This provides flexibility for a digital output through either One-Wire or Two-Wire interface, as well as the possibility for an external microcontroller to perform real-time custom calibration of the PGA309.

**EXTERNAL EEPROM AND TEMPERATURE COEFFICIENTS**

The PGA309 uses an industry-standard Two-Wire external EEPROM (typically, a SOT23-5 package). A 1k-bit (minimum) EEPROM is needed when using all 17 temperature coefficients. Larger EEPROMs may be used to provide space for a serial number, lot code, or other data.

The first part of the external EEPROM contains the configuration data for the PGA309, with settings for:

- Register 3—Reference Control and Linearization
- Register 4—PGA Coarse Offset and Gain/Output Amplifier Gain
- Register 5—PGA Configuration and Over/Under-Scale Limit
- Register 6—Temp ADC Control

This section of the EEPROM contains its own individual checksum (Checksum1).

The second part of the external EEPROM contains up to 17 temperature index values and corresponding temperature coefficients for the Zero DAC and Gain DAC adjustments with measured temperature, and also contains its own checksum (Checksum2).

The PGA309 lookup logic contains a linear interpolation algorithm for accurate DAC adjustments between stored temperature indexes. This approach allows for a piecewise linear temperature compensation of up to 17 temperature indexes and associated temperature coefficients.

If either Checksum1, Checksum2, or both are incorrect, the output of the PGA309 is set to high-impedance.

**FAULT MONITOR**

To detect sensor burnout or a short, a set of four comparators are connected to the inputs of the Front-End PGA. If any of the inputs are taken to within 100mV of ground or $V_{EXC}$, or violate the input CMR of the Front-End PGA, then the corresponding comparator sets a sensor fault flag that causes the PGA309 $V_{OUT}$ to be driven within 100mV of either $V_{SA}$ or ground, depending upon the alarm configuration setting (Register 5—PGA Configuration and Over/Under-Scale Limit). This will be well above the set Over-Scale Limit level or well below the set Under-Scale Limit level. The state of the fault condition can be read in digital form in Register 8—Alarm Status Register. If the Over/Under-Scale Limit is disabled, the PGA309 output voltage will still be driven within 100mV of either $V_{SA}$ or ground, depending upon the alarm configuration setting.

There are five other fault detect comparators that help detect subtle PGA309 front-end violations that could otherwise result in linear voltages at $V_{OUT}$ that would be interpreted as valid states. These are especially useful during factory calibration and setup, and are configured through Register 5—PGA Configuration and Over/Under-Scale Limit. Their status can also be read back through Register 8—Alarm Status Register.

**OVER-SCALE AND UNDER-SCALE LIMITS**

The over-scale and under-scale limit circuitry combined with the fault monitor circuitry provides a means for system diagnostics. A typical sensor-conditioned output may be scaled for 10% to 90% of the system ADC range for the sensor normal operating range. If the conditioned pressure sensor is below 4%, it is considered under-pressure; if over 96%, it is considered over-pressure.

The PGA309 over/under-scale limit circuit can be programmed individually for under-scale and over-scale values that clip or limit the PGA309 output. From a system diagnostic view, 10% to 90% of ADC range is normal operation, < 4% is under-pressure, and > 96% is over-pressure. If the fault detect circuitry is used, a detected fault will cause the PGA309 output to be driven to positive or negative saturation. If this fault

flag is programmed for high, then > 97% ADC range will be a fault; if programmed for low, then < 3% ADC range will be a fault. In this configuration, the system software can be used to distinguish between over- or under-pressure condition, which indicates an out-of-control process, or a sensor fault.

## POWER-UP AND NORMAL OPERATION

The PGA309 has circuitry to detect when the power supply is applied to the PGA309, and reset the internal registers and circuitry to an initial state. This reset also occurs when the supply is detected to be invalid, so that the PGA309 is in a known state when the supply becomes valid again. The rising threshold for this circuit is typically 2.2V and the falling threshold is typically 1.7V. After the power supply becomes valid, the PGA309 waits for approximately 25ms and then attempts to read the configuration data from the external EEPROM device.

If the EEPROM has the proper flag set in address locations 0 and 1, then the PGA309 continues reading the first part of the EEPROM; otherwise, the PGA309 waits for one second before trying again. If the PGA309 detects no response from the EEPROM, the PGA309 waits for one second and tries again; otherwise, the PGA309 tries to free the bus and waits for 25ms before trying to read the EEPROM again. If a successful read of the first part of the EEPROM is accomplished, (including valid Checksum1 data), the PGA309 triggers the Temp ADC to measure temperature. For 16-bit resolution results, the converter takes approximately 125ms to complete a conversion. Once the conversion is complete, the PGA309 begins reading the Lookup Table information from the EEPROM (second part) to calculate the settings for the Gain DAC and Zero DAC.

The PGA309 reads the entire Lookup Table so that it can determine if the checksum for the Lookup Table (Checksum2) is correct. Each entry in the Lookup Table requires approximately 500µs to read from the EEPROM. Once the checksum is determined to be valid, the calculated values for the Gain and Zero DACs are updated into their respective registers, and the output amplifier is enabled. The PGA309 then begins looping through this entire procedure, starting with reading the EEPROM configuration registers from the first part of the EEPROM, then starting a new conversion on the Temp ADC, which then triggers reading the Lookup Table data from the second part of the EEPROM. This loop continues indefinitely.

## DIGITAL INTERFACE

There are two digital interfaces on the PGA309. The PRG pin uses a One-Wire, UART-compatible interface with bit rates from 4.8Kbits/s to 38.4Kbits/s. The SDA and SCL pins together form an industry standard Two-Wire interface at clock rates from 1kHz to 400kHz. The external EEPROM uses the Two-Wire interface. Communication to the PGA309 internal registers, as well as to the external EEPROM, for programming and readback can be conducted through either digital interface.

It is also possible to connect the One-Wire communication pin, PRG, to the $V_{OUT}$ pin in true three-wire sensor modules and still allow for programming. In this mode, the PGA309 output amplifier may be enabled for a set time period and then disabled again to allow sharing of the PRG pin with the $V_{OUT}$ connection. This allows for both digital calibration and analog readback during sensor calibration in a three-wire sensor module.

The Two-Wire interface has timeout mechanisms to prevent bus lockup from occurring. The Two-Wire master controller in the PGA309 has a mode that attempts to free up a stuck-at-zero SDA line by issuing SCL pulses, even when the bus is not indicated as idle after a timeout period has expired. The timeout will only apply when the master portion of the PGA309 is attempting to initiate a Two-Wire communication.
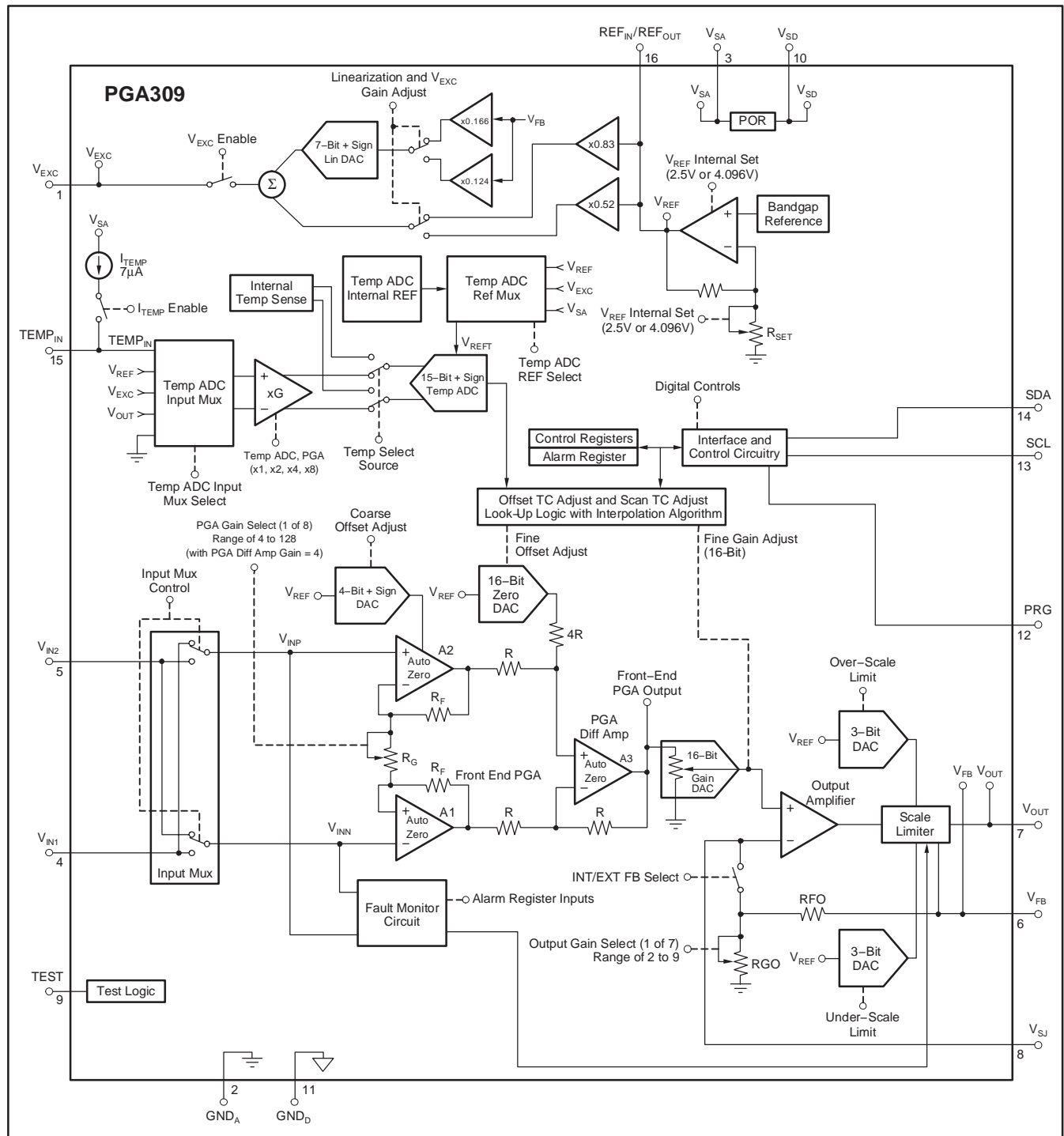
# DETAILED BLOCK DIAGRAM



Figure 2. Detailed Block Diagram

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| PGA309AIPWR | ACTIVE | TSSOP | PW | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SNPB | Level-1-260C-UNLIM |
| PGA309AIPWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | CU SNPB | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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**PW (R-PDSO-G\*\*)**  **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**

| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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