

- Peripheral Component Interconnect (PCI) Power Management Compliant
- ACPI 1.0 Compliant
- Packaged in 256-Pin BGA
- PCI Local Bus Specification Revision 2.1 Compliant
- 1995 PC Card™ Standard Compliant
- 3.3-V Core Logic With Universal PCI Interfaces Compatible With 3.3-V and 5-V PCI Signaling Environments
- Mix-and-Match 5-V/3.3-V PC Card16 Cards and 3.3-V CardBus Cards
- Supports Two PC Card or CardBus Slots With Hot Insertion and Removal
- Uses Serial Interface to TI™ TPS2206 Dual Power Switch
- Supports Burst Transfers to Maximize Data Throughput on Both PCI Buses
- Supports Serialized Interrupt request (IRQ) With PCI Interrupts
- 8-Way Legacy IRQ Multiplexing
- System Interrupts Can Be Programmed as PCI Style or Industry Standard Architecture (ISA-IRQ) Style
- ISA-IRQ Interrupts Can Be Serialized Onto a Single IRQ Serial (IRQSER) Pin
- EEPROM Interface for Loading Subsystem ID and Subsystem Vendor ID
- Pipelined Architecture Allows Greater Than 130M-Bytes-Per-Second Throughput From CardBus to PCI and From PCI to CardBus
- Supports Zoom Video With Internal Buffering
- Programmable Output Select for CLKRUN
- Four General Purpose I/Os
- Multifunction PCI Device With Separate Configuration Space for Each Socket
- Five PCI Memory Windows and Two I/O Windows Available for Each PC Card16 Socket
- Two I/O Windows and Two Memory Windows Available to Each CardBus Socket
- Exchangeable Card Architecture (ExCA) Compatible Registers Are Mappable in Memory and I/O Space
- Supports Distributed DMA (DDMA) and PC/PCI DMA
- Intel™ 82365SL-DF Register Compatible
- Supports 16-Bit DMA on Both PC Card Sockets
- Supports Ring Indicate, SUSPEND, PCI CLKRUN, and CardBus CCLKRUN
- Advanced Submicron, Low-Power CMOS Technology
- Provides VGA/Palette Memory and I/O and Subtractive Decoding Options
- LED Activity Pins
- Supports PCI Bus Lock (LOCK)
- For the Complete Data Sheet for PCI1250A, Please See Literature #SCPS014B

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# PCI1250A PC CARD CONTROLLER

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## description

The TI PCI1250A is a high-performance PC Card controller with a 32-bit PCI interface. The device supports two independent PC Card sockets compliant with the 1995 PC Card Standard. The PCI1250A provides a rich feature set that makes it the best choice for bridging between PCI and PC Cards in both notebook and desktop computers. The 1995 PC Card Standard retains the 16-bit PC Card specification defined in PCMCIA Release 2.1, and defines the new 32-bit PC Card, CardBus, capable of full 32-bit data transfers at 33 MHz. The PCI1250A supports any combination of 16-bit and CardBus PC Cards in the two sockets, powered at 5 V or 3.3 V, as required.

The PCI1250A is compliant with the latest PCI Bus Power Management Specification. It is also compliant with the PCI Local Bus Specification 2.1, and its PCI interface can act as either a PCI master device or a PCI slave device. The PCI bus mastering is initiated during 16-bit PC Card direct memory access (DMA) transfers or CardBus PC Card bridging transactions.

Multiple system-interrupt signaling options are provided and they include:

- Parallel PCI interrupts
- Parallel ISA interrupts
- Serialized ISA interrupts
- Serialized ISA and PCI interrupts

Additionally, general-purpose inputs and outputs are provided for the board designer to implement sideband functions.

All card signals are internally buffered to allow hot insertion and removal without external buffering. The PCI1250A is register compatible with the Intel 82365SL-DF ExCA controller. The PCI1250A internal data path logic allows the host to access 8-, 16-, and 32-bit cards using full 32-bit PCI cycles for maximum performance. Independent buffering and a pipeline architecture provide an unsurpassed performance level with sustained bursting. The PCI1250A can also be programmed to accept fast posted writes to improve system-bus utilization.

The PCI1250A provides an internally buffered zoom video (ZV) path. This reduces the design effort of PC board manufacturers to add a ZV-compatible solution and guarantees compliance with the CardBus loading specifications. Many other features are designed into the PCI1250A, such as socket activity light-emitting diode (LED) outputs, and are discussed in detail throughout the design specification.

An advanced complementary metal-oxide semiconductor (CMOS) process is used to achieve low system-power consumption while operating at PCI clock rates up to 33 MHz. Several low-power modes enable the host power management system to further reduce power consumption.

Unused PCI1250A inputs must be pulled up using a 43 k $\Omega$  resistor.



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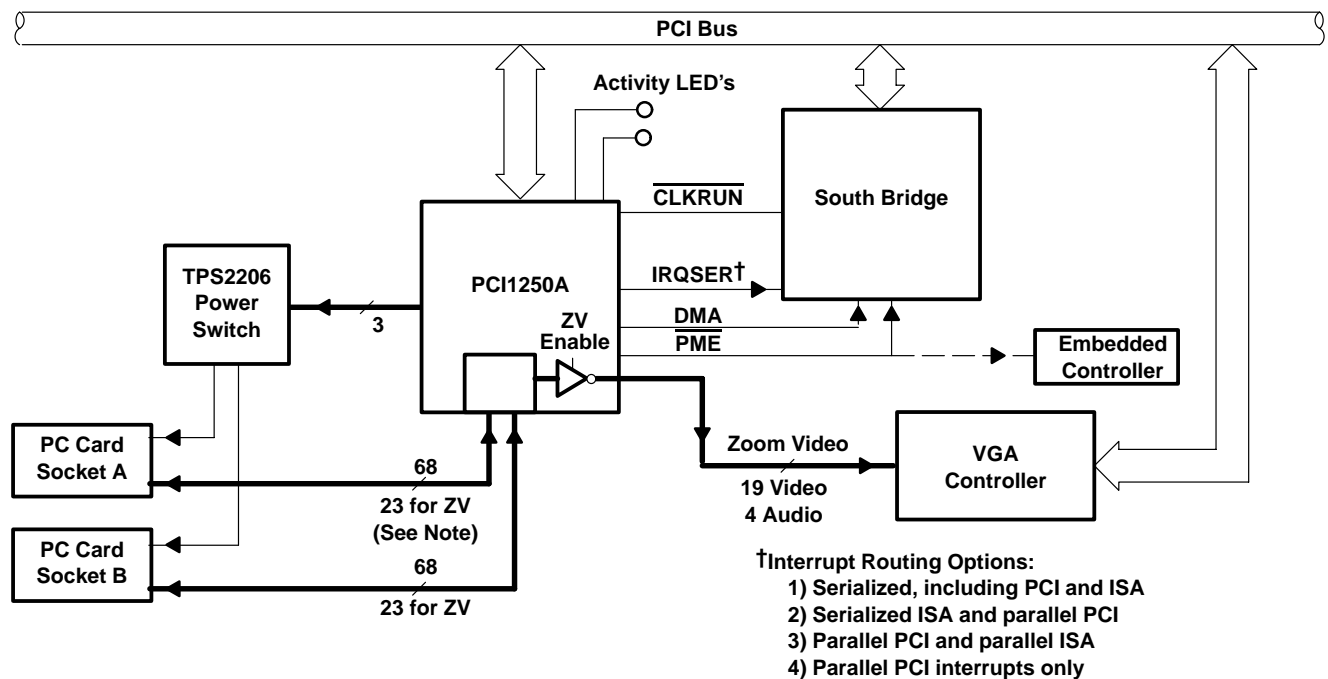
## system block diagram

A simplified system block diagram using the PCI1250A is provided below. The zoomed video (ZV) capability can be used to route the ZV data directly to the VGA controller.

The PCI interface includes all address/data and control signals for PCI protocol. The 68-pin PC Card interface includes all address/data and control signals for CardBus and 16-bit (R2) protocols. When zoomed video (ZV) is enabled (in 16-bit PC Card mode) 23 of the 68 signals are redefined to support the ZV protocol.

The interrupt interface includes terminals for parallel PCI, parallel ISA, and serialized PCI and ISA signaling. The ring indicate terminal is included in the interrupt interface because its function is to perform system wake up on incoming PC Card modem rings. Other miscellaneous system interface terminals are available on the PCI1250A that include:

- Programmable general purpose multifunction terminals
- SUSPEND, RI\_OUT/PME (power management control signal)
- SPKROUT.



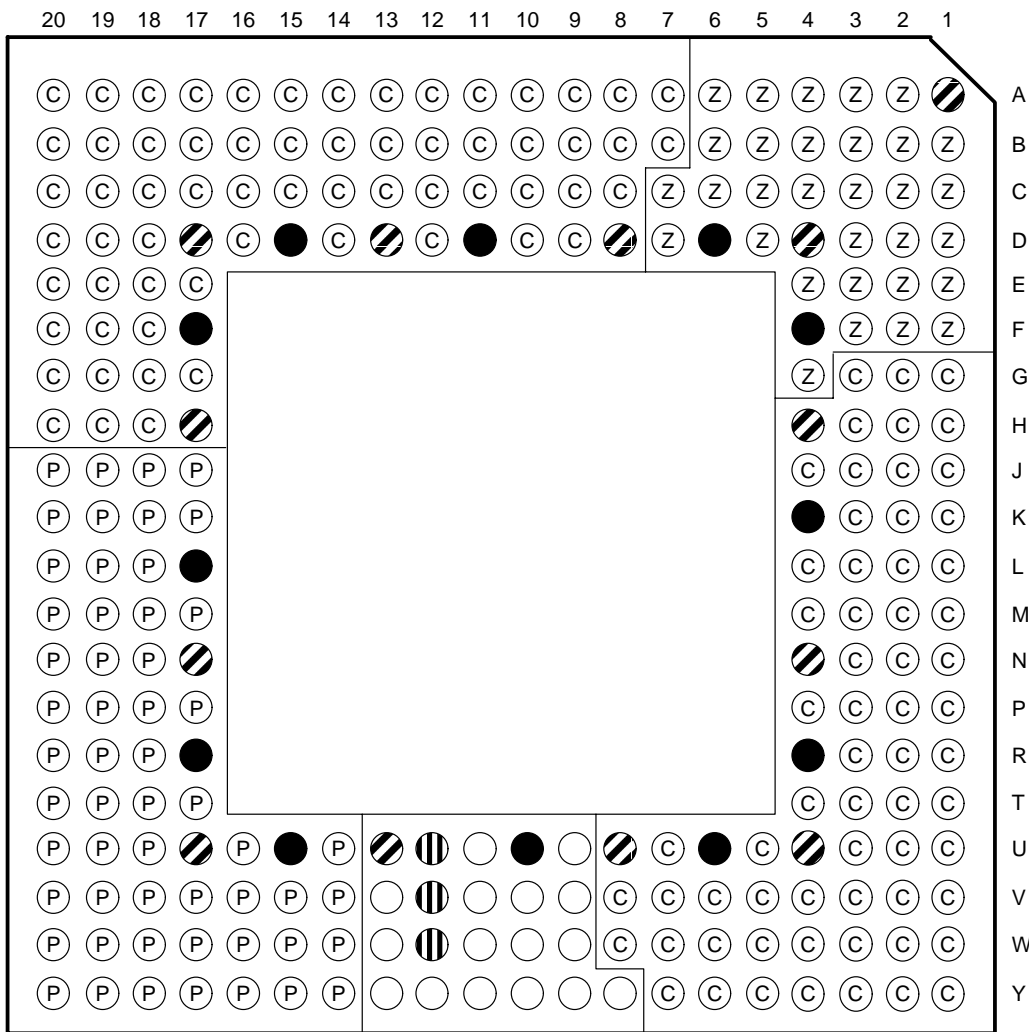
NOTE: The PC Card interface is 68 pins for CardBus and 16-bit PC Cards. In zoomed-video mode 23 pins are used for routing the zoomed video signals too the VGA controller.

## PC CARD CONTROLLER

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## terminal groups and locations

**GFN PACKAGE  
(BOTTOM VIEW)**



●  $V_{CC}$

 **Power Switch**

### © CardBus Signals

 **GND**

## ○ Interrupt and Miscellaneous

Ⓟ **PCI Signals**

## ② Zoom Video Signals

## Terminal Functions

The terminals are grouped in tables by functionality, such as PCI system function, power-supply function, etc. The terminal numbers are also listed for convenient reference.

### power supply

| TERMINAL<br>NAME NO. |  | FUNCTION  |
|----------------------|--|---|
| GND                  | A1, D4, D8, D13, D17, H4, H17, N4, N17, U4, U8, U13, U17 | Device ground terminals   |
| V <sub>CC</sub>      | D6, D11, D15, F4, F17, K4, L17, R4, R17, U6, U10, U15    | Power supply terminal for core logic (3.3 V)  |
| V <sub>CCA</sub>     | K2, R3, W5   | Rail power input for PC Card A interface. Indicates Card A signaling environment.   |
| V <sub>CCB</sub>     | B16, C10, F18,   | Rail power input for PC Card B interface. Indicates Card B signaling environment.   |
| V <sub>CCI</sub>     | V10  | Rail power input for interrupt subsystem interface and miscellaneous I/O. Indicates signaling level of the following inputs and shared outputs: IRQSER, PCGNT, PCREQ, SUSPEND, SPKROUT, GPIO1:0, IRQMUX7–IRQMUX0, INTA, INTB, CLOCK, DATA, LATCH, and RI_OUT. |
| V <sub>CCP</sub>     | K20, P18, V15, W20                                       | Rail power input for PCI signaling (3.3 V or 5 V)   |
| V <sub>CCZ</sub>     | A4, D1   | Rail power input for zoom video interface (3.3 V or 5 V)  |

### PCI system

| TERMINAL<br>NAME NO. | I/O<br>TYPE | FUNCTION |
|----------------------|-------------|----------|
| CLKRUN               | J18         | I/O      |
| PCLK                 | J17         | I        |
| PRST                 | J19         | I        |

### PC Card power switch

| TERMINAL<br>NAME NO. | I/O<br>TYPE | FUNCTION |
|----------------------|-------------|----------|
| CLOCK                | U12         | I/O      |
| DATA                 | V12         | O        |
| LATCH                | W12         | O        |

# PCI1250A PC CARD CONTROLLER

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## Terminal Functions (Continued)

### PCI address and data

| TERMINAL<br>NAME | NO. | I/O<br>TYPE | FUNCTION   |
|------------------|-----|-------------|--|
| AD31             | K18 | I/O         | PCI address/data bus. These signals make up the multiplexed PCI address and data bus on the primary interface. During the address phase of a primary bus PCI cycle, AD31–AD0 contain a 32-bit address or other destination information. During the data phase, AD31–AD0 contain data.  |
| AD30             | K19 |             |  |
| AD29             | L20 |             |  |
| AD28             | L18 |             |  |
| AD27             | L19 |             |  |
| AD26             | M20 |             |  |
| AD25             | M19 |             |  |
| AD24             | M18 |             |  |
| AD23             | N19 |             |  |
| AD22             | N18 |             |  |
| AD21             | P20 |             |  |
| AD20             | P19 |             |  |
| AD19             | R20 |             |  |
| AD18             | R19 |             |  |
| AD17             | P17 |             |  |
| AD16             | R18 |             |  |
| AD15             | V18 |             |  |
| AD14             | Y19 |             |  |
| AD13             | W18 |             |  |
| AD12             | V17 |             |  |
| AD11             | U16 |             |  |
| AD10             | Y18 |             |  |
| AD9              | W17 |             |  |
| AD8              | V16 |             |  |
| AD7              | W16 |             |  |
| AD6              | U14 |             |  |
| AD5              | Y16 |             |  |
| AD4              | W15 |             |  |
| AD3              | V14 |             |  |
| AD2              | Y15 |             |  |
| AD1              | W14 |             |  |
| AD0              | Y14 |             |  |
| C/ <u>BE3</u>    | M17 | I/O         | PCI bus commands and byte enables. These signals are multiplexed on the same PCI terminals. During the address phase of a primary bus PCI cycle, C/ <u>BE3</u> –C/ <u>BE0</u> define the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. C/ <u>BE0</u> applies to byte 0 (AD7–AD0), C/ <u>BE1</u> applies to byte 1 (AD15–AD8), C/ <u>BE2</u> applies to byte 2 (AD23–AD16), and C/ <u>BE3</u> applies to byte 3 (AD31–AD24). |
| C/ <u>BE2</u>    | T20 |             |  |
| C/ <u>BE1</u>    | W19 |             |  |
| C/ <u>BE0</u>    | Y17 |             |  |
| PAR              | Y20 | I/O         | PCI bus parity. In all PCI bus read and write cycles, the PCI1250A calculates even parity across the AD31–AD0 and C/ <u>BE3</u> –C/ <u>BE0</u> buses. As an initiator during PCI cycles, the PCI1250A outputs this parity indicator with a one-PCLK delay. As a target during PCI cycles, the calculated parity is compared to the initiator's parity indicator. A compare error results in the assertion of a parity error (PERR).  |

## Terminal Functions (Continued)

### PCI interface control

| TERMINAL<br>NAME                      | NO. | I/O<br>TYPE | FUNCTION   |
|---------------------------------------|-----|-------------|--|
| $\overline{\text{DEVSEL}}$            | V20 | I/O         | PCI device select. The PCI1250A asserts $\overline{\text{DEVSEL}}$ to claim a PCI cycle as the target device. As a PCI initiator on the bus, the PCI1250A monitors $\overline{\text{DEVSEL}}$ until a target responds. If no target responds before timeout occurs, the PCI1250A terminates the cycle with an initiator abort.   |
| $\overline{\text{FRAME}}$             | T19 | I/O         | PCI cycle frame. $\overline{\text{FRAME}}$ is driven by the initiator of a bus cycle. $\overline{\text{FRAME}}$ is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When $\overline{\text{FRAME}}$ is deasserted, the PCI bus transaction is in the final data phase.  |
| $\overline{\text{GNT}}$               | J20 | I           | PCI bus grant. $\overline{\text{GNT}}$ is driven by the PCI bus arbiter to grant the PCI1250A access to the PCI bus after the current data transaction has completed. $\overline{\text{GNT}}$ may or may not follow a PCI bus request, depending on the PCI bus parking algorithm.   |
| $\text{GPIO2}/\overline{\text{LOCK}}$ | V19 | I/O         | PCI bus general-purpose I/O pins or PCI bus lock. $\text{GPIO2}/\overline{\text{LOCK}}$ can be configured as PCI $\overline{\text{LOCK}}$ and used to gain exclusive access downstream. Since this functionality is not typically used, a general-purpose I/O may be accessed through this terminal. $\text{GPIO2}/\overline{\text{LOCK}}$ defaults to a general-purpose input and can be configured through the GPIO2 control register. |
| IDSEL                                 | N20 | I           | Initialization device select. IDSEL selects the PCI1250A during configuration space accesses. IDSEL can be connected to one of the upper 24 PCI address lines on the PCI bus.  |
| $\overline{\text{IRDY}}$              | T18 | I/O         | PCI initiator ready. $\overline{\text{IRDY}}$ indicates the PCI bus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK where both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted. Until $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are both sampled asserted, wait states are inserted.  |
| $\overline{\text{PERR}}$              | U18 | I/O         | PCI parity error indicator. $\overline{\text{PERR}}$ is driven by a PCI device to indicate that calculated parity does not match PAR when PERR is enabled through bit 6 of the command register.   |
| REQ                                   | K17 | O           | PCI bus request. REQ is asserted by the PCI1250A to request access to the PCI bus as an initiator.   |
| $\overline{\text{SERR}}$              | U19 | O           | PCI system error. $\overline{\text{SERR}}$ is an output that is pulsed from the PCI1250A when enabled through the command register, indicating a system error has occurred. The PCI1250A need not be the target of the PCI cycle to assert this signal. When $\overline{\text{SERR}}$ is enabled in the bridge control register, this signal also pulses, indicating that an address parity error has occurred on a CardBus interface.   |
| $\overline{\text{STOP}}$              | T17 | I/O         | PCI cycle stop signal. $\overline{\text{STOP}}$ is driven by a PCI target to request the initiator to stop the current PCI bus transaction. $\overline{\text{STOP}}$ is used for target disconnects and is commonly asserted by target devices that do not support burst data transfers.   |
| $\overline{\text{TRDY}}$              | U20 | I/O         | PCI target ready. $\overline{\text{TRDY}}$ indicates the primary bus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of PCLK when both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted. Until both $\overline{\text{IRDY}}$ and $\overline{\text{TRDY}}$ are asserted, wait states are inserted.   |

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## Terminal Functions (Continued)

### system interrupt

| TERMINAL<br>NAME NO.  | I/O<br>TYPE | FUNCTION  |
|---|-------------|---|
| GPIO3/ <u>INTA</u> V13  | I/O         | Parallel PCI interrupt. GPIO3/ <u>INTA</u> can be connected to an available PCI interrupt if parallel PCI interrupts are used, and the PCI1250A outputs PCI INTA through this terminal. GPIO3/ <u>INTA</u> defaults to a general-purpose input.   |
| IRQSER/ <u>INTB</u> W13   | I/O         | Serial interrupt signal/parallel PCI interrupt. When IRQSER/ <u>INTB</u> is configured as IRQSER, it provides the IRQSER-style serial interrupting scheme. Serialized PCI interrupts can also be sent in the IRQSER stream. IRQSER/ <u>INTB</u> can be configured as the parallel PCI <u>INTB</u> interrupt. IRQSER/ <u>INTB</u> defaults to IRQSER because this is the default interrupt signaling method.   |
| IRQMUX7 Y12<br>IRQMUX6 U11<br>IRQMUX5 W10<br>IRQMUX4 Y9<br>IRQMUX3 W9<br>IRQMUX2 V9<br>IRQMUX1 U9<br>IRQMUX0 Y8 | O           | Interrupt request/secondary functions multiplexed. The primary function of these terminals is to provide the ISA-type IRQ signaling supported by the PCI1250A. These interrupt multiplexer outputs can be mapped to any of 15 IRQs. The device control register must be programmed for the ISA IRQ interrupt mode and the IRQMUX routing register must have the IRQ routing programmed before these terminals are enabled.<br><br>All of these terminals have secondary functions, such as PC/PCI DMA request/grant, ring indicate output, and zoom video status, that can be selected with the appropriate programming of this register. When the secondary functions are enabled, the respective terminals are not available for IRQ routing.<br><br>See the IRQMUX routing register for programming options. |
| <u>RI_OUT</u> /PME Y13  | O           | Ring indicate output/power management event. <u>RI_OUT</u> allows the <u>RI</u> input from a PC Card to pass through to the system. This pin can be configured as the <u>PME</u> pin by setting bit 0 in the system control register. This pin is <u>RI_OUT</u> when RIENB is enabled in the card control register and ExCA interrupt and general control register. This pin is PME when RIENB is disabled and bit 1 of the system control register is 1.<br><br>IRQMUX4 or IRQMUX3 can be used to route the <u>RI_OUT</u> signal when the <u>PME</u> signal is routed on pin Y13 and a ring indicate signal is still required.   |

### PC/PCI DMA

| TERMINAL<br>NAME NO.          | I/O<br>TYPE | FUNCTION  |
|-------------------------------|-------------|---|
| <u>PCGNT</u> /<br>IRQMUX6 U11 | I/O         | PC/PCI DMA grant. <u>PCGNT</u> is used to grant the DMA channel to a requester in a system supporting the PC/PCI DMA scheme.<br><br>Interrupt request MUX 6. When configured for IRQMUX6, this terminal provides the IRQMUX6 interrupt output of the interrupt multiplexer, and can be mapped to any of 15 ISA-type IRQs. IRQMUX6 takes precedence over <u>PCGNT</u> , and should not be enabled in a system using PC/PCI DMA.<br><br>This terminal is also used for the serial EEPROM interface.   |
| <u>PCREQ</u> /<br>IRQMUX7 Y12 | O           | PC/PCI DMA request. <u>PCREQ</u> is used to request DMA transfers as <u>DREQ</u> in a system supporting the PC/PCI DMA scheme.<br><br>Interrupt request MUX 7. When configured for IRQMUX7, this terminal provides the IRQMUX7 interrupt output of the interrupt multiplexer, and can be mapped to any of 15 ISA-type IRQs. IRQMUX7 takes precedence over <u>PCREQ</u> , and should not be enabled in a system using PC/PCI DMA.<br><br>This terminal is also used for the serial EEPROM interface. |



## Terminal Functions (Continued)

### zoom video

| TERMINAL<br>NAME   | NO.  | I/O AND MEMORY<br>INTERFACE<br>SIGNAL                | I/O<br>TYPE | FUNCTION   |
|--|--|--|-------------|--|
| ZV_HREF  | A6   | A10  | O           | Horizontal sync to the zoom video port   |
| ZV_VSYNC   | C7   | A11  | O           | Vertical sync to the zoom video port   |
| ZV_Y7<br>ZV_Y6<br>ZV_Y5<br>ZV_Y4<br>ZV_Y3<br>ZV_Y2<br>ZV_Y1<br>ZV_Y0         | A3<br>B4<br>C5<br>B5<br>C6<br>D7<br>A5<br>B6 | A20<br>A14<br>A19<br>A13<br>A18<br>A8<br>A17<br>A9   | O           | Video data to the zoom video port in YV:4:2:2 format   |
| ZV_UV7<br>ZV_UV6<br>ZV_UV5<br>ZV_UV4<br>ZV_UV3<br>ZV_UV2<br>ZV_UV1<br>ZV_UV0 | D2<br>C3<br>B1<br>B2<br>A2<br>C4<br>B3<br>D5 | A25<br>A12<br>A24<br>A15<br>A23<br>A16<br>A22<br>A21 | O           | Video data to the zoom video port in YV:4:2:2 format   |
| ZV_SCLK  | C2   | A7   | O           | Audio SCLK PCM   |
| ZV_MCLK  | D3   | A6   | O           | Audio MCLK PCM   |
| ZV_PCLK  | E1   | $\overline{\text{IOIS16}}$                           | O           | Pixel clock to the zoom video port   |
| ZV_LRCLK   | E3   | $\overline{\text{INPACK}}$                           | O           | Audio LRCLK PCM  |
| ZV_SDATA   | E2   | $\overline{\text{SPKR}}$                             | O           | Audio SDATA PCM  |
| ZV_RSVD  | F1, F2, F3, G4                               |  | O           | Reserved. No connection.   |
| ZV_RSV1<br>ZV_RSV0   | C1<br>E4                                     | A5<br>A4   | O           | Reserved. No connection in the PC Card. ZV_RSVD1 and ZV_RSVD0 are put into the high-impedance state by host adapter. |

### miscellaneous

| TERMINAL<br>NAME            | NO. | I/O<br>TYPE | FUNCTION  |
|-----------------------------|-----|-------------|---|
| GPIO0/LEDA1                 | V11 | I/O         | GPIO0/socket activity LED indicator 1. When GPIO0/LEDA1 is configured as LEDA1, it provides an output indicating PC Card socket 0 activity. Otherwise, GPIO0/LEDA1 can be configured as a general-purpose input and output, GPIO0. The zoom video enable signal (ZV_STAT) can also be routed to this signal through the GPIO0 control register. GPIO0/LEDA1 defaults to a general-purpose input.  |
| GPIO1/LEDA2                 | W11 | I/O         | GPIO1/socket activity LED indicator 2. When GPIO1/LEDA2 is configured as LEDA2, it provides an output indicating PC Card socket 1 activity. Otherwise, GPIO1/LEDA2 can be configured as a general-purpose input and output, GPIO1. A CSC interrupt can be generated on a GPDATA change, and this input can be used for power switch overcurrent (OC) sensing. See <i>GPIO1 control register</i> for programming details. GPIO1/LEDA2 defaults to a general-purpose input. |
| SPKROUT                     | Y10 | O           | Speaker output. SPKROUT is the output to the host system that can carry $\overline{\text{SPKR}}$ or CAUDIO through the PCI1250A from the PC Card interface. SPKROUT is driven as the exclusive-OR combination of card $\overline{\text{SPKR}}$ /CAUDIO inputs.  |
| $\overline{\text{SUSPEND}}$ | Y11 | I           | Suspend. $\overline{\text{SUSPEND}}$ is used to protect the internal registers from clearing when $\overline{\text{PRST}}$ is asserted. See <i>SUSPEND mode</i> for details.  |

# PCI1250A PC CARD CONTROLLER

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## Terminal Functions (Continued)

### 16-bit PC Card address and data (slots A and B)

| TERMINAL NO. |         |         | I/O TYPE | FUNCTION  |
|--------------|---------|---------|----------|---|
| NAME         | SLOT A† | SLOT B‡ |          |   |
| A25          | T4      | C14     | O        | PC Card address. 16-bit PC Card address lines. A25 is the most-significant bit. |
| A24          | U2      | B15     |          |   |
| A23          | U1      | C15     |          |   |
| A22          | P4      | C16     |          |   |
| A21          | R2      | A18     |          |   |
| A20          | R1      | C17     |          |   |
| A19          | P1      | B18     |          |   |
| A18          | N2      | A20     |          |   |
| A17          | M4      | C18     |          |   |
| A16          | T1      | A17     |          |   |
| A15          | T2      | A16     |          |   |
| A14          | P2      | B17     |          |   |
| A13          | N3      | A19     |          |   |
| A12          | T3      | D14     |          |   |
| A11          | M1      | D18     |          |   |
| A10          | L1      | E18     |          |   |
| A9           | M3      | B20     |          |   |
| A8           | N1      | B19     |          |   |
| A7           | V1      | A15     |          |   |
| A6           | V2      | A14     |          |   |
| A5           | V3      | B13     |          |   |
| A4           | W2      | A13     |          |   |
| A3           | W3      | C12     |          |   |
| A2           | W4      | A12     |          |   |
| A1           | V4      | B11     |          |   |
| A0           | U5      | C11     |          |   |
| D15          | K3      | E19     | I/O      | PC Card data. 16-bit PC Card data lines. D15 is the most-significant bit.       |
| D14          | J2      | E20     |          |   |
| D13          | J4      | G18     |          |   |
| D12          | H2      | G19     |          |   |
| D11          | G1      | H18     |          |   |
| D10          | W8      | B7      |          |   |
| D9           | Y7      | C8      |          |   |
| D8           | V7      | A8      |          |   |
| D7           | J1      | G17     |          |   |
| D6           | J3      | F19     |          |   |
| D5           | H1      | F20     |          |   |
| D4           | H3      | G20     |          |   |
| D3           | G2      | H19     |          |   |
| D2           | V8      | A7      |          |   |
| D1           | W7      | B8      |          |   |
| D0           | Y6      | D9      |          |   |

† Terminal name for slot A is preceded with A\_. For example, the full name for terminal T4 is A\_T4.

‡ Terminal name for slot B is preceded with B\_. For example, the full name for terminal C14 is B\_C14.



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## Terminal Functions (Continued)

### 16-bit PC Card interface control (slots A and B)

| TERMINAL<br>NO.   |            |            | I/O<br>TYPE | FUNCTION   |
|---|------------|------------|-------------|--|
| NAME  | SLOT<br>A† | SLOT<br>B‡ |             |  |
| $\overline{\text{BVD1}}$<br>( $\overline{\text{STSCHG/RI}}$ ) | V6         | A9         | I           | <p>Battery voltage detect 1. BVD1 is generated by 16-bit memory PC Cards that include batteries. BVD1 is used with BVD2 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are kept high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost.</p> <p>Status change. <math>\overline{\text{STSCHG}}</math> is used to alert the system to a change in the READY, write protect, or battery voltage dead condition of a 16-bit I/O PC Card.</p> <p>Ring indicate. <math>\overline{\text{RI}}</math> is used by 16-bit modem cards to indicate a ring detection.</p>   |
| $\overline{\text{BVD2}}$<br>( $\overline{\text{SPKR}}$ )      | Y5         | D10        | I           | <p>Battery voltage detect 2. BVD2 is generated by 16-bit memory PC Cards that include batteries. BVD2 is used with BVD1 as an indication of the condition of the batteries on a memory PC Card. Both BVD1 and BVD2 are high when the battery is good. When BVD2 is low and BVD1 is high, the battery is weak and should be replaced. When BVD1 is low, the battery is no longer serviceable and the data in the memory PC Card is lost.</p> <p>Speaker. <math>\overline{\text{SPKR}}</math> is an optional binary audio signal available only when the card and socket have been configured for the 16-bit I/O interface. The audio signals from cards A and B are combined by the PCI1250A and are output on SPKROUT.</p> <p>DMA request. BVD2 can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. The PC Card asserts BVD2 to indicate a request for a DMA operation.</p> |
| $\overline{\text{CD1}}$<br>$\overline{\text{CD2}}$            | G3<br>W6   | H20<br>C9  | I           | <p>PC Card detect 1 and PC Card detect 2. <math>\overline{\text{CD1}}</math> and <math>\overline{\text{CD2}}</math> are internally connected to ground on the PC Card. When a PC Card is inserted into a socket, CD1 and CD2 are pulled low.</p>   |
| $\overline{\text{CE1}}$<br>$\overline{\text{CE2}}$            | K1<br>L2   | D20<br>D19 | O           | <p>Card enable 1 and card enable 2. <math>\overline{\text{CE1}}</math> and <math>\overline{\text{CE2}}</math> enable even- and odd-numbered address bytes. CE1 enables even-numbered address bytes, and CE2 enables odd-numbered address bytes.</p>  |
| $\overline{\text{INPACK}}$                                    | Y1         | D12        | I           | <p>Input acknowledge. <math>\overline{\text{INPACK}}</math> is asserted by the PC Card when it can respond to an I/O read cycle at the current address.</p> <p>DMA request. <math>\overline{\text{INPACK}}</math> can be used as the DMA request signal during DMA operations from a 16-bit PC Card that supports DMA. If used as a strobe, the PC Card asserts this signal to indicate a request for a DMA operation.</p>   |
| $\overline{\text{IORD}}$                                      | L4         | E17        | O           | <p>I/O read. <math>\overline{\text{IORD}}</math> is asserted by the PCI1250A to enable 16-bit I/O PC Card data output during host I/O read cycles.</p> <p>DMA write. <math>\overline{\text{IORD}}</math> is used as the DMA write <u>strobe</u> during DMA operations from a 16-bit PC Card that supports DMA. The PCI1250A asserts IORD during DMA transfers from the PC Card to host memory.</p>   |
| $\overline{\text{IOWR}}$                                      | M2         | C19        | O           | <p>I/O write. <math>\overline{\text{IOWR}}</math> is driven low by the PCI1250A to strobe write data into 16-bit I/O PC Cards during host I/O write cycles.</p> <p>DMA read. <math>\overline{\text{IOWR}}</math> is used as the DMA write <u>strobe</u> during DMA operations from a 16-bit PC Card that supports DMA. The PCI1250A asserts IOWR during transfers from host memory to the PC Card.</p>   |
| $\overline{\text{OE}}$  | L3         | C20        | O           | <p>Output enable. <math>\overline{\text{OE}}</math> is driven low by the PCI1250A to enable 16-bit memory PC Card data output during host memory read cycles.</p> <p>DMA terminal count. <math>\overline{\text{OE}}</math> is used as terminal <u>count</u> (TC) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1250A asserts <math>\overline{\text{OE}}</math> to indicate TC for a DMA write operation.</p>   |

† Terminal name for slot A is preceded with A\_. For example, the full name for terminal Y1 is A\_ $\overline{\text{INPACK}}$ .

‡ Terminal name for slot B is preceded with B\_. For example, the full name for terminal D12 is B\_ $\overline{\text{INPACK}}$ .

# PCI1250A PC CARD CONTROLLER

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## Terminal Functions (Continued)

### 16-bit PC Card interface control (slots A and B) (continued)

| TERMINAL<br>NUMBER |            |            | I/O<br>TYPE | FUNCTION   |
|--------------------|------------|------------|-------------|--|
| NAME               | SLOT<br>A† | SLOT<br>B‡ |             |  |
| READY<br>(IREQ)    | Y4         | A10        | I           | Ready. The ready function is provided by READY when the 16-bit PC Card and the host socket are configured for the memory-only interface. READY is driven low by the 16-bit memory PC Cards to indicate that the memory card circuits are busy processing a previous write command. READY is driven high when the 16-bit memory PC Card is ready to accept a new data transfer command.<br><br>Interrupt request. IREQ is asserted by a 16-bit I/O PC Card to indicate to the host that a device on the 16-bit I/O PC Card requires service by the host software. IREQ is high (deasserted) when no interrupt is requested.   |
| REG                | Y2         | B12        | O           | Attribute memory select. REG remains high for all common memory accesses. When REG is asserted, access is limited to attribute memory (OE or WE active) and to the I/O space (IORD or IOWR active). Attribute memory is a separately accessed section of card memory and is generally used to record card capacity and other configuration and attribute information.<br><br>DMA acknowledge. REG is used as a DMA acknowledge (DACK) during DMA operations to a 16-bit PC Card that supports DMA. The PCI1250A asserts REG to indicate a DMA operation. REG is used in conjunction with the DMA read (IOWR) or DMA write (IORD) strobes to transfer data.                           |
| RESET              | W1         | C13        | O           | PC Card reset. RESET forces a hard reset to a 16-bit PC Card.  |
| WAIT               | V5         | B10        | I           | Bus cycle wait. WAIT is driven by a 16-bit PC Card to delay the completion of (i.e., extend) the memory or I/O cycle in progress.  |
| WE                 | P3         | D16        | O           | Write enable. WE is used to strobe memory write data into 16-bit memory PC Cards. WE is also used for memory PC Cards that employ programmable memory technologies.<br><br>DMA terminal count. WE is used as TC during DMA operations to a 16-bit PC Card that supports DMA. The PC1250 asserts WE to indicate TC for a DMA read operation.  |
| WP<br>(IOIS16)     | U7         | B9         | I           | Write protect. WP applies to 16-bit memory PC Cards. WP reflects the status of the write-protect switch on 16-bit memory PC Cards. For 16-bit I/O cards, WP is used for the 16-bit port (IOIS16) function.<br><br>I/O is 16 bits. IOIS16 applies to 16-bit I/O PC Cards. IOIS16 is asserted by the 16-bit PC Card when the address on the bus corresponds to an address to which the 16-bit PC Card responds, and the I/O port that is addressed is capable of 16-bit accesses.<br><br>DMA request. WP can be used as the DMA request signal during DMA operations to a 16-bit PC Card that supports DMA. If used, the PC Card asserts WP to indicate a request for a DMA operation. |
| VS1<br>VS2         | Y3<br>U3   | A11<br>B14 | I/O         | Voltage sense 1 and voltage sense 2. VS1 and VS2, when used in conjunction with each other, determine the operating voltage of the 16-bit PC Card.   |

† Terminal name for slot A is preceded with A\_. For example, the full name for terminal P3 is A\_WE.

‡ Terminal name for slot B is preceded with B\_. For example, the full name for terminal D16 is B\_WE.



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## Terminal Functions (Continued)

### CardBus PC Card interface system (slots A and B)

| TERMINAL NO.                |                     |                     | I/O TYPE | FUNCTION   |
|-----------------------------|---------------------|---------------------|----------|--|
| NAME                        | SLOT A <sup>†</sup> | SLOT B <sup>‡</sup> |          |  |
| CCLK                        | T1                  | A17                 | O        | CardBus PC Card clock. CCLK provides synchronous timing for all transactions on the CardBus interface. All signals except $\overline{\text{CRST}}$ , $\overline{\text{CCLKRUN}}$ , $\overline{\text{CINT}}$ , $\text{CSTSCHG}$ , $\text{CAUDIO}$ , $\overline{\text{CCD2:1}}$ , and $\text{CVS2-CVS1}$ are sampled on the rising edge of CCLK, and all timing parameters are defined with the rising edge of this signal. CCLK operates at the PCI bus clock frequency, but it can be stopped in the low state or slowed down for power savings. |
| $\overline{\text{CCLKRUN}}$ | U7                  | B9                  | O        | CardBus PC Card clock run. $\overline{\text{CCLKRUN}}$ is used by a CardBus PC Card to request an increase in the CCLK frequency, and by the PCI1250A to indicate that the CCLK frequency is decreased.  |
| $\overline{\text{CRST}}$    | W1                  | C13                 | I/O      | CardBus PC Card reset. $\overline{\text{CRST}}$ is used to bring CardBus PC Card-specific registers, sequencers, and signals to a known state. When $\overline{\text{CRST}}$ is asserted, all CardBus PC Card signals must be 3-stated, and the PCI1250A drives these signals to a valid logic level. Assertion can be asynchronous to CCLK, but deassertion must be synchronous to CCLK.  |

<sup>†</sup> Terminal name for slot A is preceded with A\_. For example, the full name for terminal T1 is A\_CCLK.

<sup>‡</sup> Terminal name for slot B is preceded with B\_. For example, the full name for terminal A17 is B\_CCLK.

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## Terminal Functions (Continued)

### CardBus PC Card address and data (slots A and B)

| TERMINAL NO. |         |         | I/O TYPE | FUNCTION  |
|--------------|---------|---------|----------|---|
| NAME         | SLOT A† | SLOT B‡ |          |   |
| CAD31        | W8      | B7      | I/O      | PC Card address and data. These signals make up the multiplexed CardBus address and data bus on the CardBus interface. During the address phase of a CardBus cycle, CAD31–CAD0 contain a 32-bit address. During the data phase of a CardBus cycle, CAD31–CAD0 contain data. CAD31 is the most-significant bit.  |
| CAD30        | Y7      | C8      |          |   |
| CAD29        | W7      | B8      |          |   |
| CAD28        | V7      | A8      |          |   |
| CAD27        | Y6      | D9      |          |   |
| CAD26        | U5      | C11     |          |   |
| CAD25        | V4      | B11     |          |   |
| CAD24        | W4      | A12     |          |   |
| CAD23        | W3      | C12     |          |   |
| CAD22        | W2      | A13     |          |   |
| CAD21        | V3      | B13     |          |   |
| CAD20        | V2      | A14     |          |   |
| CAD19        | T4      | C14     |          |   |
| CAD18        | V1      | A15     |          |   |
| CAD17        | U2      | B15     |          |   |
| CAD16        | M4      | C18     |          |   |
| CAD15        | M2      | C19     |          |   |
| CAD14        | M3      | B20     |          |   |
| CAD13        | L4      | E17     |          |   |
| CAD12        | M1      | D18     |          |   |
| CAD11        | L3      | C20     |          |   |
| CAD10        | L2      | D19     |          |   |
| CAD9         | L1      | E18     |          |   |
| CAD8         | K3      | E19     |          |   |
| CAD7         | J1      | G17     |          |   |
| CAD6         | J4      | G18     |          |   |
| CAD5         | J3      | F19     |          |   |
| CAD4         | H2      | G19     |          |   |
| CAD3         | H1      | F20     |          |   |
| CAD2         | G1      | H18     |          |   |
| CAD1         | H3      | G20     |          |   |
| CAD0         | G2      | H19     |          |   |
| CC/BE3       | Y2      | B12     | I/O      | CardBus bus commands and byte enables. CC/BE3–CC/BE0 are multiplexed on the same CardBus terminals. During the address phase of a CardBus cycle, CC/BE3–CC/BE0 defines the bus command. During the data phase, this 4-bit bus is used as byte enables. The byte enables determine which byte paths of the full 32-bit data bus carry meaningful data. CC/BE0 applies to byte 0 (CAD7–CAD0), CC/BE1 applies to byte 1 (CAD15–CAD8), CC/BE2 applies to byte 2 (CAD23–CAD8), and CC/BE3 applies to byte 3 (CAD31–CAD24). |
| CC/BE2       | T3      | D14     |          |   |
| CC/BE1       | N1      | B19     |          |   |
| CC/BE0       | K1      | D20     |          |   |
| CPAR         | N3      | A19     | I/O      | CardBus parity. In all CardBus read and write cycles, the PCI1250A calculates even parity across the CAD and CC/BE buses. As an initiator during CardBus cycles, the PCI1250A outputs CPAR with a one-CCLK delay. As a target during CardBus cycles, the calculated parity is compared to the initiator's parity indicator; a compare error results in a parity error assertion.  |

† Terminal name for slot A is preceded with A\_. For example, the full name for terminal N3 is A\_CPAP.

‡ Terminal name for slot B is preceded with B\_. For example, the full name for terminal A19 is B\_CPAP.



## Terminal Functions (Continued)

### CardBus PC Card interface control (slots A and B)

| TERMINAL<br>NO.                                      |            |            | I/O<br>TYPE | FUNCTION   |
|--|------------|------------|-------------|--|
| NAME   | SLOT<br>A† | SLOT<br>B‡ |             |  |
| CAUDIO   | Y5         | D10        | I           | CardBus audio. CAUDIO is a digital input signal from a PC Card to the system speaker. The PCI1250A supports the binary audio mode and outputs a binary signal from the card to SPKROUT.  |
| CBLOCK   | P1         | B18        | I/O         | CardBus lock. CBLOCK is used to gain exclusive access to a target.   |
| $\overline{\text{CCD1}}$<br>$\overline{\text{CCD2}}$ | G3<br>W6   | H20<br>C9  | I           | CardBus detect 1 and CardBus detect 2. $\overline{\text{CCD1}}$ and $\overline{\text{CCD2}}$ are used in conjunction with CVS1 and CVS2 to identify card insertion and interrogate cards to determine the operating voltage and card type.   |
| $\overline{\text{CDEVSEL}}$                          | R2         | A18        | I/O         | CardBus device select. The PCI1250A asserts $\overline{\text{CDEVSEL}}$ to claim a CardBus cycle as the target device. As a CardBus initiator on the bus, the PCI1250A monitors $\overline{\text{CDEVSEL}}$ until a target responds. If no target responds before timeout occurs, the PCI1250A terminates the cycle with an initiator abort.   |
| $\overline{\text{CFRAME}}$                           | U1         | C15        | I/O         | CardBus cycle frame. $\overline{\text{CFRAME}}$ is driven by the initiator of a CardBus bus cycle. $\overline{\text{CFRAME}}$ is asserted to indicate that a bus transaction is beginning, and data transfers continue while this signal is asserted. When $\overline{\text{CFRAME}}$ is deasserted, the CardBus bus transaction is in the final data phase.   |
| $\overline{\text{CGNT}}$                             | P3         | D16        | I           | CardBus bus grant. $\overline{\text{CGNT}}$ is driven by the PCI1250A to grant a CardBus PC Card access to the CardBus bus after the current data transaction has been completed.  |
| $\overline{\text{CINT}}$                             | Y4         | A10        | I           | CardBus interrupt. $\overline{\text{CINT}}$ is asserted low by a CardBus PC Card to request interrupt servicing from the host.   |
| $\overline{\text{CIRDY}}$                            | T2         | A16        | I/O         | CardBus initiator ready. $\overline{\text{CIRDY}}$ indicates the CardBus initiator's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK when both $\overline{\text{CIRDY}}$ and $\overline{\text{CTRDY}}$ are asserted. Until $\overline{\text{CIRDY}}$ and $\overline{\text{CTRDY}}$ are both sampled asserted, wait states are inserted.              |
| $\overline{\text{CPERR}}$                            | P2         | B17        | I/O         | CardBus parity error. $\overline{\text{CPERR}}$ is used to report parity errors during CardBus transactions, except during special cycles. It is driven low by a target two clocks following that data when a parity error is detected.  |
| $\overline{\text{CREQ}}$                             | Y1         | D12        | I           | CardBus request. $\overline{\text{CREQ}}$ indicates to the arbiter that the CardBus PC Card desires use of the CardBus bus as an initiator.  |
| $\overline{\text{CSERR}}$                            | V5         | B10        | I           | CardBus system error. $\overline{\text{CSERR}}$ reports address parity errors and other system errors that could lead to catastrophic results. $\overline{\text{CSERR}}$ is driven by the card synchronous to CCLK, but deasserted by a weak pullup, and may take several CCLK periods. The PCI1250A can report $\overline{\text{CSERR}}$ to the system by assertion of $\overline{\text{SERR}}$ on the PCI interface. |
| $\overline{\text{CSTOP}}$                            | R1         | C17        | I/O         | CardBus stop. $\overline{\text{CSTOP}}$ is driven by a CardBus target to request the initiator to stop the current CardBus transaction. $\overline{\text{CSTOP}}$ is used for target disconnects, and is commonly asserted by target devices that do not support burst data transfers.   |
| CSTSCHG  | V6         | A9         | I           | CardBus status change. CSTSCHG is used to alert the system to a change in the card's status, and is used as a wake-up mechanism.   |
| $\overline{\text{CTRDY}}$                            | P4         | C16        | I/O         | CardBus target ready. $\overline{\text{CTRDY}}$ indicates the CardBus target's ability to complete the current data phase of the transaction. A data phase is completed on a rising edge of CCLK, when both $\overline{\text{CIRDY}}$ and $\overline{\text{CTRDY}}$ are asserted; until this time, wait states are inserted.   |
| CVS1<br>CVS2   | Y3<br>U3   | A11<br>B14 | I/O         | CardBus voltage sense 1 and CardBus voltage sense 2. CVS1 and CVS2 are used in conjunction with $\overline{\text{CCD1}}$ and $\overline{\text{CCD2}}$ to identify card insertion and interrogate cards to determine the operating voltage and card type.   |

† Terminal name for slot A is preceded with A\_. For example, the full name for terminal Y5 is A\_CAUDIO.

‡ Terminal name for slot B is preceded with B\_. For example, the full name for terminal D10 is B\_CAUDIO.

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## PC CARD CONTROLLER

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### absolute maximum ratings over operating temperature ranges (unless otherwise noted)<sup>†</sup>

|   |                             |
|---|-----------------------------|
| Supply voltage range, $V_{CC}$  | –0.5 V to 4.6 V             |
| Supply voltage range, $V_{CCP}$ , $V_{CCA}$ , $V_{CCB}$ , $V_{CCZ}$ , $V_{CCI}$ | –0.5 V to 6 V               |
| Input voltage range, $V_I$ : PCI  | –0.5 V to $V_{CCP} + 0.5$ V |
| Card A  | –0.5 to $V_{CCA} + 0.5$ V   |
| Card B  | –0.5 to $V_{CCB} + 0.5$ V   |
| ZV  | –0.5 to $V_{CCZ} + 0.5$ V   |
| MISC  | –0.5 to $V_{CCI} + 0.5$ V   |
| Fail safe   | –0.5 V to $V_{CC} + 0.5$ V  |
| Output voltage range, $V_O$ : PCI   | –0.5 V to $V_{CCP} + 0.5$ V |
| Card A  | –0.5 to $V_{CCA} + 0.5$ V   |
| Card B  | –0.5 to $V_{CCB} + 0.5$ V   |
| ZV  | –0.5 to $V_{CCZ} + 0.5$ V   |
| MISC  | –0.5 to $V_{CCI} + 0.5$ V   |
| Fail safe   | –0.5 V to $V_{CC} + 0.5$ V  |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)      | $\pm 20$ mA                 |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 2)     | $\pm 20$ mA                 |
| Storage temperature range, $T_{stg}$  | –65°C to 150°C              |
| Virtual junction temperature, $T_J$   | 150°C                       |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Applies for external input and bidirectional buffers.  $V_I > V_{CC}$  does not apply to fail-safe terminals. PCI terminals are measured with respect to  $V_{CCP}$  instead of  $V_{CC}$ . PC Card terminals are measured with respect to  $V_{CCA}$  or  $V_{CCB}$ . ZV terminals are measured with respect to  $V_{CCZ}$ , and miscellaneous signals are measured with respect to  $V_{CCI}$ . The limit specified applies for a dc condition.
2. Applies for external output and bidirectional buffers.  $V_O > V_{CC}$  does not apply to fail-safe terminals. PCI terminals are measured with respect to  $V_{CCP}$  instead of  $V_{CC}$ . PC Card terminals are measured with respect to  $V_{CCA}$  or  $V_{CCB}$ . ZV terminals are measured with respect to  $V_{CCZ}$ , and miscellaneous signals are measured with respect to  $V_{CCI}$ . The limit specified applies for a dc condition.



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recommended operating conditions (see Note 3)

|                              |                           |                        | OPERATION | MIN                      | NOM | MAX                      | UNIT |
|------------------------------|---------------------------|------------------------|-----------|--------------------------|-----|--------------------------|------|
| V <sub>CC</sub>              | Core voltage              | Commercial             | 3.3 V     | 3                        | 3.3 | 3.6                      | V    |
| V <sub>CCP</sub>             | PCI I/O voltage           | Commercial             | 3.3 V     | 3                        | 3.3 | 3.6                      | V    |
|                              |                           |                        | 5 V       | 4.75                     | 5   | 5.25                     |      |
| V <sub>CC(A/B)</sub>         | PC Card I/O voltage       | Commercial             | 3.3 V     | 3                        | 3.3 | 3.6                      | V    |
|                              |                           |                        | 5 V       | 4.75                     | 5   | 5.25                     |      |
| V <sub>CCZ</sub>             | ZV port I/O voltage       | Commercial             | 3.3 V     | 3                        | 3.3 | 3.6                      | V    |
|                              |                           |                        | 5 V       | 4.75                     | 5   | 5.25                     |      |
| V <sub>CCI</sub>             | Miscellaneous I/O voltage | Commercial             | 3.3 V     | 3                        | 3.3 | 3.6                      | V    |
|                              |                           |                        | 5 V       | 4.75                     | 5   | 5.25                     |      |
| V <sub>IH</sub> <sup>†</sup> | High-level input voltage  | PCI                    | 3.3 V     | 0.5 V <sub>CCP</sub>     |     | V <sub>CCP</sub>         | V    |
|                              |                           |                        | 5 V       | 2                        |     | V <sub>CCP</sub>         |      |
|                              | PC Card                   |                        | 3.3 V     | 0.475 V <sub>CCA/B</sub> |     | V <sub>CCA/B</sub>       |      |
|                              |                           |                        | 5 V       | 2.4                      |     | V <sub>CCA/B</sub>       |      |
|                              | ZV                        |                        |           | 2                        |     | V <sub>CCZ</sub>         |      |
|                              | MISC <sup>‡</sup>         |                        |           | 2                        |     | V <sub>CCI</sub>         |      |
|                              | Fail safe <sup>§</sup>    |                        |           | 2                        |     | V <sub>CC</sub>          |      |
| V <sub>IL</sub> <sup>†</sup> | Low-level input voltage   | PCI                    | 3.3 V     | 0                        |     | 0.3 V <sub>CCP</sub>     | V    |
|                              |                           |                        | 5 V       | 0                        |     | 0.8                      |      |
|                              | PC Card                   |                        | 3.3 V     | 0                        |     | 0.325 V <sub>CCA/B</sub> |      |
|                              |                           |                        | 5 V       | 0                        |     | 0.8                      |      |
|                              | ZV                        |                        |           | 0                        |     | 0.8                      |      |
|                              | MISC <sup>‡</sup>         |                        |           | 0                        |     | 0.8                      |      |
|                              | Fail safe <sup>§</sup>    |                        |           | 0                        |     | 0.8                      |      |
| V <sub>I</sub>               | Input voltage             | PCI                    |           | 0                        |     | V <sub>CCP</sub>         | V    |
|                              |                           | PC Card                |           | 0                        |     | V <sub>CCA/B</sub>       |      |
|                              |                           | ZV                     |           | 0                        |     | V <sub>CCZ</sub>         |      |
|                              |                           | MISC <sup>‡</sup>      |           | 0                        |     | V <sub>CCI</sub>         |      |
|                              |                           | Fail safe <sup>§</sup> |           | 0                        |     | V <sub>CC</sub>          |      |
| V <sub>O</sub> <sup>¶</sup>  | Output voltage            | PCI                    |           | 0                        |     | V <sub>CCP</sub>         | V    |
|                              |                           | PC Card                |           | 0                        |     | V <sub>CCA/B</sub>       |      |
|                              |                           | ZV                     |           | 0                        |     | V <sub>CCZ</sub>         |      |
|                              |                           | MISC <sup>‡</sup>      |           | 0                        |     | V <sub>CCI</sub>         |      |
|                              |                           | Fail safe <sup>§</sup> |           | 0                        |     | V <sub>CC</sub>          |      |

<sup>†</sup> Applies to external inputs and bidirectional buffers without hysteresis

<sup>‡</sup> Miscellaneous pins are V13, W13, Y13, U12, V12, W12, U11, V11, W11, Y11, Y10, W10, Y09, W09, V09, U09, Y08, all IRQMUXx pins, LEDAx pins, SUSPEND, SPKROUT, RI\_OUT, INTA, INTB, and power switch control pins.

<sup>§</sup> Fail-safe pins are A11, B14, C09, G03, H20, U03, W06, and Y03 (card detect and voltage sense pins).

<sup>¶</sup> Applies to external output buffers

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

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## recommended operating conditions (see Note 3) (continued)

|               |  |                                  | OPERATION | MIN | NOM | MAX | UNIT |
|---------------|--|----------------------------------|-----------|-----|-----|-----|------|
| $t_t$         | Input transition time<br>( $t_r$ and $t_f$ ) | PCI and PC Card                  |           | 1   |     | 4   | ns   |
|               |  | ZV, miscellaneous, and fail safe |           | 0   |     | 6   |      |
| $T_A$         | Operating ambient temperature range          |                                  |           | 0   | 25  | 70  | °C   |
| $T_J^\dagger$ | Virtual junction temperature                 |                                  |           | 0   | 25  | 115 | °C   |

$^\dagger$  These junction temperatures reflect simulation conditions. The customer is responsible for verifying junction temperature.

NOTE 3: Unused pins (input or I/O) must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER   | PINS           | OPERATION | TEST CONDITIONS             | MIN            | MAX | UNIT          |
|---|----------------|-----------|-----------------------------|----------------|-----|---------------|
| $V_{OH}$ High-level output voltage (see Note 4)                     | PCI            | 3.3 V     | $I_{OH} = -0.5 \text{ mA}$  | $0.9 V_{CC}$   |     | V             |
|   |                | 5 V       | $I_{OH} = -2 \text{ mA}$    | 2.4            |     |               |
|   | PC Card        | 3.3 V     | $I_{OH} = -0.15 \text{ mA}$ | $0.9 V_{CC}$   |     |               |
|   |                | 5 V       | $I_{OH} = -0.15 \text{ mA}$ | 2.4            |     |               |
|   | ZV             |           | $I_{OH} = -4 \text{ mA}$    | $V_{CC} - 0.6$ |     |               |
|   | MISC           |           | $I_{OH} = -4 \text{ mA}$    | $V_{CC} - 0.6$ |     |               |
| $V_{OL}$ Low-level output voltage                                   | PCI            | 3.3 V     | $I_{OL} = 1.5 \text{ mA}$   | $0.1 V_{CC}$   |     | V             |
|   |                | 5 V       | $I_{OL} = 6 \text{ mA}$     | 0.55           |     |               |
|   | PC Card        | 3.3 V     | $I_{OL} = 0.7 \text{ mA}$   | $0.1 V_{CC}$   |     |               |
|   |                | 5 V       | $I_{OL} = 0.7 \text{ mA}$   | 0.55           |     |               |
|   | ZV             |           | $I_{OL} = 4 \text{ mA}$     | 0.5            |     |               |
|   | MISC           |           | $I_{OL} = 4 \text{ mA}$     | 0.5            |     |               |
|   | SERR           |           | $I_{OL} = 12 \text{ mA}$    | 0.5            |     |               |
| $I_{OZL}$ 3-state output, high-impedance state current (see Note 4) | Output pins    | 3.6 V     | $V_I = V_{CC}$              |                | -1  | $\mu\text{A}$ |
|   |                | 5.25 V    | $V_I = V_{CC}$              |                | -1  |               |
| $I_{OZH}$ 3-state output, high-impedance state current              | Output pins    | 3.6 V     | $V_I = V_{CC}^\ddagger$     |                | 10  | $\mu\text{A}$ |
|   |                | 5.25 V    | $V_I = V_{CC}^\ddagger$     |                | 25  |               |
| $I_{IL}$ Low-level input current                                    | Input pins     |           | $V_I = \text{GND}$          |                | -1  | $\mu\text{A}$ |
|   | I/O pins       |           | $V_I = \text{GND}$          |                | -10 |               |
|   | Latch          |           | $V_I = \text{GND}$          |                | -2  |               |
| $I_{IH}$ High-level input current (see Note 5)                      | Input pins     | 3.6 V     | $V_I = V_{CC}^\S$           |                | 10  | $\mu\text{A}$ |
|   |                | 5.25 V    | $V_I = V_{CC}^\S$           |                | 20  |               |
|   | I/O pins       | 3.6 V     | $V_I = V_{CC}^\S$           |                | 10  |               |
|   |                | 5.25 V    | $V_I = V_{CC}^\S$           |                | 25  |               |
|   | Fail-safe pins |           | $V_I = V_{CC}$              |                | 10  |               |
|   |                |           |                             |                |     |               |

$^\ddagger$  For PCI pins,  $V_I = V_{CCP}$ . For PC Card pins,  $V_I = V_{CC(A/B)}$ . For ZV pins,  $V_I = V_{CCZ}$ . For miscellaneous pins,  $V_I = V_{CCI}$ .

$^\S$  For I/O pins, input leakage ( $I_{IL}$  and  $I_{IH}$ ) includes  $I_{OZ}$  leakage of the disabled output.

NOTES: 4.  $V_{OH}$  and  $I_{OL}$  are not tested on SERR (pin U19) and RI\_OUT (pin Y13) because they are open-drain outputs.

5.  $I_{IH}$  is not tested on LATCH (pin W12) because it is pulled up with an internal resistor.



**PCI clock/reset timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 20 and 21)**

| PARAMETER           |  | ALTERNATE SYMBOL | TEST CONDITIONS | MIN | MAX | UNIT    |
|---------------------|--|------------------|-----------------|-----|-----|---------|
| $t_c$               | Cycle time, PCLK                                     | $t_{cyc}$        |                 | 30  |     | ns      |
| $t_{wH}$            | Pulse duration, PCLK high                            | $t_{high}$       |                 | 11  |     | ns      |
| $t_{wL}$            | Pulse duration, PCLK low                             | $t_{low}$        |                 | 11  |     | ns      |
| $\Delta v/\Delta t$ | Slew rate, PCLK                                      | $t_r, t_f$       |                 | 1   | 4   | V/ns    |
| $t_w$               | Pulse duration, RSTIN                                | $t_{rst}$        |                 | 1   |     | ms      |
| $t_{su}$            | Setup time, PCLK active at end of $\overline{RSTIN}$ | $t_{rst-clk}$    |                 | 100 |     | $\mu s$ |

**PCI timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4 and Figures 19 and 22)**

| PARAMETER |   | ALTERNATE SYMBOL                                      | TEST CONDITIONS                    | MIN | MAX | UNIT |
|-----------|---|---|------------------------------------|-----|-----|------|
| $t_{pd}$  | Propagation delay time, See Note 6                          | PCLK-to-shared signal valid delay time<br>$t_{val}$   | $C_L = 50 \text{ pF}$ , See Note 7 |     | 11  | ns   |
|           |   | PCLK-to-shared signal invalid delay time<br>$t_{inv}$ |                                    | 2   |     |      |
| $t_{en}$  | Enable time, high impedance-to-active delay time from PCLK  | $t_{on}$  |                                    | 2   |     | ns   |
| $t_{dis}$ | Disable time, active-to-high impedance delay time from PCLK | $t_{off}$   |                                    |     | 28  | ns   |
| $t_{su}$  | Setup time before PCLK valid                                | $t_{su}$  |                                    | 7   |     | ns   |
| $t_h$     | Hold time after PCLK high                                   | $t_h$   |                                    | 0   |     | ns   |

6. PCI shared signals are AD31–0, C/BE3–0,  $\overline{FRAME}$ , TRDY, IRDY, STOP, IDSEL, DEVSEL, and PAR.
- NOTES: 7. This data sheet uses the following conventions to describe time (  $t$  ) intervals. The format is  $t_A$ , where *subscript A* indicates the type of dynamic parameter being represented. One of the following is used:  $t_{pd}$  = propagation delay time,  $t_d$  = delay time,  $t_{su}$  = setup time, and  $t_h$  = hold time.

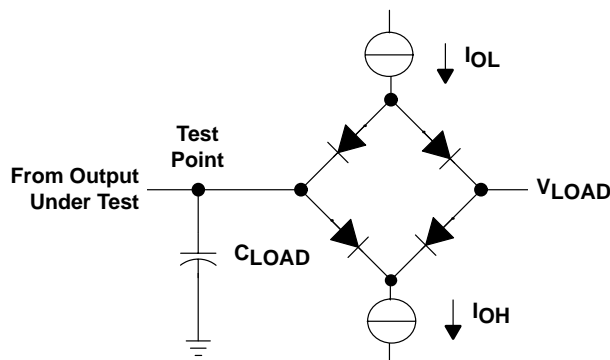
## PARAMETER MEASUREMENT INFORMATION

### LOAD CIRCUIT PARAMETERS

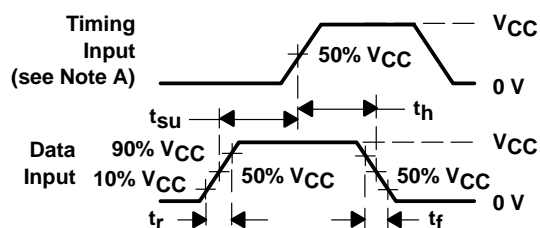
| TIMING<br>PARAMETER |           | $C_{LOAD}^{\dagger}$<br>(pF) | $I_{OL}$<br>(mA) | $I_{OH}$<br>(mA) | $V_{LOAD}$<br>(V) |
|---------------------|-----------|------------------------------|------------------|------------------|-------------------|
| $t_{en}$            | $t_{PZH}$ | 50                           | 8                | -8               | 0                 |
|                     | $t_{PZL}$ |                              |                  |                  | 3                 |
| $t_{dis}$           | $t_{PHZ}$ | 50                           | 8                | -8               | 1.5               |
|                     | $t_{PLZ}$ |                              |                  |                  | 1.5               |
| $t_{pd}$            |           | 50                           | 8                | -8               | †                 |

†  $C_{LOAD}$  includes the typical load-circuit distributed capacitance.

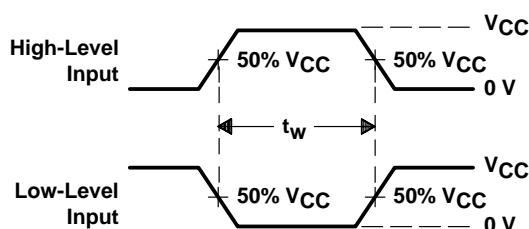
‡  $\frac{V_{LOAD} - V_{OL}}{I_{OL}} = 50 \Omega$ , where  $V_{OL} = 0.6 V$ ,  $I_{OL} = 8 mA$



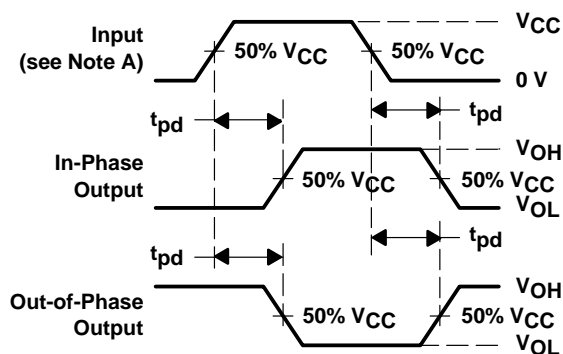
LOAD CIRCUIT



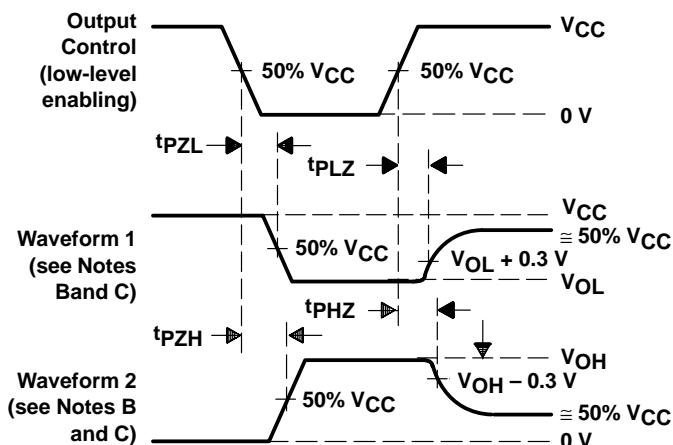
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by pulse generators having the following characteristics: PRR = 1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6 ns$ .
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. For  $t_{PLZ}$  and  $t_{PHZ}$ ,  $V_{OL}$  and  $V_{OH}$  are measured values.

Figure 1. Load Circuit and Voltage Waveforms

## PCI BUS PARAMETER MEASUREMENT INFORMATION

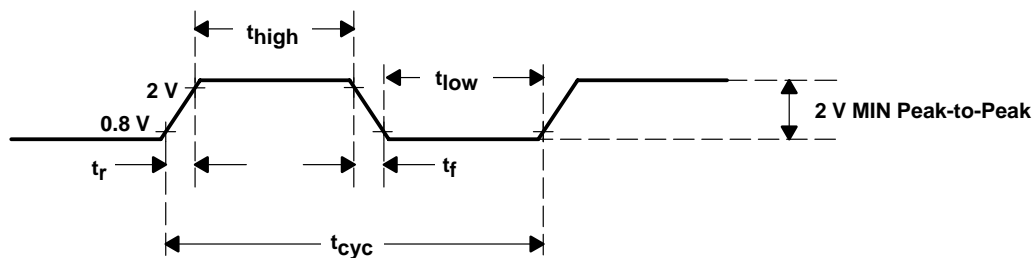


Figure 2. PCLK Timing Waveform

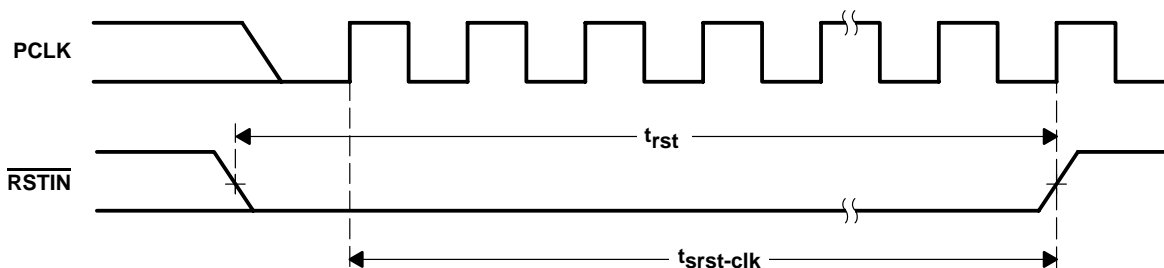


Figure 3.  $\overline{RSTIN}$  Timing Waveforms

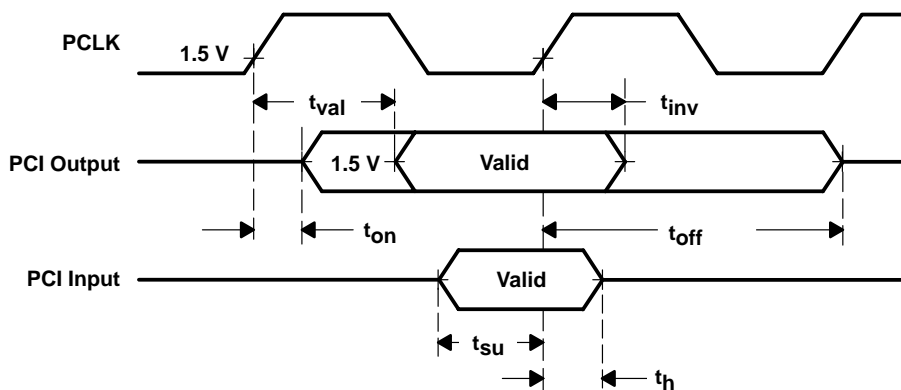


Figure 4. Shared Signals Timing Waveforms

### PC Card cycle timing

The PC Card cycle timing is controlled by the wait-state bits in the Intel 82365SL-DF compatible memory and I/O window registers. The PC Card cycle generator uses the PCI clock to generate the correct card address setup and hold times and the PC Card command active (low) interval. This allows the cycle generator to output PC Card cycles that are as close to the Intel 82365SL-DF timing as possible while always slightly exceeding the Intel 82365SL-DF values. This ensures compatibility with existing software and maximizes throughput.

The PC Card address setup and hold times are a function of the wait-state bits. Table 1 shows address setup time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 2 and Table 3 show command active time in PCLK cycles and nanoseconds for I/O and memory cycles. Table 4 shows address hold time in PCLK cycles and nanoseconds for I/O and memory cycles.

**Table 1. PC Card Address Setup Time,  $t_{su}(A)$ , 8-Bit and 16-Bit PCI Cycles**

| WAIT-STATE BITS |     |   | TS1 – 0 = 01<br>(PCLK/ns) |
|-----------------|-----|---|---------------------------|
| I/O             |     |   | 3/90                      |
| Memory          | WS1 | 0 | 2/60                      |
| Memory          | WS1 | 1 | 4/120                     |

**Table 2. PC Card Command Active Time,  $t_c(A)$ , 8-Bit PCI Cycles**

| WAIT-STATE BITS |    |     | TS1 – 0 = 01<br>(PCLK/ns) |
|-----------------|----|-----|---------------------------|
|                 | WS | ZWS |                           |
| I/O             | 0  | 0   | 19/570                    |
|                 | 1  | X   | 23/690                    |
|                 | 0  | 1   | 7/210                     |
| Memory          | 00 | 0   | 19/570                    |
|                 | 01 | X   | 23/690                    |
|                 | 10 | X   | 23/690                    |
|                 | 11 | X   | 23/690                    |
|                 | 00 | 1   | 7/210                     |

**Table 3. PC Card Command Active Time,  $t_c(A)$ , 16-Bit PCI Cycles**

| WAIT-STATE BITS |    |     | TS1 – 0 = 01<br>(PCLK/ns) |
|-----------------|----|-----|---------------------------|
|                 | WS | ZWS |                           |
| I/O             | 0  | 0   | 7/210                     |
|                 | 1  | X   | 11/330                    |
|                 | 0  | 1   | N/A                       |
| Memory          | 00 | 0   | 9/270                     |
|                 | 01 | X   | 13/390                    |
|                 | 10 | X   | 17/510                    |
|                 | 11 | X   | 23/630                    |
|                 | 00 | 1   | 5/150                     |

Table 4. PC Card Address Hold Time,  $t_{h(A)}$ , 8-Bit and 16-Bit PCI Cycles

| WAIT-STATE BITS |     |   | TS1 – 0 = 01<br>(PCLK/ns) |
|-----------------|-----|---|---------------------------|
| I/O             |     |   | 2/60                      |
| Memory          | WS1 | 0 | 2/60                      |
| Memory          | WS1 | 1 | 3/90                      |

timing requirements over recommended ranges of supply voltage and operating free-air temperature, memory cycles (for 100-ns common memory) (see Note 5 and Figure 5)

|   | ALTERNATE SYMBOL | MIN               | MAX | UNIT |
|---|------------------|-------------------|-----|------|
| $t_{su}$ Setup time, $\overline{CE1}$ and $\overline{CE2}$ before $\overline{WE}/\overline{OE}$ low | T1               | 60                |     | ns   |
| $t_{su}$ Setup time, CA25–CA0 before $\overline{WE}/\overline{OE}$ low                              | T2               | $t_{su(A)}+2PCLK$ |     | ns   |
| $t_{su}$ Setup time, $\overline{REG}$ before $\overline{WE}/\overline{OE}$ low                      | T3               | 90                |     | ns   |
| $t_{pd}$ Propagation delay time, $\overline{WE}/\overline{OE}$ low to $\overline{WAIT}$ low         | T4               |                   |     | ns   |
| $t_w$ Pulse duration, $\overline{WE}/\overline{OE}$ low   | T5               | 200               |     | ns   |
| $t_h$ Hold time, $\overline{WE}/\overline{OE}$ low after $\overline{WAIT}$ high                     | T6               |                   |     | ns   |
| $t_h$ Hold time, $\overline{CE1}$ and $\overline{CE2}$ after $\overline{WE}/\overline{OE}$ high     | T7               | 120               |     | ns   |
| $t_{su}$ Setup time (read), CDATA15–CDATA0 valid before $\overline{OE}$ high                        | T8               |                   |     | ns   |
| $t_h$ Hold time (read), CDATA15–CDATA0 valid after $\overline{OE}$ high                             | T9               | 0                 |     | ns   |
| $t_h$ Hold time, CA25–CA0 and $\overline{REG}$ after $\overline{WE}/\overline{OE}$ high             | T10              | $t_{h(A)}+1PCLK$  |     | ns   |
| $t_{su}$ Setup time (write), CDATA15–CDATA0 valid before $\overline{WE}$ low                        | T11              | 60                |     | ns   |
| $t_h$ Hold time (write), CDATA15–CDATA0 valid after $\overline{WE}$ low                             | T12              | 240               |     | ns   |

NOTE 8: These times are dependent on the register settings associated with ISA wait states and data size. They are also dependent on cycle type (read/write, memory/I/O) and WAIT from PC Card. The times listed here represent absolute minimums (the times that would be observed if programmed for zero wait state, 16-bit cycles) with a 33-MHz PCI clock.

timing requirements over recommended ranges of supply voltage and operating free-air temperature, I/O cycles (see Figure 6)

|   | ALTERNATE SYMBOL | MIN               | MAX | UNIT |
|---|------------------|-------------------|-----|------|
| $t_{su}$ Setup time, $\overline{REG}$ before $\overline{IORD}/\overline{IOWR}$ low                      | T13              | 60                |     | ns   |
| $t_{su}$ Setup time, $\overline{CE1}$ and $\overline{CE2}$ before $\overline{IORD}/\overline{IOWR}$ low | T14              | 60                |     | ns   |
| $t_{su}$ Setup time, CA25–CA0 valid before $\overline{IORD}/\overline{IOWR}$ low                        | T15              | $t_{su(A)}+2PCLK$ |     | ns   |
| $t_{pd}$ Propagation delay time, $\overline{IOIS16}$ low after CA25–CA0 valid                           | T16              |                   | 35  | ns   |
| $t_{pd}$ Propagation delay time, $\overline{IORD}$ low to $\overline{WAIT}$ low                         | T17              | 35                |     | ns   |
| $t_w$ Pulse duration, $\overline{IORD}/\overline{IOWR}$ low   | T18              | $T_{cA}$          |     | ns   |
| $t_h$ Hold time, $\overline{IORD}$ low after $\overline{WAIT}$ high                                     | T19              |                   |     | ns   |
| $t_h$ Hold time, $\overline{REG}$ low after $\overline{IORD}$ high                                      | T20              | 0                 |     | ns   |
| $t_h$ Hold time, $\overline{CE1}$ and $\overline{CE2}$ after $\overline{IORD}/\overline{IOWR}$ high     | T21              | 120               |     | ns   |
| $t_h$ Hold time, CA25–CA0 after $\overline{IORD}/\overline{IOWR}$ high                                  | T22              | $t_{h(A)}+1PCLK$  |     | ns   |
| $t_{su}$ Setup time (read), CDATA15–CDATA0 valid before $\overline{IORD}$ high                          | T23              | 10                |     | ns   |
| $t_h$ Hold time (read), CDATA15–CDATA0 valid after $\overline{IORD}$ high                               | T24              | 0                 |     | ns   |
| $t_{su}$ Setup time (write), CDATA15–CDATA0 valid before $\overline{IOWR}$ low                          | T25              | 90                |     | ns   |
| $t_h$ Hold time (write), CDATA15–CDATA0 valid after $\overline{IOWR}$ high                              | T26              | 90                |     | ns   |

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PC CARD CONTROLLER

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, miscellaneous (see Figure 7)

| PARAMETER                              |                           | ALTERNATE SYMBOL | MIN | MAX | UNIT |
|--|---------------------------|------------------|-----|-----|------|
| t <sub>pd</sub> Propagation delay time | BVD2 low to SPKROUT low   | T27              |     | 30  | ns   |
|  | BVD2 high to SPKROUT high |                  |     | 30  |      |
|  | IREQ to IRQ15–IRQ3        | T28              |     | 30  |      |
|  | STSCHG to IRQ15–IRQ3      |                  |     | 30  |      |

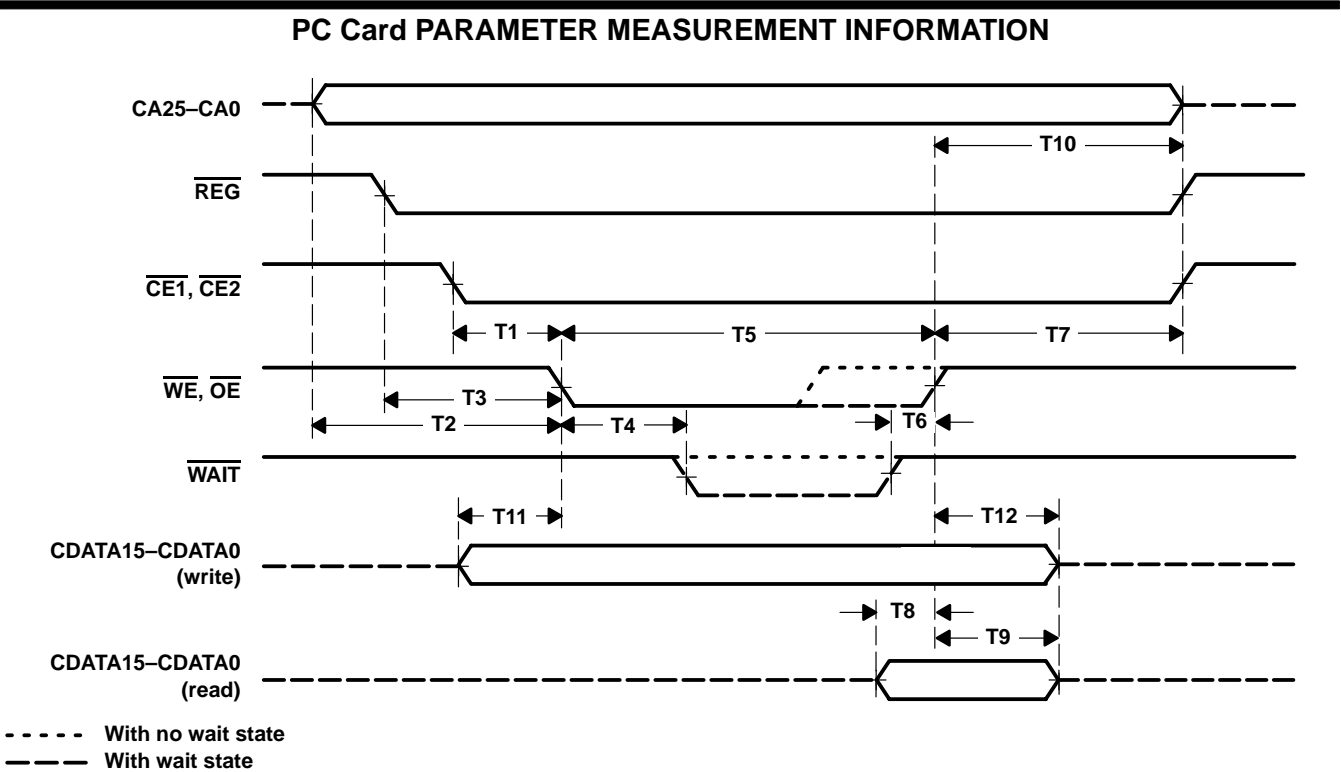


Figure 5. PC Card Memory Cycle



## PC Card PARAMETER MEASUREMENT INFORMATION

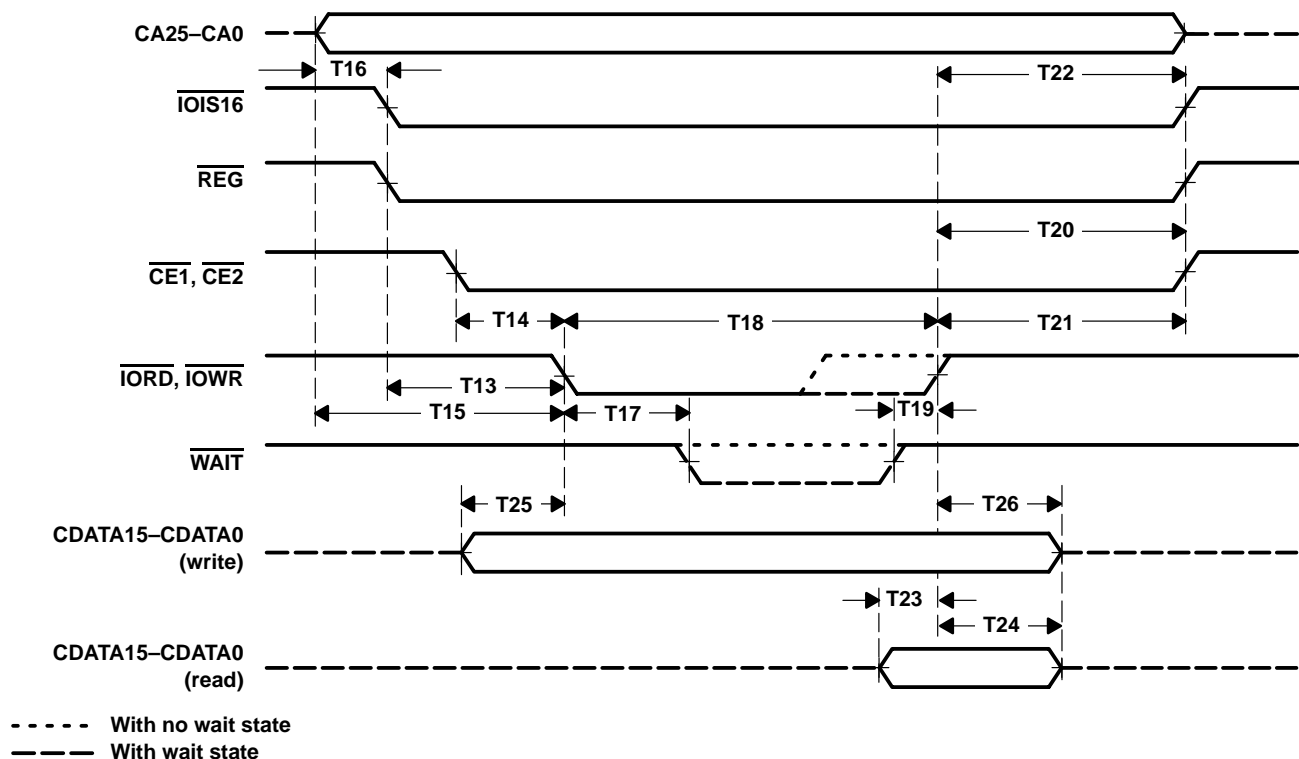


Figure 6. PC Card I/O Cycle

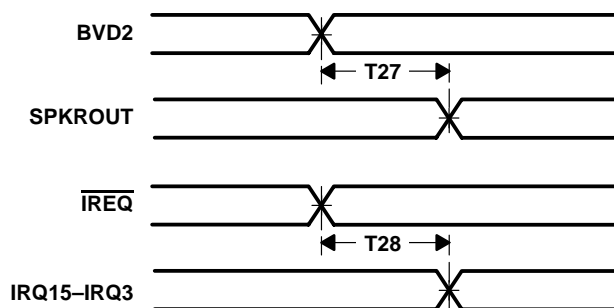


Figure 7. Miscellaneous PC Card Delay Times

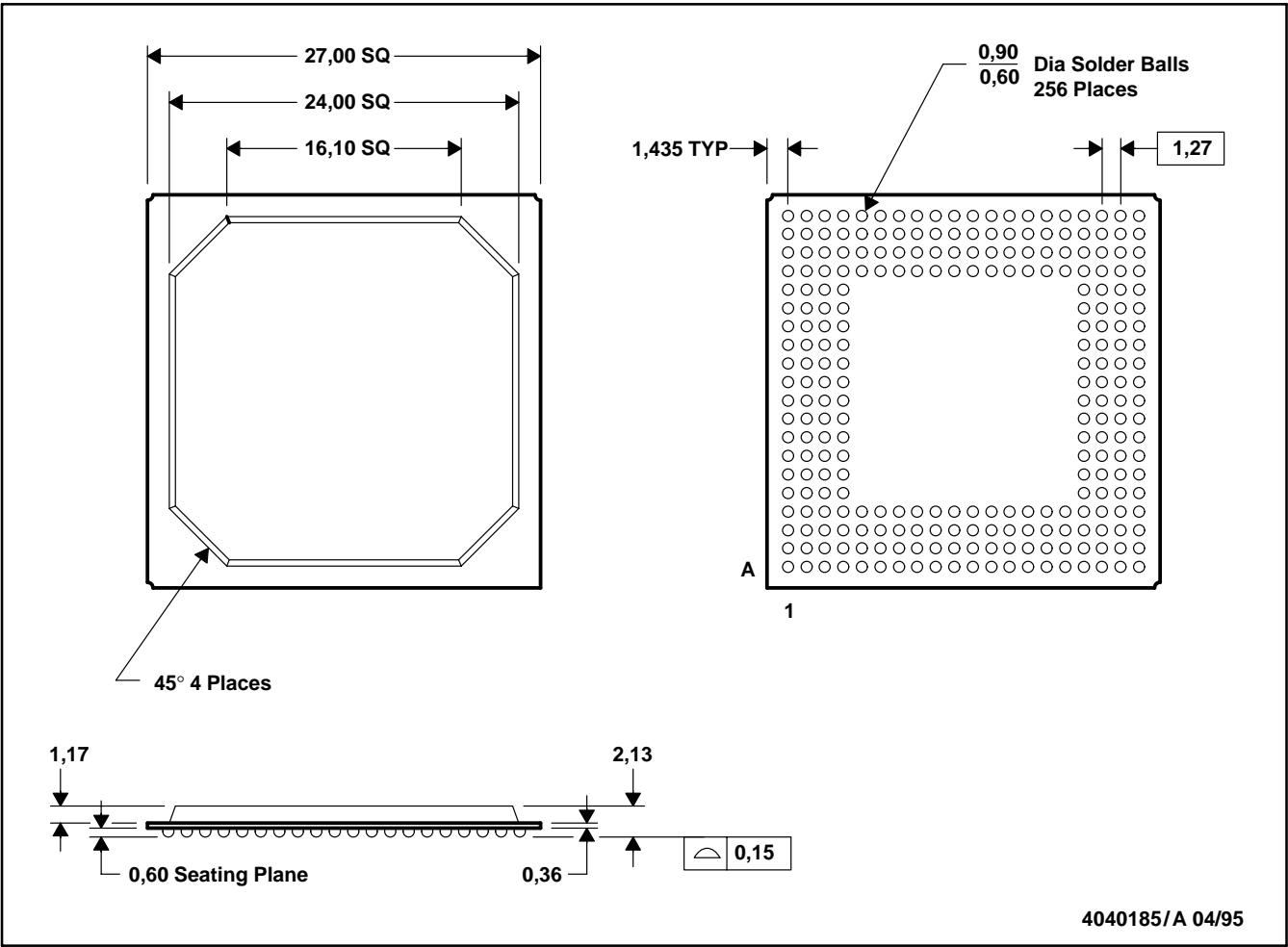
PCI1250A  
PC CARD CONTROLLER

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MECHANICAL DATA

GFN (S-PBGA-N256)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.

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