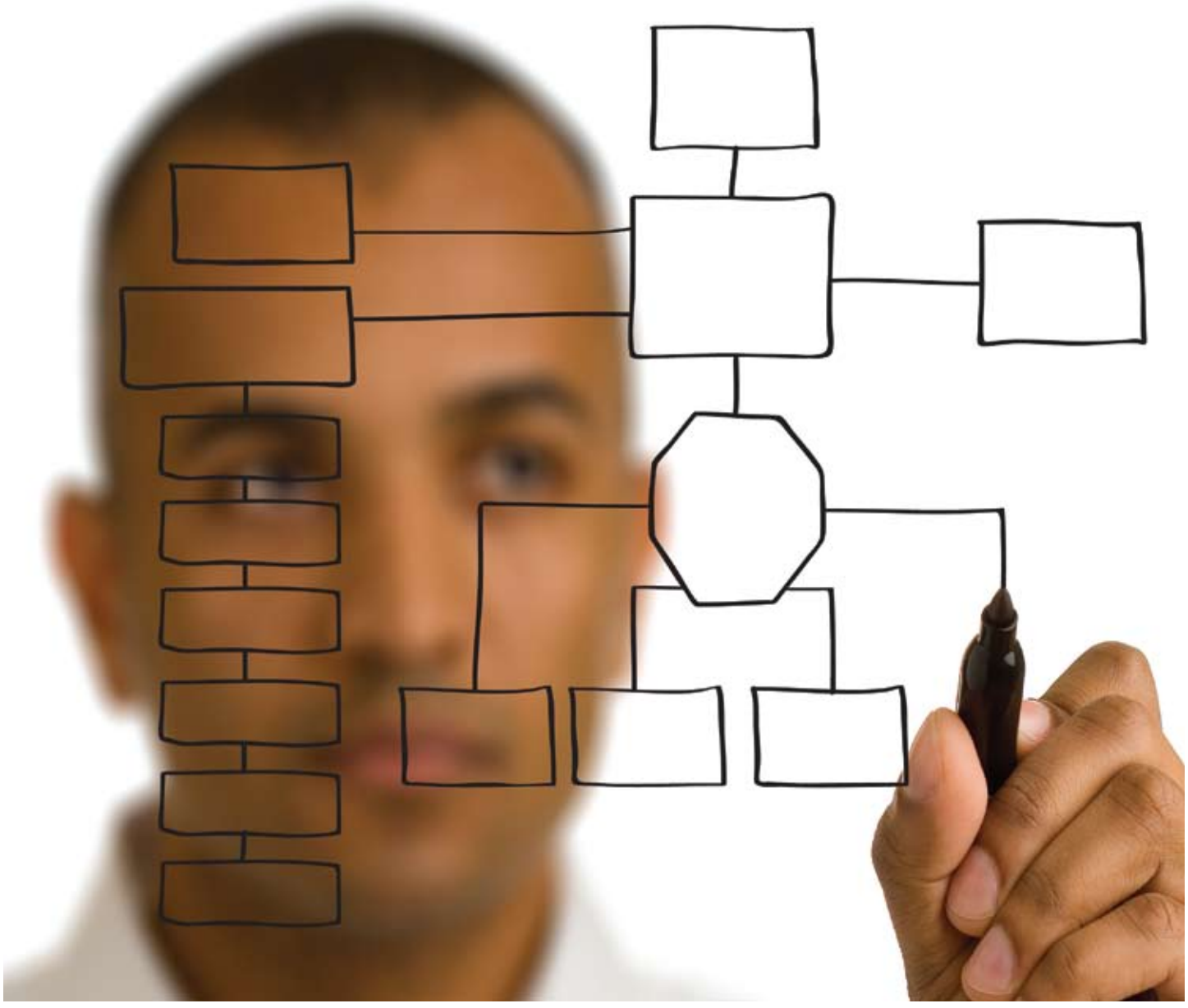
PCI Express

Migrate. Integrate. Accelerate.

Texas Instruments



PCI Express

XIO2000A PCI Express® bridge chip

Key features

- Compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Compliant with PCI Express Base Specification, Revision 1.0a
- Compliant with PCI Local Bus Specification revision 2.3
- Utilizes 100-MHz differential PCI Express common reference clock or 125-MHz single-ended reference clock
- Full PCI Local Bus 66-MHz/32-bit throughput
- Wake/Beacon event support
- Robust architecture to minimize latency

Texas Instruments' PCI Express bridge chip, the XIO2000A, is an industry first. It is designed for seamless migration from the legacy PCI to the PCI Express interface. It bridges a x1 PCI Express bus to a 32-bit, 33-/66-MHz PCI bus capable of supporting up to six PCI devices downstream. The XIO2000A fully supports PCI Express rates of 2.5 Gbps. Its architecture supports the PCI 2.3 interface. The chip's design enables PC and I/O add-on card manufacturers to begin transitioning to native PCI Express technology while preserving compatibility with existing PCI system software and firmware.

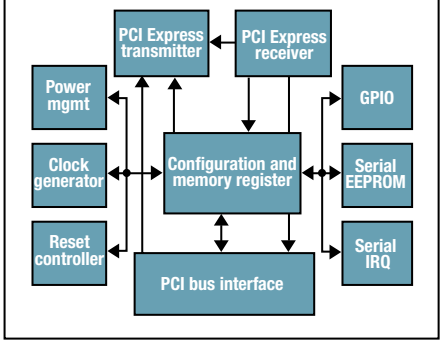
Target markets

The XIO2000A meets the needs of multiple market segments, including desktop and mobile PC, server, storage, PC add-in cards, and embedded systems.

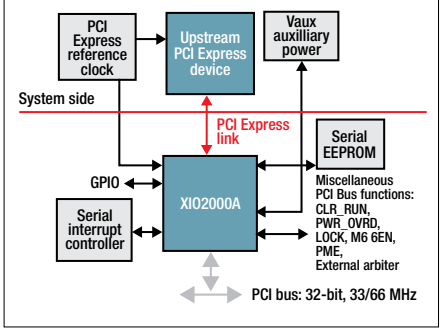
Key benefits

- Proven capability and interoperability with leading PCI-e chipsets and plethora of PCI devices
- Built-in adaptive receiver equalizer
  - Improves jitter tolerance thereby reliably increasing PCB trace or cable length supported by the XIO2000A
- Seven buffered PCI clock outputs (33-MHz or 66-MHz)
  - Reduces external components and costs and saves valuable board space
- 32-bit secondary PCI bus with 33-MHz or 66-MHz clocking option
  - Customized to meet the needs of high-performance or low-power applications
- Compact footprint (12 mm x 12 mm)
  - Allows placement in ExpressCard and mini-PCI cards in limited board space
- Advanced power management features
  - Software-programmable and hardware-autonomous power management features for low-power applications such as ExpressCard

XIO2000A functional block diagram



Typical system implementation

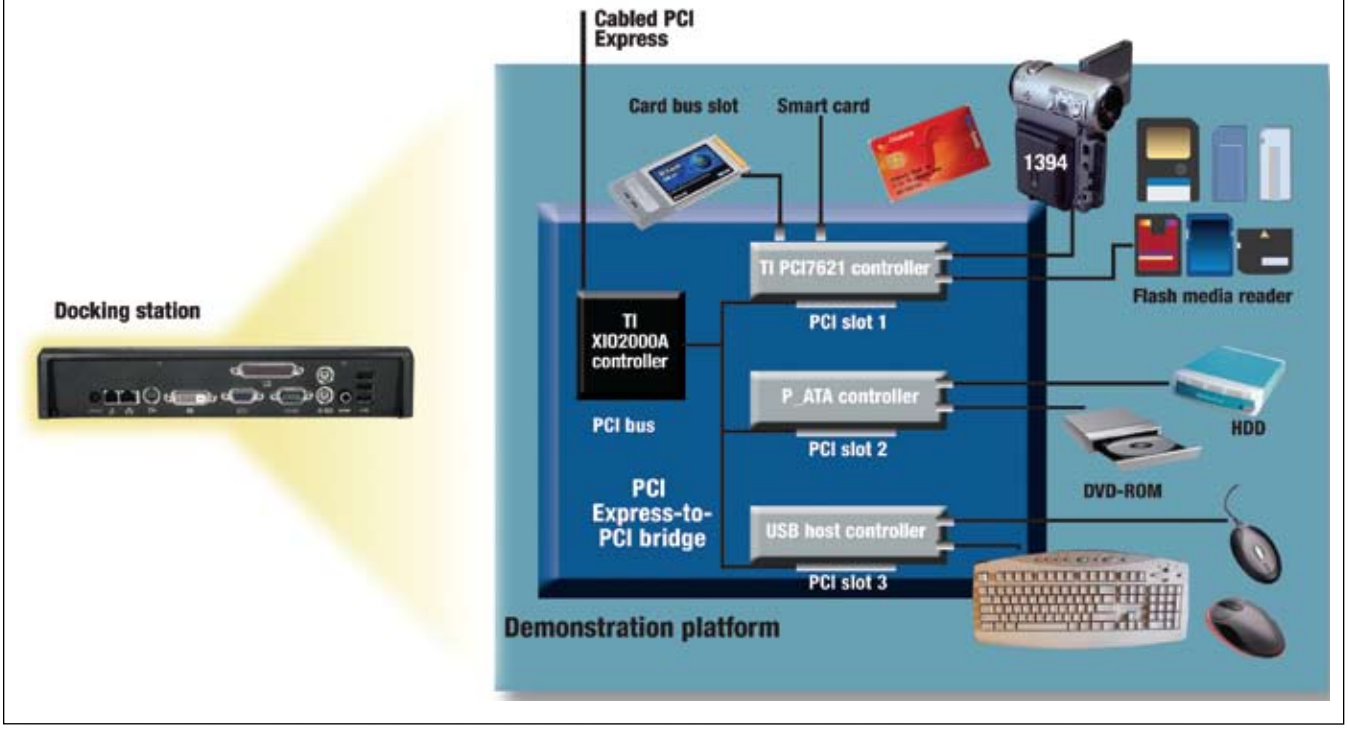


XIO2000A

Part number	Package (MicroStar BGA)	Data manual/ implementation guide/ evaluation board	Production
XIO2000AGZZ	201-ball Pb	www.ti.com/sc/device/XIO2000A	Now available
XIO2000AZZZ	201-ball Pb-free (RoHS-compliant)		
XIO2000AZHH	176-ball Pb-free (RoHS-compliant)		

XIO2000A Target applications

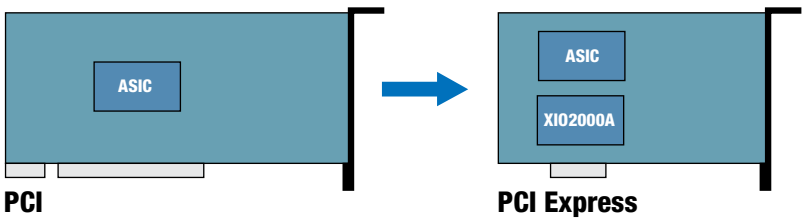
Docking station/split-chassis implementation



ExpressCard enabled

1394b ExpressCard built with the XIO2000A (Reference design and sample available from TI).

Transitioning PCI riser card and add-in cards to PCI Express



XIO2200A PCI Express to 1394a chip

Key features

- Full x1 PCI Express throughput
- Fully compliant with PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0
- Fully compliant with PCI Express Base Specification, Revision 1.0a
- Fully compliant with provisions of IEEE standard 1394-1995 for a high-performance serial bus and IEEE standard 1394a-2000
- Fully-compliant with 1394 Open Host Controller Interface Specification 1.1
- Full IEEE standard 1394a-2000 support includes: connection debounce, arbitrated short reset and multi-speed
- Concatenation, arbitration acceleration, fly-by concatenation and port disable/suspend/resume
- Two IEEE standard 1394a-2000 fully compliant cable ports at 100, 200 and 400 Mbps
- Cable ports monitor line conditions for active connection to remote nodes
- Cable power presence monitoring
- EEPROM configuration support to load the global unique ID for the 1394 fabric

The XIO2200A is a single-function PCI Express-to-PCI translation bridge where the PCI bus interface is internally connected to a 1394a Open-Host Controller Link-Layer Controller with a two-port 1394a PHY. The device is capable of transferring data between the PCI Express bus and the 1394 bus at 100, 200 and 400 Mbps. The XIO2200A provides two 1394 ports that have separate cable bias (TPBIAS). The device also supports IEEE standards such as 1394a-2000 power-down features for battery-operated applications and arbitration enhancements.

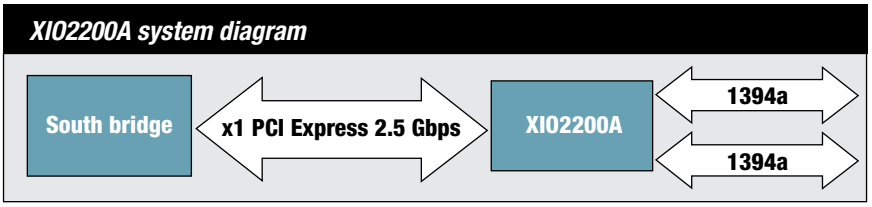
Target markets

ExpressCards, PC motherboards and embedded applications

Key benefits

- Proven compatibility and interoperability with leading PCIe chipsets and 1394a devices
- One-chip solution for 1394a ExpressCards
- Software-programmable and hardware-autonomous power-management features for low-power applications such as ExpressCard
- Compact footprint, 12 mm x 12 mm 175-ball MicroStar BGA™
- EEPROM configuration support to load the global unique ID for the 1394 fabric

XIO2200A system diagram



1394a ExpressCard built with the XIO2200A (sample available from TI).

XIO2200A

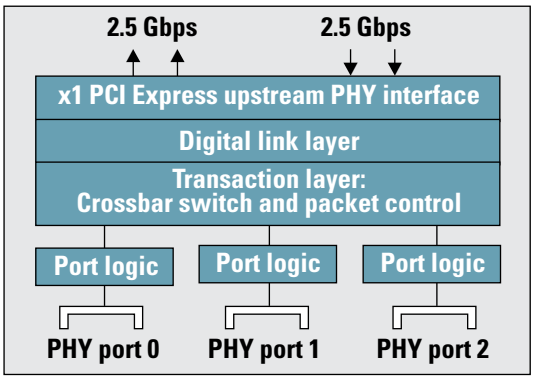
Part number	Package (MicroStar BGA)	Data manual/ implementation guide/ evaluation board	Production
XIO2200AGGW	176-ball Pb	www.ti.com/sc/device/XIO2200A	Now available
XIO2200AZGW	176-ball Pb-free (RoHS-compliant)		
XIO2200AZHH	175-ball Pb-free (RoHS-compliant)		

XIO3130 PCI Express fan-out switch

The XIO3130 is an integrated PCI Express fan-out switch solution supporting four lanes and four ports. This high-performance, integrated solution provides the latest in PCI Express switch technology compliant to PCI Express Base Specification, Revision 1.1 and PCI Local Bus Specification, Revsion 2.3 and beyond.

Target markets

The primary purpose of the XIO3130 as a fan-out device is to efficiently expand the root complex computing resources to multiple I/O ports, thereby enhancing system functionality and flexibility. Target applications for the XIO3130 include PCs, server HBA, embedded systems, industrial control and backplanes, docking stations, and add-in cards.

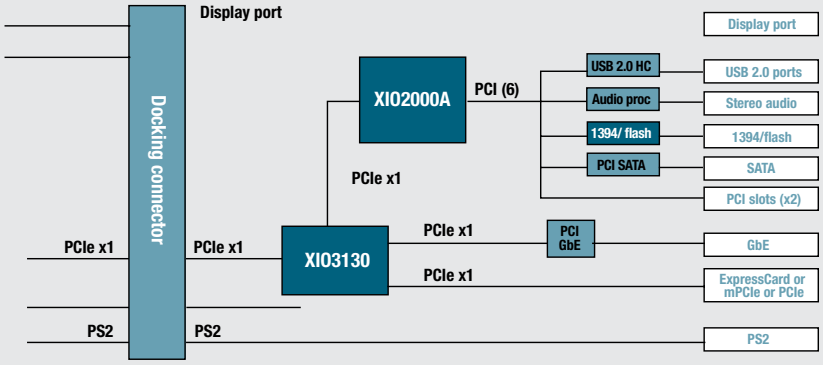


Key features

- PCI Express fan-out switch with x1 upstream port and three x1 downstream ports
- Fully compliant with PCI Express Base Specification, Revsion. 1.1
- Cut-through architecture
- Peer-to-peer support on all downstream ports
- Integrated AUX power switch drains VAUX power only when main power is off
- Integrated hot-plug support for each of the three downstream ports
- Seamless support for ExpressCard slot using the TPS2231/TPS2236 power interface switch
- Integrated REFCLK buffers for switch downstream ports
- Built-in adaptive equalizer in each of the four ports
- Wake-event and beacon support
- Support for D1, D2, D3hot, and D3cold
- Low-power PCI Express transmitter mode (pre-emphasis disabled)
- Advanced error reporting
- 3.3-V multifunction I/O pins (e.g. for hot-plug status and control, or general-purpose I/Os)
- Listed in PCI-SIG PCI Express Integrators List

XIO3130 functional block diagram

Docking station example



XIO3130

Part number	Package (MicroStar BGA)	Data manual/ implementation guide/ evaluation board	Production
XIO3130ZHC	196-ball Pb-free (RoHS-compliant)	www.ti.com/sc/device/XIO3130	Q2 2008

XIO1100 PIPE-compliant X1 PCI Express PHY

Key features

- x1 PCI Express stand-alone PHY
- Support for 16-bit or 8-bit modified PIPE (M-PIPE) architecture
- Robust clocking scheme supported by source-synchronous clock mode
- Support for L0/L0s/L1/L2/L3 power-management states
- Pin-selectable clock source, 100-MHz differential or 125-MHz single-ended
- 100-ball BGA package

The XIO1100 is a PCI Express PHY that interfaces the PCI Express media access control (MAC) layer to a PCI Express serial link using a modified version of the PHY interface for the PCI Express (PIPE) architecture. This version of the PIPE interface provides a pin-configurable interface that can be pin-configured as either a 16-bit or 8-bit interface.

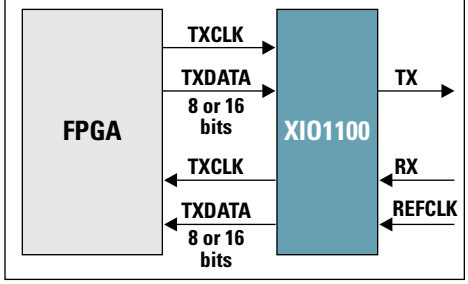
The M-PIPE supports source-synchronous clocking where TXCLK/RXCLK travels in parallel with the data. In this way, the clock experiences the same delay and drift as the data, enabling the data to be reliably clocked into the receiving device.

The PHY interfaces to a 2.5-Gbps PCI Express serial link with a transmit-differential pair and a receive-differential pair. The PHY is responsible for handling the 8b/10b encoding/decoding and scrambling/unscrambling of the outgoing data. In addition, the PHY must recover/interpolate the clock on the receiver side based on the transitions guaranteed by the 8b/10b mechanism and supply the recovered clock to the receive side of the data link-layer logic.

Target markets

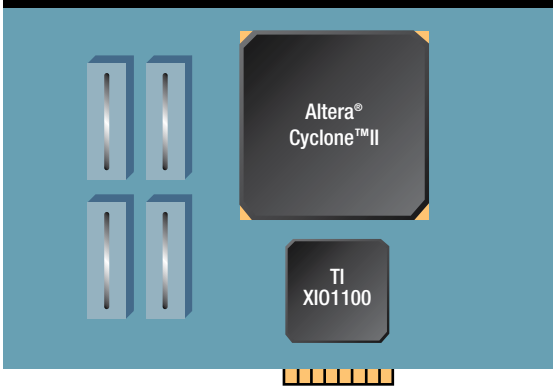
TI has partnered with Altera, a leading low-cost FPGA provider, to bring new solutions in the FPGA market. The XIO1100 is ideal for the FPGA market where a PHY is not integrated into the low-cost FPGA product lines. The XIO1100 is also targeted at ASIC applications to avoid the expense of integrating a PHY.

Essentials of M-PIPE interface



For a detailed description, consult the XIO1100 Data manual available at www.ti.com/sc/device/XIO1100.

TI Altera x1 PCI Express evaluation board



XIO1100

Part number	Package (PBGA)	Samples	Data manual/ implementation guide	Production
XIO1100GGB	100-ball Pb	Now available	www.ti.com/sc/device/XIO1100	Now
XIO1100ZGB	100-ball Pb-free (RoHS-compliant)			

PCIE412 x1 four-channel 2:1 mux switch

The PCIE412 x1, four-channel, PCIe 2:1, multiplexer/demultiplexer passive FET switch is ideal for routing either one PCIe data lane between two possible destinations or two PCIe data lanes to one destination. You can also route differential pairs of receive (RX) and transmit (TX) signals through a single PCB skew.

The switch operates at a signal-processing bandwidth speed of 2.5 Gbps and is controlled with one select input pin, which controls the data path of the mux/demux and can be connected to any GPIO in the system using an external voltage divider system.

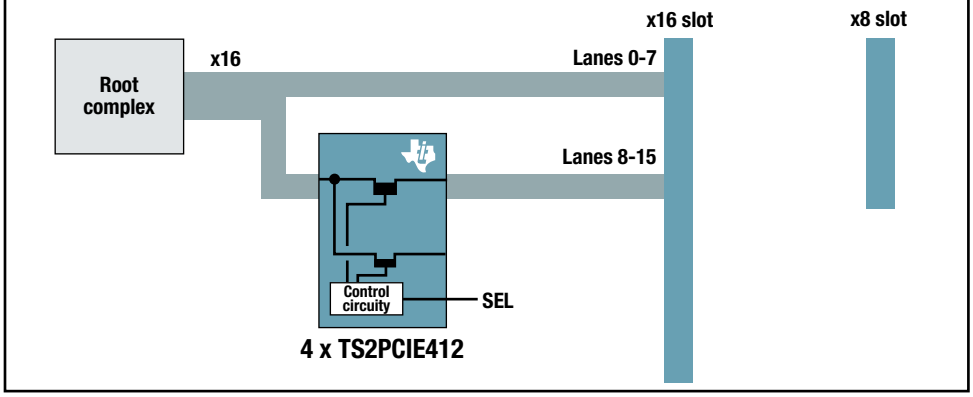
Target markets

Computing (desktop and notebook), servers and telecom, or applications using PCIe

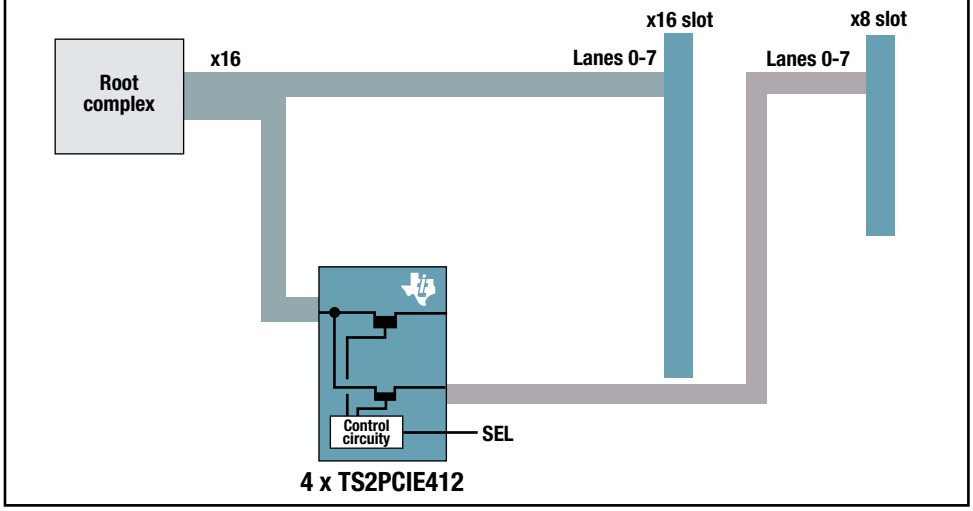
Key features

- Compatible with PCIe generation 1 standard
- Low R_{on} and C_{on}, assuring maximum signal transfer while maintaining low distortion
- Low crosstalk of -40 dB, minimizing transmission noise
- Low channel-to-channel and bit-to-bit skew, optimizing synchronization on the signal path
- 42-pin QFN package

Usage case example 1



Usage case example 2



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