Burr-Brown Products
from Texas Instruments

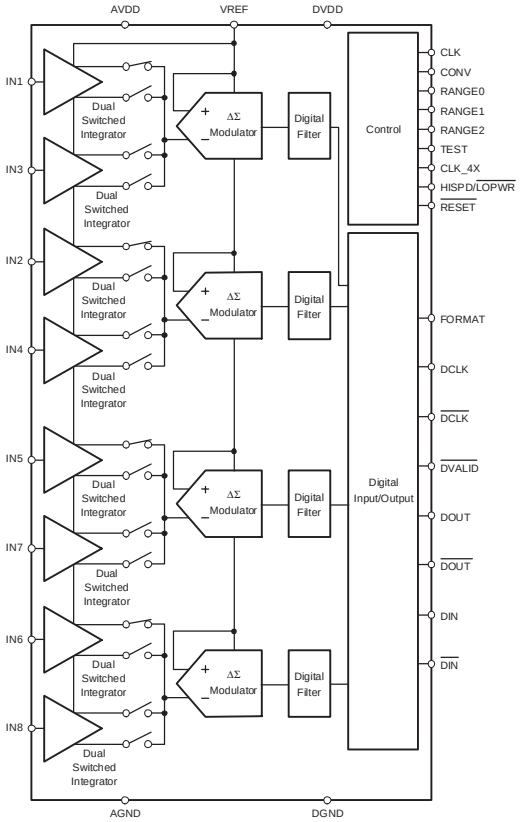
DDC118

SBAS325A − JUNE 2004 − REVISED JUNE 2005

Octal Current Input 20-Bit Analog-To-Digital Converter

FEATURES

- SINGLE-CHIP SOLUTION TO DIRECTLY MEASURE EIGHT LOW-LEVEL CURRENTS
- HIGH PRECISION, TRUE INTEGRATING FUNCTION
- INTEGRAL LINEARITY: ±0.01% of Reading ±0.5ppm of FSR
- VERY LOW NOISE: 5.2ppm of FSR
- LOW POWER: 13.5mW/channel
- ADJUSTABLE DATA RATE: Up to 3.125kSPS
- PROGRAMMABLE FULL SCALE
- DAISY-CHAINABLE SERIAL INTERFACE



APPLICATIONS

- CT SCANNER DAS
- PHOTODIODE SENSORS
- INFRARED PYROMETER
- LIQUID/GAS CHROMATOGRAPHY

Protected by US Patent #5841310

DESCRIPTION

The DDC118 is a 20-bit octal channel, current-input analog-to-digital (A/D) converter. It combines both current-to-voltage and A/D conversion so that eight low-level current output devices, such as photodiodes, can be directly connected to its inputs and digitized.

For each of the eight inputs, the DDC118 provides a dual-switched integrator front-end. This design allows for continuous current integration: while one integrator is being digitized by the onboard A/D converter, the other is integrating the input current. Adjustable full-scale ranges from 12pC to 350pC and adjustable integration times from 50µs to 1s allow currents from fAs to µAs to be measured with outstanding precision. Low-level linearity is ±0.5ppm of the full-scale range and noise is 5.2ppm of the full-scale range.

Two modes of operation are provided. In Low-Power mode, total power dissipation is only 13.5mW per channel with a maximum data rate of 2.5kSPS. High-Speed mode supports data rates up to 3.125kSPS with a corresponding dissipation of 18mW per channel.

The DDC118 has a serial interface designed for daisy-chaining in multi-device systems. Simply connect the output of one device to the input of the next to create the chain. Common clocking feeds all the devices in the chain so that the digital overhead in a multi-DDC118 system is minimal.

The DDC118 is a single-supply device using a +5V analog supply and supporting a +2.7V to +5.25V digital supply. Operating over the industrial temperature range of −40°C to 85°C, the DDC118 is offered in a QFN-48 package.

ABSOLUTE MAXIMUM RATINGS(1)

Analog Input Current	750µA
AVDD to DVDD	−0.3V to +6V
AVDD to AGND	−0.3V to +6V
DVDD to DGND	−0.3V to +6V
AGND to DGND	±0.2V
VREF Input to AGND	2.0V to AVDD + 0.3V
Analog Input to AGND	−0.3V to +0.7V
Digital Input Voltage to DGND	−0.3V to DVDD + 0.3V
Digital Output Voltage to DGND	−0.3V to AVDD + 0.3V
Operating Temperature	−40°C to +85°C
Storage Temperature	−60°C to +150°C
Junction Temperature (T_J)	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = 3V, VREF = +4.096V, Range 5 (250pC), and continuous mode operation, unless otherwise noted.
Low-Power Mode: T_{INT} = 400µs and CLK = 4MHz; High-Speed Mode: T_{INT} = 320µs and CLK = 4.8MHz.

PARAMETER	TEST CONDITIONS	Low-Power Mode			High-Speed Mode			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT RANGE								
Range 0		10.2	12	13.8	*(1)	*	*	pC
Range 1		47.5	50	52.5	*	*	*	pC
Range 2		95	100	105	*	*	*	pC
Range 3		142.5	150	157.5	*	*	*	pC
Range 4		190	200	210	*	*	*	pC
Range 5		237.5	250	262.5	*	*	*	pC
Range 6		285	300	315	*	*	*	pC
Range 7		332.5	350	367.5	*	*	*	pC
Negative Full-Scale Range		−0.4% of Positive Full-Scale Range				*		pC
Input Current(2)				750			*	µA
DYNAMIC CHARACTERISTICS								
Data Rate				2.5			3.125	kSPS
Integration Time, T_{INT}	Continuous Mode	400		1,000,000	320		*	µS
	Non-continuous Mode, Range 1 to 7	50			*			µS
System Clock Input (CLK)								
CLK_4X = 0				4			4.8	MHz
CLK_4X = 1				16			19.2	MHz
Data Clock (DCLK)				16			*	MHz
ACCURACY								
Noise, Low-Level Input(3)	C_{SENSOR}(4) = 50pF, Range 5 (250pC)		5.2	6.5		5.5	7	ppm of FSR(5), rms
Integral Linearity Error(6)		±0.01% Reading ± 0.5ppm FSR, typ				*		
		±0.025% Reading ± 1.0ppm FSR, max				*		
Resolution	FORMAT = 1	20			*			Bits
	FORMAT = 0	16			*			Bits
Input Bias Current			0.1	10		*	*	pA
Range Error Match(7)	All Ranges		0.1	0.5		*	*	% of FSR
Range Sensitivity to VREF	V_{REF} = 4.096 ± 0.1V		1:1			*		
Offset Error	Range 5 (250pC)		±400	±1000		*	*	ppm of FSR
Offset Error Match(7)			±100			*		ppm of FSR
DC Bias Voltage(9)	Low-Level Input (< 1% FSR)		±0.05	±2		*	*	mV
Power-Supply Rejection Ratio	at dc		±25	±200		*	*	ppm of FSR/V
Internal Test Signal			11			*		pC
Internal Test Accuracy			±10			*		%
PERFORMANCE OVER TEMPERATURE								
Offset Drift			±0.5	±3(8)		*	*	ppm of FSR/°C
Offset Drift Stability			±0.2	±1(8)		*	*	ppm of FSR/ minute
DC Bias Voltage Drift(9)			3			*		µV/°C
Input Bias Current Drift	T_A = +25°C to +45°C		0.01	1(8)		*	*	pA/°C
Range Drift(10)			25			*		ppm/°C
REFERENCE								
Voltage		4.000	4.096	4.200	*	*	*	V
Input Current(11)	Average Value		150			190		µA

(1) * indicates that specification is the same as Low-Power Mode.
(2) Exceeding maximum input current specification may damage device.
(3) Input is less than 1% of full scale.
(4) C_{SENSOR} is the capacitance seen at the DDC118 inputs from wiring, photodiode, etc.
(5) FSR is Full-Scale Range.
(6) A best-fit line is used in measuring nonlinearity.
(7) Matching between side A and side B of the same input.
(8) Ensured by design, not production tested.
(9) Voltage produced by the DDC118 at its input which is applied to the sensor.
(10) Range drift does not include external reference drift.
(11) Input reference current decreases with increasing T_{INT} (see the *Voltage Reference* section, page 11).
(12) Data format is Straight Binary with a small offset. The number of bits in the output word is controlled by the FORMAT pin (see text).

ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +5V, DVDD = 3V, VREF = +4.096V, Range 5 (250pC), and continuous mode operation, unless otherwise noted.
Low-Power Mode: T_{INT} = 400µs and CLK = 4MHz; High-Speed Mode: T_{INT} = 320µs and CLK = 4.8MHz.

PARAMETER	TEST CONDITIONS	Low-Power Mode			High-Speed Mode			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT								
Logic Levels								
V_{IH}		0.8DVDD		DVDD + 0.1	*		*	V
V_{IL}		− 0.1		0.2DVDD	*		*	V
V_{OH}	I_{OH} = −500µA	DVDD − 0.4						V
V_{OL}	I_{OL} = 500µA			0.4			*	V
Input Current (I_{IN})	0 < V_{IN} < DVDD			±10			*	µA
Data Format(12)			Straight Binary			*		
POWER-SUPPLY REQUIREMENTS								
Analog Power-Supply Voltage (AVDD)		4.75		5.25	*		*	V
Digital Power-Supply Voltage (DVDD)		2.7		5.25	*		*	V
Supply Current								
Total Analog Current			21			28		mA
Total Digital Current	DVDD = +3V		1			1.34		mA
Total Power Dissipation	DVDD = +3V		108	150		144	200	mW
Total Power Dissipation per Channel	DVDD = +3V		13.5	18.75		18	25	mW

(1) * indicates that specification is the same as Low-Power Mode.
(2) Exceeding maximum input current specification may damage device.
(3) Input is less than 1% of full scale.
(4) C_{SENSOR} is the capacitance seen at the DDC118 inputs from wiring, photodiode, etc.
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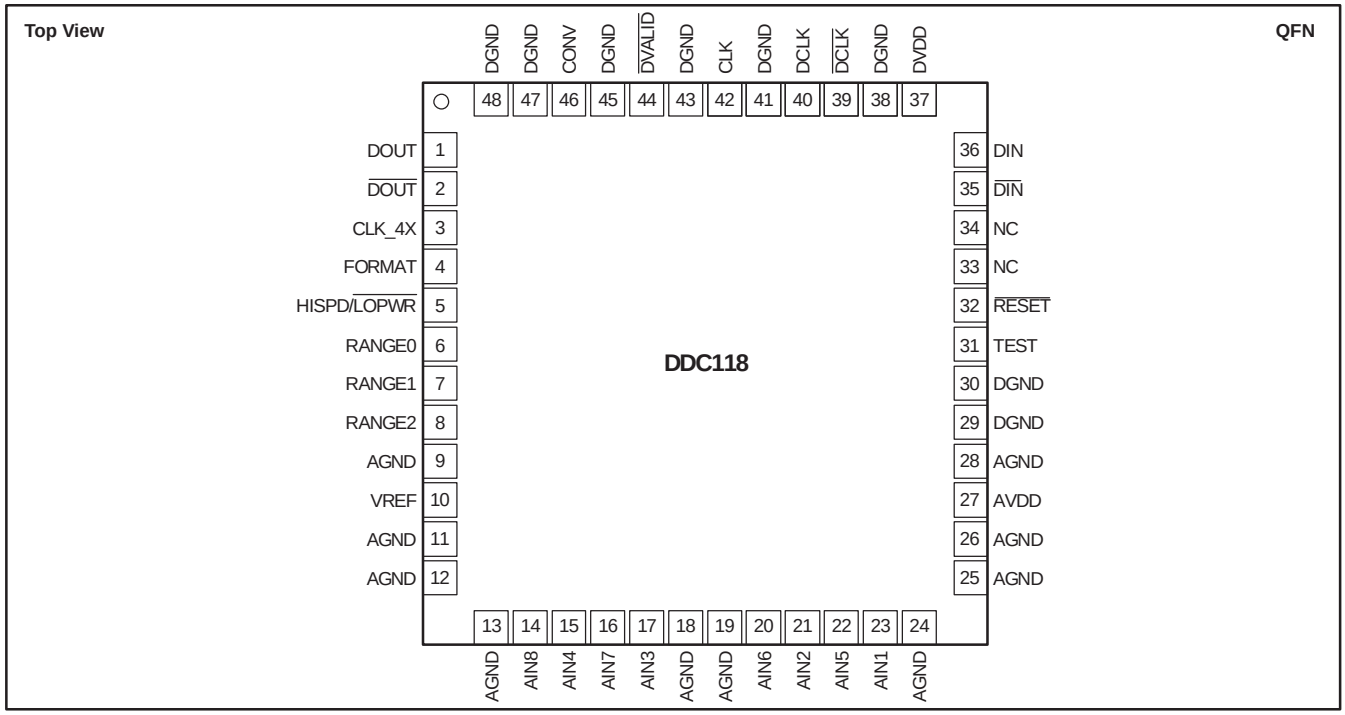
PIN CONFIGURATION



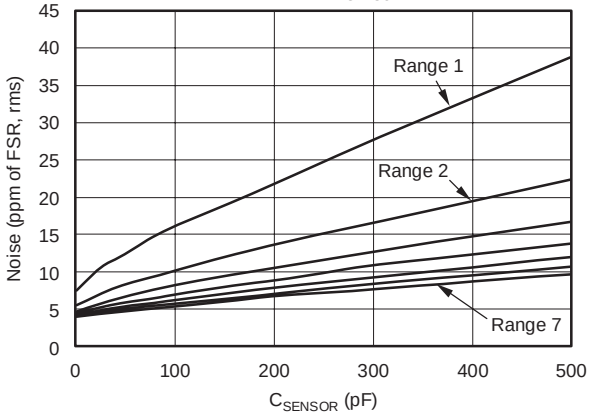
PIN DESCRIPTIONS

PIN	NUMBER	FUNCTION	DESCRIPTION
DOUT	1	Digital Output	Serial Data Output
$\overline{\text{DOUT}}$	2	Digital Output	Serial Data Output: Complementary Signal (optional, see text on page 13)
CLK_4X	3	Digital Input	Master Clock Divider Control: 0 = divide by 1, 1 = divide by 4
FORMAT	4	Digital Input	Digital Output Word Format: 0 = 16 Bits, 1 = 20 Bits
HISPD/$\overline{\text{LOPWR}}$	5	Digital Input	Mode Control: 0 = Low-Power, 1 = High-Speed
RANGE0	6	Digital Input	Range Control 0 (least significant bit)
RANGE1	7	Digital Input	Range Control 1
RANGE2	8	Digital Input	Range Control 2 (most significant bit)
AGND	9, 11-13, 18, 19, 24-26, 28	Analog	Analog Ground
VREF	10	Analog Input	External Voltage Reference Input, 4.096V Nominal
AIN8	14	Analog Input	Analog Input 8
AIN7	16	Analog Input	Analog Input 7
AIN6	20	Analog Input	Analog Input 6
AIN5	22	Analog Input	Analog Input 5
AIN4	15	Analog Input	Analog Input 4
AIN3	17	Analog Input	Analog Input 3
AIN2	21	Analog Input	Analog Input 2
AIN1	23	Analog Input	Analog Input 1
AVDD	27	Analog	Analog Power Supply, 5V Nominal
DGND	29, 30, 38, 41, 43, 45, 47, 48	Digital	Digital Ground
TEST	31	Digital Input	Test Mode Control
$\overline{\text{RESET}}$	32	Digital Input	Resets the Digital Circuitry, Active Low
NC	33, 34	—	No connection. These pins must be left unconnected.
$\overline{\text{DIN}}$	35	Digital Input	Serial Data Input: Complementary Signal (optional, see text on page 13)
DIN	36	Digital Input	Serial Data Input
DVDD	37	Digital	Digital Power Supply, 3V Nominal
$\overline{\text{DCLK}}$	39	Digital Input	Serial Data Clock Input: Complementary Signal (optional, see text on page 13)
DCLK	40	Digital Input	Serial Data Clock Input
CLK	42	Digital Input	Master Clock Input
$\overline{\text{DVALID}}$	44	Digital Output	Data Valid Output, Active Low
CONV	46	Digital Input	Conversion Control Input: 0 = Integrate on Side B, 1 = Integrate on Side A

TYPICAL CHARACTERISTICS

At T_A = +25°C, characterization done with Range 5 (250pC), AVDD = +5V, DVDD = 3V, VREF = +4.096V, and Low-Power Mode: T_{INT} = 400µs and CLK = 4MHz, unless otherwise noted.

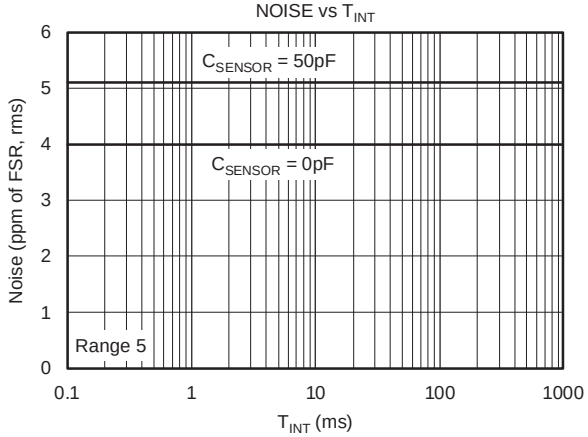
NOISE vs C_{SENSOR}



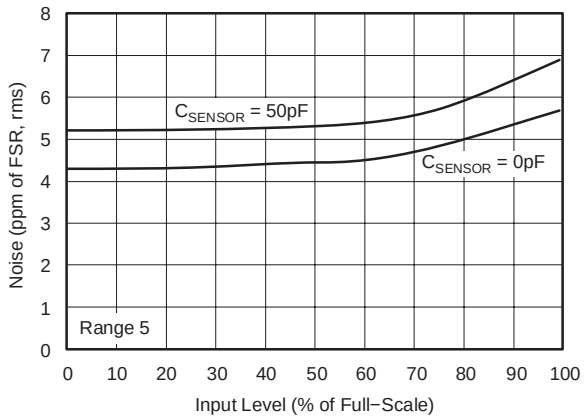
NOISE vs C_{SENSOR}

C_{SENSOR} (pF)	Noise (ppm of FSR, rms)							
	Range 0	Range 1	Range 2	Range 3	Range 4	Range 5	Range 6	Range 7
0	23.6	7.3	5.2	4.4	4.2	4.0	3.8	3.7
24	30.8	10.4	6.7	5.5	4.9	4.5	4.3	4.1
50	36.3	12.3	8.2	6.5	5.6	5.1	4.8	4.4
75	41.3	14.4	8.9	7.2	6.0	5.4	5.1	4.7
100	46.1	16.0	10.0	8.0	6.7	5.9	5.4	5.0
150	57.0	18.8	11.9	9.2	7.8	6.8	6.1	5.7
200	68.1	21.7	13.5	10.2	8.6	7.6	6.8	6.4
300	89.3	27.7	16.3	12.5	10.6	9.0	8.1	7.4
500	134.0	38.9	22.4	16.6	13.5	11.7	10.4	9.5

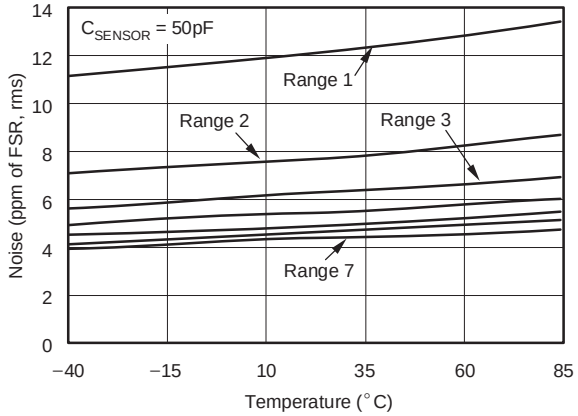
NOISE vs T_{INT}



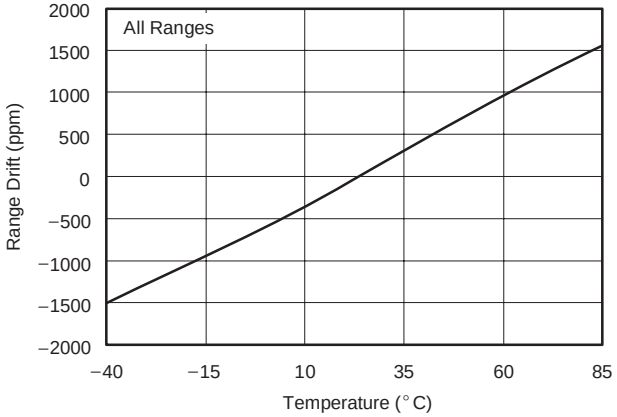
NOISE vs INPUT LEVEL



NOISE vs TEMPERATURE



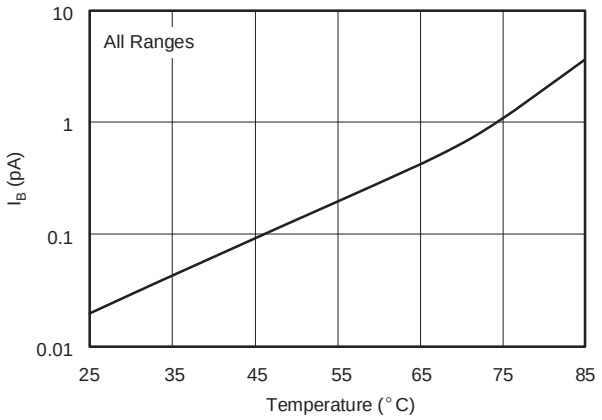
RANGE DRIFT vs TEMPERATURE



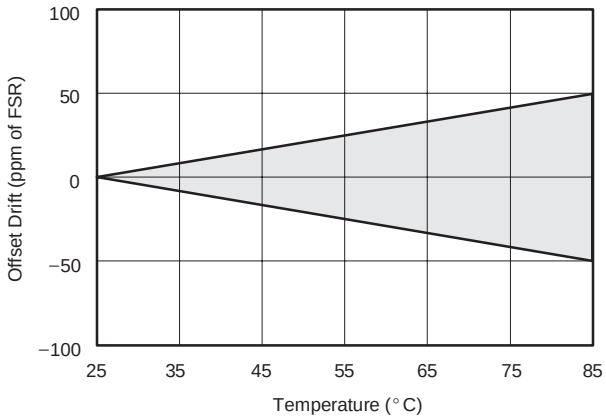
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, characterization done with Range 5 (250pC), AVDD = +5V, DVDD = 3V, VREF = +4.096V, and Low-Power Mode: T_{INT} = 400µs and CLK = 4MHz, unless otherwise noted.

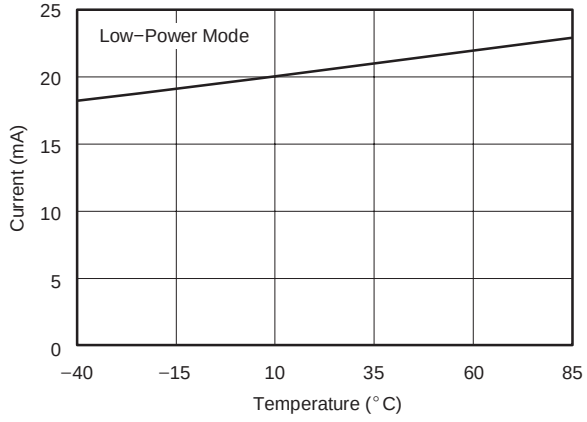
I_B vs TEMPERATURE



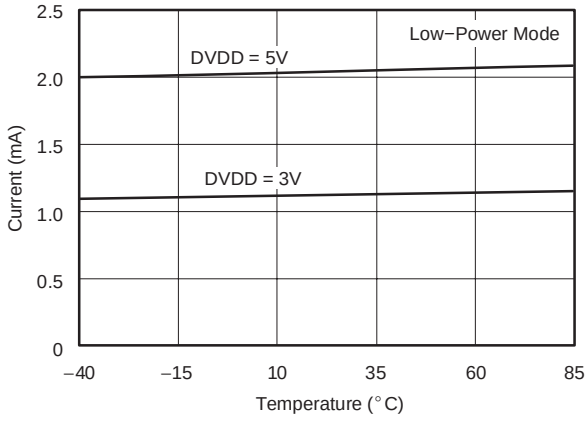
OFFSET DRIFT vs TEMPERATURE



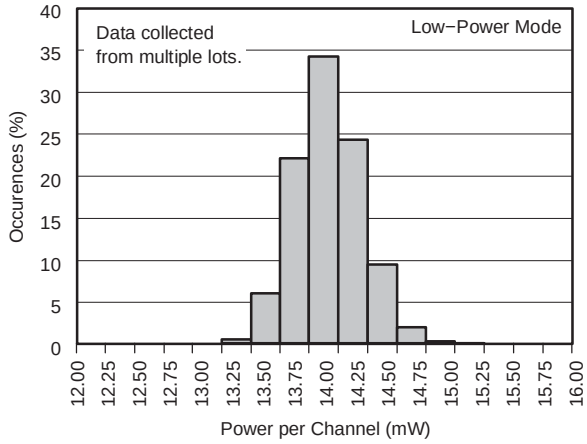
ANALOG SUPPLY CURRENT vs TEMPERATURE



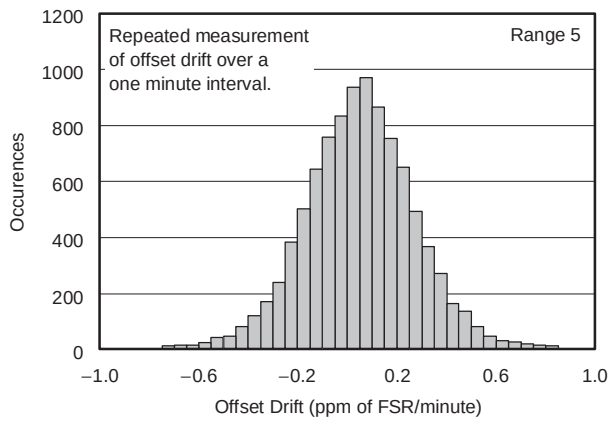
DIGITAL SUPPLY CURRENT vs TEMPERATURE



POWER CONSUMPTION HISTOGRAM



OFFSET DRIFT HISTOGRAM AT ROOM TEMPERATURE



THEORY OF OPERATION

The block diagram of the DDC118 is shown in Figure 1. The device contains eight identical input channels that perform the function of current-to-voltage integration followed by a multiplexed A/D conversion. Each input has two integrators so that the current-to-voltage integration can be continuous in time. The output of the sixteen integrators are switched to four delta-sigma (ΔΣ) converters via four four-input multiplexers. With the DDC118 in the continuous integration mode, the output of the integrators from one side of the inputs will be digitized while the other eight integrators are in the integration mode, as illustrated in the timing diagram in Figure 2. This integration and A/D conversion process is controlled by the system clock, CLK. The results from side A and side B of each signal input are stored in a serial output shift register. The $\overline{\text{DVALID}}$ output goes low when the shift register contains valid data.

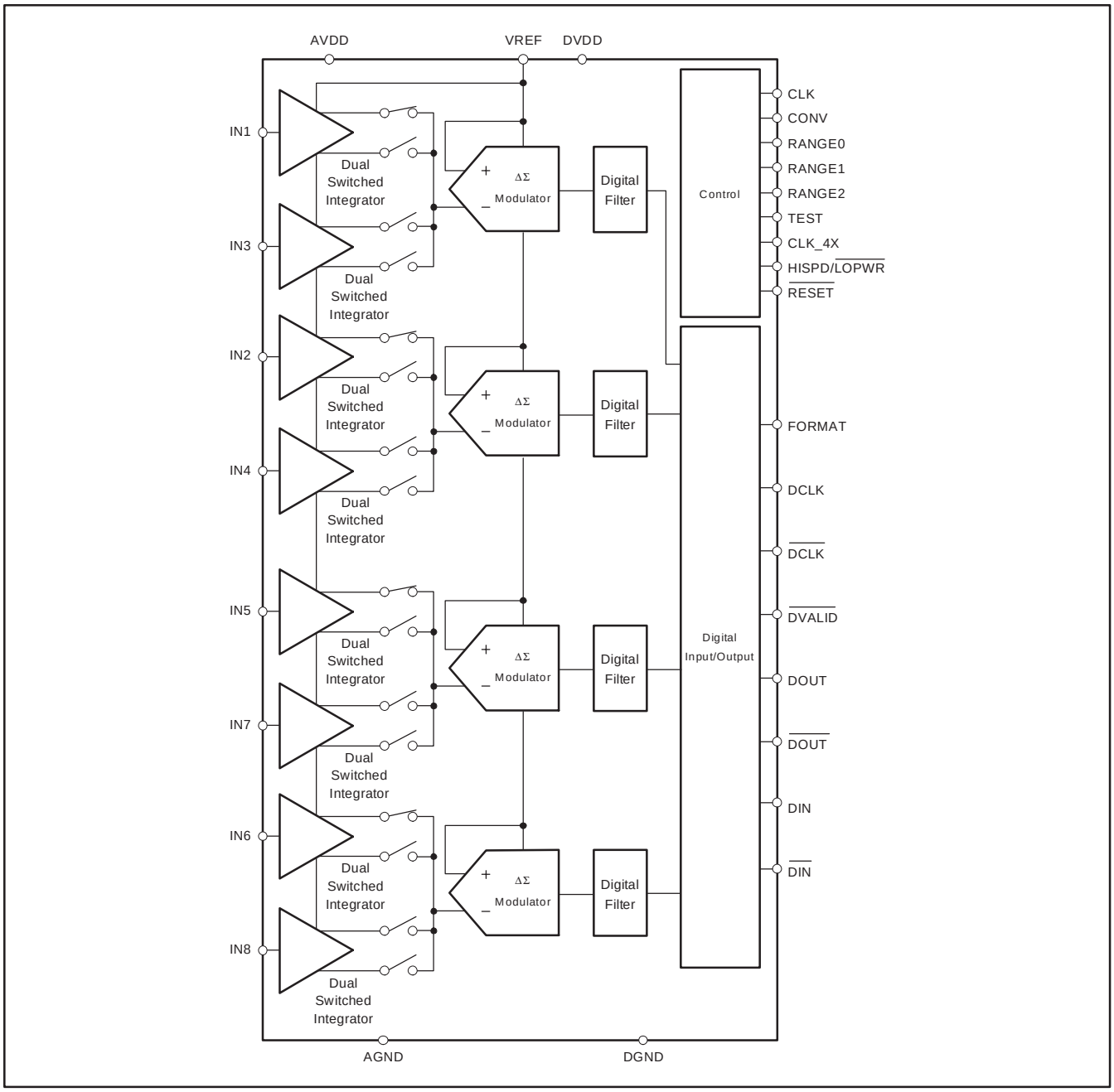


Figure 1. DDC118 Block Diagram

The digital interface of the DDC118 provides the digital results via a synchronous serial interface consisting of differential data clocks (DCLK and $\overline{\text{DCLK}}$), a valid data pin ($\overline{\text{DVALID}}$), differential serial data output pins (DOUT and $\overline{\text{DOUT}}$), and differential serial data input pins (DIN and $\overline{\text{DIN}}$). The DDC118 contains only four A/D converters, so the conversion process is interleaved (see Figure 2). The integration and conversion process is fundamentally independent of the data retrieval process. Consequently, the CLK frequency and DCLK frequencies need not be the same. DIN and $\overline{\text{DIN}}$ are only used when multiple converters are cascaded and should be tied to DGND and DVDD otherwise.

DEVICE OPERATION

Basic Integration Cycle

The topology of the front end of the DDC118 is an analog integrator as shown in Figure 3. In this diagram, only Input IN1 is shown. This representation of the input stage consists of an operational amplifier, a selectable feedback capacitor network (C_F), and several switches that implement the integration cycle. The timing relationships of all of the switches shown in Figure 3 are illustrated in Figure 4. Figure 4 is used to conceptualize the operation of the integrator input stage of the DDC118 and should not be used as an exact timing tool for design. See Figure 5 for the block diagrams of the reset, integrate, wait and convert states of the integrator section of the DDC118. This internal switching network is controlled externally with the convert pin (CONV), range selection pins (RANGE0-RANGE2), and the system clock (CLK). For the best noise performance, CONV must be synchronized with the rising edge of CLK. It is recommended that CONV toggle within ±10ns of the rising edge of CLK.

The noninverting inputs of the integrators are connected to ground. Consequently, the DDC118 analog ground should be as clean as possible. The range switches, along with the internal and external capacitors (C_F), are shown in parallel between the inverting input and output of the operational amplifier. At the beginning of a conversion, the switches $S_{A/D}$, S_{INTA}, S_{INTB}, S_{REF1}, S_{REF2}, and S_{RESET} are set (see Figure 4).

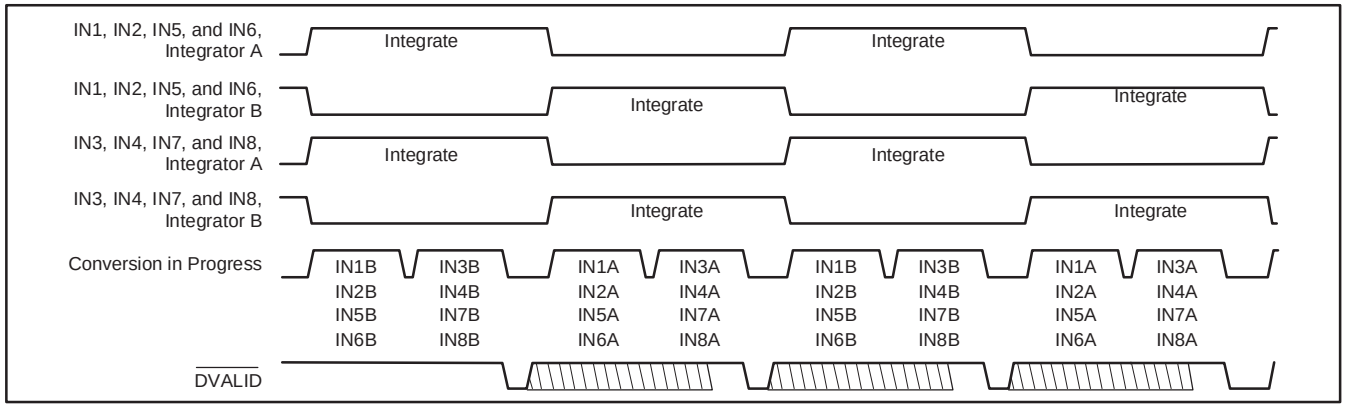


Figure 2. Basic Integration and Conversion Timing for the DDC118 (continuous mode)

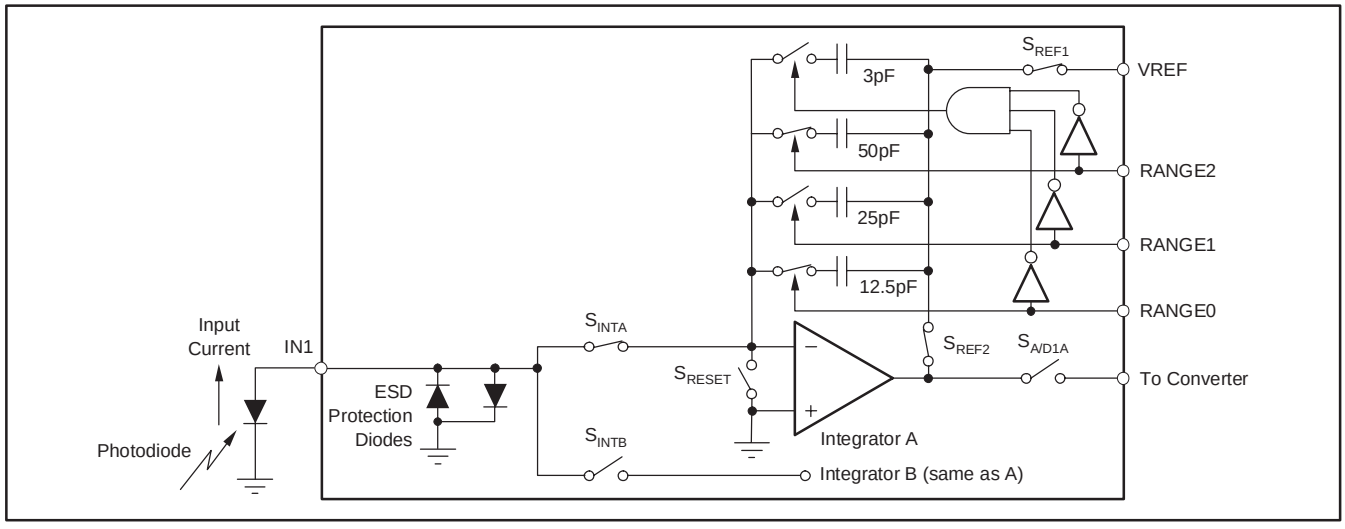


Figure 3. Basic Integration Configuration for Input 1, shown with a 250pC (C_F = 62.5pF) Input Range

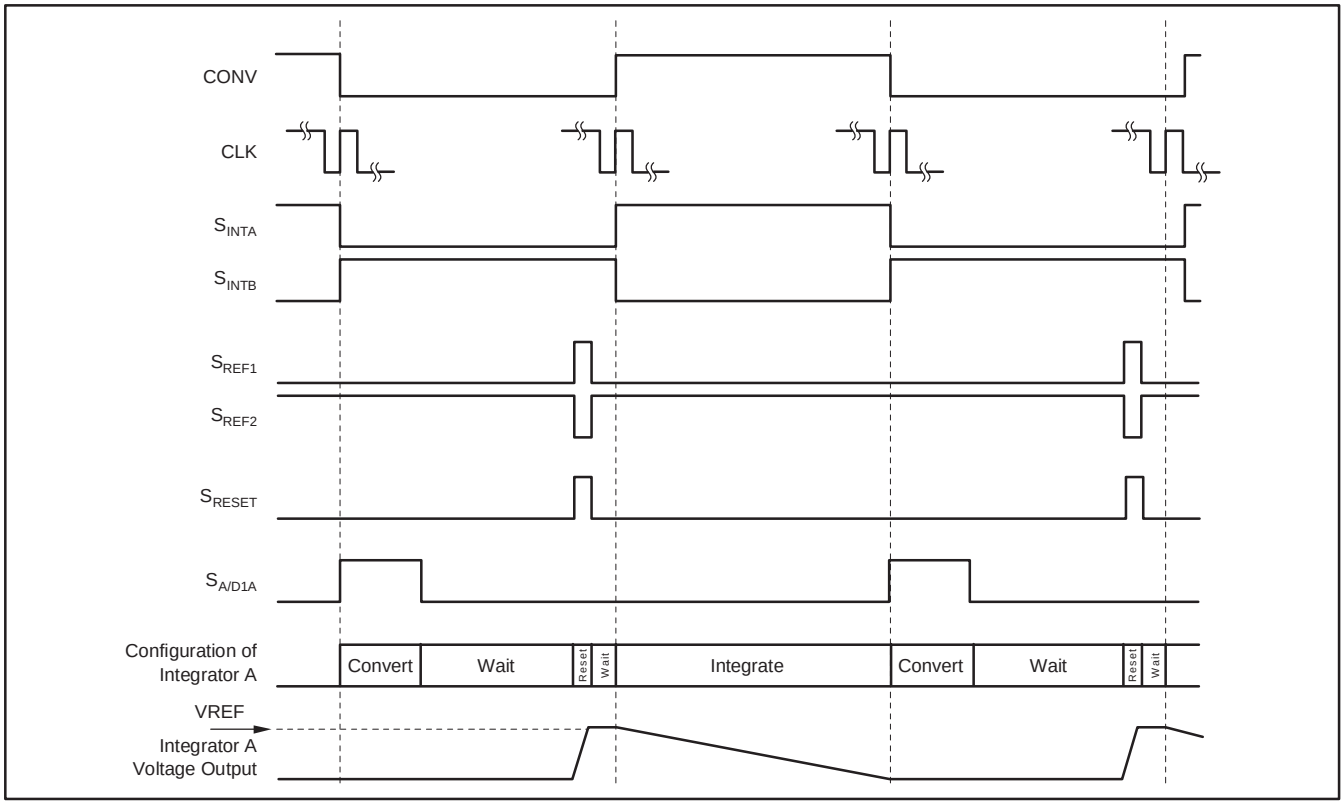


Figure 4. Basic Integration Timing Diagram (as shown in Figure 3)

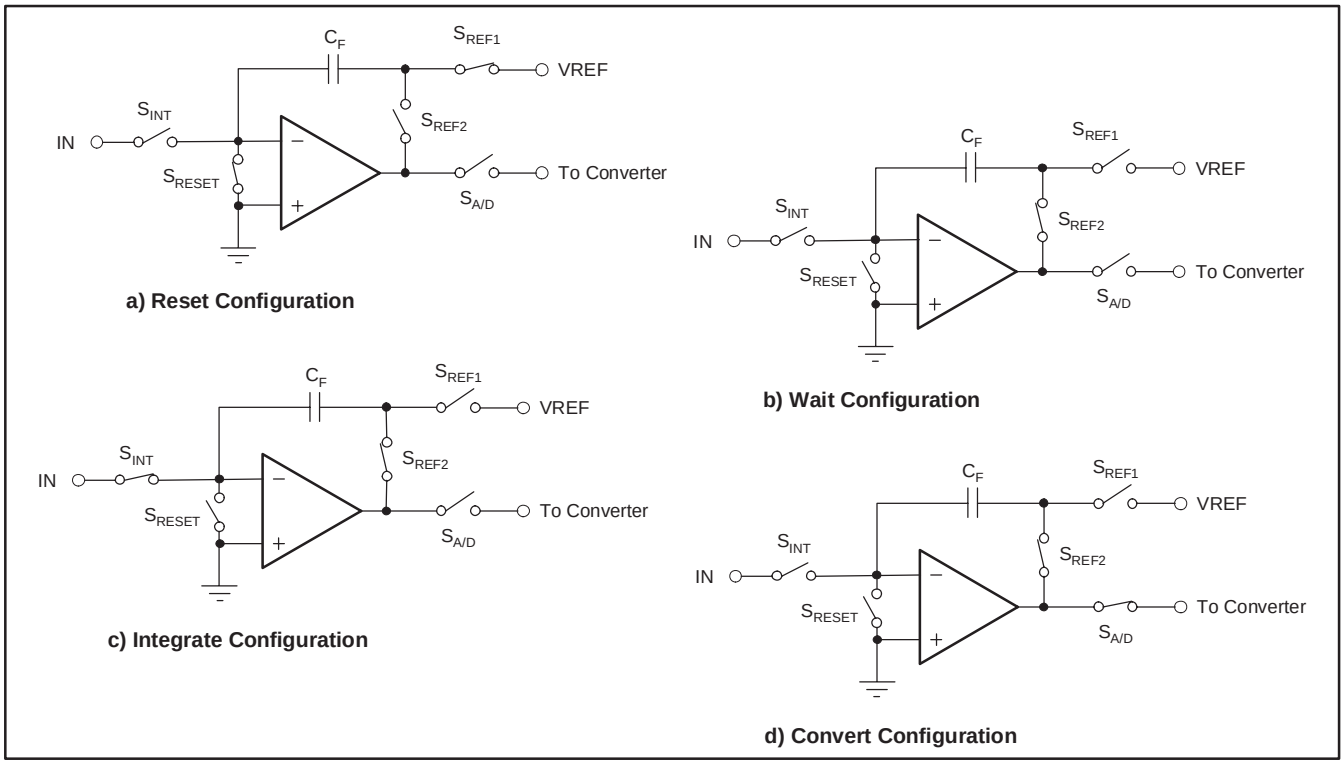


Figure 5. Diagrams for the Four Configurations of the Front End Integrators of the DDC118

At the completion of an A/D conversion, the charge on the integration capacitor (C_F) is reset with S_{REF1} and S_{RESET} (see Figure 4 and Figure 5a). In this manner, the selected capacitor is charged to the reference voltage, VREF. Once the integration capacitor is charged, S_{REF1} and S_{RESET} are switched so that VREF is no longer connected to the amplifier circuit while it waits to begin integrating (see Figure 5b). With the rising edge of CONV, S_{INTA} closes, which begins the integration of side A. This process puts the integrator stage into its integrate mode (see Figure 5c).

Charge from the input signal is collected on the integration capacitor, causing the voltage output of the amplifier to decrease. The falling edge of CONV stops the integration by switching the input signal from side A to side B (S_{INTA} and S_{INTB}). Prior to the falling edge of CONV, the signal on side B was converted by the A/D converter and reset during the time that side A was integrating. With the falling edge of CONV, side B starts integrating the input signal. Now the output voltage of the side A operational amplifier is presented to the input of the ΔΣ A/D converter (see Figure 5d).

Integration Capacitors

There are eight different capacitors available on-chip for both sides of every channel in the DDC118. These internal capacitors are trimmed in production to achieve the specified performance for range error of the DDC118. The range control pins (RANGE0-RANGE2) change the capacitor value for all four integrators. Consequently, all inputs and both sides of each input will always have the same full-scale range. Table 1 shows the capacitor value selected for each range selection.

Table 1. Range Selection of the DDC118

RANGE2	RANGE1	RANGE0	C_F (pF, typ)	INPUT RANGE (pC, typ)
0	0	0	3	−0.048 to 12
0	0	1	12.5	–0.2 to 50
0	1	0	25	–0.4 to 100
0	1	1	37.5	–0.6 to 150
1	0	0	50	–0.8 to 200
1	0	1	62.5	–0.1 to 250
1	1	0	75	–1.2 to 300
1	1	1	87.5	–1.4 to 350

Voltage Reference

The external voltage reference is used to reset the integration capacitors before an integration cycle begins. It is also used by the ΔΣ converter while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling, the external reference must supply the charge needed by the ΔΣ converter. For an integration time of 400μs, this charge translates to an average VREF current of approximately 150μA. The amount of charge needed by the ΔΣ converter is independent of the integration time; therefore, increasing the integration time lowers the average current. For example, an integration time of 800μs lowers the average VREF current to 75μA.

It is critical that VREF be stable during the different modes of operation (see Figure 5). The ΔΣ converter measures the voltage on the integrator with respect to VREF. Since the integrator capacitors are initially reset to VREF, any drop in VREF from the time the capacitors are reset to the time when the converter measures the integrator output will introduce an offset. It is also important that VREF be stable over longer periods of time because changes in VREF correspond directly to changes in the full-scale range. Finally, VREF should introduce as little additional noise as possible.

For these reasons, it is strongly recommended that the external reference source be buffered with an operational amplifier, as shown in Figure 6. In this circuit, the voltage reference is generated by a 4.096V reference. A low-pass filter to reduce noise connects the reference to an operational amplifier configured as a buffer. This amplifier should have low noise, and input/output common-mode ranges that support VREF. Following the buffer are capacitors placed close to the DDC118 VREF pin. Even though the circuit in Figure 6 might appear to be unstable because of the large output capacitors, it works well for most operational amplifiers. It is NOT recommended that series resistance be placed in the output lead to improve stability since this can cause a drop in VREF, which producing large offsets.

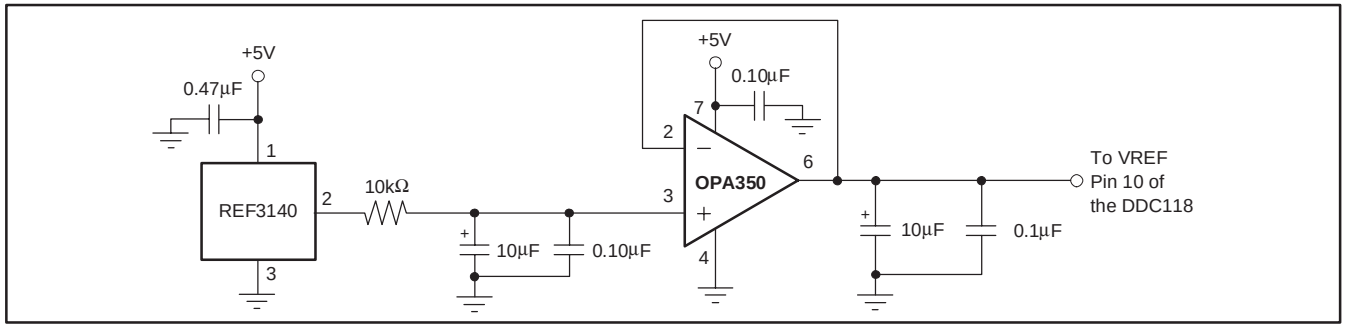


Figure 6. Recommended External Voltage Reference Circuit for Best Low-Noise Operation with the DDC118

DDC118 Frequency Response

The frequency response of the DDC118 is set by the front end integrators and is that of a traditional continuous time integrator, as shown in Figure 7. By adjusting T_{INT}, the user can change the 3dB bandwidth and the location of the notches in the response. The frequency response of the ΔΣ converter that follows the front end integrator is of no consequence because the converter samples a held signal from the integrators. That is, the input to the ΔΣ converter is always a DC signal. Since the output of the front end integrators are sampled, aliasing can occur. Whenever the frequency of the input signal exceeds one-half of the sampling rate, the signal will fold back down to lower frequencies.

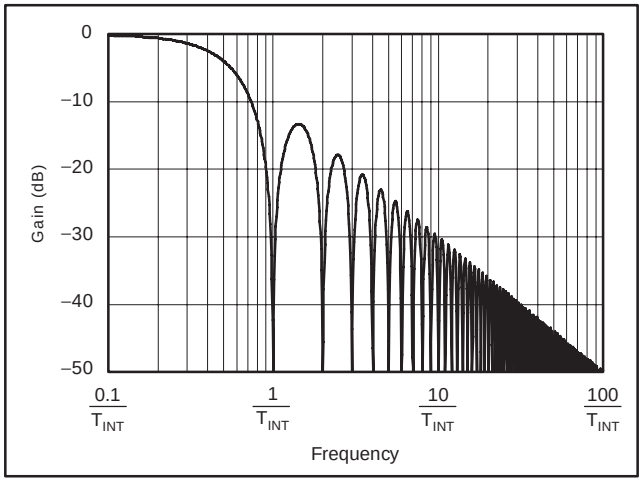


Figure 7. Frequency Response of the DDC118

Test Mode

When Test Mode is used, the inputs (IN1, IN2, IN3, IN4, IN5, IN6, IN7, and IN8) are disconnected from the DDC118 integrators to enable the user to measure a zero input signal regardless of the current supplied to the inputs. In addition, packets of charge can be transferred to the integrators in 11pC intervals to measure non-zero values. The test mode works with both the continuous and non-continuous modes. The timing diagram for the test mode is shown in Figure 8 with the timing specifications given in Table 2.

To enter Test Mode, hold TEST high while CONV transitions. If TEST is held high during the entire integration period, the integrators measure a zero value. This mode can be used to help debug a design or perform diagnostic tests. To apply packets of charge during Test Mode, simply strobe TEST low then high before the next CONV transition. Each rising edge of TEST causes approximately 11pC of charge to be transferred to the integrators. This charge transfer is independent of the integration time. Data retrieval during Test Mode is identical to normal operation. To exit Test Mode, take TEST low and allow several cycles after exiting before using the data.

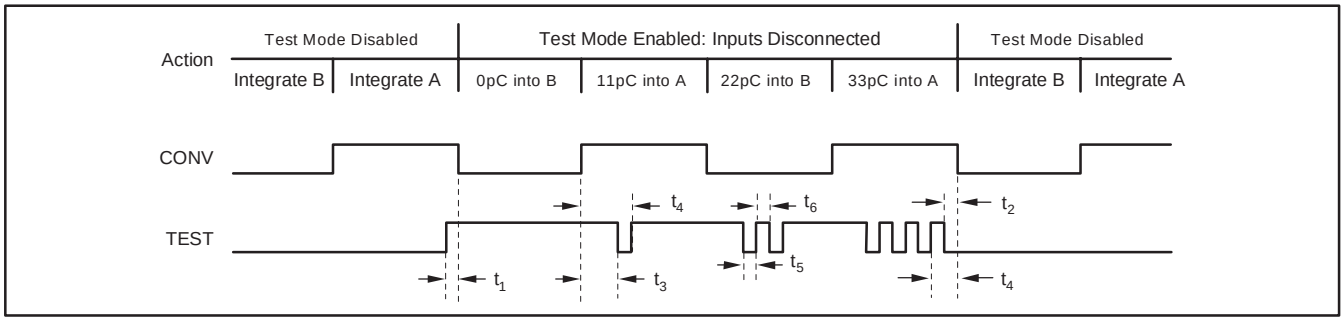


Figure 8. Timing Diagram of the Test Mode of the DDC118

Table 2. Timing for the DDC118 in the Test Mode

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Setup Time for Test Mode Enable	100			ns
t_2	Setup Time for Test Mode Disable	100			ns
t_3	Hold Time for Test Mode Enable	100			ns
t_4	From Rising Edge of TEST to the Edge of CONV while Test Mode Enabled	1			µs
t_5	Falling Edge to Rising Edge of TEST	1			µs
t_6	Rising Edge to Falling Edge of TEST	1			µs

DIGITAL INTERFACE

The digital interface of the DDC118 provides the digital results via a synchronous serial interface consisting of differential data clocks (DCLK and $\overline{\text{DCLK}}$), a valid data pin ($\overline{\text{DVALID}}$), differential serial data output pins (DOUT and $\overline{\text{DOUT}}$), and differential serial data input pins (DIN and $\overline{\text{DIN}}$). The DDC118 contains only four A/D converters, so the conversion process is interleaved (see Figure 2, page 9). The integration and conversion processes are independent of the data retrieval process. Consequently, the CLK frequency and DCLK frequencies need not be the same. DIN and $\overline{\text{DIN}}$ are used when multiple converters are cascaded. Cascading or *daisy-chaining* greatly simplifies the interconnection and routing of the digital outputs in cases where a large number of converters are needed. Refer to the *Cascading Multiple Converters* section of this data sheet for more detail.

Complementary Signals ($\overline{\text{DCLK}}$, $\overline{\text{DIN}}$, and $\overline{\text{DOUT}}$)

The DDC118 provides optional complementary inputs ($\overline{\text{DCLK}}$, $\overline{\text{DIN}}$) to help reduce digital coupling to the analog inputs. If using these inputs, connect a complementary signal to each. If these inputs are not connected on the DDC118, they should be tied to DGND. $\overline{\text{DOUT}}$ is a complementary output designed to drive $\overline{\text{DIN}}$. If not using $\overline{\text{DOUT}}$, leave it floating.

System and Data Clocks (CLK and CONV)

The system clock is supplied to CLK and the data clock is supplied to DCLK. Make sure the clock signals are clean—avoid overshoot or ringing. For best performance, generate both clocks from the same clock source. DCLK should be disabled by taking it low after the data has been shifted out or while CONV is transitioning.

When using multiple DDC118s, pay close attention to the DCLK distribution on the printed circuit board (PCB). In particular, make sure to minimize skew in the DCLK signal as this can lead to timing violations in the serial interface specifications. See the *Cascading Multiple Converters* section for more details.

System Clock Divider (CLK_4X)

The CLK_4X input enables an internal divider on the system clock as shown in Table 3. When CLK_4X = 1, the system clock is divided by four. This allows a 4X faster system clock, which in turn provides a finer quantization of the integration time as the CONV signal needs to be synchronized with the system clock for the best performance.

Table 3. CLK_4X Pin Operation

CLK_4X PIN	CLK DIVIDER VALUE	TYPICAL CLK FREQUENCY	INTERNAL CLOCK FREQUENCY
0	1	4MHz	4MHz
1	4	16MHz	4MHz

High-Speed and Low-Power Modes (HISPD/$\overline{\text{LOPWR}}$)

The HISPD/$\overline{\text{LOPWR}}$ input controls the power dissipation and in turn, the maximum allowable CLK frequency and data rate, as shown in Table 4. With HISPD/$\overline{\text{LOPWR}}$ = 0, the Low-Power Mode is selected with a typical 13.5mW/channel and a maximum data rate of 2.5kSPS. Setting HISPD/$\overline{\text{LOPWR}}$ = 1 selects the High-Speed Mode, which supports a maximum data rate of 3.125kSPS with a corresponding typical power of 18.0mW/channel.

Table 4. HISPD/$\overline{\text{LOPWR}}$ Pin Operation

HISPD/$\overline{\text{LOPWR}}$	MODE	TYPICAL POWER/CHANNEL	MAXIMUM CLK FREQUENCY (CLK_4X = 0)	MAXIMUM DATA RATE
0	Low-Power	13.5mW/ch	4.0MHz	2.5kSPS
1	High-Speed	18.0mW/ch	4.8MHz	3.125kSPS

Data Valid ($\overline{\text{DVALID}}$)

The $\overline{\text{DVALID}}$ signal indicates that data is ready. Data retrieval may begin after $\overline{\text{DVALID}}$ goes low. This signal is generated using an internal clock divided down from the system clock CLK. The phase relationship between this internal clock and CLK is set when power is first applied and is random. Since the user must synchronize CONV with CLK, the $\overline{\text{DVALID}}$ signal will have a random phase relationship with CONV. This uncertainty is $\pm$ 1/f_{CLK}. Polling $\overline{\text{DVALID}}$ eliminates any concern about this relationship. If data read back is timed from CONV, wait the maximum value of t_7 or t_8 to insure data is valid.

Reset ($\overline{\text{RESET}}$)

The DDC118 is reset asynchronously by taking the $\overline{\text{RESET}}$ input low, as shown in Figure 9. Make sure the reset pulse is at least 50µs wide. After resetting the DDC118, wait at least four conversions before using the data. It is very important to make sure the $\overline{\text{RESET}}$ is glitch free to avoid unintended resets. The $\overline{\text{RESET}}$ pin is used during power-up; see the *Power-Up Sequence* section for more details.

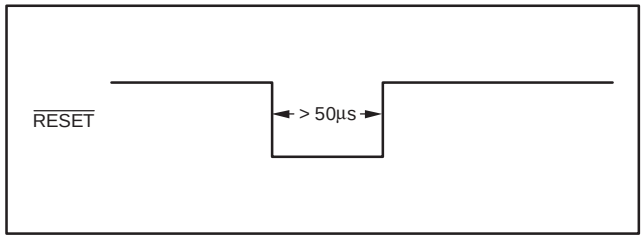


Figure 9. Reset Timing

Convert (CONV)

CONV controls the integration time (T_{INT}). For optimum analog performance, make sure CONV is synchronized to CLK.

This recommendation implies that while SPEED is low, T_{INT} needs to be adjusted in steps of 250ns if CLK_4X is low and CLK = 4MHz. If CLK_4X is high and CLK = 16MHz, this allows T_{INT} to be adjusted in steps of 62.5ns.

Conversion Rate

The conversion rate of the DDC118 is set by a combination of the integration time (determined by the user) and the speed of the A/D conversion process. The A/D conversion time is primarily a function of the system clock (CLK) speed. One A/D conversion cycle encompasses the conversion of two signals (one side of each dual integrator feeding the modulator) and the reset time for each of the integrators involved in the two conversions. In most situations, the A/D conversion time is shorter than the integration time. If this condition exists, the DDC118 will operate in the continuous mode. When the DDC118 is in the continuous mode, the sensor output is continuously integrated by one of the two sides of each input.

In the event that the A/D conversion takes longer than the integration time, the DDC118 will switch into a non-continuous mode. In non-continuous mode, the A/D converter is not able to keep pace with the speed of the integration process. Consequently, the integration process is periodically halted until the digitizing process catches up. These two basic modes of operation for the DDC118—continuous and non-continuous modes—are described below.

Continuous and Non-Continuous Operational Modes

Figure 10 shows the state diagram of the DDC118. In all, there are eight states. Table 5 provides a brief explanation of each state.

Table 5. State Descriptions

STATE	MODE	DESCRIPTION
1	Ncont	Complete m/r/az of side A, then side B (if previous state is state 4). Initial power-up state when CONV is initially held HIGH.
2	Ncont	Prepare side A for integration.
3	Cont	Integrate on side A.
4	Cont	Integrate on side B; m/r/az on side A.
5	Cont	Integrate on side A; m/r/az on side B.
6	Cont	Integrate on side B.
7	Ncont	Prepare side B for integration.
8	Ncont	Complete m/r/az of side B, then side A (if previous state is state 5). Initial power-up state when CONV is initially held LOW.

Four signals are used to control progression around the state diagram: CONV, mbsy, and their complements. The state machine uses the level as opposed to the edges of CONV to control the progression. *mbsy* is an internally-generated signal not available to the user. It is active whenever a measurement/reset/auto-zero (m/r/az) cycle is in progress.

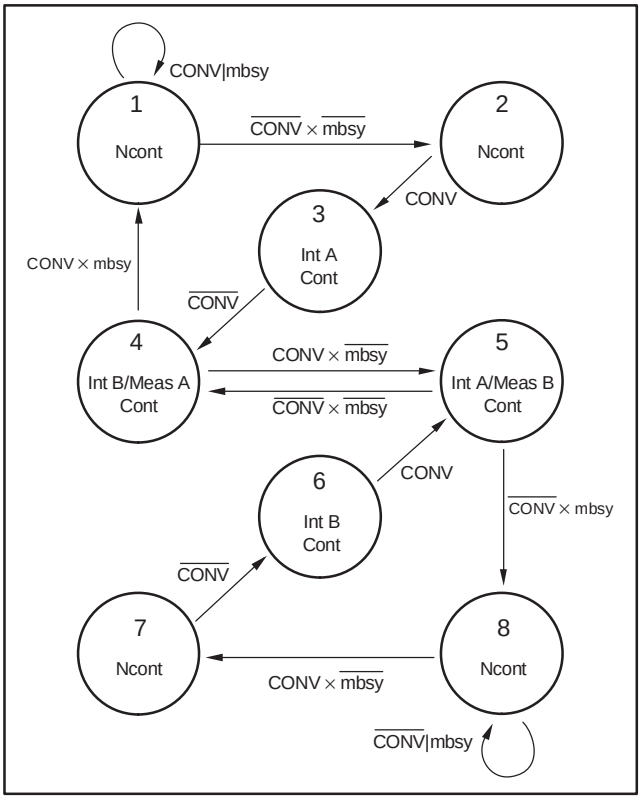


Figure 10. Integrate/Measure State Diagram

During the cont mode, mbsy is not active when CONV toggles. The non-integrating side is always ready to begin integrating when the other side finishes its integration. Consequently, monitoring the current status of CONV is all that is needed to know the current state. Cont mode operation corresponds to states 3-6. Two of the states, 3 and 6, only perform an integration (no m/r/az cycle).

mbsy becomes important when operating in the ncont mode, states 1, 2, 7, and 8. Whenever CONV is toggled while mbsy is active, the DDC118 will enter or remain in either ncont state 1 (or 8). After mbsy goes inactive, state 2 (or 7) is entered. This state prepares the appropriate side for integration. In the ncont states, the inputs to the DDC118 are grounded.

One interesting observation from the state diagram is that the integrations always alternate between sides A and B. This relationship holds for any CONV pattern and is independent of the mode. States 2 and 7 insure this relationship during the ncont mode.

When power is first applied to the DDC118, the beginning state is either 1 or 8, depending on the initial level of CONV. For CONV held high at power-up, the beginning state is 1. Conversely, for CONV held low at power-up, the beginning state is 8. In general, there is a symmetry in the state diagram between states 1-8, 2-7, 3-6, and 4-5. Inverting CONV results in the states progressing through their symmetrical match.

TIMING EXAMPLES

Cont Mode

A few timing diagrams help illustrate the operation of the state machine. These diagrams are shown in Figure 11 through Figure 19. Table 6 gives generalized timing specifications in units of CLK periods for CLK_4X = 0. If CLK_4X = 1, these values increase by a factor of four because of the internal clock divider. Values (in µs) for Table 6 can be easily found for a given CLK. For example, if CLK = 4MHz, then a CLK period = 0.25µs. t_6 in Table 6 would then be 367.50 ± 0.125µs.

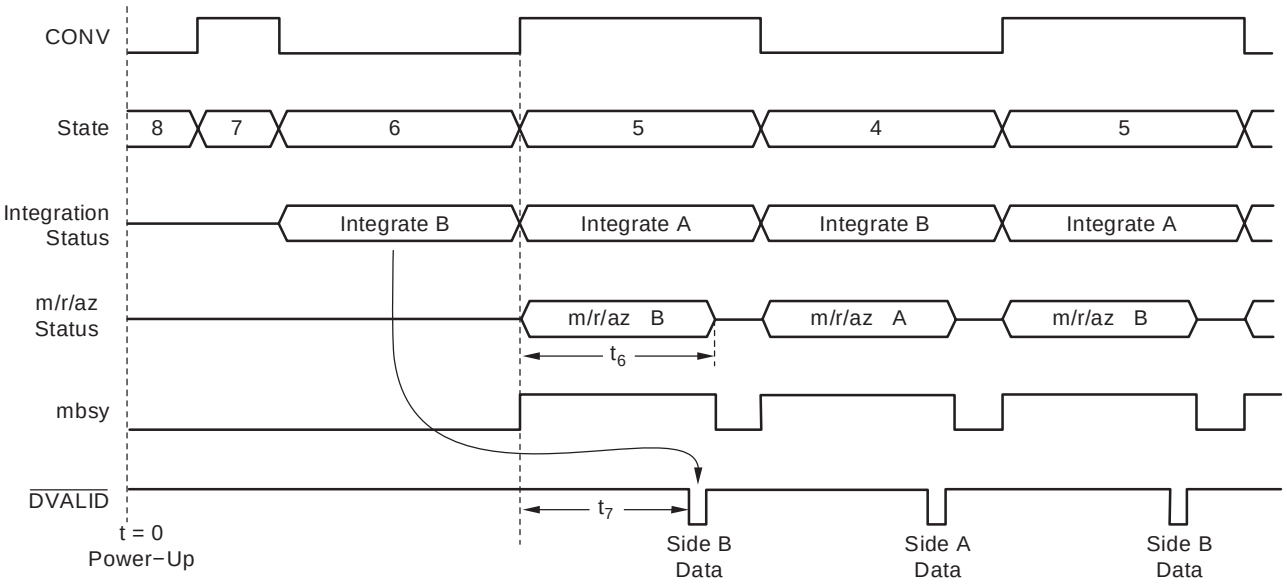
Table 6. Timing Specifications Generalized in CLK Periods

SYMBOL	DESCRIPTION	VALUE (CLK periods with CLK_4X = 0)
t_6	Cont mode m/r/az cycle	1470 ± 0.5
t_7	Cont mode data ready	1380 ± 0.5
t_8	1st ncont mode data ready	1379 ± 1
t_9	2nd ncont mode data ready	1450
t_{10}	Ncont mode m/r/az cycle	2901 ± 1

Figure 11 shows a few integration cycles beginning with initial power-up for a cont mode example. The top signal is CONV and is supplied by the user. The next line indicates the current state in the state diagram. The following two traces show when integrations and measurement cycles are underway. The internal signal mbsy is shown next. Finally, $\overline{\text{DVALID}}$ is given. $\overline{\text{DVALID}}$ goes active low when data is ready to be retrieved from the DDC118. It stays low until DCLK is taken high and then back low by the user. The text below the $\overline{\text{DVALID}}$ pulse indicates the side of the data available to be read, and arrows help match the data to the corresponding integration. The signals illustrated in Figure 11 through Figure 19 are drawn at approximately the same scale.

In Figure 11, the first state is ncont state 8. The DDC118 always powers up in the ncont mode. In this case, the first state is 8 because CONV is initially low. After the first two states, cont mode operation is reached and the states begin toggling between 4 and 5. From now on, the input is being continuously integrated, either on side A or side B. The time needed for the m/r/az cycle, or t_6, is the same time that determines the boundary between the cont and ncont modes described earlier in the Overview section. $\overline{\text{DVALID}}$ goes low after CONV toggles in time t_7, indicating that data is ready to be retrieved. As shown in Figure 11, there are two values for t_6 and t_7. The reason for this is discussed in the *Special Considerations* section.

See Figure 12 for the timing diagram of the internal operations occurring during continuous mode operation. Table 7 gives the timing specifications in the continuous mode.



SYMBOL	DESCRIPTION	VALUE (CLK = 4MHz, CLK_4X = 0)	VALUE (CLK = 4.8MHz, CLK_4X = 0)
t_6	Cont Mode m/r/az Cycle	367.50 ± 0.125µs	306.25 ± 0.104µs
t_7	Cont Mode Data Ready	345.00 ± 0.125µs	287.5 ± 0.104µs

Figure 11. Continuous Mode Timing

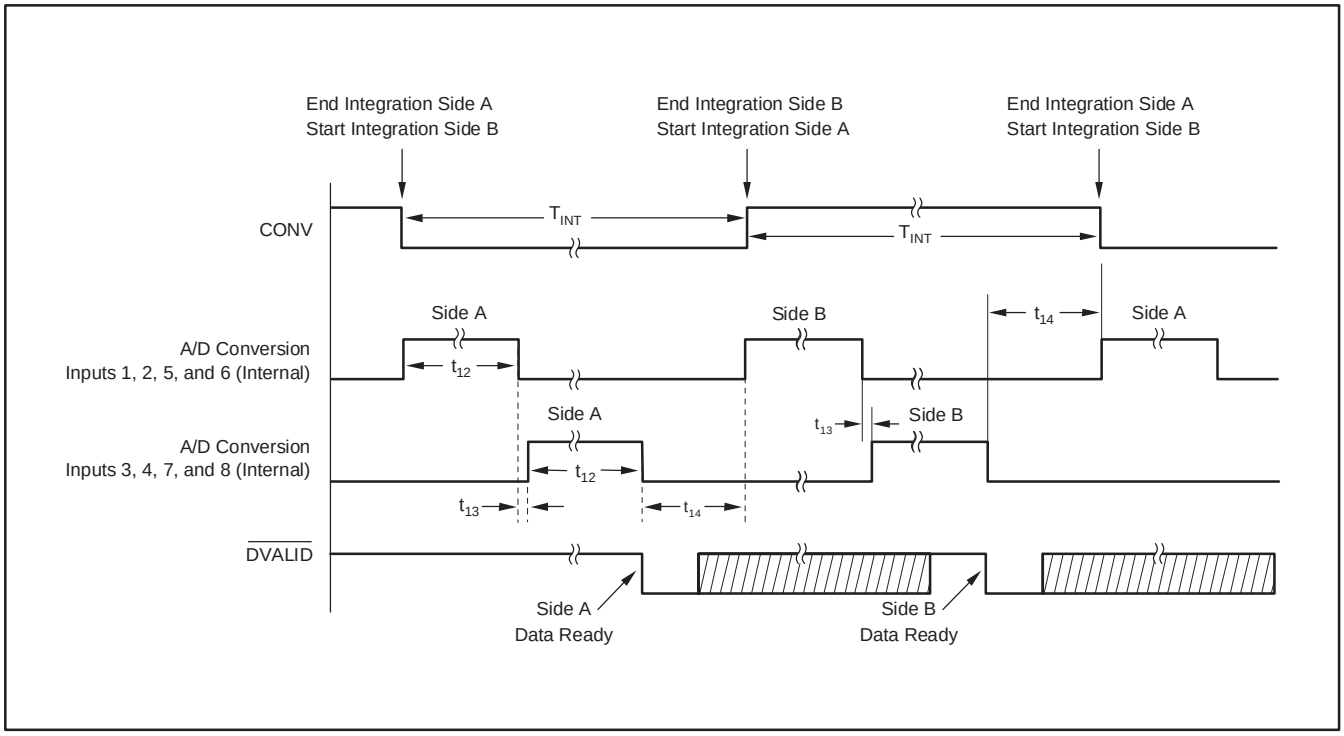


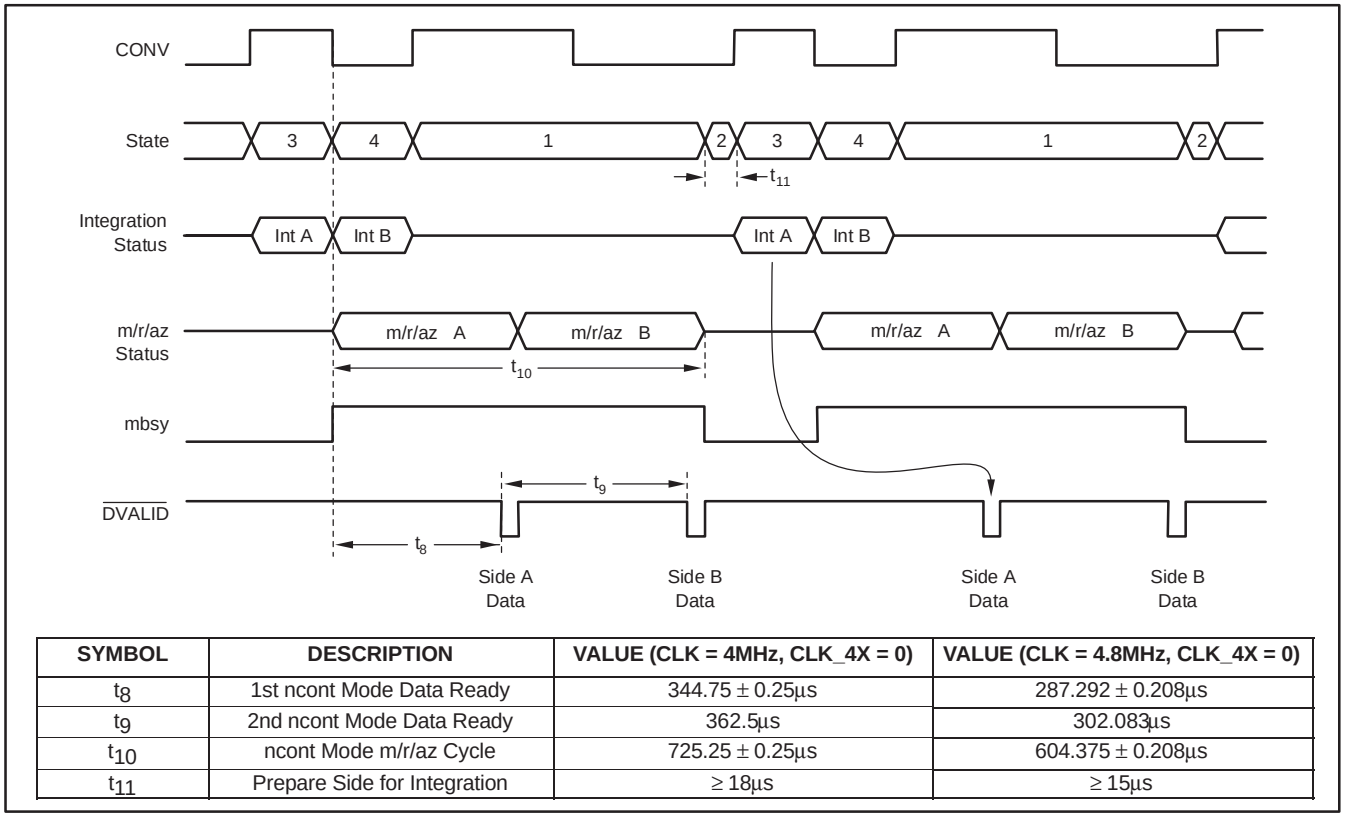
Figure 12. Timing Diagram of the Internal Operation in Continuous Mode of the DDC118

Table 7. Timing for the Internal Operation in Continuous Mode

SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
T_{INT}	Integration Period (continuous mode)	400		1,000,000	320		1,000,000	µs
t_{12}	A/D Conversion Time (internally controlled)		169.5			141.25		µs
t_{13}	A/D Conversion Reset Time (internally controlled)		4			3.333		µs
t_{14}	Integrator and A/D Conversion Reset Time (internally controlled)		23			19.167		µs

Ncont Mode

Non-continuous mode of operation is intended for Ranges 1 to 7. It is not recommended to use Range 0 when operating in non-continuous mode. Figure 13 illustrates operation in the ncont mode. The integrations come in pairs (that is, sides A/B or sides B/A) followed by a time during which no integrations occur. During that time, the previous integrations are being measured, reset and auto-zeroed. Before the DDC118 can advance to states 3 or 6, both sides A and B must be finished with the m/r/az cycle which takes time t_{10}. When the m/r/az cycles are completed, time t_{11} is needed to prepare the next side for integration. This time is required for the ncont mode because the m/r/az cycle of the ncont mode is slightly different from that of the cont mode. After the first integration ends, $\overline{\text{DVALID}}$ goes low in time t_8. This time is the same as in the cont mode. The second data will be ready in time t_9 after the first data is ready. One result of the naming convention used in this data sheet is that when the DDC118 is operating in the *ncont mode*, it passes through both *ncont mode states* and *cont mode states*. For example, in Figure 13, the state pattern is 3, 4, 1, 2, 3, 4, 1, 2, 3, 4 ... where 3 and 4 are cont mode states. *Ncont mode*, by definition, means that for some portion of the time, neither side A nor B is integrating. States that perform an integration are labeled *cont mode states*, while those that do not are called *ncont mode states*. Since integrations are performed in the ncont mode, just not continuously, some cont mode states must be used in a ncont mode state pattern.



SYMBOL	DESCRIPTION	VALUE (CLK = 4MHz, CLK_4X = 0)	VALUE (CLK = 4.8MHz, CLK_4X = 0)
t_8	1st ncont Mode Data Ready	344.75 ± 0.25µs	287.292 ± 0.208µs
t_9	2nd ncont Mode Data Ready	362.5µs	302.083µs
t_{10}	ncont Mode m/r/az Cycle	725.25 ± 0.25µs	604.375 ± 0.208µs
t_{11}	Prepare Side for Integration	≥ 18µs	≥ 15µs

Figure 13. Non-Continuous Mode Timing

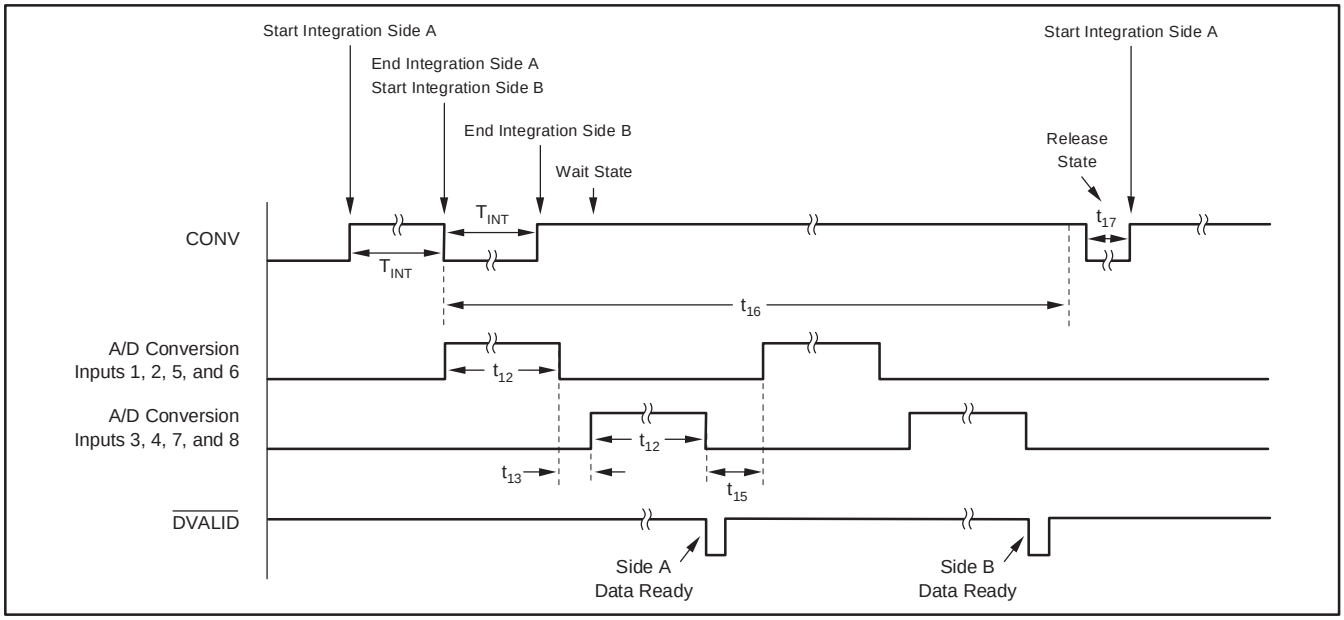


Figure 14. Conversion Detail for the Internal Operation of Non-Continuous Mode with Side A Integrated First

Table 8. Internal Timing for the DDC118 in Non-Continuous Mode

SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
T_{INT}	Integration Time (non-continuous mode)	400		1,000,000	320		1,000,000	µs
t_{12}	A/D Conversion Time (internally controlled)		169.5			141.25		µs
t_{13}	A/D Conversion Reset Time (internally controlled)		4			3.333		µs
t_{15}	Integrator and A/D Conversion Reset Time (internally controlled)		19.5			16.25		µs
t_{16}	Total A/D Conversion and Reset Time (internally controlled)	725.25 ± 0.25			604.375 ± 0.208			µs
t_{17}	Release Time	18			15			µs

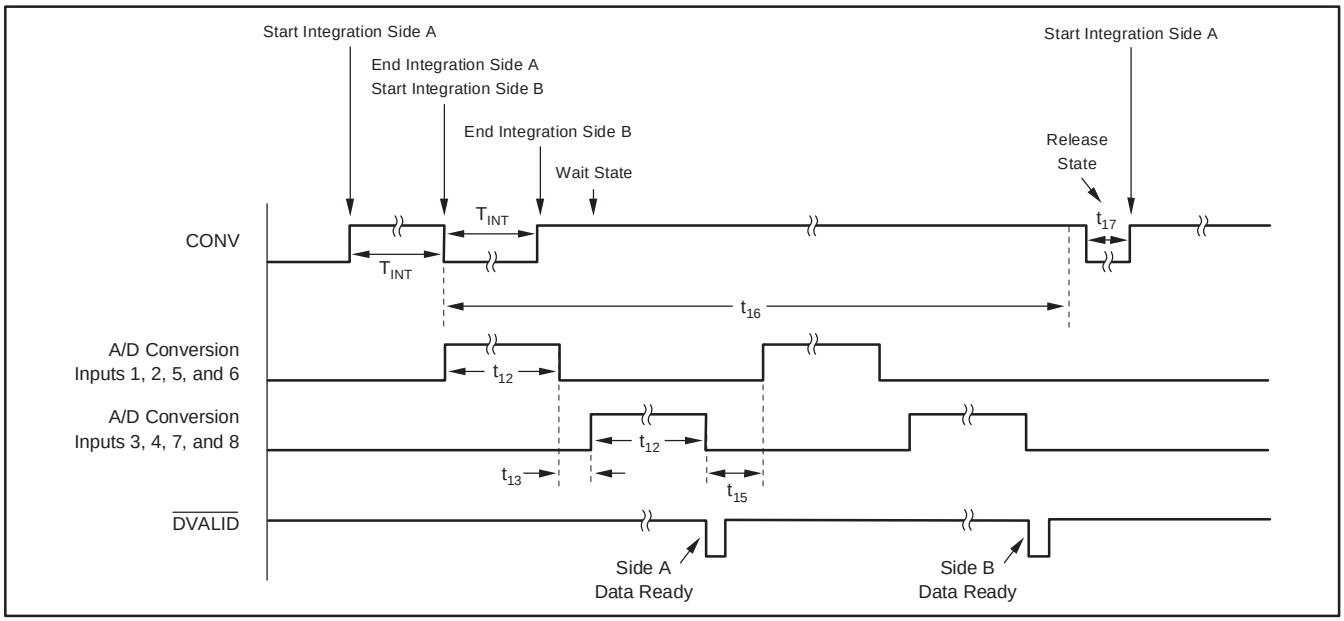


Figure 15. Internal Operation Timing Diagram of Non-Continuous Mode with Side B Integrated First

Looking at the state diagram, one can see that the CONV pattern needed to generate a given state progression is not unique. Upon entering states 1 or 8, the DDC118 remains in those states until mbsy goes low, independent of CONV. As long as the m/r/az cycle is underway, the state machine ignores CONV (see Figure 10, page 14). The top two signals in Figure 16 are different CONV patterns that produce the same state. This feature allows flexibility in generating ncont mode CONV patterns. For example, the DDC118 Evaluation Fixture operates in the ncont mode by generating a square wave with pulse width < t_6. Figure 17 illustrates operation in the ncont mode using a 50% duty cycle CONV signal with T_{INT} = 512 CLK periods. Care must be exercised when using a square wave to generate CONV. There are certain integration times that must be avoided since they produce very short intervals for state 2 (or state 7 if CONV is inverted). As seen in the state diagram, the state progresses from 2 to 3 as soon as CONV is high. The state machine does not insure that the duration of state 2 is long enough to properly prepare the next side for integration (t_{11}). This must be done by the user with proper timing of CONV. For example, if CONV is a square wave with T_{INT} = 970 CLK periods, state 2 will only be 9 CLK periods long; therefore, t_{11} will not be met.

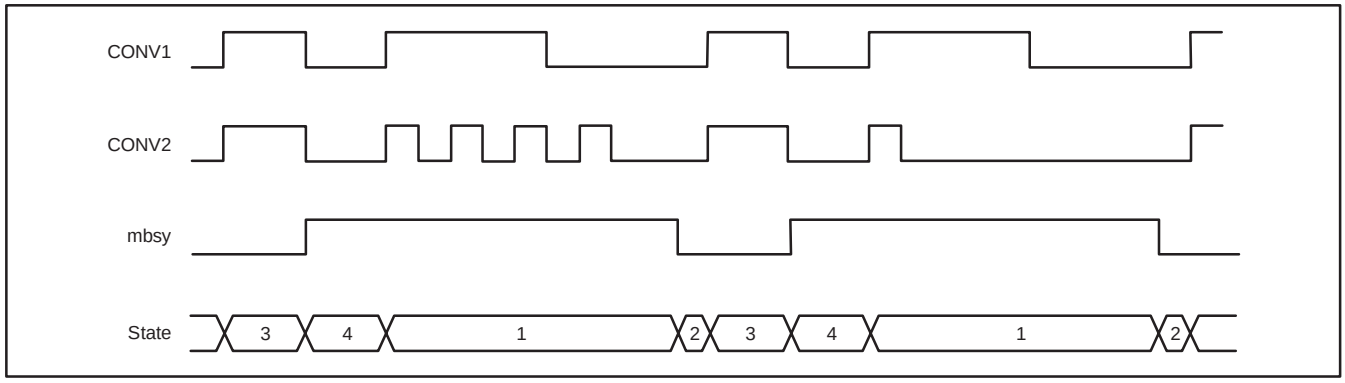


Figure 16. Equivalent CONV Signals in Non-Continuous Mode

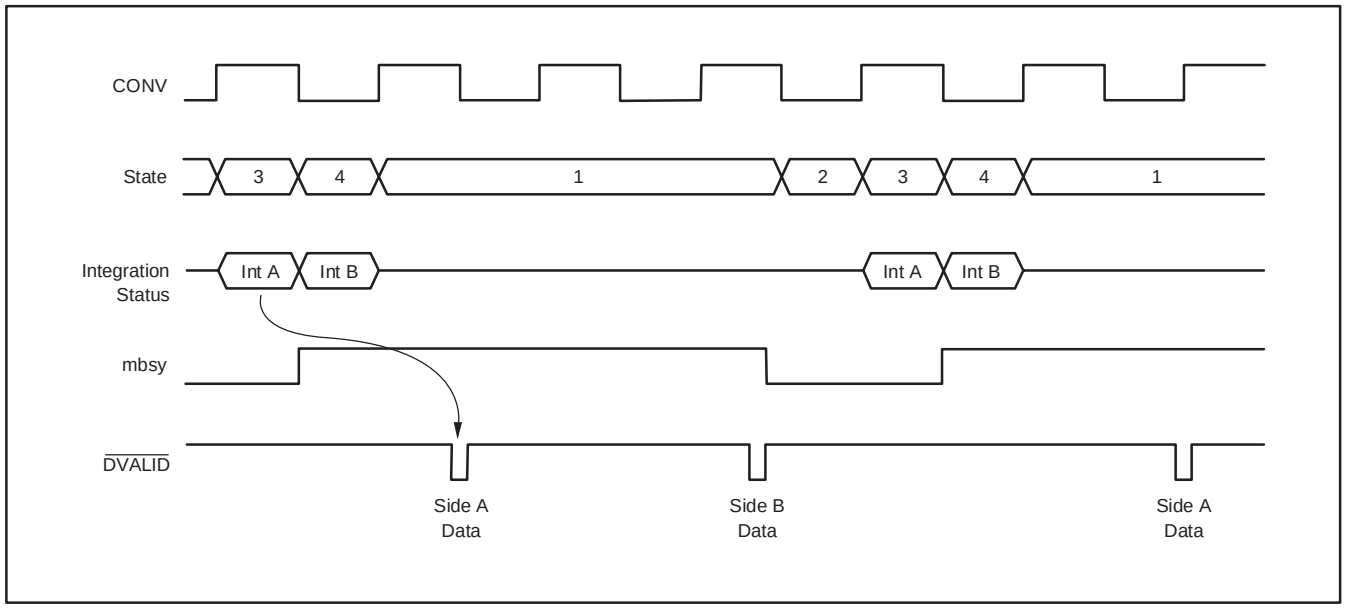


Figure 17. Non-Continuous Mode Timing with a 50% Duty Cycle CONV Signal

Changing Between Modes

Changing from the cont to ncont mode occurs whenever $T_{INT} < t_6$. Figure 18 shows an example of this transition. In this figure, the cont mode is entered when the integration on side A is completed before the m/r/az cycle on side B is complete. The DDC118 completes the measurement on sides B and A during states 8 and 7 with the input signal shorted to ground. Ncont integration begins with state 6.

Changing from the ncont to cont mode occurs when T_{INT} is increased so that T_{INT} is always $\geq t_6$, as shown in Figure 19 (see also Figure 14 and Table 8, page 18). With a longer T_{INT}, the m/r/az cycle has enough time to finish before the next integration begins and continuous integration of the input signal is possible. For the special case of the very first integration when changing to the cont mode, T_{INT} can be $< t_6$. This is allowed because there is no simultaneous m/r/az cycle on the side B during state 3—there is no need to wait for it to finish before ending the integration on side A.

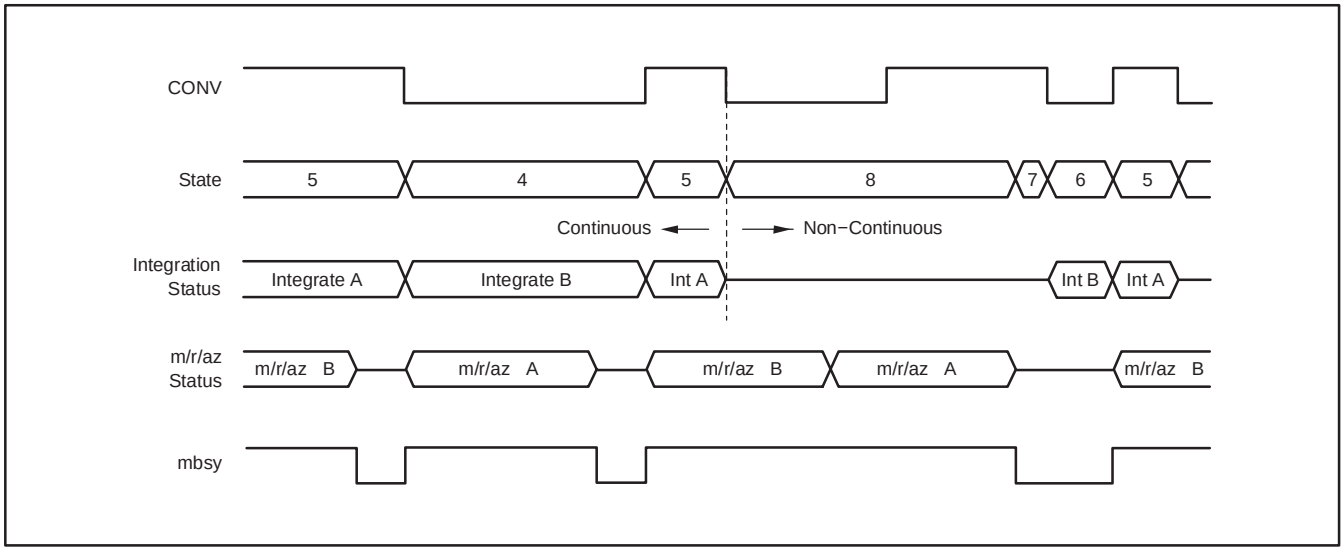


Figure 18. Changing from Continuous Mode to Non-Continuous Mode

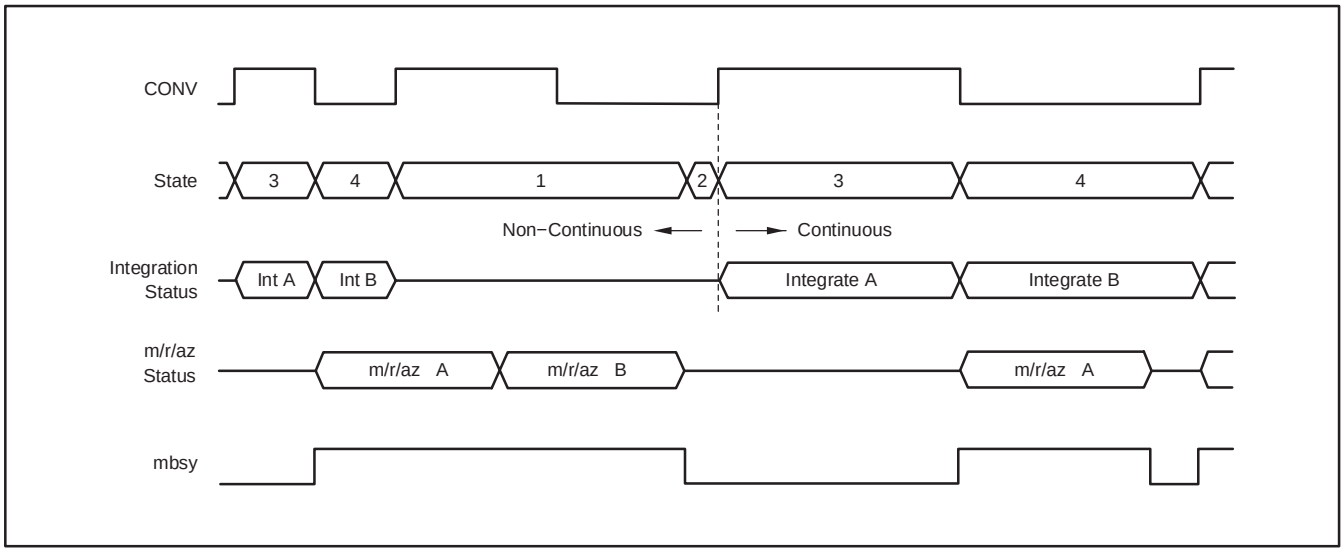


Figure 19. Changing from Non-Continuous Mode to Continuous Mode

DATA FORMAT (FORMAT)

The serial output data is provided in an offset binary code as shown in Table 9. The digital input pin FORMAT selects how many bits are used in the output word. When FORMAT is high (1), 20 bits are used. When FORMAT is low (0), the lower 4 bits are truncated so that only 16 bits are used. Note that the LSB size is 16 times bigger when FORMAT = 0. An offset is included in the output to allow slightly negative inputs, from board leakages for example, from clipping the reading. This offset is approximately 0.4% of the positive full-scale.

Table 9. Ideal Output Code(1) vs Input Signal

INPUT SIGNAL	IDEAL OUTPUT CODE FORMAT = HIGH (1)	IDEAL OUTPUT CODE FORMAT = LOW (0)
≥ 100% FS	1111 1111 1111 1111 1111	1111 1111 1111 1111
0.001531% FS	0000 0001 0000 0001 0000	0000 0001 0000 0001
0.001436% FS	0000 0001 0000 0000 1111	0000 0001 0000 0000
0.000191% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000096% FS	0000 0001 0000 0000 0001	0000 0001 0000 0000
0% FS	0000 0001 0000 0000 0000	0000 0001 0000 0000
−0.3955% FS	0000 0000 0000 0000 0000	0000 0000 0000 0000

(1) Excludes the effects of noise, INL, offset, and gain errors.

DATA RETRIEVAL

In both the continuous and non-continuous modes of operation, the data from the last conversion is available for retrieval on the falling edge of $\overline{\text{DVALID}}$ (see Figure 20 and Table 10). Data is shifted out on the falling edge of the data clock, DCLK. Make sure not to retrieve data while CONV changes as this can introduce noise. Stop activity on DCLK at least 10µs before or after a CONV transition.

Setting the FORMAT pin = 0 (16-bit output word) reduces the time needed to retrieve data by 20%, since there are fewer bits to shift out. This time reduction can be useful in multichannel systems requiring only 16 bits of resolution.

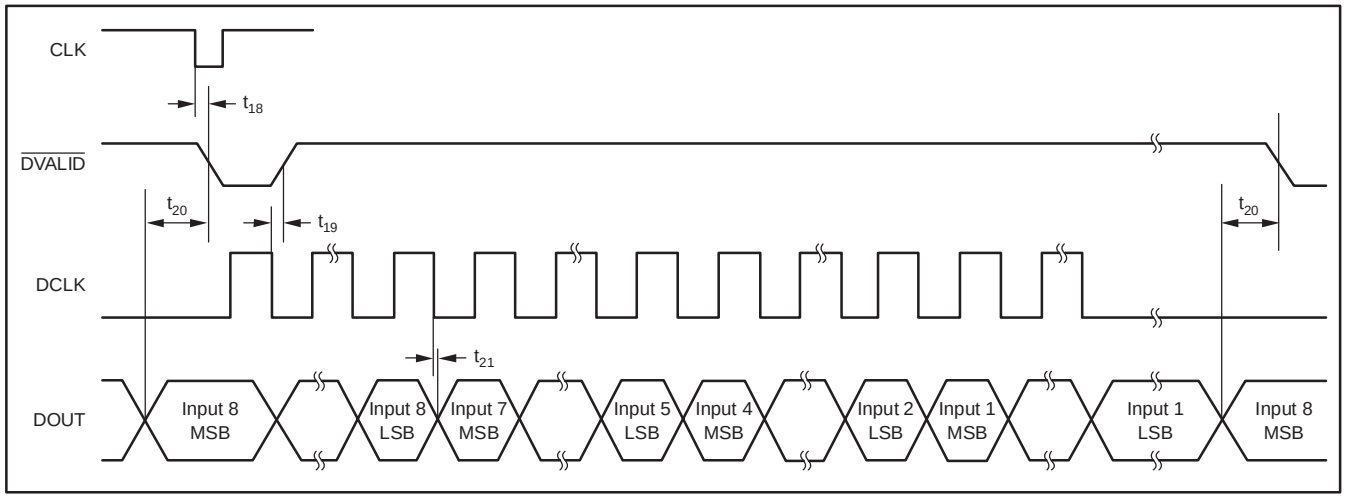


Figure 20. Digital Interface Timing Diagram for Data Retrieval From a Single DDC118

Table 10. Timing for the DDC118 Data Retrieval

SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{18}	Propagation Delay from Falling Edge of CLK to $\overline{\text{DVALID}}$ LOW	5			5			ns
t_{19}	Propagation Delay from Falling Edge of DCLK to $\overline{\text{DVALID}}$ HIGH	5			5			ns
t_{20}	Hold Time that DOUT is Valid Before the Falling Edge of $\overline{\text{DVALID}}$		1.75			1.458		µs
t_{21}	Hold Time that DOUT is Valid After Falling Edge of DCLK	5			5			ns
t_{21A}(1)	Propagation Delay from Falling Edge of DCLK to Valid DOUT			10			10	ns

(1) With a maximum load of one DDC118 (4pF typical) with an additional load of (5pF).

SPECIAL CONSIDERATIONS

Cascading Multiple Converters

Multiple DDC118 units can be connected in serial configuration, as illustrated in Figure 21.

DOUT can be used with DIN to daisy-chain several DDC118 devices together to minimize wiring. In this mode of operation, the serial data output is shifted through multiple DDC118s, as illustrated in Figure 21.

See Figure 22 for the timing diagram when the DIN input is used to daisy-chain several devices. Table 11 gives the timing specification for data retrieval using DIN.

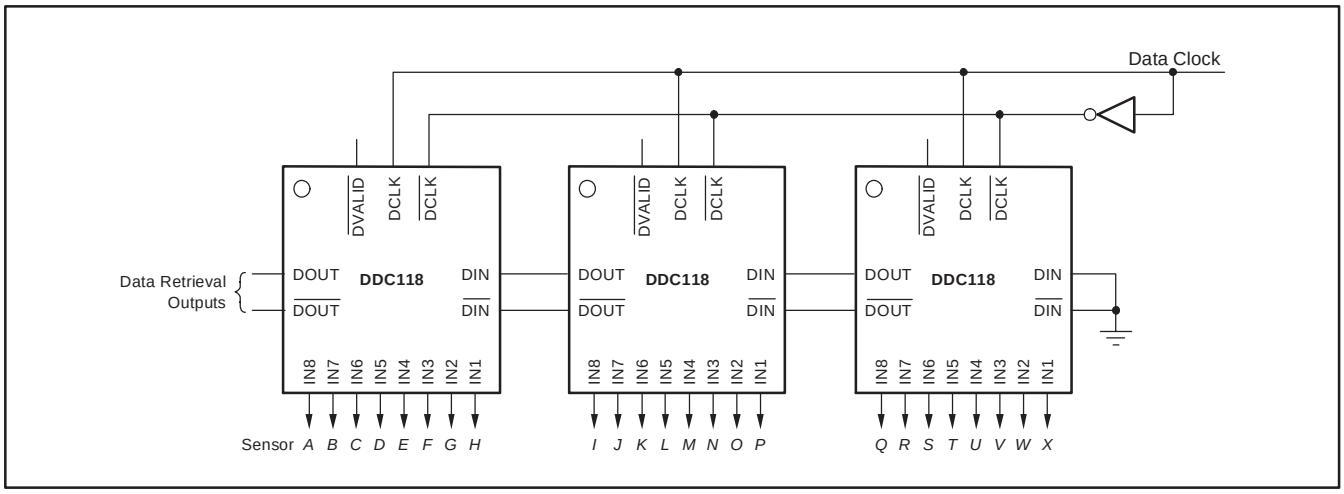


Figure 21. Daisy-Chained DDC118s

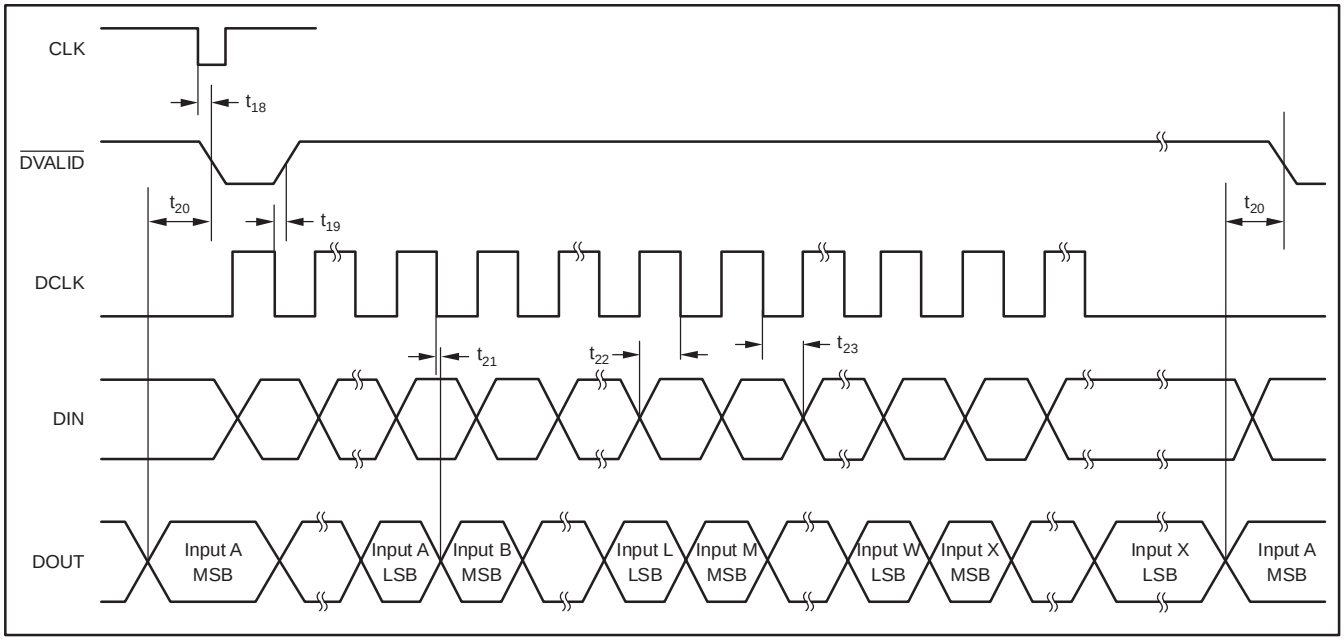


Figure 22. Timing Diagram When Using the DIN Function of the DDC118

Table 11. Timing for the DDC118 Data Retrieval Using DIN

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{22}	Set-Up Time From DIN to Falling Edge of DCLK	5			ns
t_{23}	Hold Time For DIN After Falling Edge of DCLK	4			ns

RETRIEVAL *BEFORE* CONV TOGGLES (CONTINUOUS MODE)

Date retrieval before CONV toggles is the most straightforward method. Data retrieval begins soon after $\overline{\text{DVALID}}$ goes low and finishes before CONV toggles, as shown in Figure 23. For best performance, data retrieval must stop t_{28} before CONV toggles. This method is most appropriate for longer integration times. The maximum time available for readback is $T_{INT} - t_{27} - t_{28}$. For DCLK = 10MHz and CLK = 4MHz, the maximum number of DDC118s that can be daisy-chained together (FORMAT = high) is calculated by Equation 1:

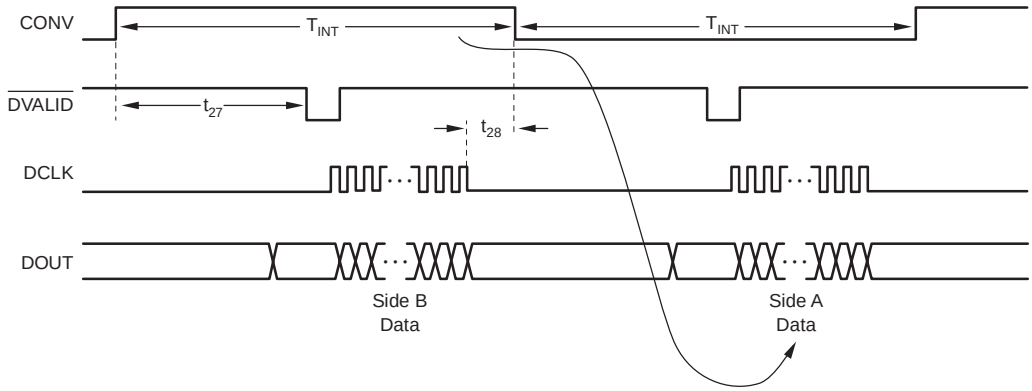
$$\frac{T_{INT} - 355.125\mu s}{160\tau_{DCLK}} \quad (1)$$

NOTE: $128\tau_{DCLK}$ is used for FORMAT = low.

where τ_{DCLK} is the period of the data clock. For example, if T_{INT} = 1000µs and DCLK = 10MHz, the maximum number of DDC118s (FORMAT = high) is shown in Equation 2:

$$\frac{1000\mu s - 355.125\mu s}{(160)(100ns)} = 40.30 \rightarrow 40 \text{DDC118s} \quad (2)$$

(or 50 for FORMAT = low).



SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{27}	Cont Mode Data Ready	345.00 ± 0.125			287.5 ± 0.104			µs
t_{28}	Data Retrieval Shutdown Before Edge of CONV	10			10			µs

Figure 23. Readback *Before* CONV Toggles

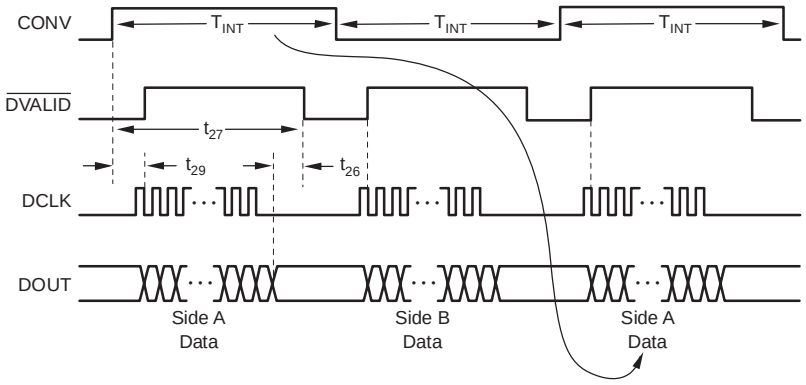
RETRIEVAL *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For shorter integration times, more time is available if data retrieval begins after CONV toggles and ends before the new data is ready. Data retrieval must wait t_{29} after CONV toggles before beginning. See Figure 24 for an example of this. The maximum time available for retrieval is $t_{27} - t_{29} - t_{26}$ (344.875µs – 10µs – 1.75µs for CLK = 4MHz), regardless of T_{INT}. The maximum number of DDC118s that can be daisy-chained together (FORMAT = high) is calculated by Equation 3:

$$\frac{333.125\mu s}{160\tau_{DCLK}} \quad (3)$$

NOTE: $128\tau_{DCLK}$ is used for FORMAT = low.

For DCLK = 10MHz, the maximum number of DDC118s is 20 (or 26 for FORMAT = low).



SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{26}	Hold Time that DOUT is Valid Before Falling Edge of $\overline{DVALID}$		1.75			1.458		µs
t_{27}	Cont Mode Data Ready		345.00 ± 0.125			287.5 ± 0.104		µs
t_{29}	Data Retrieval Start-Up After Edge of CONV	10			10			µs

Figure 24. Readback *After* CONV Toggles

RETRIEVAL *BEFORE* AND *AFTER* CONV TOGGLES (CONTINUOUS MODE)

For the absolute maximum time for data retrieval, data can be retrieved *before and after* CONV toggles. Nearly all of T_{INT} is available for data retrieval. Figure 25 illustrates how this is done by combining the two previous methods. Retrieval during CONV toggling to prevent digital noise, as discussed previously, and finished before the next data is ready. The maximum number of DDC118s that can be daisy-chained together (FORMAT = high) is:

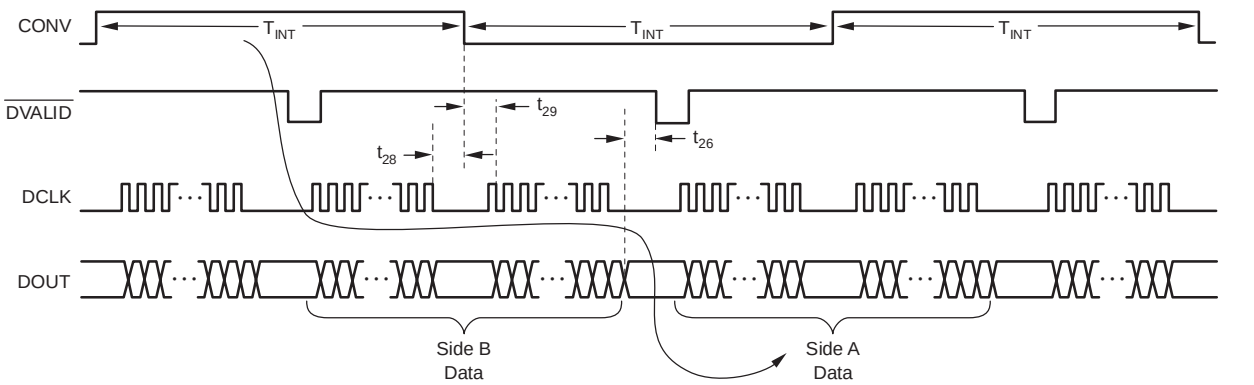
$$\frac{T_{INT} - 20\mu s - 1.75\mu s}{160\tau_{DCLK}}$$

NOTE: $128\tau_{DCLK}$ is used for FORMAT = low.

For T_{INT} = 400µs and DCLK = 10MHz, the maximum number of DDC118s is 23 (or 29 for FORMAT = low).

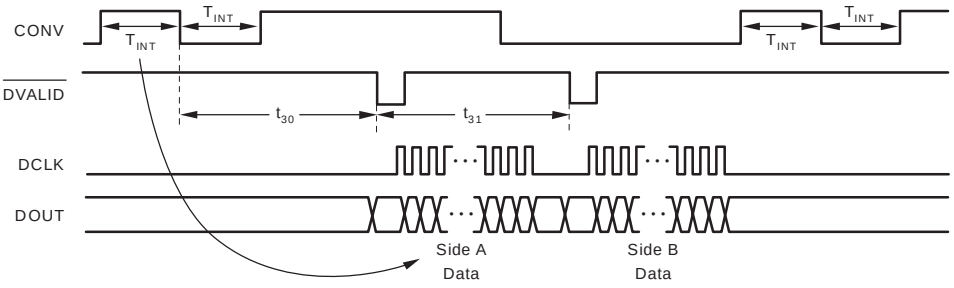
RETRIEVAL: NONCONTINUOUS MODE

Retrieving in noncontinuous mode is slightly different, compared to the continuous mode. As illustrated in Figure 26, $\overline{DVALID}$ goes low in time t_{30} after the first integration completes. If T_{INT} is shorter than this time, all of t_{31} is available to retrieve data before the other side data is ready. For $T_{INT} > t_{30}$, the first integration data is ready before the second integration completes. Data retrieval must be delayed until the second integration completes, leaving less time available for retrieval. The time available is $t_{31} – (T_{INT} – t_{30})$. The second integration's data must be retrieved before the next round of integration begins. This time is highly dependent on the pattern used to generate CONV. As with the continuous mode, data retrieval must halt before and after CONV toggles (t_{28}, t_{29}) and be completed before new data is ready (t_{26}).



SYMBOL	DESCRIPTION	CLK = 4MHZ, CLK_4X = 0			CLK = 4.8MHZ, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{26}	Hold Time that DOUT is Valid Before Falling Edge of $\overline{DVALID}$		1.75			1.458		µs
t_{28}	Data Retrieval Shutdown Before Edge of CONV	10			10			µs
t_{29}	Data Retrieval Start-Up After Edge of CONV	10			10			µs

Figure 25. Readback *Before and After* CONV Toggles



SYMBOL	DESCRIPTION	CLK = 4MHz, CLK_4X = 0			CLK = 4.8MHz, CLK_4X = 0			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{30}	1st ncont Mode Data Ready		344.75 ± 0.25			287.292 ± 0.208		µs
t_{31}	2nd ncont Mode Data Ready		362.500			302.083		µs

Figure 26. Readback in Non-Continuous Mode

POWER-UP SEQUENCING

Prior to power-up, all digital and analog inputs must be low. After the power supplies have settled, release $\overline{\text{RESET}}$ after time t_{32}. (See Figure 28 and Table 12.) Wait for time t_{33} to begin applying the digital signals CONV and CLK. The first CONV pulse will complete the release state and begin integration.

LAYOUT

POWER SUPPLIES AND GROUNDING

Both AVDD and DVDD should be as quiet as possible. It is particularly important to eliminate noise from AVDD that is non-synchronous with the DDC118 operation. Figure 27 illustrates two acceptable ways to supply power to the DDC118. The first case shows two separate +5V supplies for AVDD and DVDD. In this case, each +5V supply of the DDC118 should be bypassed with 10µF solid tantalum capacitors and 0.1µF ceramic capacitors. The second case shows the DVDD power supply derived from the AVDD supply with a < 10Ω isolation resistor. In both cases, the 0.1µF capacitors should be placed as close to the DDC118 package as possible. It is recommended that both the analog and digital grounds (AGND and DGND) be connected to a single ground plane on the printed circuit board (PCB).

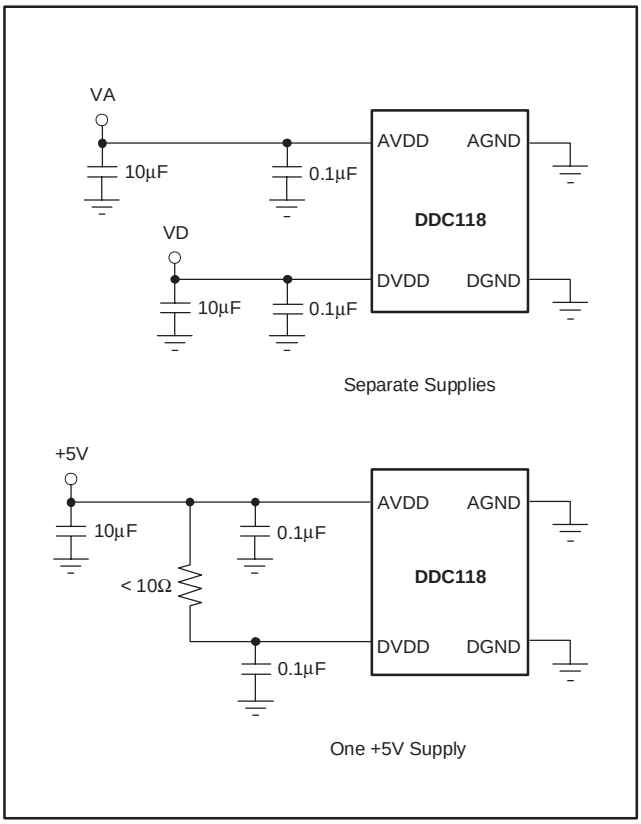


Figure 27. Power-Supply Connection Options

THERMAL PAD

It is strongly recommended that the thermal pad on the DDC118 be connected to ground on the PCB. No PCB traces should be routed underneath the thermal pad.

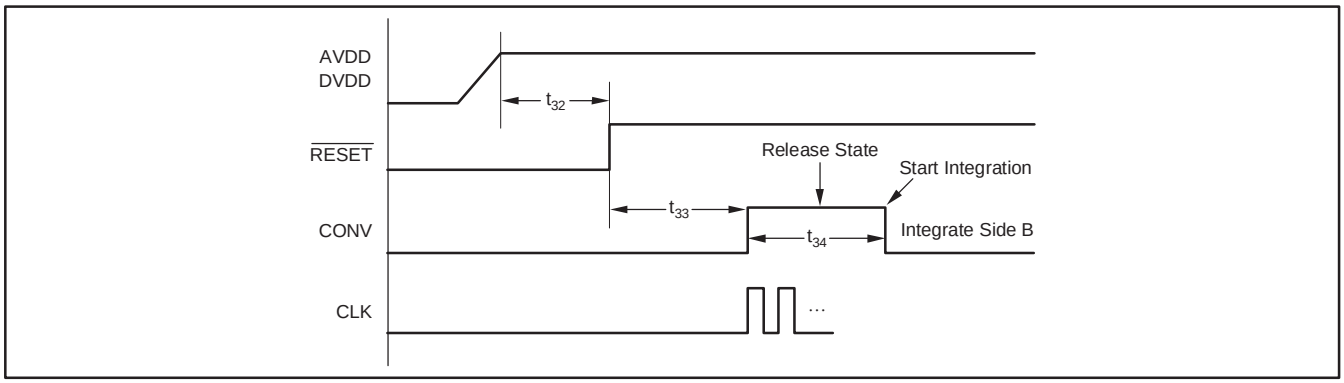


Figure 28. Timing Diagram at Power-Up of the DDC118

Table 12. Timing for the DDC118 Power-Up Sequence

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{32}	Power Supplies Settled to $\overline{\text{RESET}}$ Release	10			ms
t_{33}	$\overline{\text{RESET}}$ Release to CONV, CLK Begin	50			µs
t_{34}	First CONV Pulse Width	50			µs

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins. Digital signals should be kept as far from the analog input signals as possible on the PCB.

Input shielding practices should be taken into consideration when designing the circuit layout for the DDC118. The inputs to the DDC118 are high impedance and extremely sensitive to extraneous noise. Leakage currents between the PCB traces can exceed the input bias current of the DDC118 if shielding is not implemented. Figure 29 illustrates an acceptable approach to this problem. A PC ground plane is placed around the inputs of the DDC118. This shield helps minimize coupled noise into the input pins.

This approach reduces leakage effects by surrounding these sensitive pins with a low impedance analog ground. Leakage currents from other portions of the circuit will flow harmlessly to the low impedance analog ground rather than into the analog input stage of the DDC118.

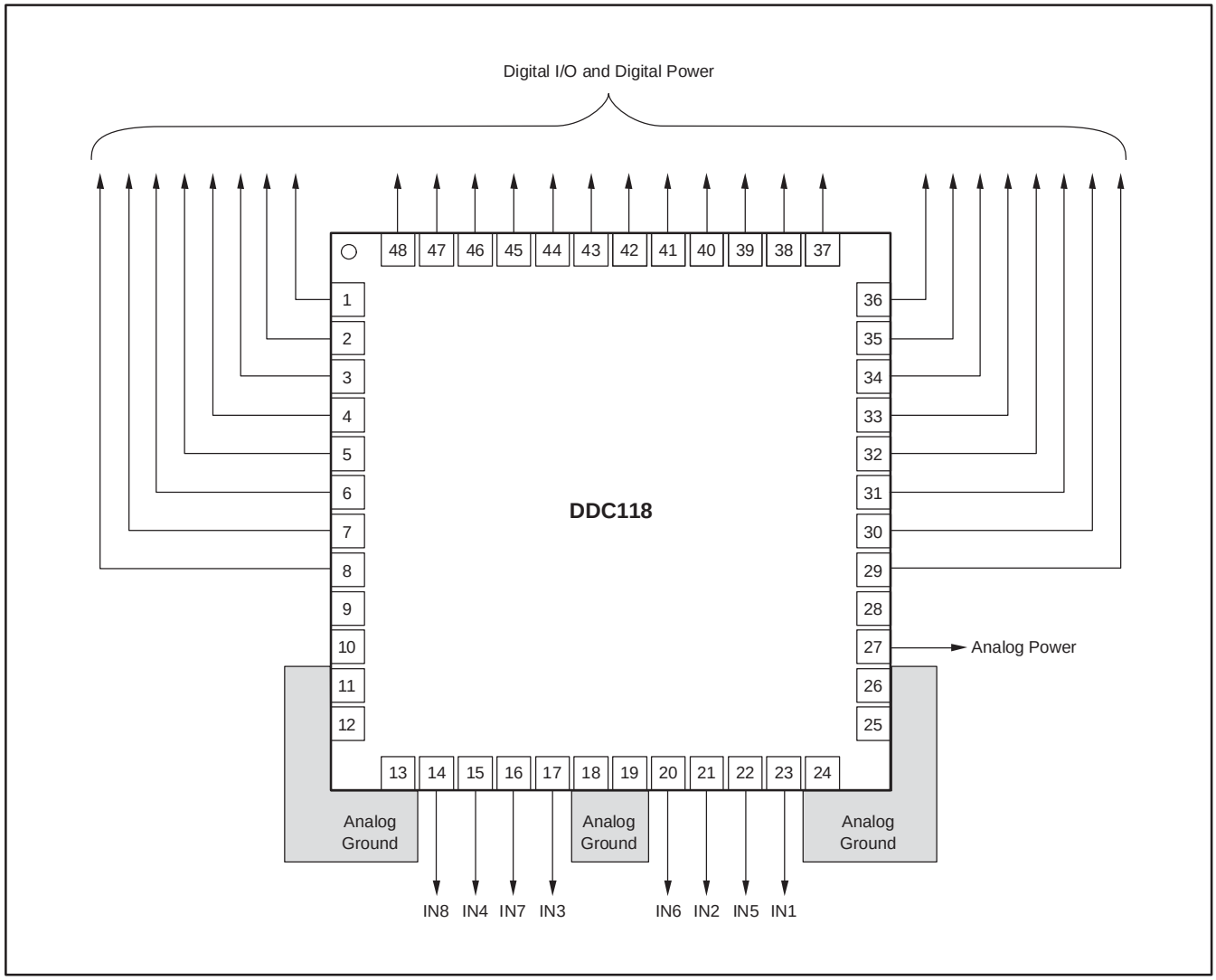


Figure 29. Recommended Shield for DDC118 Layout Design

PACKAGING INFORMATION

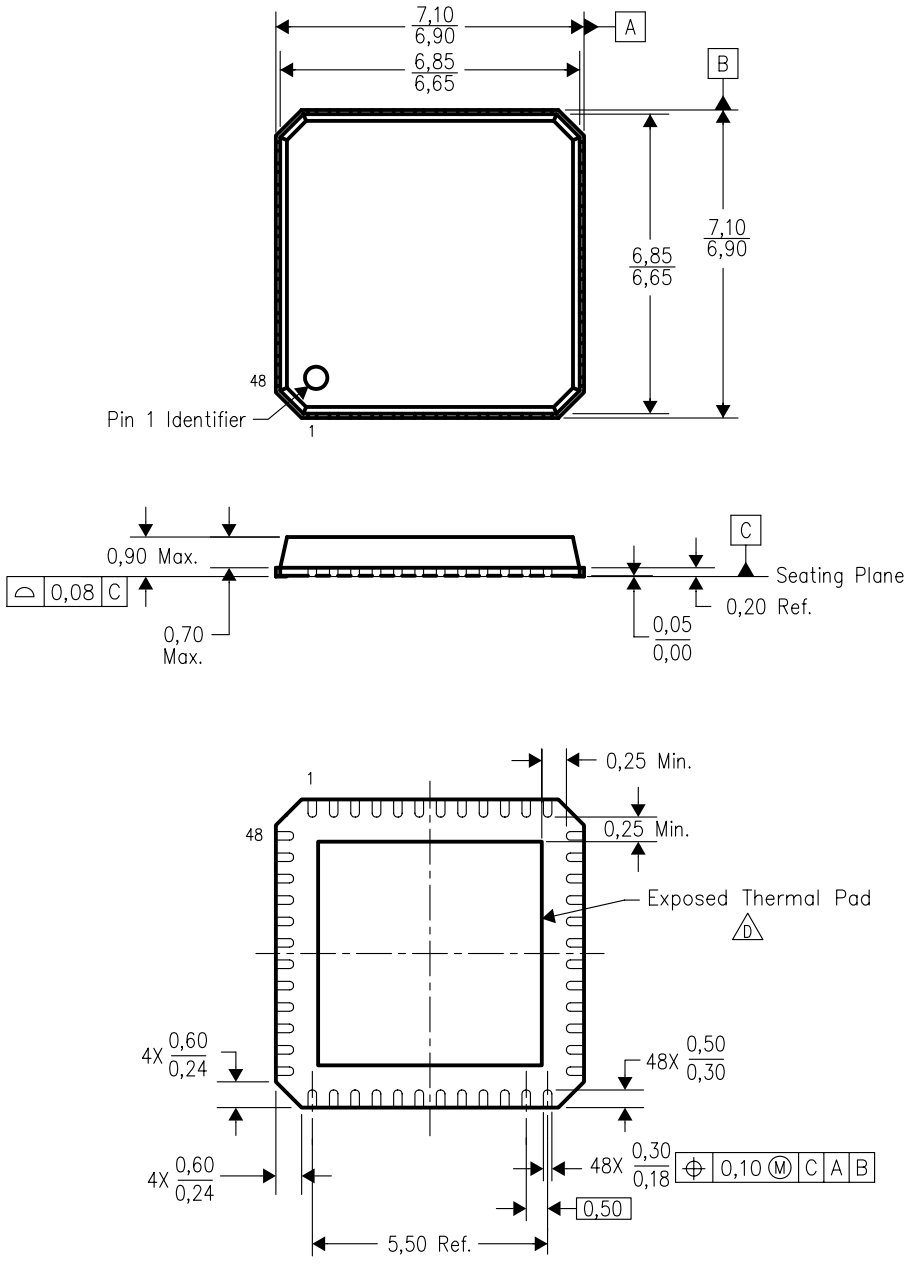
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DDC118IRTCR	ACTIVE	QFN	RTC	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DDC118IRTCT	ACTIVE	QFN	RTC	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RTC (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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