### 简CDCR61A供应商

#### CDCR61A DIRECT RAMBUS™ CLOCK GENERATOR – LITE

- 400-MHz Differential Clock Source for Direct Rambus Memory Systems for an 800-MHz Data Transfer Rate
- Operates From Two (3.3-V and 1.80-V) Power Supplies With 180 mW (Typ) at 400 MHz Total
- Packaged in a Thin Shrink Small-Outline Package (PW)
- External Crystal Required for Input

#### **PW PACKAGE** (TOP VIEW) V<sub>DDP</sub> 16 10 1 S0 GNDP 🗖 2 15 XOUT I 3 14 ⊐ GND 13 4 🗖 CLK V<sub>DDL</sub> 🗖 5 12 🗖 CLKB 6 11 🖵 GND II V<sub>DD</sub> 10 7 GNDL 🗖 8 9 S1 🗆 🗖 S2

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#### description

The Direct Rambus clock generator – lite (DRCG-Lite) is an independent crystal clock generator. It performs clock multiplication using PLL, sourced by an internal crystal oscillator. It provides one differential, high-speed Rambus channel compatible output pair. Also, one single-ended output is available to deliver 1/2 of the crystal frequency. The Rambus channel operates at up to 400 MHz with an option to select 300 MHz as well. The desired crystal is a 18.75-MHz crystal in a series resonance fundamental application.

The CDCR61A is characterized for operation over free-air temperatures of 0°C to 85°C.

#### functional block diagram



VDDP	S1	S2	MODE	CLK	CLKB	LCLK		
ON	0	0	Normal	CLK CLKB		XIN divided by 2		
ON	1	1	Normal	CLK CLKB		CLK CLKB X		XIN divided by 2
ON	0	1	Test	Divided by 2	Divided by 2	XIN divided by 2		
ON	1	0	Test	Divided by 4	Divided by 4	XIN divided by 2		
0 V	0	0	Test	XIN	XIN (invert)	XIN divided by 2		
0 V	1	1	Test	XIN	XIN (invert)	XIN divided by 2		
0 V	0	1	Test	XIN divided by 2	XIN (invert) divided by 2	XIN divided by 2		
0 V	1	0	Test	XIN divided by 4	XIN (invert) divided by 4	XIN divided by 2		



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TERMINAL		1/0	DESCRIPTION				
NAME	NO.	1/0	DESCRIPTION				
CLK	13	0	Output clock, connect to Rambus channel				
CLKB	12	0	Output clock (complement), connect to Rambus channel				
GNDP, GNDL, GND	2, 7, 11, 14		Ground				
LCLK	6	0	LVCMOS output, 1/2 of crystal frequency				
S0, S1, S2	16, 8, 9	Ι	LVTTL level logic select terminal for function selection				
V <sub>DD</sub>	10, 15		Power supply, 3.3 V				
VDDP	1		Power supply for PLL, 3.3 V (0 V for Test mode)				
VDDL	5		Power supply for LCLK, 1.8 V				
XIN	4	I	Reference crystal input				
XOUT	3	0	Reference crystal feedback				

#### **Terminal Functions**

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>DD</sub> or V <sub>DDP</sub> (see Note 1)	
Supply voltage range, V <sub>DDL</sub> (see Note 1)	
Input voltage range, VI, at any input terminal	–0.5 V to V <sub>DD</sub> + 0.5 V
Output voltage range, VO, at any output terminal (CLK, CLKB)	–0.5 V to V <sub>DD</sub> + 0.5 V
Output voltage range, V <sub>O</sub> , at any output terminal (LCLK)	
ESD rating (MIL-STD 883C, Method 3015)	> 2 kV, Machine Model >200 V
Continuous total power dissipation	see Dissipation Rating Table
Operating free-air temperature range, T <sub>A</sub>	0°C to 85°C
Storage temperature range, T <sub>stg</sub>	
Lead temperature 1,6 mm $(1/16)$ inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

#### DISSIPATION RATING TABLE

PACKAGE	T <sub>A</sub> ≤ 25°C	DERATING FACTOR	T <sub>A</sub> = 85°C
	POWER RATING	ABOVE T <sub>A</sub> = 25°C‡	POWER RATING
PW	1400 mW	11 mW/°C	740 mW

<sup>‡</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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#### recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V <sub>DD</sub>	3	3.3	3.6	V		
LCLK supply voltage, VDDL		1.7	1.8	2.1	V	
	SO			0.35×V <sub>DD</sub>	V	
	S1, S2			0.35×V <sub>DD</sub>	v	
	S0	0.65×V <sub>DD</sub>			v	
Thigh never input voitage, VIH	S1, S2	0.65×V <sub>DD</sub>				
	S0	10	55	100	ko	
Internal pullup resistance	S1, S2	90	145	250	K52	
	CLK, CLKB			16	m۸	
	LCLK			10	IIIA	
	CLK, CLKB			-16	–16 mA –10	
High-level output current, IOH	LCLK			-10		
Input frequency at crystal input		14.0625	18.75		MHz	
	S0, S1, S2			2.5	<b>р</b> Г	
	XIN, XOUT			20	рг	
Operating free-air temperature, T <sub>A</sub>		0		85	°C	

 $^\dagger$  Capacitance measured at f = 1 MHz, dc bias = 0.9 V, and V\_{AC} < 100 mV

#### timing requirements

	MIN	MAX	UNIT
Clock cycle time, t <sub>(cycle)</sub>	2.5	3.7	ns
Input slew rate, SR	0.5	4	V/ns
State transition latency (V <sub>DDX</sub> or S0 to CLKs – normal mode), t <sub>(STL)</sub>		3	ms

### crystal specifications

	MIN	MAX	UNIT
Frequency	14.0625	18.75	MHz
Frequency tolerance (at 25°C ±3°C)	-15	15	ppm
Equivalent resistance ( $C_L = 10 \text{ pF}$ )		100	Ω
Temperature drift (-10°C to 75°C)		10	ppm
Drive level	0.01	1500	μW
Motional inductance	20.7	25.3	mH
Insulation resistance	500		MΩ
Spurious attenuation ratio (at frequency $\pm$ 500 kHz)	3		dB
Overtone spurious	8		dB



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CON	DITIONS <sup>†</sup>	MIN	TYP <sup>‡</sup>	MAX	UNIT
V <sub>O(X)</sub>	Differential crossing-point o	utput voltage	See Figures 1 and 7		1.25		1.85	V
V <sub>O(PP)</sub>	Peak-to-peak output voltag single ended	Peak-to-peak output voltage swing, single ended		See Figure 1	0.4		0.7	V
VIK	Input clamp voltage		V <sub>DD</sub> = 3 V,	lj = -18 mA			-1.2	V
Rl	Input resistance	XIN, XOUT	V <sub>DD</sub> = 3.3 V,	$V_I = V_O$		>50		kΩ
		XOUT	V <sub>DD</sub> = 3.3 V,	$V_{O} = 2 V$			27	mA
Ιн	High-level input current	S0	V <sub>DD</sub> = 3.6 V,	$V_I = V_{DD}$			10	
		S1, S2	V <sub>DD</sub> = 3.6 V,	$V_I = V_{DD}$			10	μΑ
		XOUT	V <sub>DD</sub> = 3.3 V,	$V_{O} = 0 V$			-5.7	mA
۱ <sub>IL</sub>	Low-level input current	S0	V <sub>DD</sub> = 3.6 V,	$V_{I} = 0 V$	-30		-100	
		S1, S2	V <sub>DD</sub> = 3.6 V,	$V_{I} = 0 V$	-10		-50	μΑ
			See Figure 1				2.1	
		CLK, CLKB	V <sub>DD</sub> = min to max,	I <sub>OH</sub> = -1 mA	V <sub>DD</sub> - 0.1 V			V
⊻ОН	High-level output voltage		V <sub>DD</sub> = 3 V,	I <sub>OH</sub> = -16 mA	2.2			V
		LCLK	V <sub>DDL</sub> = min to max,	I <sub>OH</sub> = - 10 mA	V <sub>DDL</sub> – 0.45 V		V <sub>DDL</sub>	
	Low-level output voltage	CLK, CLKB	See Figure 1		1			
N			V <sub>DD</sub> = min to max,	I <sub>OL</sub> = 1 mA			0.1	v
VOL			V <sub>DD</sub> = 3 V,	I <sub>OL</sub> = 16 mA			0.5	
		LCLK	V <sub>DDL</sub> = min to max,	I <sub>OL</sub> = 10 mA	0		0.45	
			V <sub>DD</sub> = 3.135 V,	$V_{O} = 1 V$	-32	-52		mA
		CLK, CLKB	V <sub>DD</sub> = 3.3 V,	V <sub>O</sub> = 1.65 V		-51		
lou	High lovel output current		V <sub>DD</sub> = 3.465 V,	V <sub>O</sub> = 3.135 V		-14.5	-21	
OH	r ligh-level output current		V <sub>DDL</sub> = 1.7 V,	$V_{O} = 0.5 V$	-11	-26		
		LCLK	V <sub>DDL</sub> = 1.8 V,	$V_{O} = 0.9 V$		-28		
			V <sub>DDL</sub> = 2.1 V,	V <sub>O</sub> = 1.6 V		-24.5	-35	
			V <sub>DD</sub> = 3.135 V,	V <sub>O</sub> = 1.95 V	43	61.5		
		CLK, CLKB	V <sub>DD</sub> = 3.3 V,	V <sub>O</sub> = 1.65 V		65		
	l ow-level output current		V <sub>DD</sub> = 3.465 V,	$V_{O} = 0.4 V$		25.5	36	mΔ
UL	Low level output current		V <sub>DDL</sub> = 1.7 V,	V <sub>O</sub> = 1.2 V	11	27		
		LCLK	V <sub>DDL</sub> = 1.8 V,	V <sub>O</sub> = 0.9 V		30		
			V <sub>DDL</sub> = 2.1 V,	$V_{O} = 0.5 V$		28	38	
rон	High-level dynamic output r	esistance§	$\Delta I_{O}$ – 14.5 mA to $\Delta I_{O}$	– 16.5 mA	12	25	40	Ω
rol	Low-level dynamic output re	esistance§	$\Delta I_{O}$ + 14.5 mA to $\Delta I_{O}$	+ 16.5 mA	12	17	40	Ω
Go		CLK, CLKB					3	nF
50	Culput capacitance	LCLK					3	

<sup>†</sup> V<sub>DD</sub> refers to any of the following; V<sub>DD</sub>, V<sub>DDL</sub>, and V<sub>DDP</sub> <sup>‡</sup> All typical values are at V<sub>DD</sub> = 3.3 V, V<sub>DDL</sub> = 1.8 V, T<sub>A</sub> = 25°C. §  $r_O = \Delta V_O / \Delta I_O$ . This is defined at the output terminals, not at the measurement point of Figure 1.



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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

	PARAMETER	TEST CONDITIONS <sup>†</sup>	MIN	TYP‡	MAX	UNIT
IDD	Static supply current	Outputs high or low ( $V_{DDP} = 0 V$ )			6.5	mA
IDDL	Static supply current (LVCMOS)	Outputs high or low ( $V_{DDP} = 0 V$ )			50	μA
IDD(NORMAL)	Supply surrent in normal state	300 MHz			39	mA
	Supply current in normal state	400 MHz			50	mA
IDDL(NORMAL)	Supply current in normal state (LVCMOS)	400 MHz			8	mA

 $^{\dagger}$  V<sub>DD</sub> refers to any of the following; V<sub>DD</sub>, V<sub>DDL</sub>, and V<sub>DDP</sub>

<sup>‡</sup> All typical values are at  $V_{DD} = 3.3 \text{ V}$ ,  $V_{DDL} = 1.8 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	ΤΥΡ <sup>†</sup> ΜΑΧ	UNIT
t(cycle)	Clock cycle time (CLK, CLKB)			2.5	3.7	ns
<b>.</b> .	Total jitter over 1, 2, 3, 4, 5, or 6	300 MHz	See Figure 2		140	
ĽCj	clock cycles‡	400 MHz	See Figure 3		100	ps
	Long torm iittor	300 MHz	See Figure 4		400	
ΥĽ	Long-term jitter	400 MHz	See Figure 4		300	ps
<sup>t</sup> DC	Output duty cycle over 10,000 cycles		See Figure 5	45%	55%	
		300 MHz			70	
<sup>I</sup> DC,ERR	Output cycle-to-cycle duty cycle error	400 MHz	See Figure 6		55	ps
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (measured at 20%-80% of output voltage)#	CLK, CLKB	See Figure 9,	160	400	ps
Δt	Difference between rise and fall times device (20%–80%) $ t_{f}-t_{f} ^{\#}$	Difference between rise and fall times on a single device (20%–80%) $ t_f - t_r ^{\#}$			100	ps
<sup>t</sup> c(LCLK)	Clock cycle time (LCLK)			106.6	142.2	ns
t <sub>(ci)</sub>	LCLK cycle jitter§		See Figure 11	-0.2	0.2	ns
<sup>t</sup> (cj10)	LCLK 10-cycle jitter§¶		See Figure 11	-1.3 t <sub>(cj)</sub>	1.3 t <sub>(cj)</sub>	ns
tDC	Output duty cycle	LCLK		40%	60%	
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (measured at 20%-80% of output voltage)	LCLK	See Figure 9		1	ns
	DI L loop hondwidth		f <sub>mod</sub> = 50 kHz		-3	dP
			f <sub>mod</sub> = 8 MHz	-20		

<sup>†</sup> All typical values are at  $V_{DD} = 3.3$  V,  $T_A = 25^{\circ}$ C.

<sup>‡</sup>Output short-term jitter specification is peak-to-peak (see Figure 9).

§ LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period.

ILCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter.

<sup>#</sup>V<sub>DD</sub>= 3.3 V



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PARAMETER MEASUREMENT INFORMATION

NOTE A: These capacitors represent parasitic capacitance. No discrete capacitors are used on the test board during device characterization.





Cycle-to-cycle jitter =  $|t_{C1} - t_{C2}|$  over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



 $t_{C(i)}$  = nominal expected time Cycle-to-cycle jitter = |  $t_{C(i)} - t_{C(i+1)}$ | over 10000 consecutive cycles

Figure 3. Short-Term Cycle-to-Cycle Jitter over 2, 3, 4, or 6 Cycles



t<sub>jL</sub> = | t<sub>(cycle)</sub>, max<sup>-</sup> t<sub>(cycle)</sub>, min| over 10000 consecutive cycles

Figure 4. Long-Term Jitter



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Figure 8. LCLK Test Load Circuit and Voltage Waveform for CLK/CLKB and LCLK



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#### MECHANICAL DATA

#### PLASTIC SMALL-OUTLINE PACKAGE





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



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