16-Bit, 5MSPS ANALOG-TO-DIGITAL CONVERTER

FEATURES

- Data Rate: 5MSPS
- Signal-to-Noise Ratio: 88dB
- Total Harmonic Distortion: –99dB
- Spurious-Free Dynamic Range: 101dB
- Linear Phase with 2.45 MHz Bandwidth
- Passband Ripple: ±0.0025dB
- Selectable On-Chip Reference
- Directly Connects to TMS320C6000 DSPs
- Adjustable Power Dissipation: 315 to 570mW
- Power Down Mode
- Supplies: Analog +5V
  Digital +3V
  Digital I/O +2.7 to +5.25V

APPLICATIONS

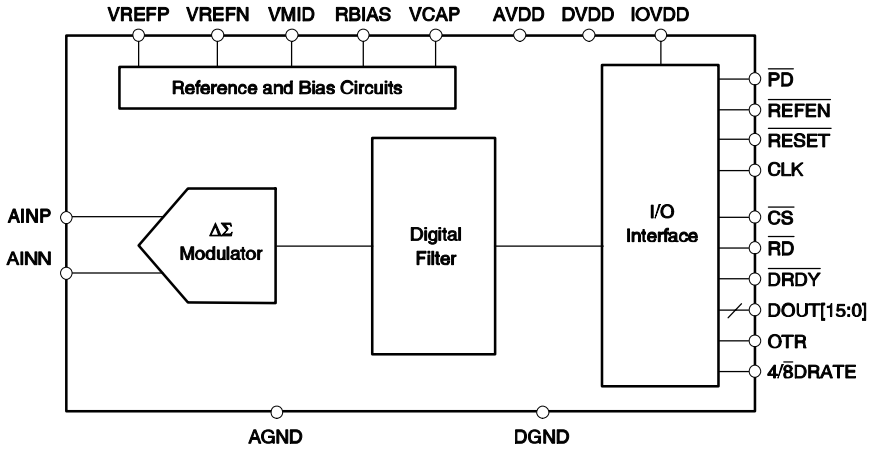
- Scientific Instruments
- Automated Test Equipment
- Data Acquisition
- Medical Imaging
- Vibration Analysis

DESCRIPTION

The ADS1605 is a high-speed, high-precision, delta–sigma analog-to-digital converter (ADC) with 16-bit resolution. The data rate is 5MSPS, the bandwidth (–3dB) is 2.45MHz, and passband ripple is less than ±0.0025dB (to 2.2MHz). The ADS1605 offers outstanding performance at these speeds with a signal-to-noise ratio up to 88dB, total harmonic distortion down to –99dB, and a spurious-free dynamic range up to 101dB.

The input signal is measured against a voltage reference that can be generated on-chip or supplied externally. The digital output data is provided over a simple parallel interface that easily connects to DSPs. An out-of-range monitor reports when the input range has been exceeded. The ADS1605 operates from a +5V analog supply (AVDD) and +3V digital supply (DVDD). The digital I/O supply (IOVDD) operates from +2.7 to +5.25V, enabling the digital interface to support a range of logic families. The analog power dissipation is set by an external resistor and can be reduced when operating at slower speeds. A power down mode, activated by a digital I/O pin, shuts down all circuitry. The ADS1605 is offered in a 64-pin TQFP package using TI PowerPAD™ technology.

The ADS1605, with its outstanding high-speed performance is well suited for the demanding measurement requirements of scientific instrumentation, automated test equipment, data acquisition, and medical imaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

ORDERING INFORMATION

PRODUCT	PACKAGE–LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1605	TQFP–64 PowerPAD	PAP	–40°C to +85°C	ADS1605I	ADS1605IPAPT	Tape and Reel, 250
					ADS1605IPAPR	Tape and Reel, 1000

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
AVDD to AGND	–0.3 to +6	V
DVDD to DGND	–0.3 to +3.6	V
IOVDD to DGND	–0.3 to +6	V
AGND to DGND	–0.3 to +0.3	V
Input Current	100mA, Momentary	
Input Current	10mA, Continuous	
Analog I/O to AGND	–0.3 to AVDD + 0.3	V
Digital I/O to DGND	–0.3 to IOVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +105	°C
Storage Temperature Range	–60 to +150	°C
Lead Temperature (soldering, 10s)	+260	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Input					
Differential input voltage (V_{IN}) (AINP – AINN)	0dBFS		±1.57V_{REF}		V
	–2dBFS		±1.25V_{REF}		V
	–6dBFS		±0.79V_{REF}		V
	–20dBFS		±0.157V_{REF}		V
Common-mode input voltage (V_{CM}) (AINP + AINN) / 2			2.0		V
Absolute input voltage (AINP or AINN with respect to AGND)	0dBFS	–0.1		4.7	V
	–2dBFS input and smaller	0.1		4.2	V
Dynamic Specifications					
Data rate			$5.0\left(\frac{f_{CLK}}{40MHz}\right)$		MSPS
Signal–to–noise ratio (SNR)	f_{IN} = 100kHz, –2dBFS		88		dB
	f_{IN} = 100kHz, –6dBFS		84		dB
	f_{IN} = 100kHz, –20dBFS	62	70		dB
	f_{IN} = 500kHz, –2dBFS		86		dB
	f_{IN} = 500kHz, –6dBFS		83		dB
	f_{IN} = 500kHz, –20dBFS		69		dB
	f_{IN} = 2MHz, –2dBFS		84		dB
	f_{IN} = 2MHz, –6dBFS		82		dB
	f_{IN} = 2MHz, –20dBFS		69		dB
Total harmonic distortion (THD)	f_{IN} = 100kHz, –2dBFS		–93		dB
	f_{IN} = 100kHz, –6dBFS		–99		dB
	f_{IN} = 100kHz, –20dBFS	–85	–94		dB
	f_{IN} = 500kHz, –2dBFS		–94		dB
	f_{IN} = 500kHz, –6dBFS		–97		dB
	f_{IN} = 500kHz, –20dBFS		–93		dB
	f_{IN} = 2MHz, –2dBFS		–98		dB
	f_{IN} = 2MHz, –6dBFS		–101		dB
	f_{IN} = 2MHz, –20dBFS		–92		dB
Signal–to–noise and distortion (SINAD)	f_{IN} = 100kHz, –2dBFS		86		dB
	f_{IN} = 100kHz, –6dBFS		84		dB
	f_{IN} = 100kHz, –20dBFS	62	70		dB
	f_{IN} = 500kHz, –2dBFS		86		dB
	f_{IN} = 500kHz, –6dBFS		83		dB
	f_{IN} = 500kHz, –20dBFS		69		dB
	f_{IN} = 2MHz, –2dBFS		84		dB
	f_{IN} = 2MHz, –6dBFS		82		dB
	f_{IN} = 2MHz, –20dBFS		69		dB

ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Spurious free dynamic range (SFDR)	f_{IN} = 100kHz, –2dBFS		96		dB
	f_{IN} = 100kHz, –6dBFS		101		dB
	f_{IN} = 100kHz, –20dBFS	85	96		dB
	f_{IN} = 500kHz, –2dBFS		95		dB
	f_{IN} = 500kHz, –6dBFS		100		dB
	f_{IN} = 500kHz, –20dBFS		95		dB
	f_{IN} = 2MHz, –2dBFS		102		dB
	f_{IN} = 2MHz, –6dBFS		105		dB
	f_{IN} = 2MHz, –20dBFS		96		dB
Intermodulation distortion (IMD)	f_1 = 1.99MHz, –2dBFS f_2 = 2.00MHz, –2dBFS		94		dB
Aperture delay			4		ns
Digital Filter Characteristics					
Pass band		0		$2.2\left(\frac{f_{CLK}}{40MHz}\right)$	MHz
Pass band ripple				±0.0025	dB
Pass band transition	–0.1dB attenuation		$2.3\left(\frac{f_{CLK}}{40MHz}\right)$		MHz
	–3.0dB attenuation		$2.45\left(\frac{f_{CLK}}{40MHz}\right)$		MHz
Stop band		$2.8\left(\frac{f_{CLK}}{40MHz}\right)$		$37.2\left(\frac{f_{CLK}}{40MHz}\right)$	MHz
Stop band attenuation		72			dB
Group delay			$5.2\left(\frac{40MHz}{f_{CLK}}\right)$		µs
Settling time	To ±0.001%		$9.4\left(\frac{40MHz}{f_{CLK}}\right)$		µs
Static Specifications					
Resolution			16		Bits
No missing codes		16			Bits
Input referred noise			1.0		LSB, rms
Integral nonlinearity	–1.5dBFS signal		±0.75		LSB
Differential nonlinearity			±0.25		LSB
Offset error			0.05		%FSR
Offset error drift			1		ppmFSR/°C
Gain error			2.5		%
Gain error drift	Excluding reference drift		10		ppm/°C
Common-mode rejection	at DC		75		dB
Power-supply rejection	at DC		65		dB

ELECTRICAL CHARACTERISTICS (continued)

All specifications at –40°C to +85°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference(1)					
V_{REF} = (VREFP – VREFN)		2.5	3.0	3.2	V
VREFP		3.75	4.0	4.25	V
VREFN		0.75	1.0	1.25	V
VMID		2.3	2.5	2.8	V
V_{REF} drift	Internal reference ($\overline{REFEN}$ = low)		50		ppm/°C
Startup time	Internal reference ($\overline{REFEN}$ = low)		15		ms
Clock Input					
Frequency (f_{CLK})			40	50	MHz
Duty Cycle	f_{CLK} = 40MHz	45		55	%
Digital Input/Output					
V_{IH}		0.7 IOVDD		IOVDD	V
V_{IL}		DGND		0.3 IOVDD	V
V_{OH}	I_{OH} = 50µA	0.8 IOVDD			V
V_{OL}	I_{OL} = 50µA			0.2 IOVDD	V
Input leakage	DGND < V_{DIGIN} < IOVDD			±10	µA
Power-Supply Requirements					
AVDD		4.75		5.25	V
DVDD		2.7		3.3	V
IOVDD		2.7		5.25	V
AVDD current (I_{AVDD})	$\overline{REFEN}$ = low		110	135	mA
	$\overline{REFEN}$ = high		85	105	mA
DVDD current (I_{DVDD})			45	55	mA
IOVDD current (I_{IOVDD})	IOVDD = 3V		4	6	mA
Power dissipation	AVDD = 5V, DVDD = 3V, IOVDD = 3V, $\overline{REFEN}$ = high		570	710	mW
	$\overline{PD}$ = low, CLK disabled		5		mW
Temperature Range					
Specified		–40		+85	°C
Operating		–40		+105	°C
Storage		–60		+150	°C
Thermal Resistance, θ_{JA}	PowerPAD™ soldered to PCB with 2oz. trace and copper pad.		25		°C/W
θ_{JC}			0.5		°C/W

(1) The specification limits for VREF, VREFP, VREFN, and VMID apply when using the internal or an external reference. The internal reference voltages are bounded by the limits shown. When using an external reference, the limits indicate the allowable voltages that can be applied to the reference pins.

DEFINITIONS

Absolute Input Voltage

Absolute input voltage, given in volts, is the voltage of each analog input (AINN or AINP) with respect to AGND.

Aperture Delay

Aperture delay is the delay between the rising edge of CLK and the sampling of the input signal.

Common-Mode Input Voltage

Common-mode input voltage (V_{CM}) is the average voltage of the analog inputs:

$$\frac{(AINP + AINN)}{2}$$

Differential Input Voltage

Differential input voltage (V_{IN}) is the voltage difference between the analog inputs: (AINP–AINN).

Differential Nonlinearity (DNL)

DNL, given in least-significant bits of the output code (LSB), is the maximum deviation of the output code step sizes from the ideal value of 1LSB.

Full-Scale Range (FSR)

FSR is the difference between the maximum and minimum measurable input signals. For the ADS1605, FSR = $2 \times 1.57V_{REF}$.

Gain Error

Gain error, given in %, is the error of the full-scale input signal with respect to the ideal value.

Gain Error Drift

Gain error drift, given in ppm/°C, is the drift over temperature of the gain error. The gain error is specified as the larger of the drift from ambient (T = 25°C) to the minimum or maximum operating temperatures.

Integral Nonlinearity (INL)

INL, given in least-significant bits of the output code (LSB), is the maximum deviation of the output codes from a best fit line.

Intermodulation Distortion (IMD)

IMD, given in dB, is measured while applying two input signals of the same magnitude, but with slightly different frequencies. It is calculated as the difference between the rms amplitude of the input signal to the rms amplitude of the peak spurious signal.

Offset Error

Offset Error, given in % of FSR, is the output reading when the differential input is zero.

Offset Error Drift

Offset error drift, given in ppm of FSR/°C, is the drift over temperature of the offset error. The offset error is specified as the larger of the drift from ambient (T = 25°C) to the minimum or maximum operating temperatures.

Signal-to-Noise Ratio (SNR)

SNR, given in dB, is the ratio of the rms value of the input signal to the sum of all the frequency components below $f_{CLK}/2$ (the Nyquist frequency) excluding the first six harmonics of the input signal and the dc component.

Signal-to-Noise and Distortion (SINAD)

SINAD, given in dB, is the ratio of the rms value of the input signal to the sum of all the frequency components below $f_{CLK}/2$ (the Nyquist frequency) including the harmonics of the input signal but excluding the dc component.

Spurious Free Dynamic Range (SFDR)

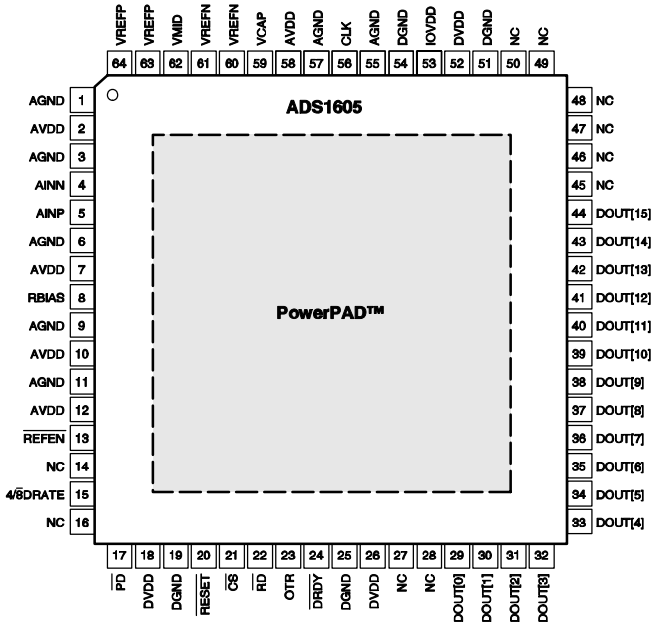
SFDR, given in dB, is the difference between the rms amplitude of the input signal to the rms amplitude of the peak spurious signal.

Total Harmonic Distortion (THD)

THD, given in dB, is the ratio of the sum of the rms value of the first six harmonics of the input signal to the rms value of the input signal.

PIN ASSIGNMENTS

TQFP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE	DESCRIPTION
AGND	1, 3, 6, 9, 11, 55, 57	Analog	Analog ground
AVDD	2, 7, 10, 12, 58	Analog	Analog supply
AINN	4	Analog input	Negative analog input
AINP	5	Analog input	Positive analog input
RBIAS	8	Analog	Terminal for external analog bias setting resistor
$\overline{\text{REFEN}}$	13	Digital input: active low	Internal reference enable. Internal pull-down resistor of 170kΩ to DGND.
NC	14,16, 27, 28, 50		Must be left unconnected
4/$\overline{8}$DRATE	15	Digital input	Digital filter decimation rate. Internal pull-down resistor of 170kΩ to DGND.
$\overline{\text{PD}}$	17	Digital input: active low	Power down all circuitry. Internal pull-up resistor of 170kΩ to DGND.
DVDD	18, 26, 52	Digital	Digital supply
DGND	19, 25, 51, 54	Digital	Digital ground
$\overline{\text{RESET}}$	20	Digital input: active low	Reset digital filter
$\overline{\text{CS}}$	21	Digital input: active low	Chip select
$\overline{\text{RD}}$	22	Digital input: active low	Read enable
OTR	23	Digital output	Analog inputs out of range
$\overline{\text{DRDY}}$	24	Digital output: active low	Data ready on falling edge
DOUT [15:0]	29–44	Digital output	Data output. DOUT[15] is the MSB and DOUT[0] is the LSB.
NC	45		Must be left unconnected
NC	46		Must be left unconnected
NC	47, 48		Must be left unconnected
IOVDD	53	Digital	Digital I/O supply
CLK	56	Digital input	Clock input
VCAP	59	Analog	Terminal for external bypass capacitor connection to internal bias voltage
VREFN	60, 61	Analog	Negative reference voltage
VMID	62	Analog	Midpoint voltage
VREFP	63, 64	Analog	Positive reference voltage

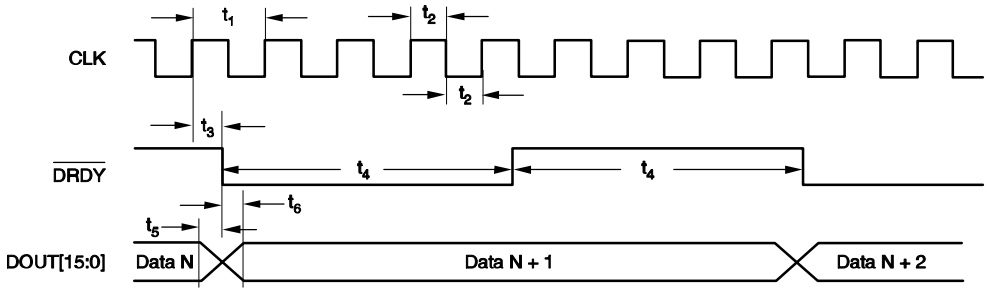


Figure 1. Data Retrieval Timing

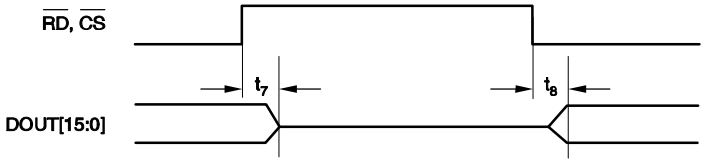


Figure 2. DOUT Inactive/Active Timing

TIMING REQUIREMENTS FOR FIGURES 1 AND 2

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1	CLK period ($1/f_{CLK}$)	20	25		ns
$1/t_1$	f_{CLK}		40	50	MHz
t_2	CLK pulse width, high or low	11.25			ns
t_3	Rising edge of CLK to $\overline{DRDY}$ low		10		ns
t_4	$\overline{DRDY}$ pulse width high or low		$4\ t_1$		ns
t_5	Falling edge of $\overline{DRDY}$ to data invalid			10	ns
t_6	Falling edge of $\overline{DRDY}$ to data valid			15	ns
t_7	Rising edge of $\overline{RD}$ and/or $\overline{CS}$ inactive (high) to DOUT high impedance			15	ns
t_8	Falling edge of $\overline{RD}$ and/or $\overline{CS}$ active (low) to DOUT active.			15	ns

NOTE: Output load = 10pF.

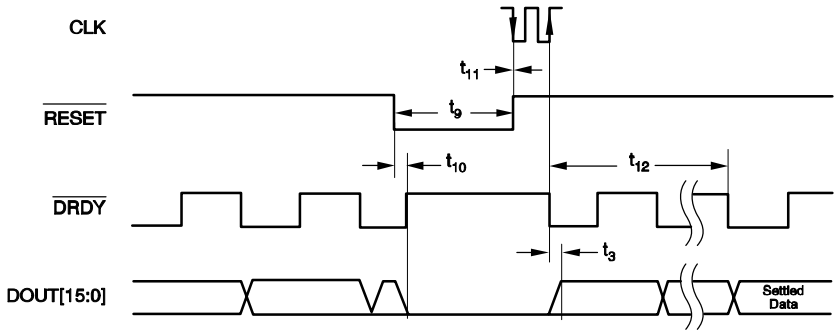


Figure 3. Reset TIming

TIMING REQUIREMENTS FOR FIGURE 3

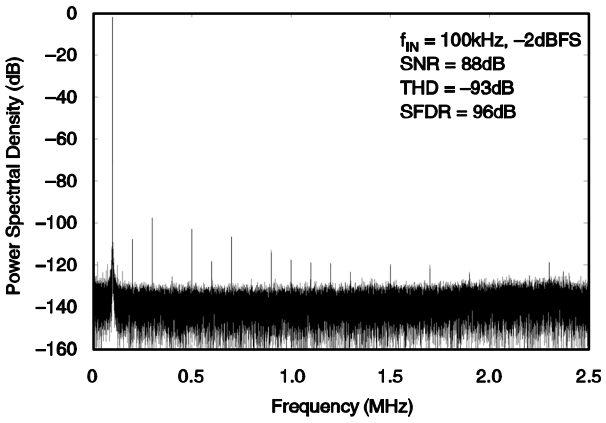
SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_3	Rising edge of CLK to $\overline{\text{DRDY}}$ low		10		ns
t_9	$\overline{\text{RESET}}$ pulse width	50			ns
t_{10}	Delay from $\overline{\text{RESET}}$ active (low) to $\overline{\text{DRDY}}$ forced high and DOUT forced low		9		ns
t_{11}	$\overline{\text{RESET}}$ rising edge to falling edge of CLK	–5		10	ns
t_{12}	Delay from DOUT active to valid DOUT (settling to 0.001%)		47		$\overline{\text{DRDY}}$ Cycles

NOTE: Output load = 10pF.

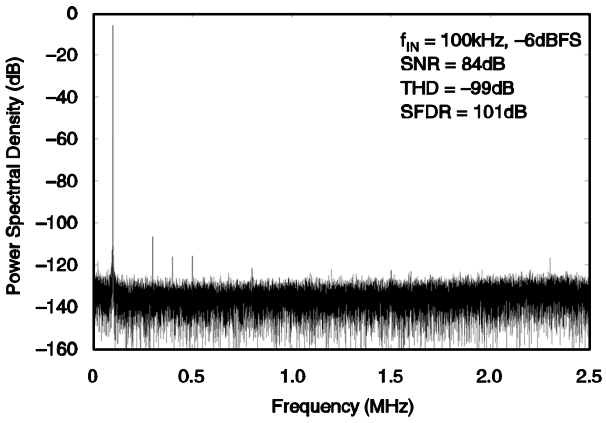
TYPICAL CHARACTERISTICS

All specifications at T_A = 25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, E.xternal V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

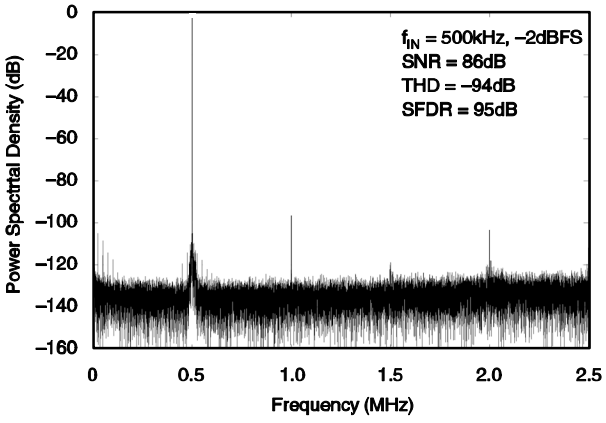
SPECTRAL RESPONSE



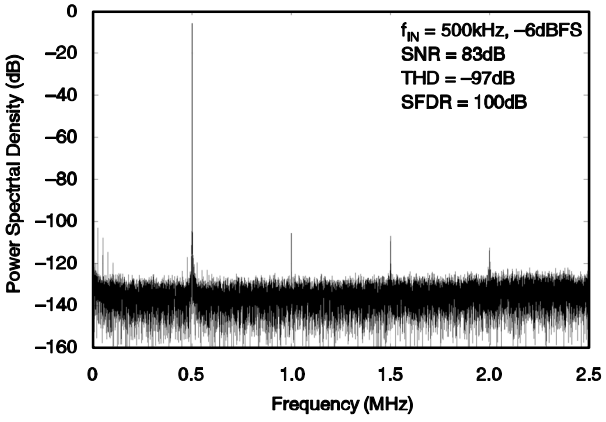
SPECTRAL RESPONSE



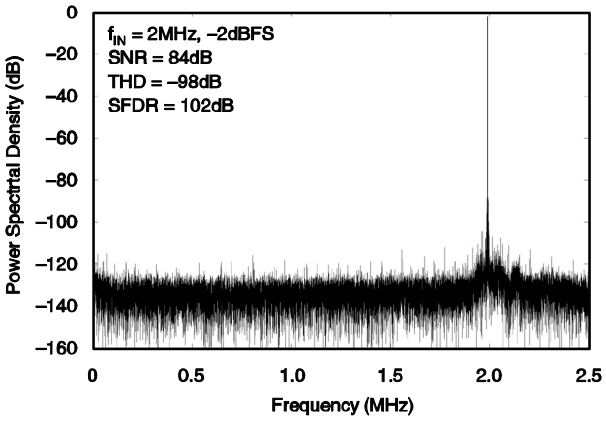
SPECTRAL RESPONSE



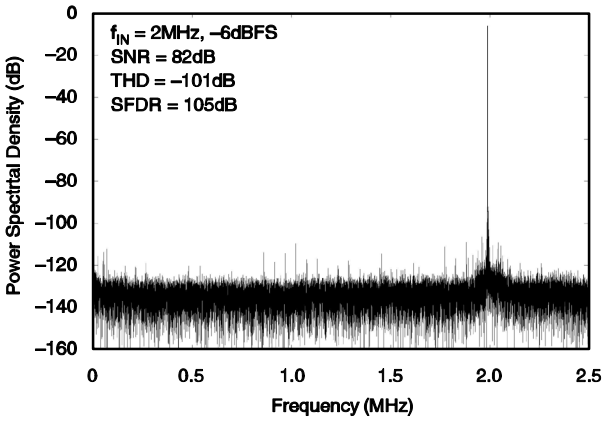
SPECTRAL RESPONSE



SPECTRAL RESPONSE



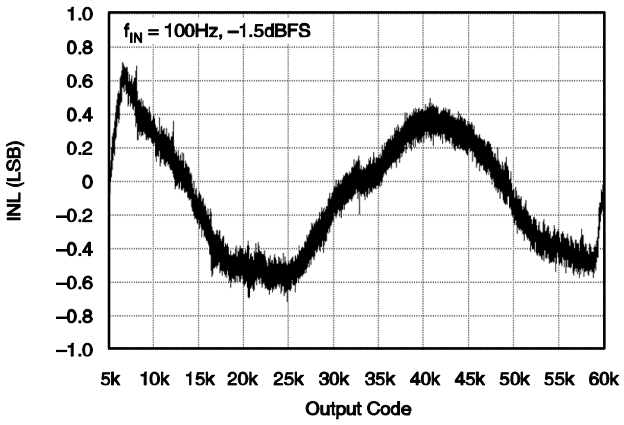
SPECTRAL RESPONSE



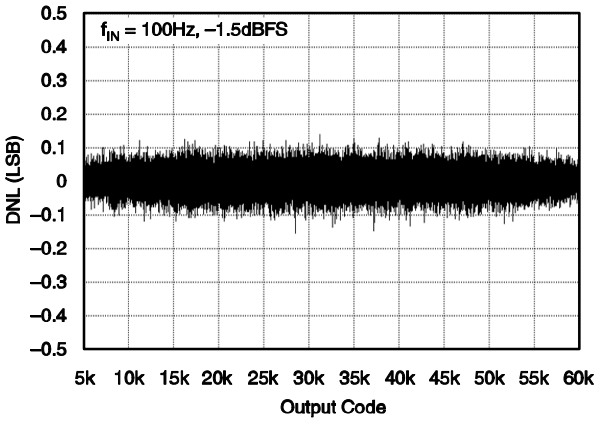
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

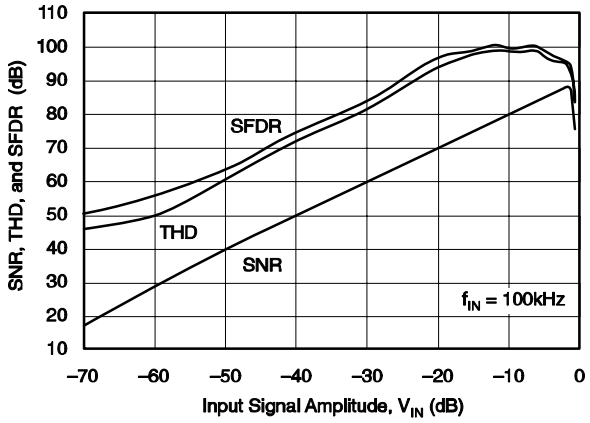
INTEGRAL NONLINEARITY



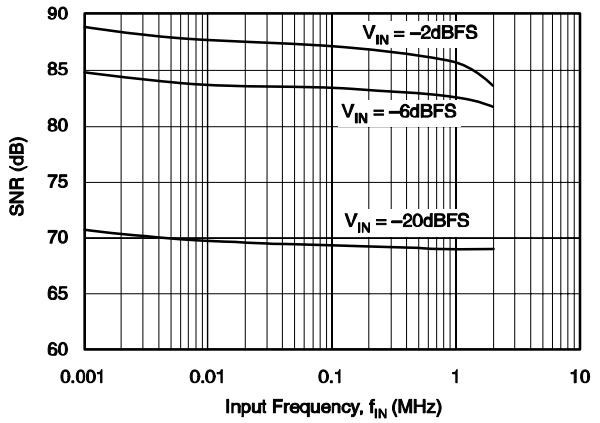
DIFFERENTIAL NONLINEARITY



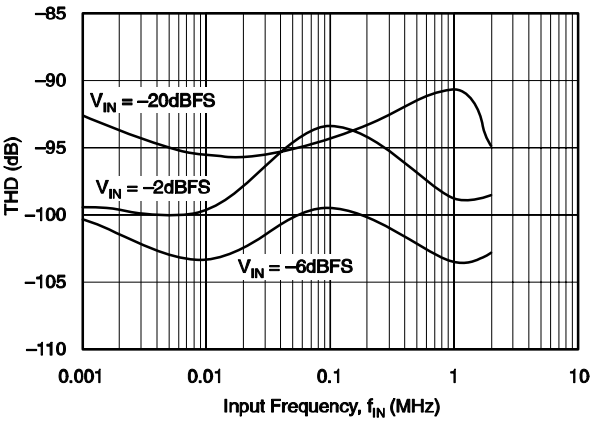
SIGNAL-TO-NOISE RATIO,
TOTAL HARMONIC DISTORTION,
AND SPURIOUS-FREE DYNAMIC RANGE
vs INPUT SIGNAL AMPLITUDE



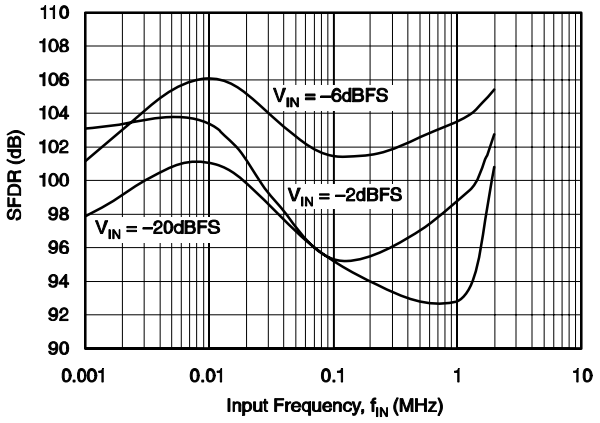
SIGNAL-TO-NOISE RATIO
vs INPUT FREQUENCY



TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



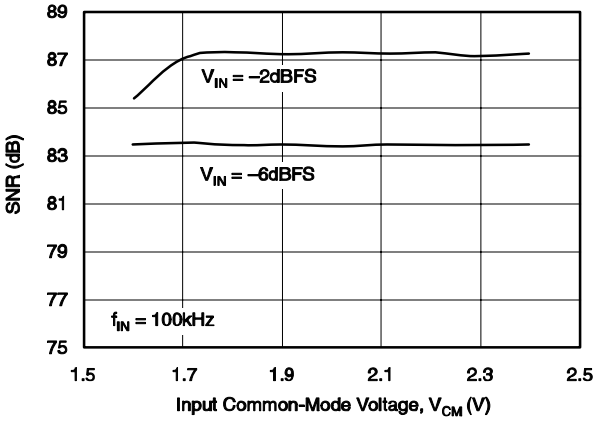
SPURIOUS-FREE DYNAMIC RANGE
vs INPUT FREQUENCY



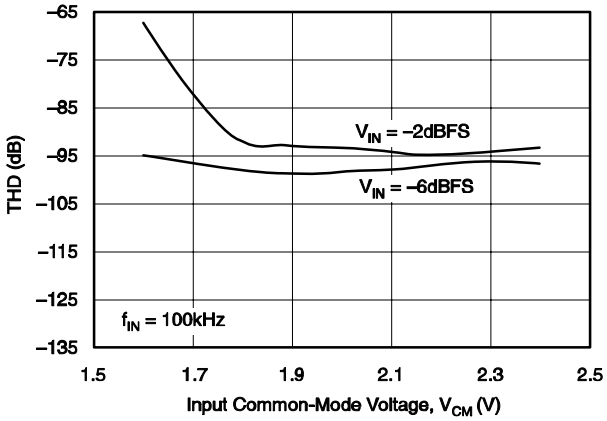
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

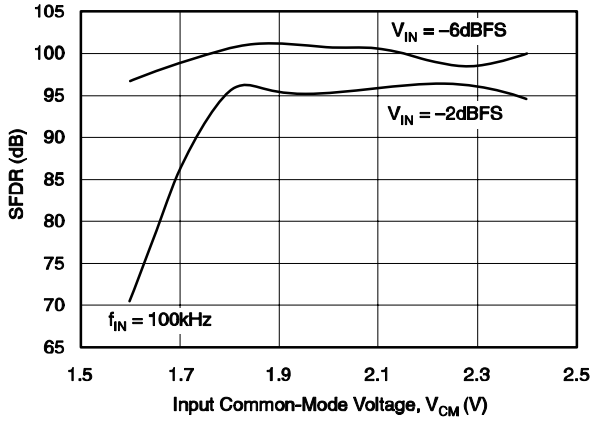
SIGNAL-TO-NOISE RATIO
vs INPUT COMMON-MODE VOLTAGE



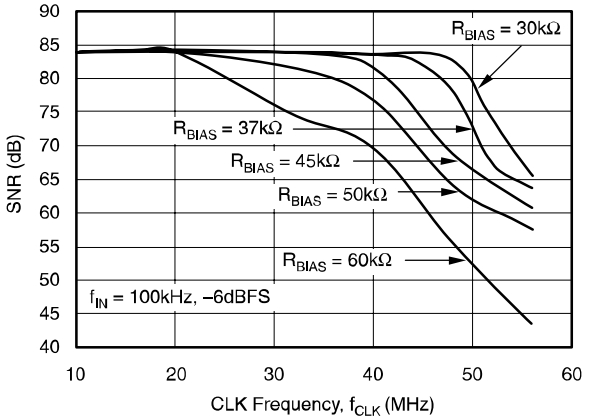
TOTAL HARMONIC DISTORTION
vs INPUT COMMON-MODE VOLTAGE



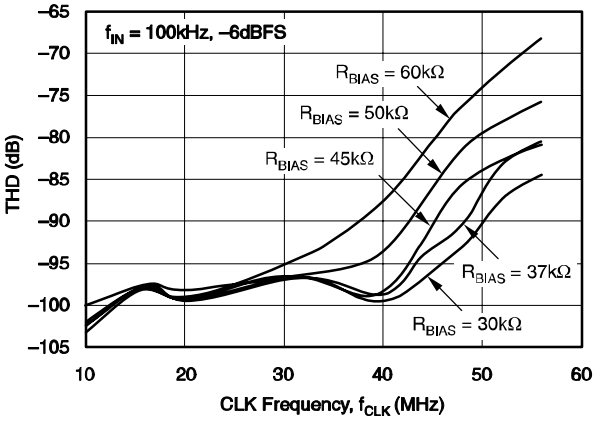
SPURIOUS-FREE DYNAMIC RANGE
vs INPUT COMMON-MODE VOLTAGE



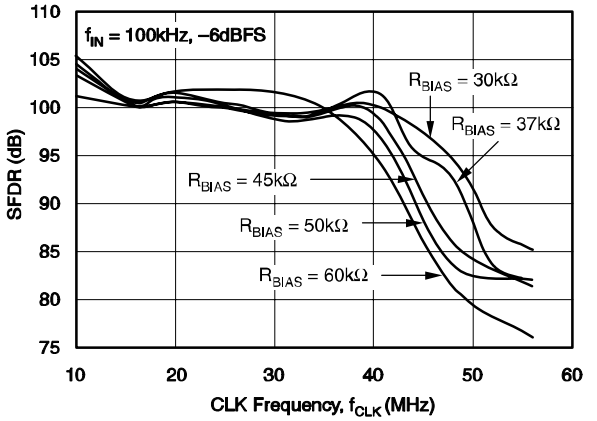
SIGNAL-TO-NOISE RATIO
vs CLK FREQUENCY



TOTAL HARMONIC DISTORTION
vs CLK FREQUENCY



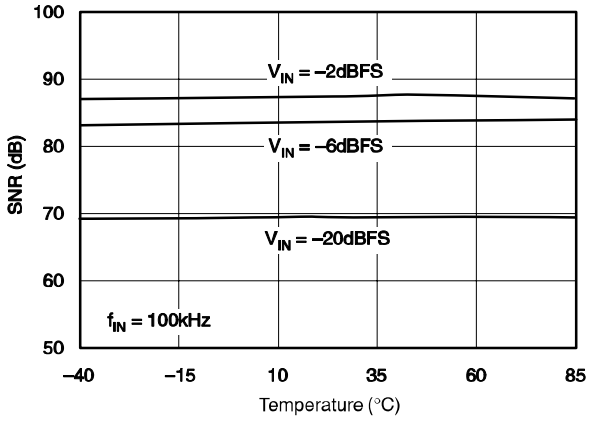
SPURIOUS-FREE DYNAMIC RANGE
vs CLK FREQUENCY



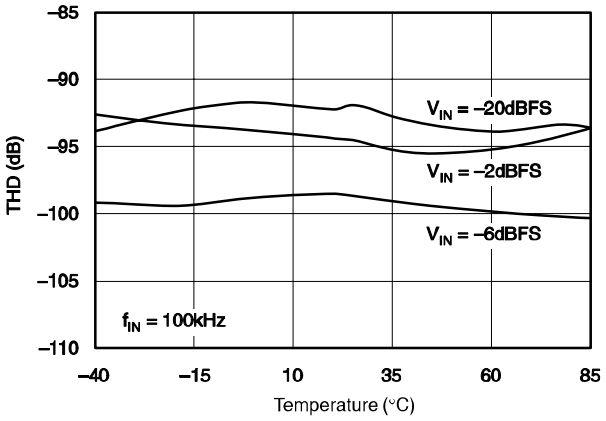
TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, AVDD = 5V, DVDD = IOVDD = 3V, f_{CLK} = 40MHz, External V_{REF} = +3V, 4/$\overline{8}$DRATE = low, V_{CM} = 2.0V, and R_{BIAS} = 37kΩ, unless otherwise noted.

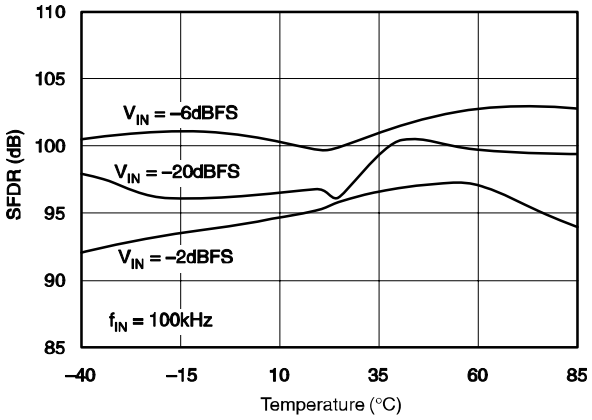
SIGNAL-TO-NOISE RATIO vs TEMPERATURE



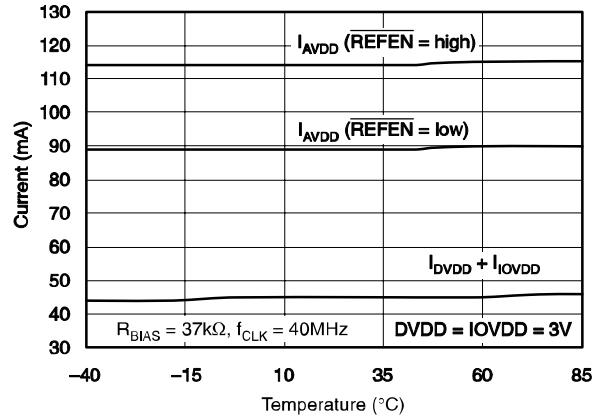
TOTAL HARMONIC DISTORTION vs TEMPERATURE



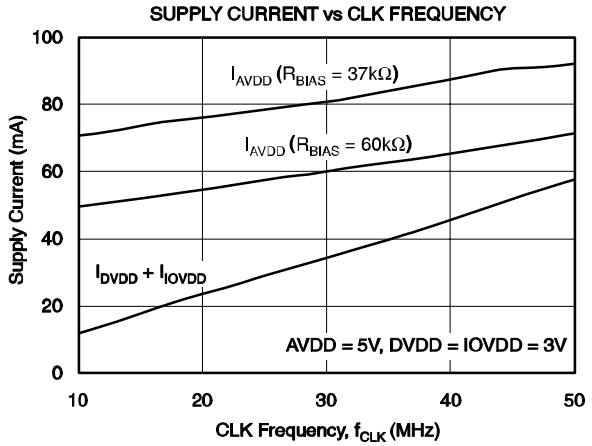
SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE



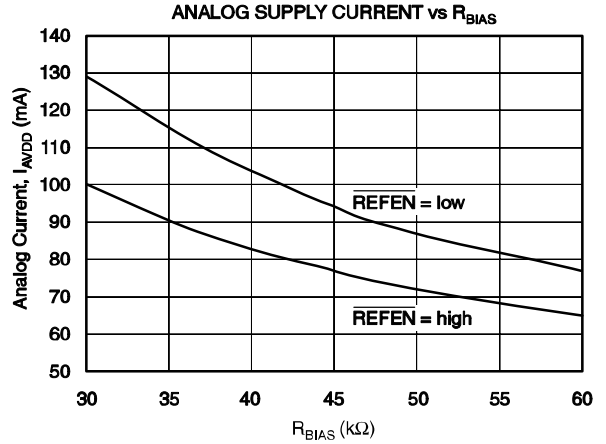
POWER-SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs CLK FREQUENCY



ANALOG SUPPLY CURRENT vs R_{BIAS}



OVERVIEW

The ADS1605 is a high performance delta-sigma ADC with a default oversampling ratio of 8. The modulator uses an inherently stable 2-1-1 MASH architecture incorporating proprietary circuitry that allows for very linear high-speed operation. The modulator samples the input signal at 40MSPS (when f_{CLK} = 40MHz). A low-ripple linear phase digital filter decimates the modulator output to provide data output word rates of 5MSPS with a signal passband out to 2.45MHz. The decimation rate of the filter is set by an external pin, 4/$\overline{8}$DRATE. The default state for this input is low, which sets the decimation rate to 8—most of the data sheet descriptions assume this condition. When this input is taken high, the decimation rate of the filter is reduced to 4. This doubles the data rate, reduces group delay and settling time, and decreases SNR performance.

Conceptually, the ADS1605 modulator and digital filter measure the differential input signal, V_{IN} = (AINP – AINN), against the scaled differential reference, V_{REF} = (VREFP – VREFN), as shown in Figure 4. The voltage reference can either be generated internally by the ADS1605 or supplied externally. A 16-bit parallel data bus, designed for direct connection to DSPs, outputs the data. A separate power supply for the I/O allows flexibility for interfacing to different logic families. Out-of-range conditions are indicated with a dedicated digital output pin. Analog power dissipation is controlled using an external resistor. This allows reduced dissipation when operating at slower speeds. When not in use, the ADS1605 power consumption can be dramatically reduced using the $\overline{PD}$ pin.

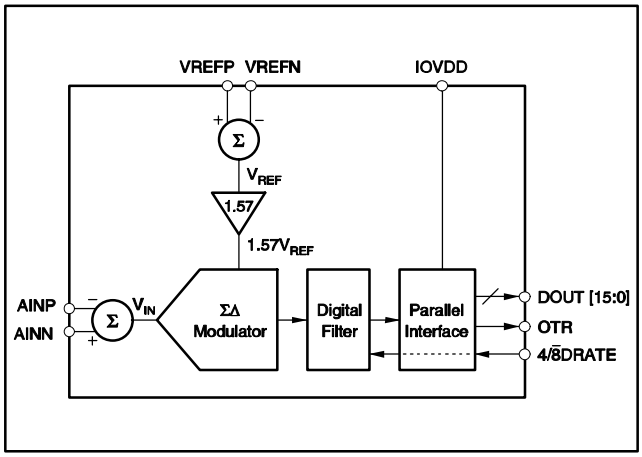


Figure 4. Conceptual Block Diagram

ANALOG INPUTS (AINP, AINN)

The ADS1605 measures the differential signal, V_{IN} = (AINP – AINN), against the differential reference, V_{REF} = (VREFP – VREFN). The reference is scaled internally so that the full-scale differential input voltage is $1.57V_{REF}$. That is, the most positive measurable differential input is $1.57V_{REF}$, which produces the most positive digital output code of 7FFFh. Likewise, the most negative measurable differential input is $–1.57V_{REF}$, which produces the most negative digital output code of 8000h.

The ADS1605 supports a very wide range of input signals. For V_{REF} = 3V, the full scale input voltages are ±4.7V. Having such a wide input range makes out-of-range signals unlikely. However, should an over-range occur, the digital output OTR will go high.

To achieve the highest analog performance, it is recommended that the inputs be limited to $\pm 1.25V_{REF}$ (–2dBFS). For V_{REF} = 3V, the corresponding recommended input range is ±3.75V.

The analog inputs must be driven with a differential signal to achieve optimum performance. The recommended common-mode voltage of the input signal, $V_{CM} = \frac{AINP + AINN}{2}$, is 2.0V. For signals larger than –2dBFS, the input common-mode needs to be raised in order to meet the absolute input voltage specifications. The typical characteristics show how performance varies with input common-mode voltage.

In addition to the differential and common-mode input voltages, the absolute input voltage is also important. This is the voltage on either input (AINP or AINN) with respect to AGND. The range for this voltage is:

–0.1V < (AINN or AINP) < 4.7V.

If either input is taken below –0.1V, ESD protection diodes on the inputs will turn on. Exceeding 4.7V on either input will result in degradation in the linearity performance. If the inputs are taken above AVDD (+5V), ESD protection diodes will turn on.

For signals below –2dBFS, the recommended absolute input voltage is:

0.1V < (AINN or AINP) < 4.2V

Keeping the inputs within this range provides for optimum performance.

INPUT CIRCUITRY

The ADS1605 uses switched-capacitor circuitry to measure the input voltage. Internal capacitors are charged by the inputs and then discharged internally with this cycle repeating at the frequency of CLK. Figure 5 shows a conceptual diagram of these circuits. Switches S2 represent the net effect of the modulator circuitry in discharging the sampling capacitors, the actual implementation is different. The timing for switches S1 and S2 is shown in Figure 6.

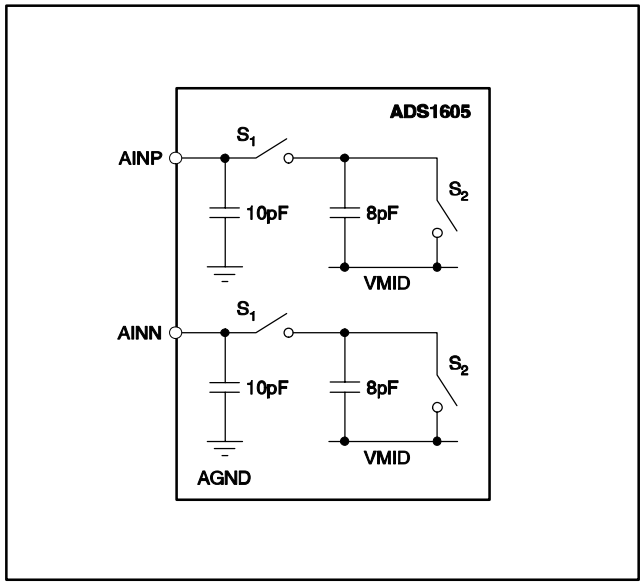


Figure 5. Conceptual Diagram of Internal Circuitry Connected to the Analog Inputs

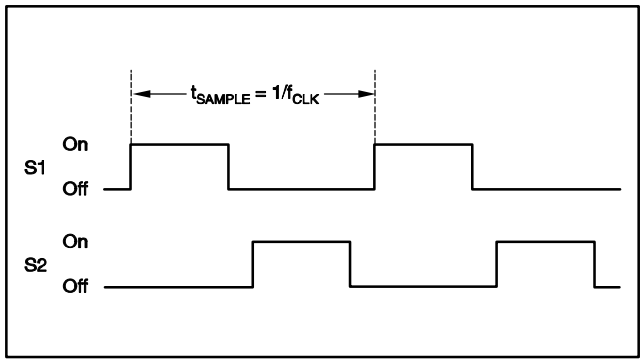


Figure 6. Timing for the Switches in Figure 2

DRIVING THE INPUTS

The external circuits driving the ADS1605 inputs must be able to handle the load presented by the switching capacitors within the ADS1605. The input switches S1 in Figure 5 are closed approximately ½ of the sampling period, t_{sample}, giving only ≈12ns for the internal capacitors to be charged by the inputs, when f_{CLK} = 40MHz.

Figure 7 shows the recommended drivers for applying the input signal. *The analog inputs must be driven differentially to achieve optimum performance.* The external capacitors, between the inputs and from each input to AGND, improve linearity and should be placed as close to the pins as possible. Place the drivers close to the inputs and use good capacitor bypass techniques on their supplies; usually a smaller high-quality ceramic capacitor in parallel with a larger capacitor. Keep the resistances used in the driver circuits low. Their thermal noise will degrade the overall noise performance. When the signal can be ac–coupled to the ADS1605 inputs, a simple RC filter can set the input common mode voltage. The ADS1605 is a high-speed, high–performance ADC. Special care must be taken when selecting the test equipment and setup used with this device. Pay particular attention to the signal sources to ensure they do not limit performance when measuring the ADS1605.

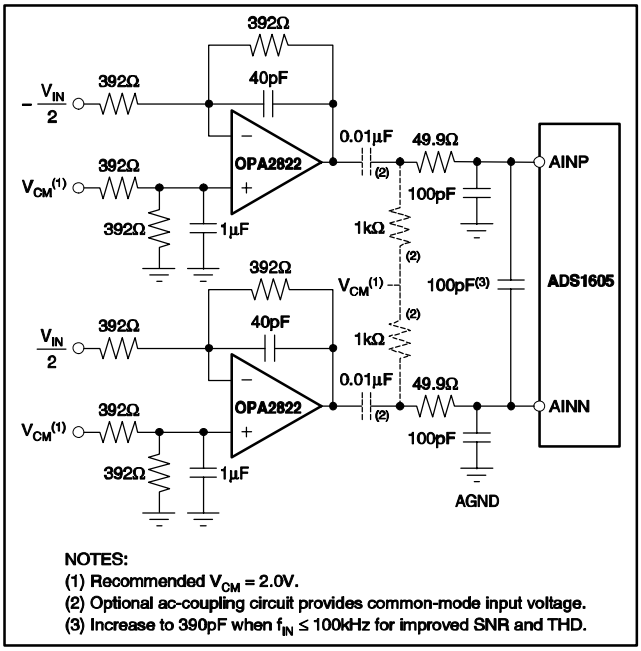


Figure 7. Recommended Driver Circuit for Analog Inputs

REFERENCE INPUTS (VREFN, VREFP, VMID)

Either the internal or an external voltage reference can be used. In either case, the reference voltage V_{REF} is set by the differential voltage between VREFN and VREFP: V_{REF} = (VREFP – VREFN). VREFP and VREFN each use two pins, which should be shorted together. VMID is a voltage equal to approximately 2.5V and is used by the modulator. VCAP connects to an internal node and also must be bypassed with an external capacitor. For the best analog performance, it is recommended that an external reference voltage, V_{REF}, of 3.0V be used.

INTERNAL REFERENCE ($\overline{\text{REFEN}}$ = LOW)

To use the internal reference, set the $\overline{\text{REFEN}}$ pin low. This activates the internal circuitry that generates the reference voltages. The internal reference voltages are applied to the pins. Good bypassing of the reference pins is critical to achieve optimum performance. Figure 8 shows the recommended arrangement. Place the bypass capacitors as close to the pins as possible. Use high quality ceramic capacitors for the smaller values. Avoid loading the internal reference with external circuitry. If the ADS1605 internal reference is to be used by other circuitry, buffer the reference voltages to prevent directly loading the reference pins.

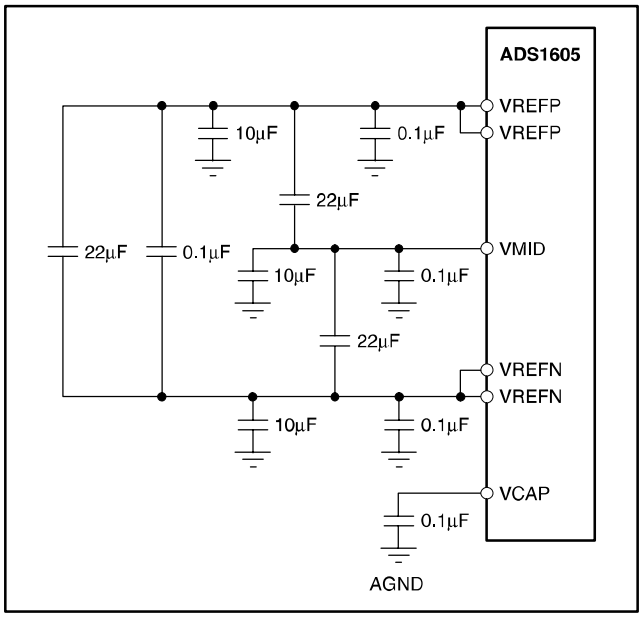


Figure 8. Reference Bypassing When Using the Internal Reference

EXTERNAL REFERENCE ($\overline{\text{REFEN}}$ = HIGH)

To use an external reference, set the $\overline{\text{REFEN}}$ pin high. This deactivates the internal generators for VREFP, VREFN and VMID, and saves approximately 25mA of current on the analog supply (AVDD). The voltages applied to these pins must be within the values specified in the Electrical Characteristics table. Typically VREFP = 4V, VMID = 2.5V and VREFN = 1V. The external circuitry must be capable of providing both a dc and a transient current. Figure 9 shows a simplified diagram of the internal circuitry of the reference when the internal reference is disabled. As with the input circuitry, switches S1 and S2 open and close as shown in Figure 6.

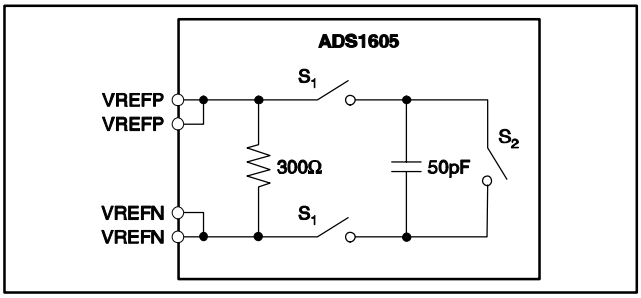


Figure 9. Conceptual Internal Circuitry for the Reference When $\overline{\text{REFEN}}$ = High

Figure 10 shows the recommended circuitry for driving these reference inputs. Keep the resistances used in the buffer circuits low to prevent excessive thermal noise from degrading performance. Layout of these circuits is critical, make sure to follow good high-speed layout practices. Place the buffers and especially the bypass capacitors as close to the pins as possible. VCAP is unaffected by the setting on $\overline{\text{REFEN}}$ and must be bypassed when using the internal or an external reference.

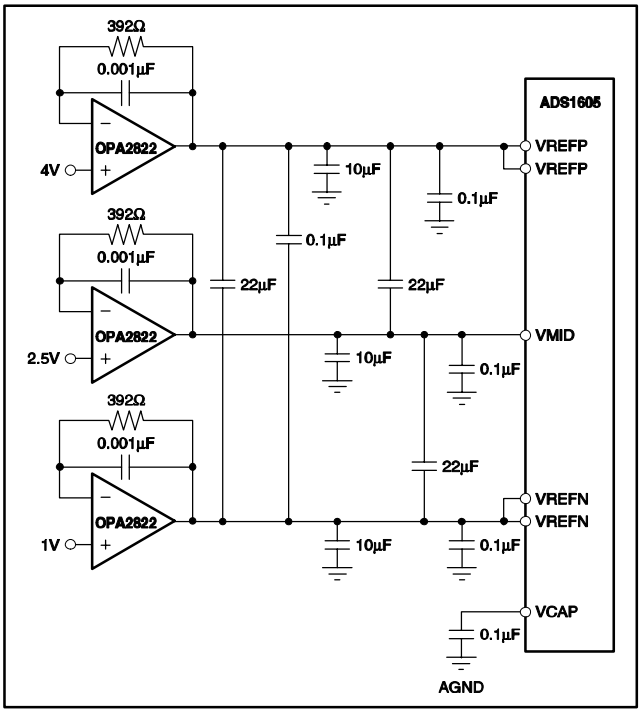


Figure 10. Recommended Buffer Circuit When Using an External Reference

CLOCK INPUT (CLK)

The ADS1605 requires an external clock signal to be applied to the CLK input pin. The sampling of the modulator is controlled by this clock signal. As with any high-speed data converter, a high quality clock is essential for optimum performance. Crystal clock oscillators are the recommended CLK source; other sources, such as frequency synthesizers are usually not adequate. Make sure to avoid excess ringing on the CLK input; keeping the trace as short as possible will help.

Measuring high frequency, large amplitude signals requires tight control of clock jitter. The uncertainty during sampling of the input from clock jitter limits the maximum achievable SNR. This effect becomes more pronounced with higher frequency and larger magnitude inputs. Fortunately, the ADS1605 oversampling topology reduces clock jitter sensitivity over that of Nyquist rate converters like pipeline and successive approximation converters by a factor of $\sqrt{8}$.

In order to not limit the ADS1605 SNR performance, keep the jitter on the clock source below the values shown in Table 1. When measuring lower frequency and lower amplitude inputs, more CLK jitter can be tolerated. In determining the allowable clock source jitter, select the worst-case input (highest frequency, largest amplitude) that will be seen in the application.

Table 1. Maximum Allowable Clock Source Jitter for Different Input Signal Frequencies and Amplitude

INPUT SIGNAL		MAXIMUM ALLOWABLE CLOCK SOURCE JITTER
MAXIMUM FREQUENCY	MAXIMUM AMPLITUDE	
2MHz	–2dB	1.9ps
2MHz	–20dB	14ps
1MHz	–2dB	3.8ps
1MHz	–20dB	28ps
500kHz	–2dB	7.6ps
500kHz	–20dB	57ps
100kHz	–2dB	38ps
100kHz	–20dB	285ps

RESET ($\overline{\text{RESET}}$)

The ADS1605 is asynchronously reset when the $\overline{\text{RESET}}$ pin is taken low. During reset, all of the digital circuits are cleared, DOUT[15:0] are forced low, and $\overline{\text{DRDY}}$ forced high. It is recommended that the $\overline{\text{RESET}}$ pin be released on the falling edge of CLK. Afterwards, $\overline{\text{DRDY}}$ goes low on the second rising edge of CLK. Allow 47 $\overline{\text{DRDY}}$ cycles for the digital filter to settle before retrieving data. See Figure 3 for the timing specifications.

Reset can be used to synchronize multiple ADS1605s. All devices to be synchronized must use a common CLK input. With the CLK inputs running, pulse $\overline{\text{RESET}}$ on the falling edge of CLK, as shown in Figure 11. Afterwards, the converters will be converting synchronously with the $\overline{\text{DRDY}}$ outputs updating simultaneously. After synchronization, allow 47 $\overline{\text{DRDY}}$ cycles (t_{12}) for output data to fully settle.

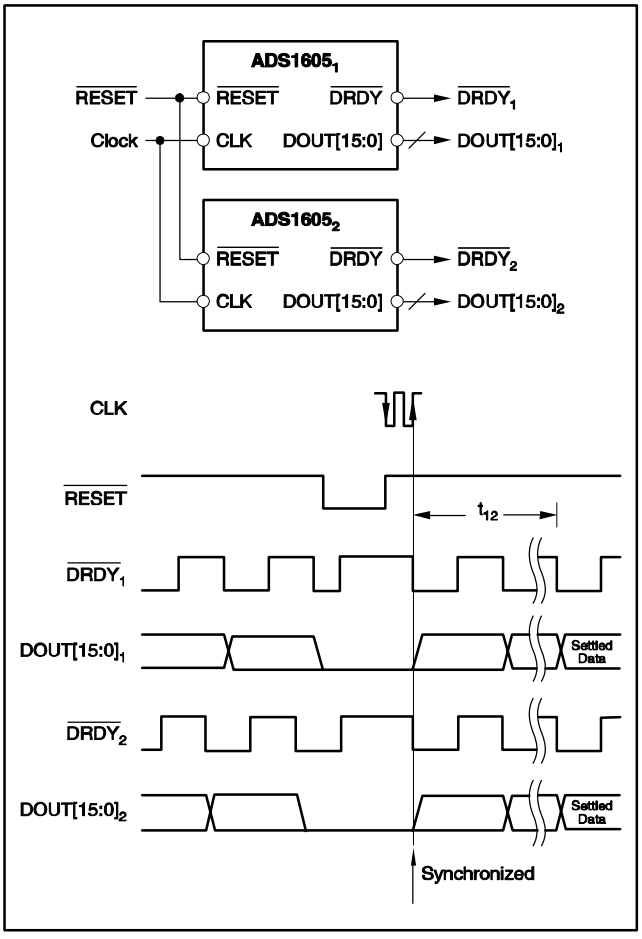


Figure 11. Synchronizing Multiple Converters

DATA FORMAT

The 16-bit output data is in binary two's complement format as shown in Table 2. When the input is positive out-of-range, exceeding the positive full-scale value of $1.57V_{REF}$, the output clips to all 7FFFh and the OTR output goes high. Likewise, when the input is negative out-of-range by going below the negative full-scale value of $-1.57V_{REF}$, the output clips to 8000h and the OTR output goes high. The OTR remains high while the input signal is out-of-range.

Table 2. Output Code Versus Input Signal

INPUT SIGNAL (INP – INN)	IDEAL OUTPUT CODE(1)	OTR
≥+1.57V_{REF} (> 0dB)	$7FFF_H$	1
1.57V_{REF} (0dB)	$7FFF_H$	0
+1.25V_{REF} (–2dB)	$50BA_H$	0
$\frac{+1.57V_{REF}}{2^{15}-1}$	0001_H	0
0	0000_H	0
$\frac{+1.57V_{REF}}{2^{15}-1}$	$FFFF_H$	0
$-1.57V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000_H	0
$\le -1.57V_{REF}\left(\frac{2^{15}}{2^{15}-1}\right)$	8000_H	1

(1) Excludes effects of noise, INL, offset and gain errors.

OUT-OF-RANGE INDICATION (OTR)

If the output code on DOUT[15:0] exceeds the positive or negative full-scale, the out-of-range digital output OTR will go high on the falling edge of $\overline{DRDY}$. When the output code returns within the full-scale range, OTR returns low on the falling edge of $\overline{DRDY}$.

DATA RETRIEVAL

Data retrieval is controlled through a simple parallel interface. The falling edge of the $\overline{DRDY}$ output indicates new data is available. To activate the output bus, both $\overline{CS}$ and $\overline{RD}$ must be low, as shown in Table 3. Make sure the DOUT bus does not drive heavy loads (> 20pF), as this will degrade performance. Use an external buffer when driving an edge connector or cables.

Table 3. Truth Table for $\overline{CS}$ and $\overline{RD}$

$\overline{CS}$	$\overline{RD}$	DOUT[15:0]
0	0	Active
0	1	High impedance
1	0	High impedance
1	1	High impedance

SETTLING TIME

The settling time is an important consideration when measuring signals with large steps or when using a multiplexer in front of the analog inputs. The ADS1605 digital filter requires time for an instantaneous change in signal level to propagate to the output.

Be sure to allow the filter time to settle after applying a large step in the input signal, switching the channel on a multiplexer placed in front of the inputs, resetting the ADS1605, or exiting the power-down mode,

Figure 12 shows the settling error as a function of time for a full-scale signal step applied at t = 0 with 4/$\overline{8}$DRATE = low. This figure uses $\overline{DRDY}$ cycles for the time scale (X-axis). After 47 $\overline{DRDY}$ cycles, the settling error drops below 0.001%. For f_{CLK} = 40MHz, this corresponds to a settling time of 9.4µs.

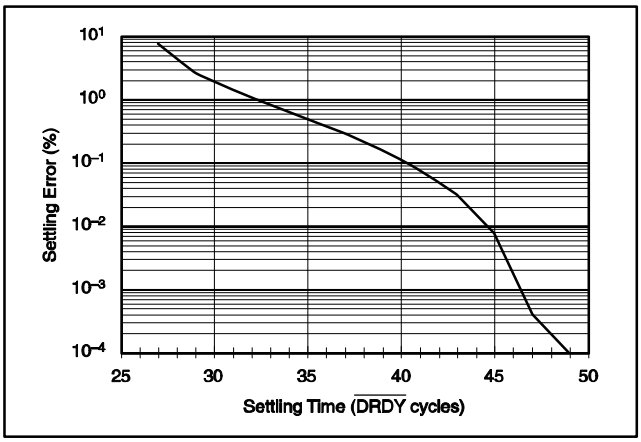


Figure 12. Settling Time

IMPULSE RESPONSE

Figure 13 plots the normalized response for an input applied at t = 0 with 4/$\overline{8}$DRATE = low. The X-axis units of time are $\overline{DRDY}$ cycles. As shown in Figure 13, the peak of the impulse takes 26 $\overline{DRDY}$ cycles to propagate to the output. For f_{CLK} = 40MHz, a $\overline{DRDY}$ cycle is 0.2µs in duration and the propagation time (or group delay) is 26 × 0.2µs = 5.2µs.

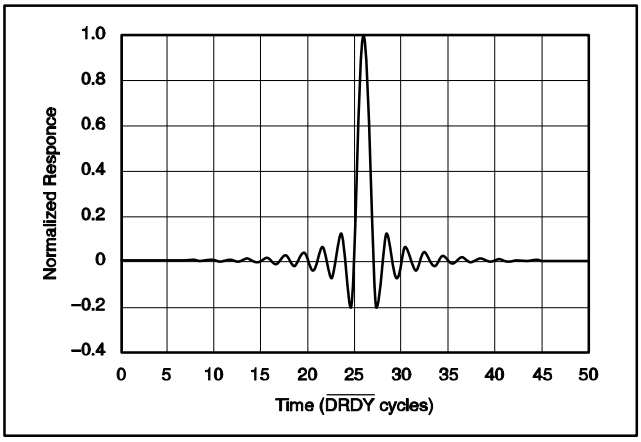


Figure 13. Impulse Response

FREQUENCY RESPONSE

The linear phase FIR digital filter sets the overall frequency response. The decimation rate is set to 8 (4/$\overline{8}$DRATE = low) for all the figures shown in this section. Figure 14 shows the frequency response from DC to 20MHz for f_{CLK} = 40MHz. The frequency response of the ADS1605 filter scales directly with CLK frequency. For example, if the CLK frequency is decreased by half (to 20MHz), the values on the X-axis in Figure 14 would need to be scaled by half, with the span becoming DC to 10MHz.

Figure 15 shows the passband ripple from DC to 2.2MHz (f_{CLK} = 40MHz). Figure 16 shows a closer view of the passband transition by plotting the response from 2.0MHz to 2.5MHz (f_{CLK} = 40MHz).

The overall frequency response repeats at multiples of the CLK frequency. To help illustrate this, Figure 17 shows the response out to 120MHz (f_{CLK} = 40MHz). Notice how the passband response repeats at 40MHz, 80MHz and 120MHz; it is important to consider this when there is high-frequency noise present with the signal. The modulator bandwidth extends to 100MHz. High-frequency noise around 40MHz and 80MHz will not be attenuated by either the modulator or the digital filter. This noise will alias back in-band and reduce the overall SNR performance unless it is filtered out prior to the ADS1605. To prevent this, place an anti-alias filter in front of the ADS1605 that rolls off before 37MHz.

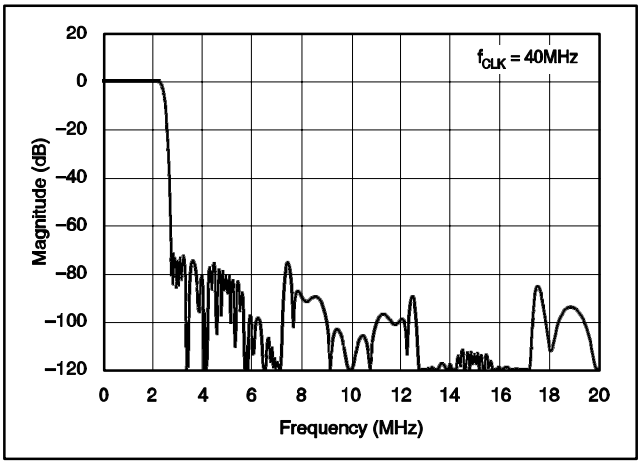


Figure 14. Frequency Response.

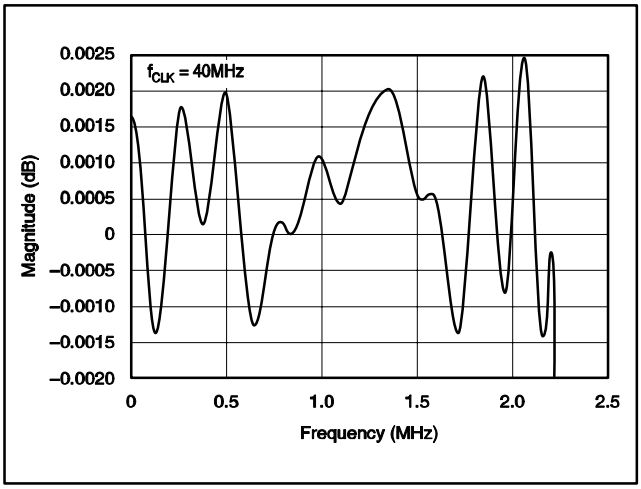


Figure 15. Passband Ripple

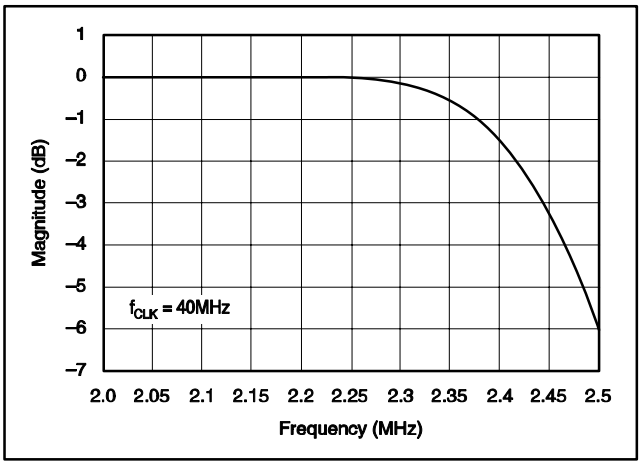


Figure 16. Passband Transition

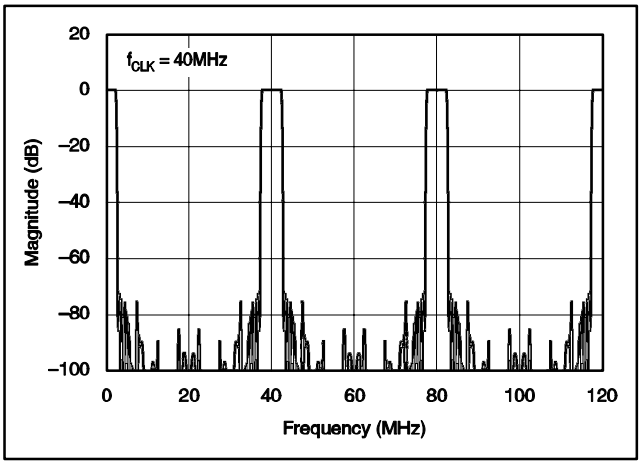


Figure 17. Frequency Response Out to 120MHz

ANALOG POWER DISSIPATION

An external resistor connected between the RBIAS pin and the analog ground sets the analog current level, as shown in Figure 18. The current is inversely proportional to the resistor value. Table 4 shows the recommended values of R_{BIAS} for different CLK frequencies. Notice that the analog current can be reduced when using a slower frequency CLK input, as the modulator has more time to settle. Avoid adding any capacitance in parallel to R_{BIAS} , as this will interfere with the internal circuitry used to set the biasing.

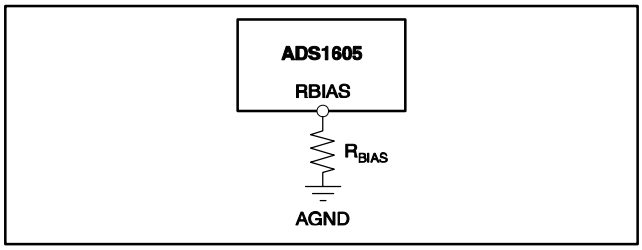


Figure 18. External Resistor Used to Set Analog Power Dissipation

Table 4. Recommended R_{BIAS} Resistor Values for Different CLK Frequencies

f_{CLK}	DATA RATE	R_{BIAS}	TYPICAL POWER DISSIPATION WITH $\overline{REFEN}$ HIGH
16MHz	2MHz	60kΩ	315mW
24MHz	3MHz	50kΩ	400mW
32MHz	4MHz	45kΩ	475mW
40MHz	5MHz	37kΩ	570mW

POWER DOWN ($\overline{PD}$)

When not in use, the ADS1605 can be powered down by taking the $\overline{PD}$ pin low. All circuitry will be shutdown, including the voltage reference. To minimize the digital current during power down, stop the clock signal supplied to the CLK input. There is an internal pull-up resistor of 170kΩ on the $\overline{PD}$ pin, but it is recommended that this pin be connected to IOVDD if not used. Make sure to allow time for the reference to startup after exiting power-down mode. The Electrical Characteristics table shows this value when using the internal reference. After the reference has stabilized, allow at least 100 $\overline{DRDY}$ cycles for the modulator and digital filter to settle before retrieving data.

POWER SUPPLIES

Three supplies are used on the ADS1605: analog (AVDD), digital (DVDD) and digital I/O (IOVDD). Each supply must be suitably bypassed to achieve the best performance. It is recommended that a 1μF and 0.1μF ceramic capacitor be placed as close to each supply pin as possible. Connect each supply-pin bypass capacitor to the associated ground, as shown in Figure 19. Each main supply bus should also be bypassed with a bank of capacitors from 47μF to 0.1μF, as shown.

The IO and digital supplies (IOVDD and DVDD) can be connected together when using the same voltage. In this case, only one bank of 47μF to 0.1μF capacitors is needed on the main supply bus, though each supply pin must still be bypassed with a 1μF and 0.1μF ceramic capacitor.

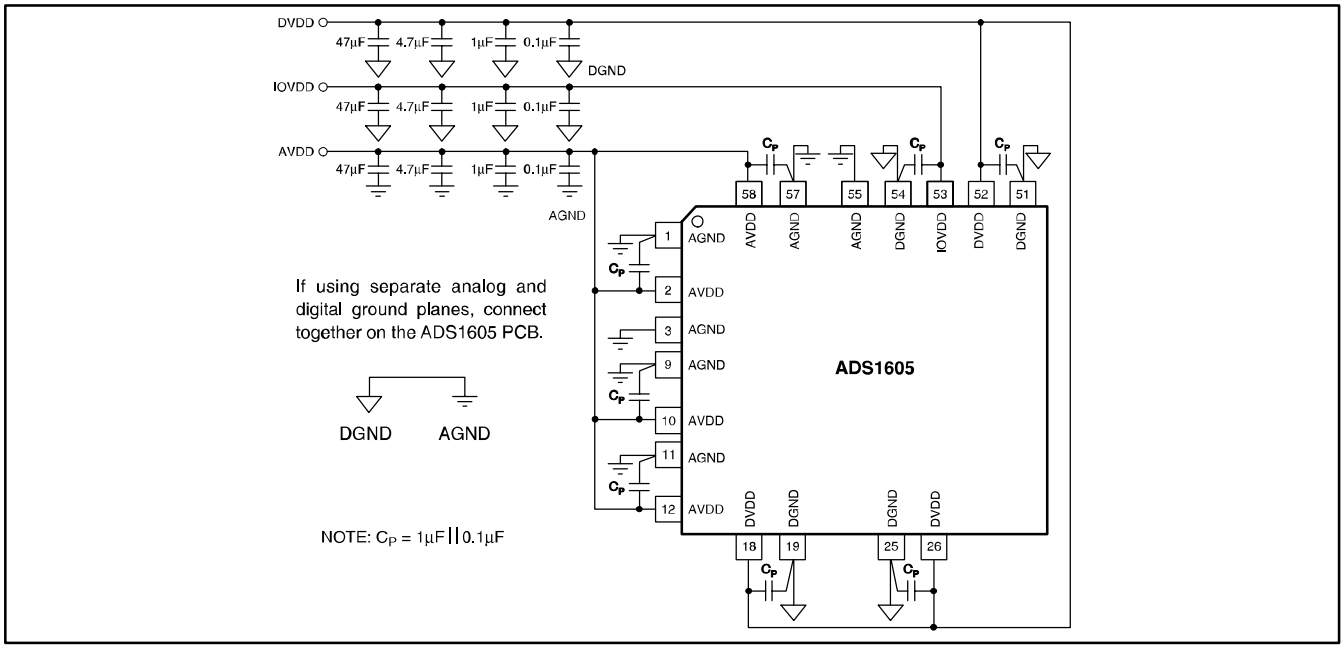


Figure 19. Recommended Power-Supply Bypassing

DECIMATION RATE (4/$\overline{8}$DRATE)

The 4/$\overline{8}$DRATE digital input sets the decimation rate of the digital filter. When 4/$\overline{8}$DRATE = low, the decimation rate = 8. When 4/$\overline{8}$DRATE = high, the decimation rate = 4. For the highest SNR performance, 4/$\overline{8}$DRATE must be set low. Decreasing the decimation rate from 8 to 4 doubles the data rate. For f_{CLK} = 40MHz, the data rate then becomes 10MSPS with this lower decimation value. In addition, the group delay decreases to 0.9µs and the settling time becomes 1.3µs or 13 $\overline{DRDY}$ cycles. With the reduced decimation rate, the noise increases. Typical SNR performance degrades by 14dB when the decimation rate is 4 versus 8. THD remains approximately the same. There is an internal pull-down resistor of 170kΩ on the 4/$\overline{8}$DRATE, however, it is recommended this pin be forced either high or low.

LAYOUT ISSUES

The ADS1605 is a very high-speed, high-resolution data converter. In order to achieve the maximum performance, careful attention must be given to the printed circuit board (PCB) layout. Use good high-speed techniques for all circuitry. Critical capacitors should be placed close to pins as possible. These include capacitors directly connected to the analog and reference inputs and the power supplies. Make sure to also properly bypass all circuitry driving the inputs and references.

Two approaches can be used for the ground planes: either a single common plane; or two separate planes, one for the analog grounds and one for the digital grounds. When using only one common plane, isolate the flow of current on pin 58 from pin 1; use breaks on the ground plane to accomplish this. Pin 58 carries the switching current from the analog clocking for the modulator and can corrupt the quiet analog ground on pin 1. When using two planes, it is recommended that they be tied together right at the PCB. Do not try to connect the ground planes together after running separately through edge connectors or cables as this reduces performance and increases the likelihood of latchup.

In general, keep the resistances used in the driving circuits for the inputs and reference low to prevent excess thermal noise from degrading overall performance. Avoid having the ADS1605 digital outputs drive heavy loads. Buffers on the outputs are recommended unless the ADS1605 is connected directly to a DSP or controller situated nearby. Additionally, make sure the digital inputs are driven with clean signals as ringing on the inputs can introduce noise.

The ADS1605 uses TI PowerPAD technology. The PowerPAD is physically connected to the substrate of the silicon inside the package and must be soldered to the analog ground plane on the PCB using the exposed metal pad underneath the package for proper heat dissipation. Please refer to application report SLMA002, located at www.ti.com, for more details on the PowerPAD package.

APPLICATIONS

INTERFACING THE ADS1605 TO THE TMS320C6000

Figure 20 illustrates how to directly connect the ADS1605 to the TMS320C6000 digital signal processor. The processor controls reading using output $\overline{ARE}$. The ADS1605 is selected using the DSP control output, $\overline{CE2}$. The ADS1605 16-bit data output bus is directly connected to the TMS320C6000 data bus. The data ready output from the ADS1605, $\overline{DRDY}$, drives interrupt $\overline{EXT\_INT7}$ on the TMS320C6000.

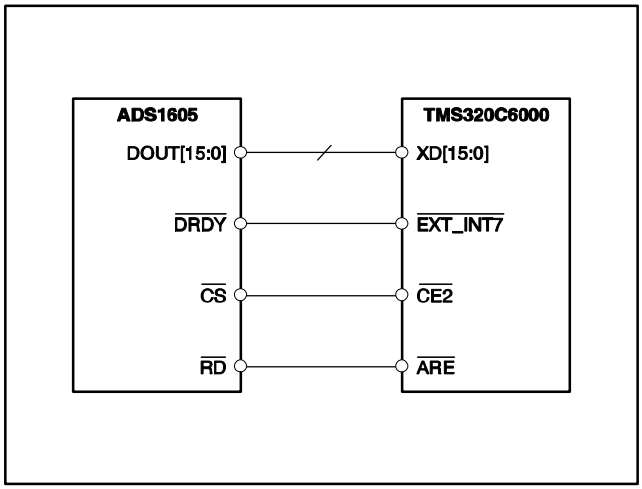


Figure 20. ADS1605/TMS320C6000 Interface Connection

INTERFACING THE ADS1605 TO THE TMS320C5400

Figure 21 illustrates how to connect the ADS1605 to the TMS320C5400 digital signal processor (DSP). The processor controls the reading using the outputs R/$\overline{W}$ and $\overline{IS}$. The I/O space select signal ($\overline{IS}$) is optional and is used to prevent the ADS1605 $\overline{RD}$ input from being strobed when the DSP is accessing other external memory spaces (address or data). This can help reduce the possibility of digital noise coupling into the ADS1605. When not using this signal, replace NAND gate U1 with an inverter between R/$\overline{W}$ and $\overline{RD}$. Two signals, $\overline{IOSTRB}$ and A15 combine using NAND gate U2 to select the ADS1605. If there are no additional devices connected to the TMS320C5400 I/O space, U2 can be eliminated. Simply connect $\overline{IOSTRB}$ directly to $\overline{CS}$. The ADS1605 16-bit data output bus is directly connected to the TMS320C5400 data bus. The data ready output from the ADS1605, $\overline{DRDY}$, drives interrupt $\overline{INT3}$ on the TMS320C5400.

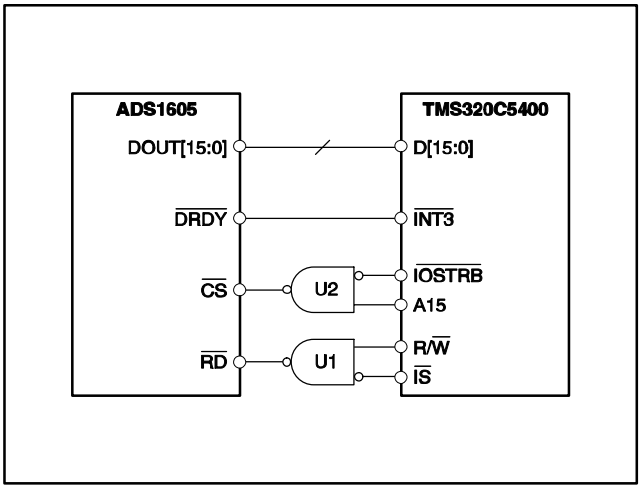
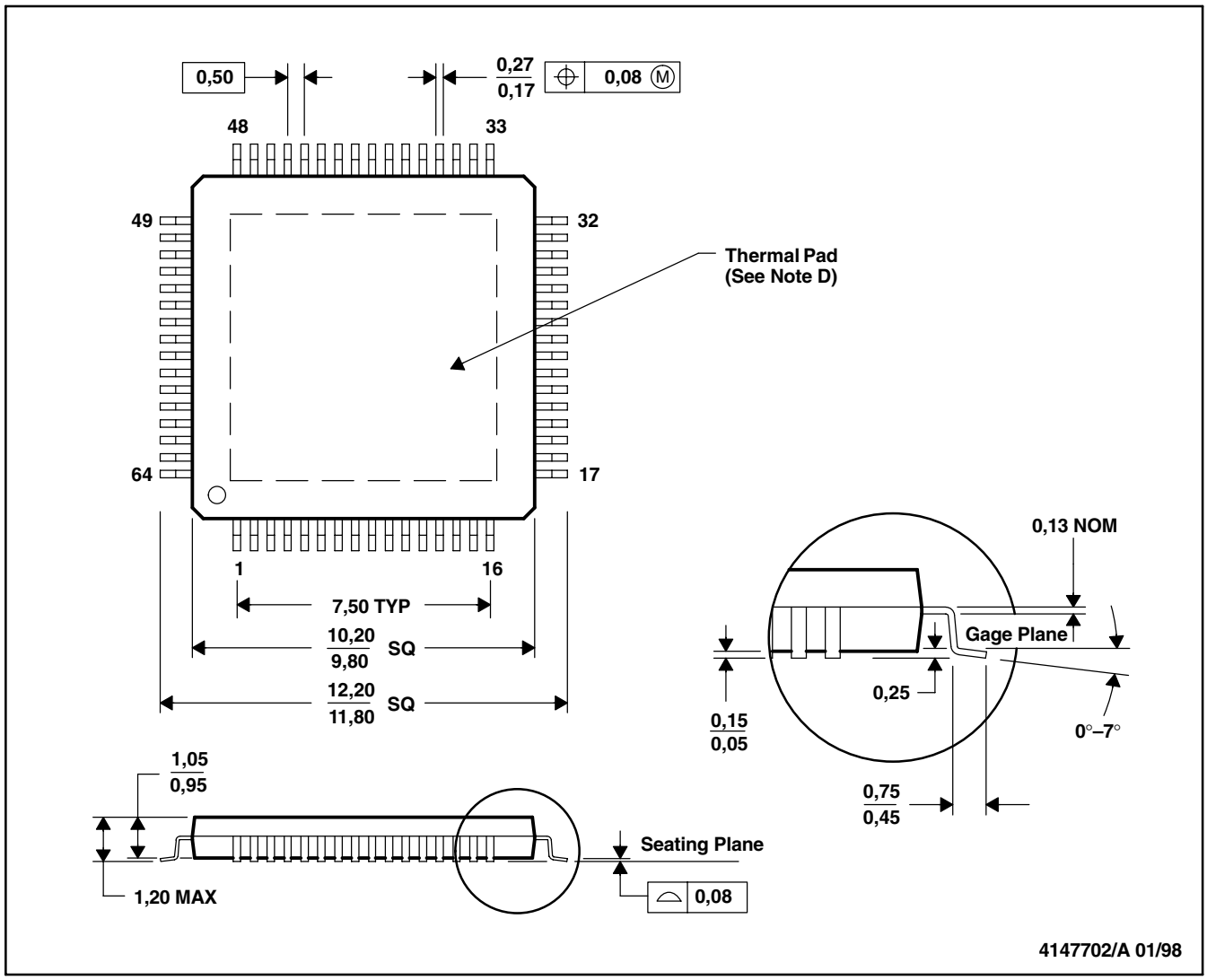


Figure 21. ADS1605/TMS320C5400 Interface Connection

Code Composer Studio, available from TI, provides support for interfacing TI DSPs through a collection of data converter plugins. Check the TI website, located at www.ti.com/sc/dcplug–in, for the latest information on ADS1605 support.

PAP (S-PQFP-G64) **PowerPAD™ PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS-026

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