SONY

LCX016AM

3.3cm (1.3-inch) Black-and-White LCD Panel

Preliminary

Description

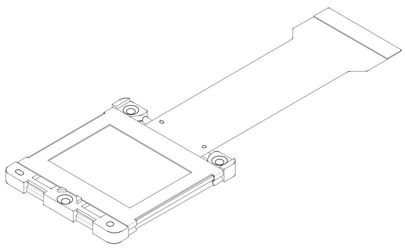
The LCX016AM is a 3.3cm diagonal active matrix TFT-LCD panel addressed by polycrystalline silicon super thin film transistors with a built-in peripheral driving circuit. Use of three LCX016AM panels provides a full-color representation. The striped arrangement suitable for data projectors is capable of displaying fine text and vertical lines.

The adoption of an advanced on-chip black matrix realizes high picture quality without cross talk by incorporating a high luminance screen and cross talk free circuit.

This panel has a polysilicon TFT high-speed scanner and built-in function to display images up/down and/or right/left inverse. The built-in 5V interface circuit leads to lower voltage of timing and control signals.

The panel contains an active area variable circuit which supports MAC17/SVGA/VGA/PC98 data signals by changing the active area according to the type of input signal. In addition, double-speed processed NTSC/PAL can also be supported.

The adoption of a micro-lens increases the utilization efficiency of incident light, resulting in an optical transmittance of 30% or more with parallel incident light.



Features

- Number of active dots: 519,000 (1.3-inch, 3.3cm in diagonal)
- Accepts the computer requirements of MAC17 (832 × 624), SVGA (800 × 600), VGA (640 × 480) and PC98 (640 × 400) platforms
- Supports NTSC (640 × 480) and PAL (762 × 572) by processing the video signal at double speed
- High optical transmittance: 30% or more (with parallel incident light)
- Built-in cross talk free circuit
- High contrast ratio with normally white mode: 200 (typ.)
- Built-in H and V drivers (built-in input level conversion circuit, 5V driving possible)
- Up/down and/or right/left inverse display function

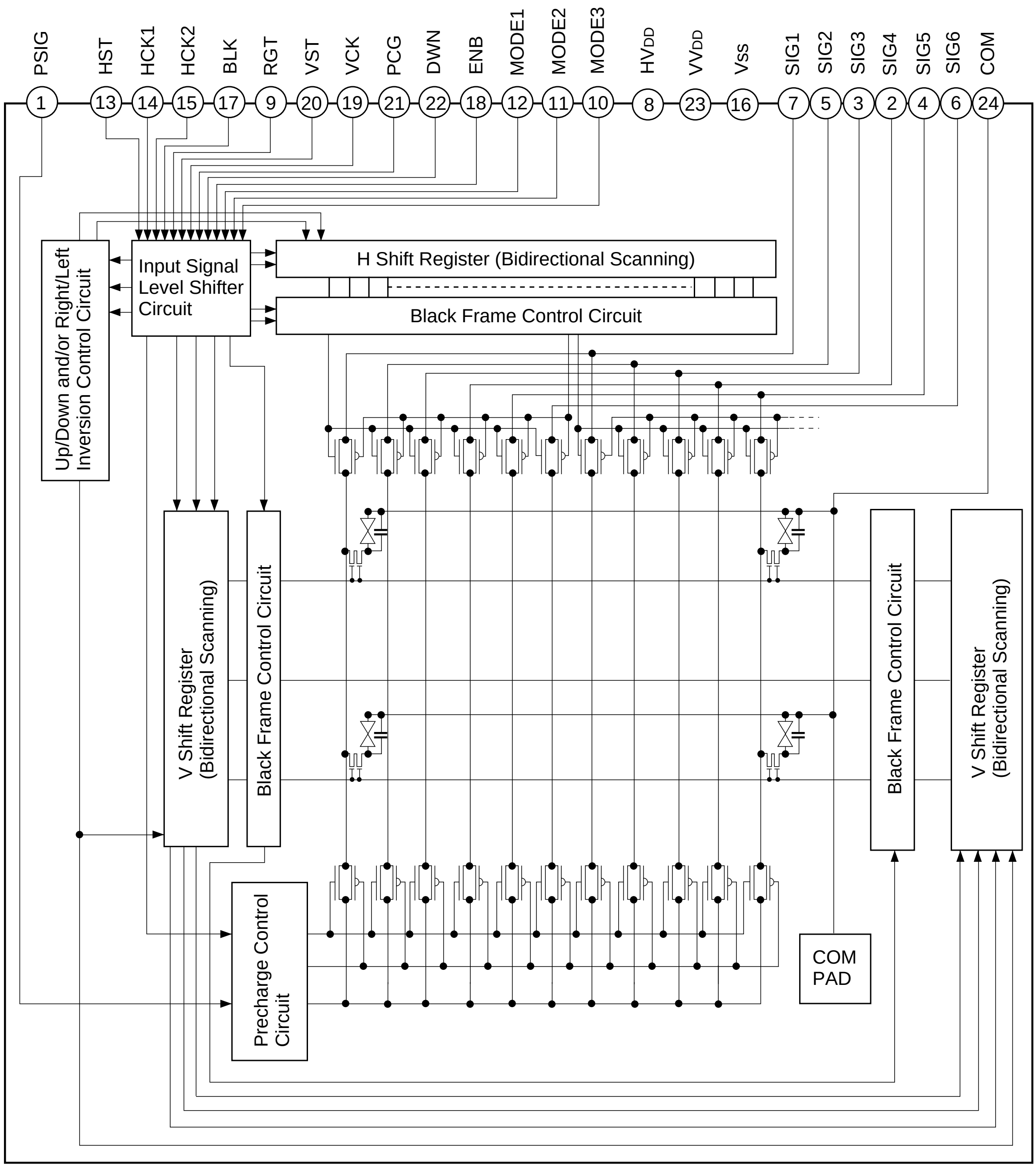
Element Structure

- Dots: 832 (H) × 624 (V) = 519,168
- Built-in peripheral driver using polycrystalline silicon super thin film transistors

Applications

- Liquid crystal data projectors
- Liquid crystal projectors, etc.

Block Diagram



Absolute Maximum Ratings (V_{SS} = 0V)

• H driver supply voltage	HV_{DD}	–1.0 to +20	V
• V driver supply voltage	VV_{DD}	–1.0 to +20	V
• Common pad voltage	COM	–1.0 to +17	V
• H shift register input pin voltage	HST, HCK1, HCK2, RGT	–1.0 to +17	V
• V shift register input pin voltage	VST, VCK, PCG, BLK, ENB, DWN MODE1, MODE2, MODE3	–1.0 to +17	V
• Video signal input pin voltage	SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG	–1.0 to +15	V
• Operating temperature	Topr	–10 to +70	°C
• Storage temperature	Tstg	–30 to +85	°C

Operating Conditions (V_{SS} = 0V)

• Supply voltage

HV_{DD} 15.5 ± 0.3V

VV_{DD} 15.5 ± 0.3V

• Input pulse voltage (Vp-p of all input pins except video signal and uniformity improvement signal input pins)

Vin 5.0 ± 0.5V

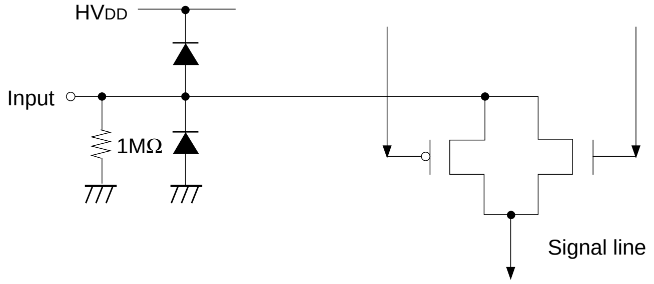
Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	PSIG	Uniformity improvement signal	13	HST	Start pulse for H shift register drive
2	SIG4	Video signal 4 to panel	14	HCK1	Clock pulse for H shift register drive
3	SIG3	Video signal 3 to panel	15	HCK2	Clock pulse for H shift register drive
4	SIG5	Video signal 5 to panel	16	Vss	GND (H, V drivers)
5	SIG2	Video signal 2 to panel	17	BLK	Black Frame display pulse
6	SIG6	Video signal 6 to panel	18	ENB	Enable pulse for gate selection
7	SIG1	Video signal 1 to panel	19	VCK	Clock pulse for V shift register drive
8	HV_{DD}	Power supply for H driver	20	VST	Start pulse for V shift register drive
9	RGT	Drive direction pulse for H shift register (H: normal, L: reverse)	21	PCG	Improvement pulse for uniformity
10	MODE3	Display area switching 3	22	DWN	Drive direction pulse for V shift register (H: normal, L: reverse)
11	MODE2	Display area switching 2	23	VV_{DD}	Power supply for V driver
12	MODE1	Display area switching 1	24	COM	Common voltage of panel

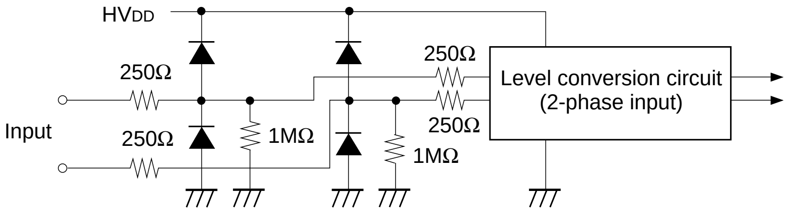
Input Equivalent Circuit

To prevent static charges, protective diodes are provided for each pin except the power supplies. In addition, protective resistors are added to all pins except the video signal inputs. All pins are connected to Vss with a high resistor of 1MΩ (typ.). The equivalent circuit of each input pin is shown below: (Resistance value: typ.)

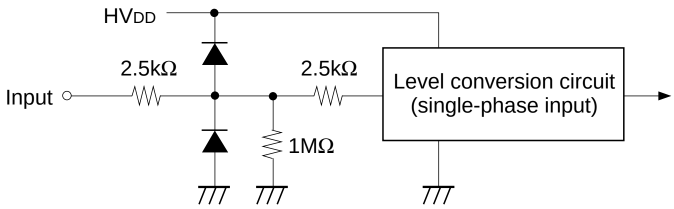
(1) SIG1, SIG2, SIG3, SIG4, SIG5, SIG6, PSIG



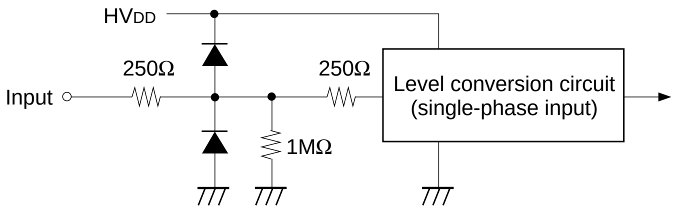
(2) HCK1, HCK2



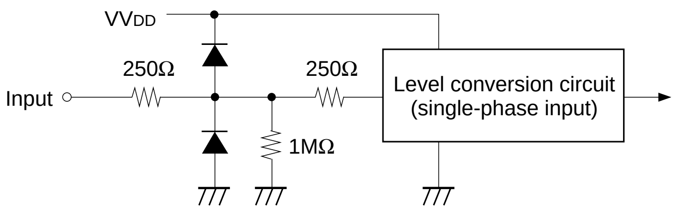
(3) RGT



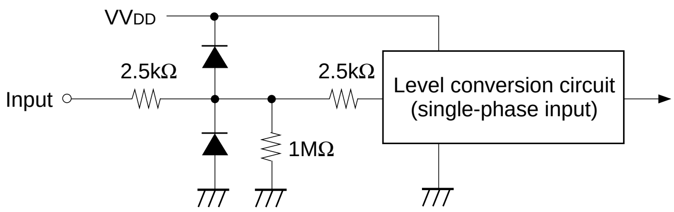
(4) HST



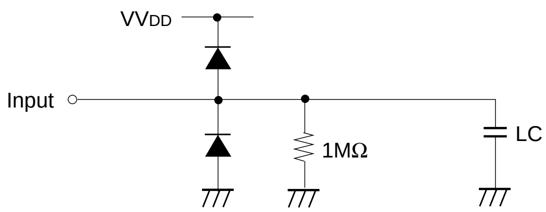
(5) PCG, VCK



(6) VST, BLK, ENB, DWN, MODE1, MODE2, MODE3



(7) COM



Input Signals

1. Input signal voltage conditions (V_{SS} = 0V)

Item		Symbol	Min.	Typ.	Max.	Unit
H shift register input voltage HST, HCK1, HCK2, RGT	(Low)	VHIL	–0.5	0.0	0.4	V
	(High)	VHIH	4.5	5.0	5.5	V
V shift register input voltage MODE1, MODE2, MODE3, BLK, VST, VCK, PCG, ENB, DWN	(Low)	VVIL	–0.5	0.0	0.4	V
	(High)	VVIH	4.5	5.0	5.5	V
Video signal center voltage		VVC		7.0		V
Video signal input range*1		Vsig	VVC – 4.5	7.0	VVC + 4.5	V
Common voltage of panel*2		Vcom		VVC – 0.4		V
Uniformity improvement signal input voltage (PSIG)*3		Vpsig	VVC ± 4.3	VVC ± 4.5	VVC ± 4.7	V

*1 Input video signal shall be symmetrical to VVC.
*2 Common voltage of the panel shall be adjusted to VVC – 0.4V.
*3 Uniformity improvement signal PSIG shall be the same polarity as video signals SIG1 to 6.

Level Conversion Circuit

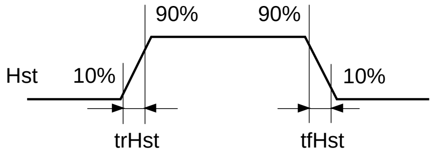
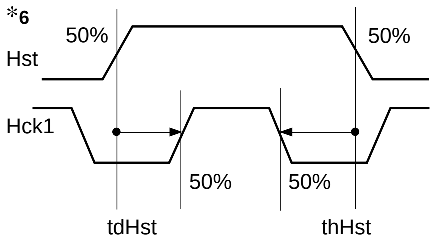
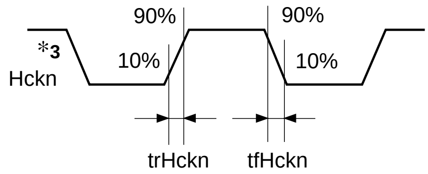
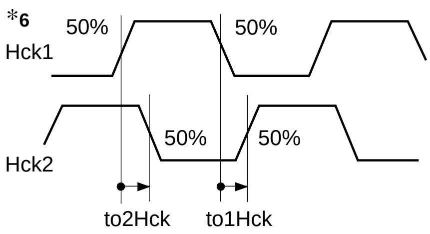
The LCX016AM has a built-in level conversion circuit in the clock input unit on the panel. The input signal level increases to HV_{DD} or VV_{DD}. The V_{CC} of external ICs are applicable to 5 ± 0.5V.

2. Clock timing conditions (Ta = 25°C) (MAC17 mode: fHCKn = 4.8MHz, fVCK = 24.9kHz)

	Item	Symbol	Min.	Typ.	Max.	Unit
HST	Hst rise time	trHst	—	—	30	ns
	Hst fall time	tfHst	—	—	30	
	Hst data set-up time	tdHst	—	50	—	
	Hst data hold time	thHst	—	50	—	
HCK	Hckn rise time*4	trHckn	—	—	30	
	Hckn fall time*4	tfHckn	—	—	30	
	Hck1 fall to Hck2 rise time	to1Hck	–15	0	15	
	Hck1 rise to Hck2 fall time	to2Hck	–15	0	15	
VST	Vst rise time	trVst	—	—	100	
	Vst fall time	tfVst	—	—	100	
	Vst data set-up time	tdVst	—	10	—	µs
	Vst data hold time	thVst	—	10	—	
VCK	Vck rise time	trVck	—	—	100	ns
	Vck fall time	tfVck	—	—	100	
ENB	Enb rise time	trEnb	—	—	100	
	Enb fall time	tfEnb	—	—	100	
	Vck rise/fall to Enb rise time	tdEnb	—	500	—	
	Enb pulse width	twEnb	—	2500	—	
PCG	Pcg rise time	trPcg	—	—	30	
	Pcg fall time	tfPcg	—	—	30	
	Pcg fall to Vck rise/fall time	toVck	—	1000	—	
	Pcg pulse width	twPcg	—	1200	—	
BLK*5	Blk rise time	trBlk	—	—	100	
	Blk fall time	tfBlk	—	—	100	
	Blk fall to Vst rise time	toVst	—	33	—	µs
	Blk pulse width	twBlk	—	21	—	

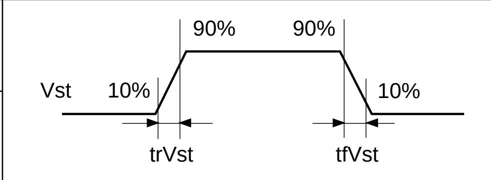
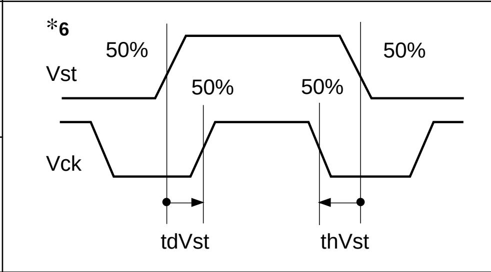
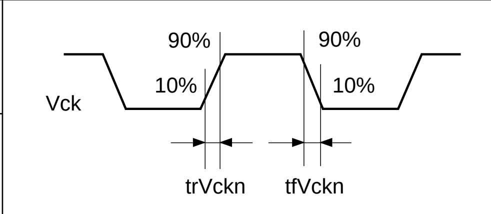
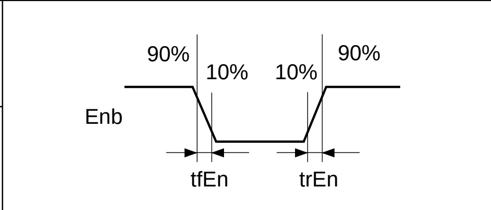
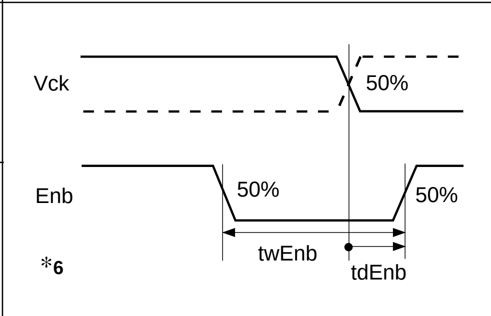
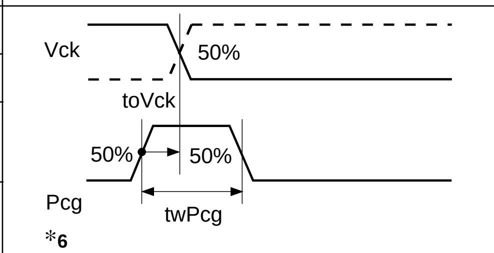
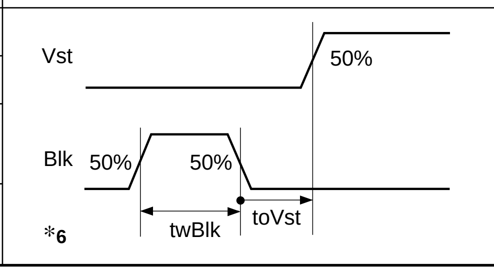
*4 Hckn means Hck1 and Hck2.
*5 Blk is the timing during SVGA mode (fHckn = 4.0MHz, fVck = 24.0kHz).

<Horizontal Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
HST	Hst rise time	trHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst fall time	tfHst		
	Hst data set-up time	tdHst		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hst data hold time	thHst		
HCK	Hckn rise time*3	trHckn		• Hckn*3 duty cycle 50% to1Hck = 0ns to2Hck = 0ns
	Hckn fall time*3	tfHckn		
	Hck1 fall to Hck2 rise time	to1Hck		
	Hck1 rise to Hck2 fall time	to2Hck		

*6 Definitions: The right-pointing arrow (•→) means +.
The left-pointing arrow (←•) means –.
The black dot at an arrow (•) indicates the start of measurement.

<Vertical Shift Register Driving Waveform>

Item		Symbol	Waveform	Conditions
VST	Vst rise time	trVst		
	Vst fall time	tfVst		
	Vst data set-up time	tdVst		
	Vst data hold time	thVst		
VCK	Vck rise time	trVck		
	Vck fall time	tfVck		
ENB	Enb rise time	trEnb		
	Enb fall time	tfEnb		
	Vck rise/fall to Enb rise time	tdEnb		
	Enb pulse width	twEnb		
PCG*7	Pcg rise time	trPcg		
	Pcg fall time	tfPcg		
	Pcg rise to Vck rise/fall time	toVck		
	Pcg pulse width	trPcg		
BLK	Blk rise time	twBlk		
	Blk fall time	tfBlk		
	Blk fall to Vst rise time	toVst		
	Blk pulse width	twBlk		

*7 Input the pulse obtained by taking the OR of the above pulse (PCG) and BLK to the PCG input pin.

Electrical Characteristics (Ta = 25°C, HV_{DD} = 15.5V, VV_{DD} = 15.5V)

1. Horizontal drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	HCKn	CHckn	—	12	—	pF	
	HST	CHst	—	12	—	pF	
Input pin current	HCK1		—	–250	—	µA	HCK1 = GND
	HCK2		—	–300	—	µA	HCK2 = GND
	HST		—	–150	—	µA	HST = GND
	RGT		—	–30	—	µA	RGT = GND
Video signal input pin capacitance		Csig	—	140	—	pF	
Current consumption		IH	—	5.0	—	mA	HCKn: HCK1, HCK2 (4.8MHz)

2. Vertical drivers

Item		Symbol	Min.	Typ.	Max.	Unit	Condition
Input pin capacitance	VCK	CVck	—	12	—	pF	
	VST	CVst	—	12	—	pF	
Input pin current	VCK		—	–150	—	µA	VCK = GND
PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3			—	–30	—	µA	PCG, VST, ENB, DWN, BLK, MODE1, MODE2, MODE3 = GND
Current consumption		IV	—	2.0	—	mA	VCK: (24.9kHz)

3. Total power consumption of the panel

Item	Symbol	Min.	Typ.	Max.	Unit
Total power consumption of the panel (MAC17)	PWR	—	100	—	mW

4. Pin input resistance

Item	Symbol	Min.	Typ.	Max.	Unit
Pin – V_{SS} input resistance	Rpin	0.4	1	—	MΩ

5. Uniformity improvement signal

Item	Symbol	Min.	Typ.	Max.	Unit
Input pin capacitance for uniformity improvement signal	CPSIGo	—	12	—	nF

Electro-optical Characteristics (Ta = 25°C, MAC17 mode)

Item			Symbol	Measurement method	Min.	Typ.	Max.	Unit
Contrast ratio		25°C	CR	1	—	200	—	—
Optical transmittance		25°C	T	2	—	20	—	%
V-T characteristics	V_{90}	25°C	RV_{90-25}	3	—	1.41	—	V
			GV_{90-25}		—	1.55	—	
			BV_{90-25}		—	1.67	—	
		60°C	RV_{90-60}		—	1.33	—	
			GV_{90-60}		—	1.46	—	
			BV_{90-60}		—	1.58	—	
	V_{50}	25°C	RV_{50-25}		—	1.75	—	
			GV_{50-25}		—	1.85	—	
			BV_{50-25}		—	1.94	—	
		60°C	RV_{50-60}		—	1.67	—	
			GV_{50-60}		—	1.75	—	
			BV_{50-60}		—	1.84	—	
	V_{10}	25°C	RV_{10-25}		—	2.25	—	
			GV_{10-25}		—	2.34	—	
			BV_{10-25}		—	2.43	—	
		60°C	RV_{10-60}		—	2.15	—	
			GV_{10-60}		—	2.23	—	
			BV_{10-60}		—	2.31	—	
Response time	ON time	0°C	ton0	4	—	30.6	—	ms
		25°C	ton25		—	12.0	—	
	OFF time	0°C	toff0		—	99.4	—	
		25°C	toff25		—	28.4	—	
Flicker		60°C	F	5	—	–68	—	dB
Image retention time		25°C	YT60	6	—	—	0	s
Cross talk		25°C	CTK	7	—	—	5	%

Reflection Preventive Processing

When a phase substrate which rotates the polarization axis is used to adjust to the polarization direction of a polarization screen or prism, use a phase substrate with reflection preventive processing on the surface. This prevents characteristic deterioration caused by luminous reflection.

<Electro-optical Characteristics Measurement>

Basic measurement conditions

(1) Driving voltage

$HV_{DD} = 15.5V$, $VV_{DD} = 15.5V$

VVC = 7.0V, Vcom = 6.6V

(2) Measurement temperature

25°C unless otherwise specified.

(3) Measurement point

One point in the center of the screen unless otherwise specified.

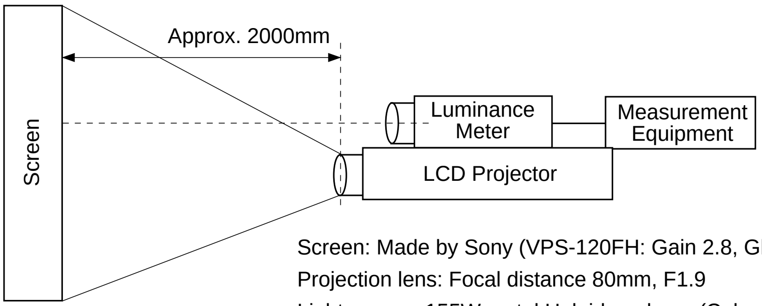
(4) Measurement systems

Two types of measurement systems are used as shown below.

(5) Video input signal voltage (Vsig)

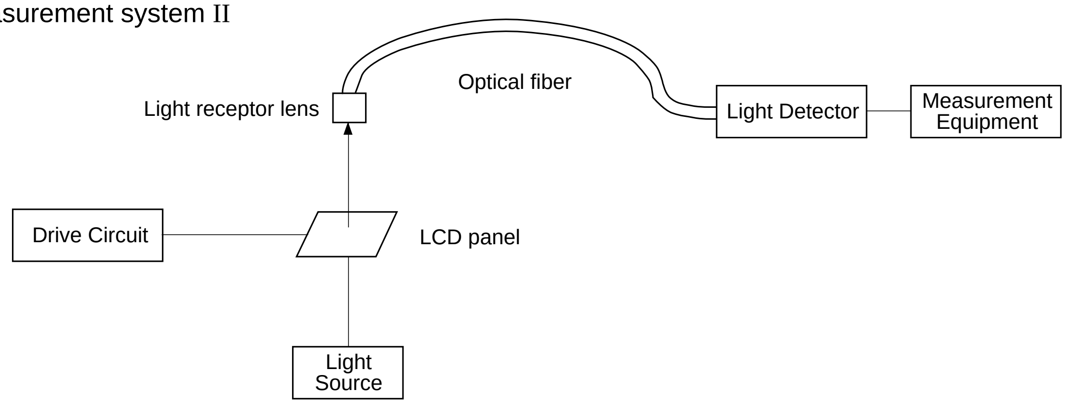
$Vsig = 7.0 \pm V_{AC}$ [V] (V_{AC} = signal amplitude)

• Measurement system I



Screen: Made by Sony (VPS-120FH: Gain 2.8, Glass Beaded Type) or equivalent
Projection lens: Focal distance 80mm, F1.9
Light source: 155W metal Haloid arc lamp (Color temperature 7500K ± 500)
(× 24, Sensor area: 7mmϕ)

• Measurement system II



1. Contrast Ratio

Contrast Ratio (CR) is given by the following formula (1).

$$CR = \frac{L\ (White)}{L\ (Black)} \quad \text{... (1)}$$

L (White): Surface luminance of the center of the screen at the input signal amplitude V_{AC} = 0.5V.
L (Black): Surface luminance of the center of the screen at V_{AC} = 4.5V.
Both luminosities are measured by System I.

2. Optical Transmittance

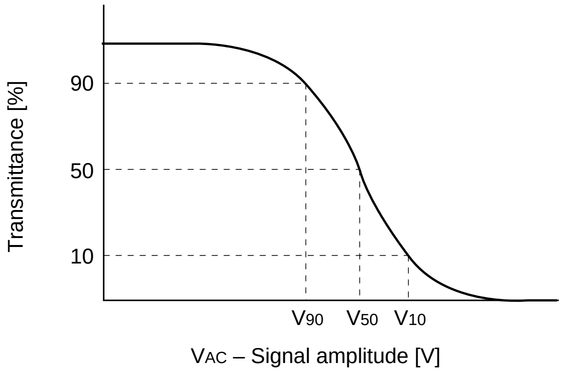
Optical Transmittance (T) is given by the following formula (2).

$$T = \frac{\text{White luminance}}{\text{Luminance of light source}} \times 100\ [\%]\ ...\ (2)$$

"White luminance" means the maximum luminance on the screen at the input signal amplitude V_{AC} = 0.5V on Measurement System I.

3. V-T Characteristics

V-T characteristics, or the relationship between signal amplitude and the transmittance of the panels, are measured by System II by inputting the same signal amplitude V_{AC} to each input pin. V_{90}, V_{50}, and V_{10} correspond to the voltages which define 90%, 50%, and 10% of transmittance respectively.



4. Response Time

Response time ton and toff are defined by formulas (5) and (6) respectively.

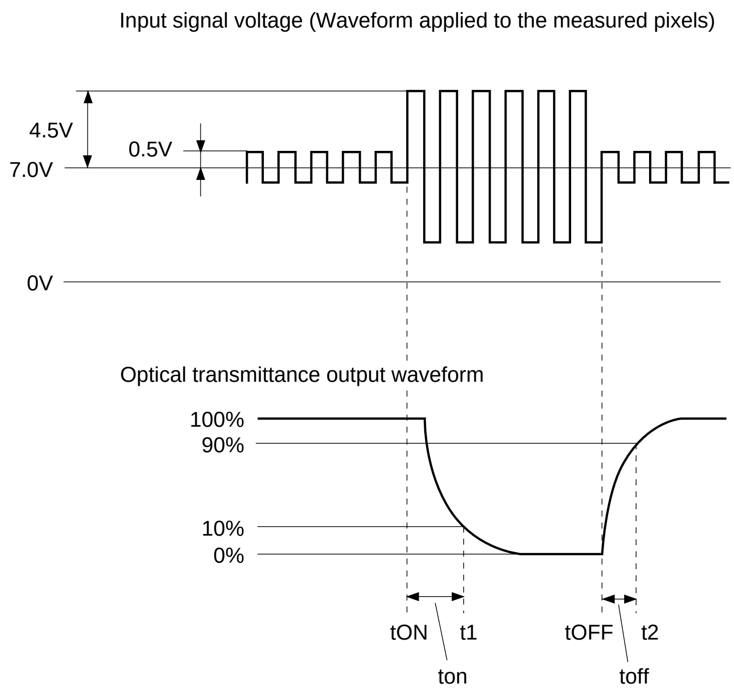
ton = t1 – tON ...(5)

toff = t2 – tOFF ...(6)

t1: time which gives 10% transmittance of the panel.

t2: time which gives 90% transmittance of the panel.

The relationships between t1, t2, tON and tOFF are shown in the right figure.



5. Flicker

Flicker (F) is given by formula (7). DC and AC (MAC17/SVGA/VGA/PC98/NTSC: 30Hz, rms, PAL: 25Hz, rms) components of the panel output signal for gray raster* mode are measured by a DC voltmeter and a spectrum analyzer in System II.

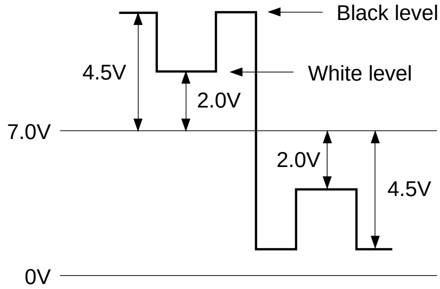
$$F\ [\mathrm{dB}] = 20\log\left\{\frac{\text{AC component}}{\text{DC component}}\right\} \quad ...(7)$$

* Each input signal voltage for gray raster mode is given by Vsig = 7.0 ± V_{50} [V] where: V_{50} is the signal amplitude which gives 50% of transmittance in V-T characteristics.

6. Image Retention Time

Apply the monoscope signal to the LCD panel for 60 minutes and then change this signal to the gray scale of Vsig = 7.0 ± V_{AC} (V_{AC}: 3 to 4V). Judging by sight at the V_{AC} that holds the maximum image retention, measure the time till the residual image becomes indistinct.

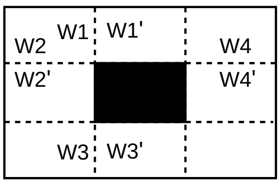
* Monoscope signal conditions:
Vsig = 7.0 ± 4.5 or ± 2.0 [V]
(shown in the right figure)
Vcom = 6.6V



Vsig waveform

7. Cross Talk

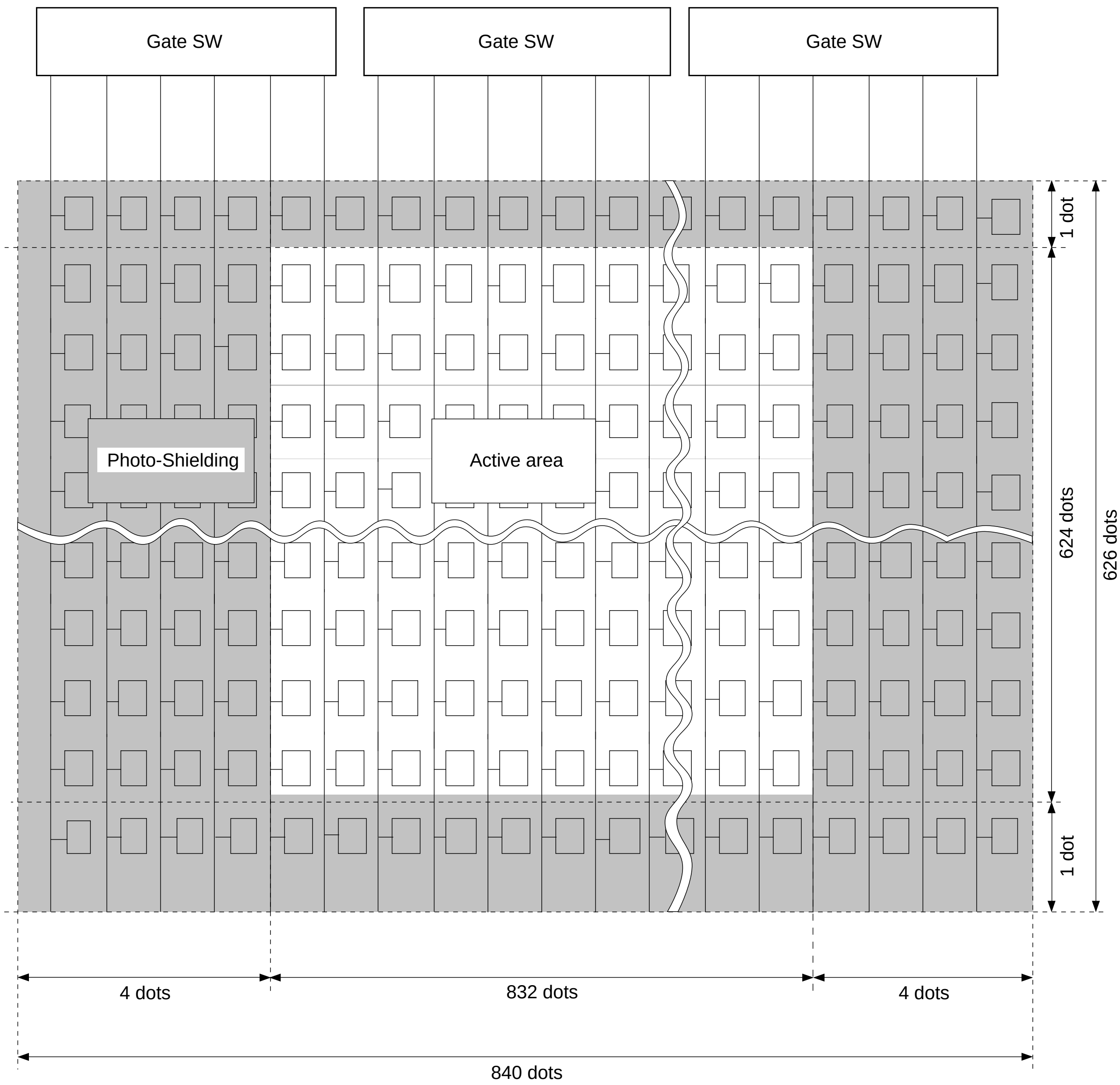
Cross talk is determined by the luminance differences between adjacent areas represented by Wi' and Wi (i = 1 to 4) around a black window (Vsig = 4.5 V/1V).



$$\text{Cross talk value CTK} = \left|\frac{Wi' - Wi}{Wi}\right| \times 100\ [\%]$$

1. Dot Arrangement

The dots are arranged in a stripe. The shaded area is used for the dark border around the display.



2. LCD Panel Operations

[Description of basic operations]

- A vertical driver, which consists of vertical shift registers, enable-gates and buffers, applies a selected pulse to every 624 gate lines sequentially in a single horizontal scanning period. (in MAC17 mode)

- A horizontal driver, which consists of horizontal shift registers, gates and CMOS sample-and-hold circuits, applies selected pulses to every 832 signal electrodes sequentially in a single horizontal scanning period. These pulses are used to supply the sampled video signal to the row signal lines.

- Vertical and horizontal shift registers address one pixel, and then Thin Film Transistors (TFTs; two TFTs) turn on to apply a video signal to the dot. The same procedures lead to the entire 624 × 832 dots to display a picture in a single vertical scanning period.

- The data and video signals shall be input with the 1H-inverted system.

[Description of operating mode]

This LCD panel can change the active area by displaying a black frame to support various computer or video signals. The active area is switched by MODE1, 2 and 3. The active area setting modes are shown below.

MODE1	MODE2	MODE3	Display mode
L	L	L	MAC17 832 × 624
L	L	H	SVGA 800 × 600
L	H	L	PAL 762 × 572
L	H	H	VGA/NTSC 640 × 480
H	L	L	PC98 640 × 400

This LCD panel has the following functions to easily apply to various uses, as well as various broadcasting systems.

- Right/left inverse mode
- Up/down inverse mode

These modes are controlled by two signals (RGT and DWN). The right/left and/or up/down setting modes are shown below.

RGT	Mode
H	Right scan
L	Left scan

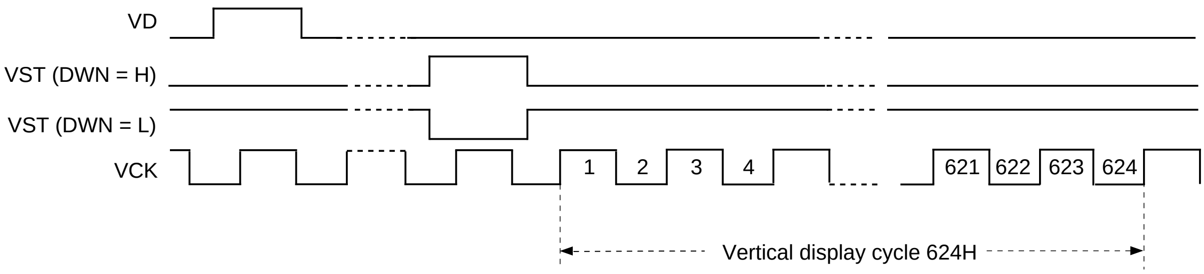
DWN	Mode
H	Down scan
L	Up scan

Right/left and/or up/down mean the direction when the Pin 1 marking is located at the right side with the pin block upside.

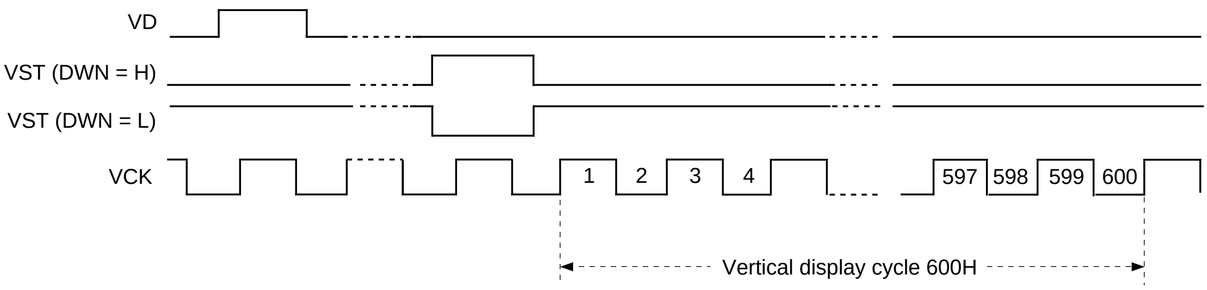
To locate the active area in the center of the panel in each mode, polarity of the start pulse and clock phase for both the H and V systems must be varied. The phase relationship between the start pulse and the clock for each mode is shown on the following pages.

(1) Vertical direction display cycle

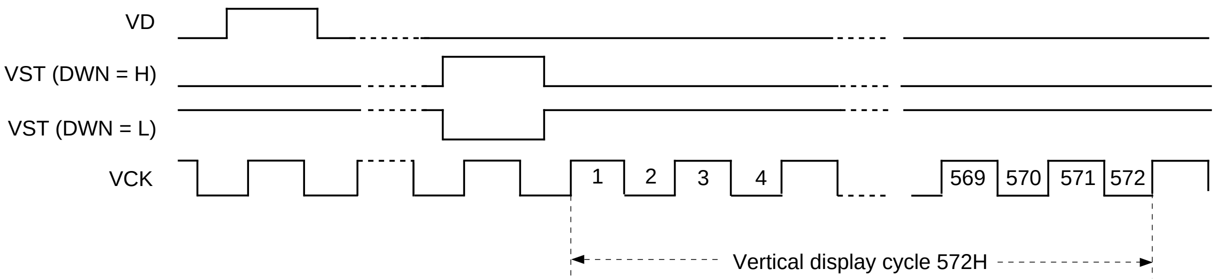
(1.1) MAC17



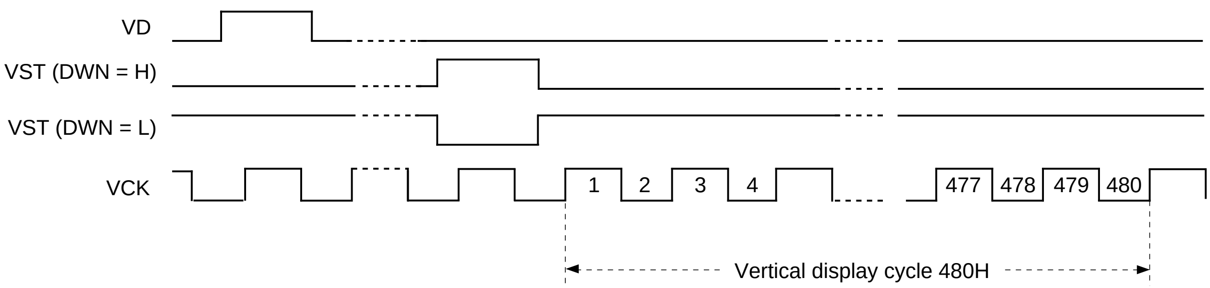
(1.2) SVGA



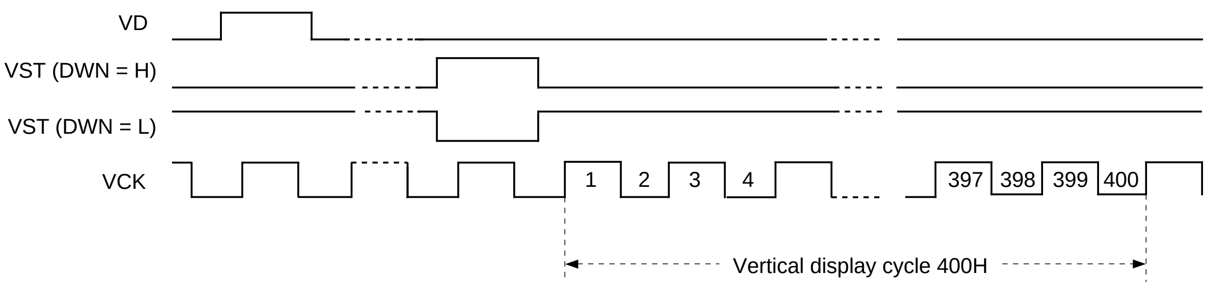
(1.3) PAL



(1.4) VGA/NTSC

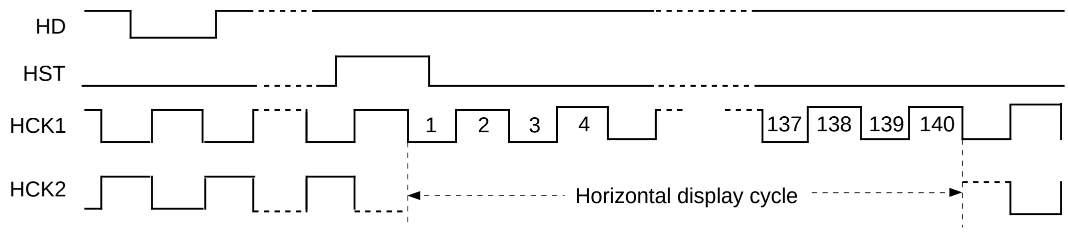


(1.5) PC98

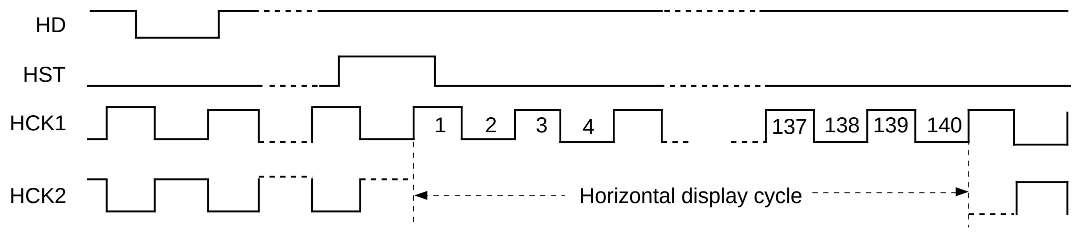


(2) Horizontal direction display cycle

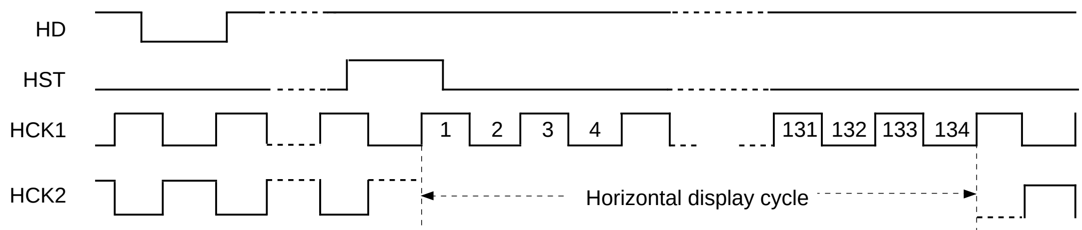
(2.1.1) MAC17, RGT = H



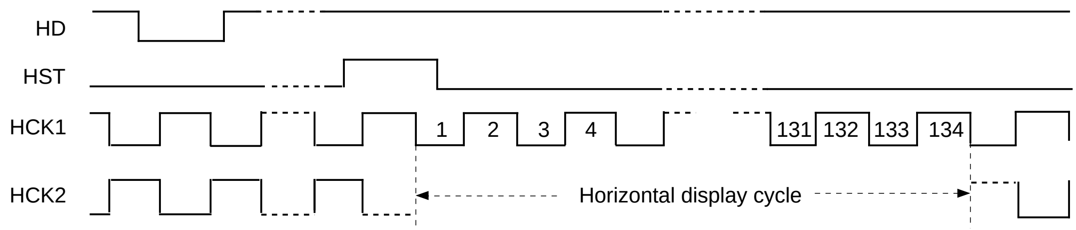
(2.1.2) MAC17, RGT = L



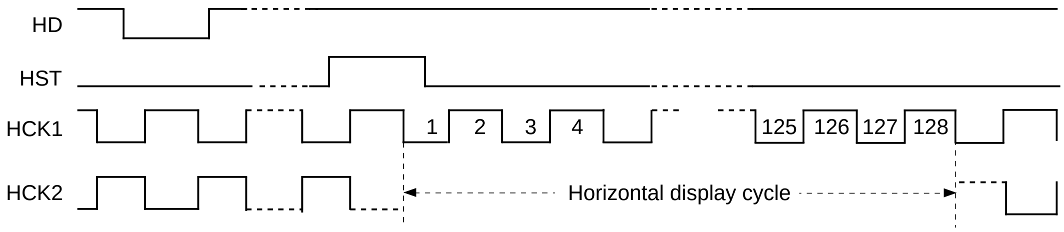
(2.2.1) SVGA, RGT = H



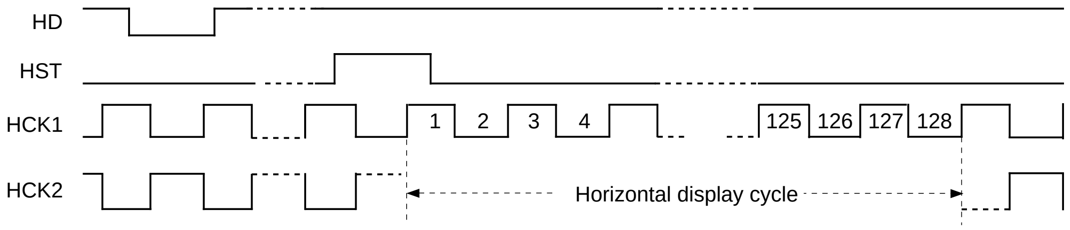
(2.2.2) SVGA, RGT = L



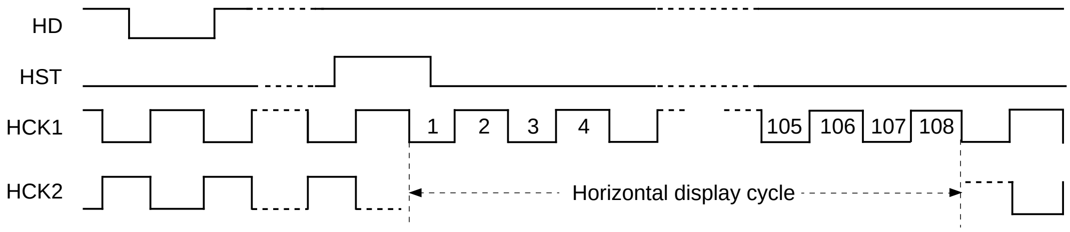
(2.3.1) PAL, RGT = H



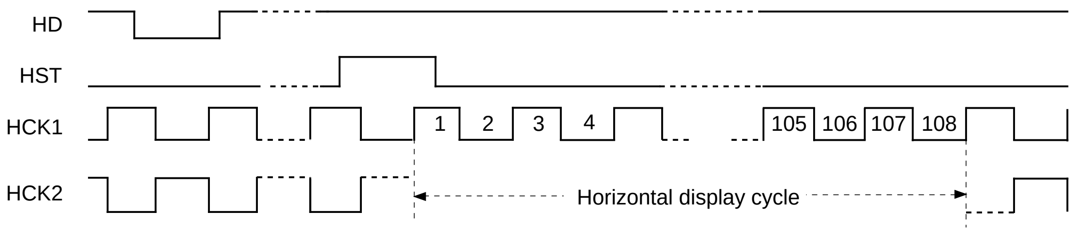
(2.3.2) PAL, RGT = L



(2.4.1) VGA/NTSC/PC98, RGT = H



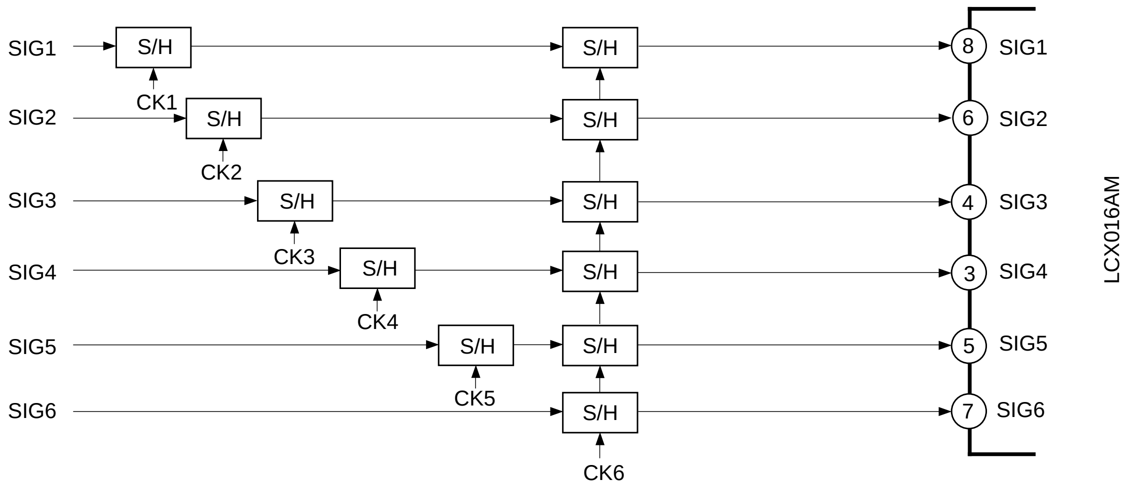
(2.4.2) VGA/NTSC/PC98, RGT = L



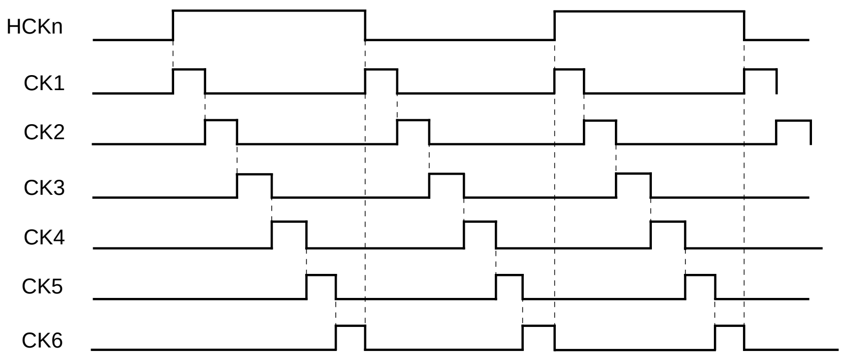
3. 6-dot Simultaneous Sampling

The horizontal shift register samples signals SIG1 to SIG6 simultaneously. This requires phase matching between signals SIG1 to SIG6 to prevent the horizontal resolution from deteriorating. Thus, phase matching between each signal is required using an external signal delaying circuit before applying the video signal to the LCD panel.

The block diagram of the delaying procedure using the sample-and-hold method is as follows. The following phase relationship diagram indicates the phase setting for right scan (RGT = High level). For left scan (RGT = Low level), the phase settings for signals SIG1 to SIG6 are exactly reversed.

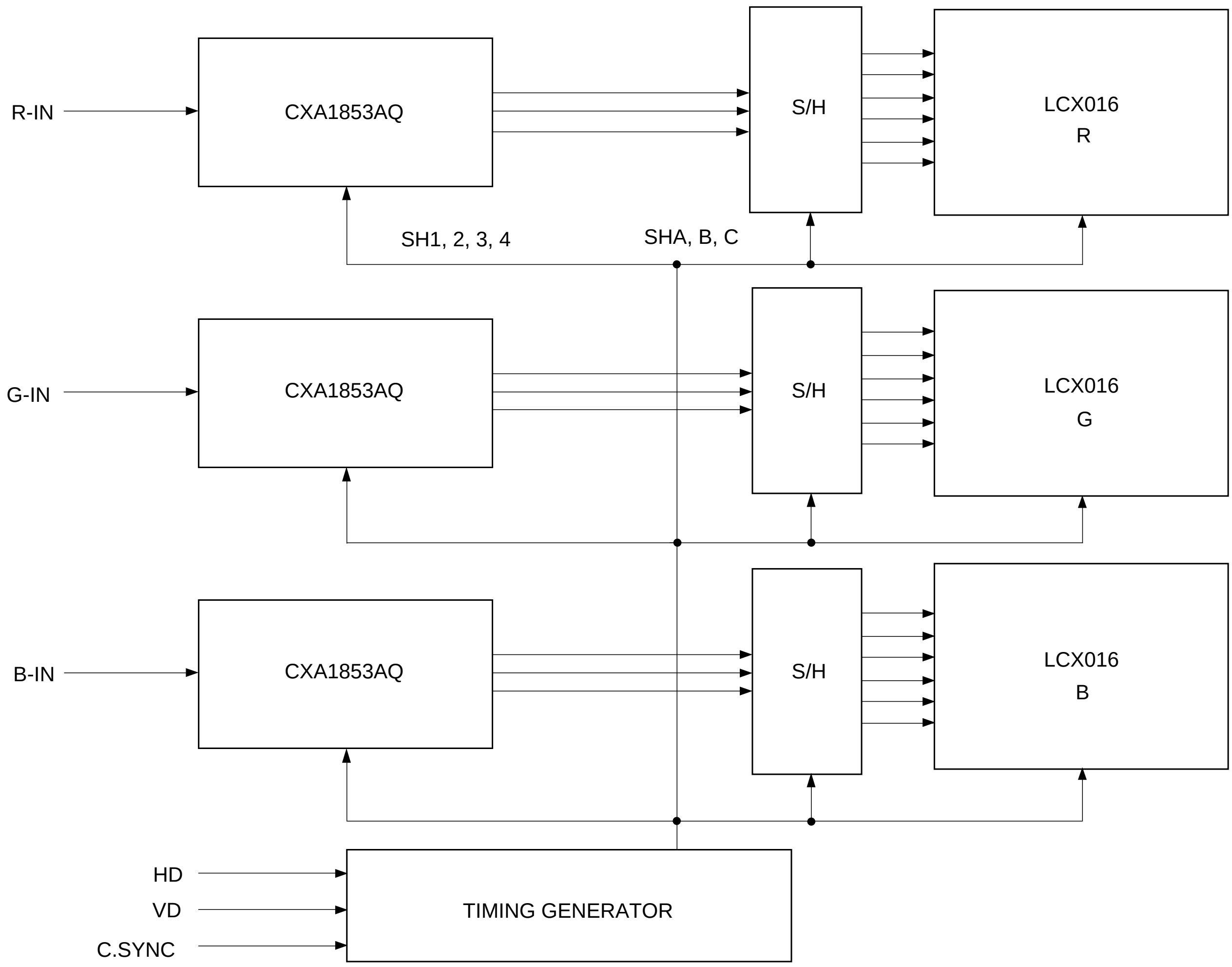


<Phase relationship of delaying sample-and-hold pulses> (right scan)



Display System Block Diagram

An example of display system is shown below.



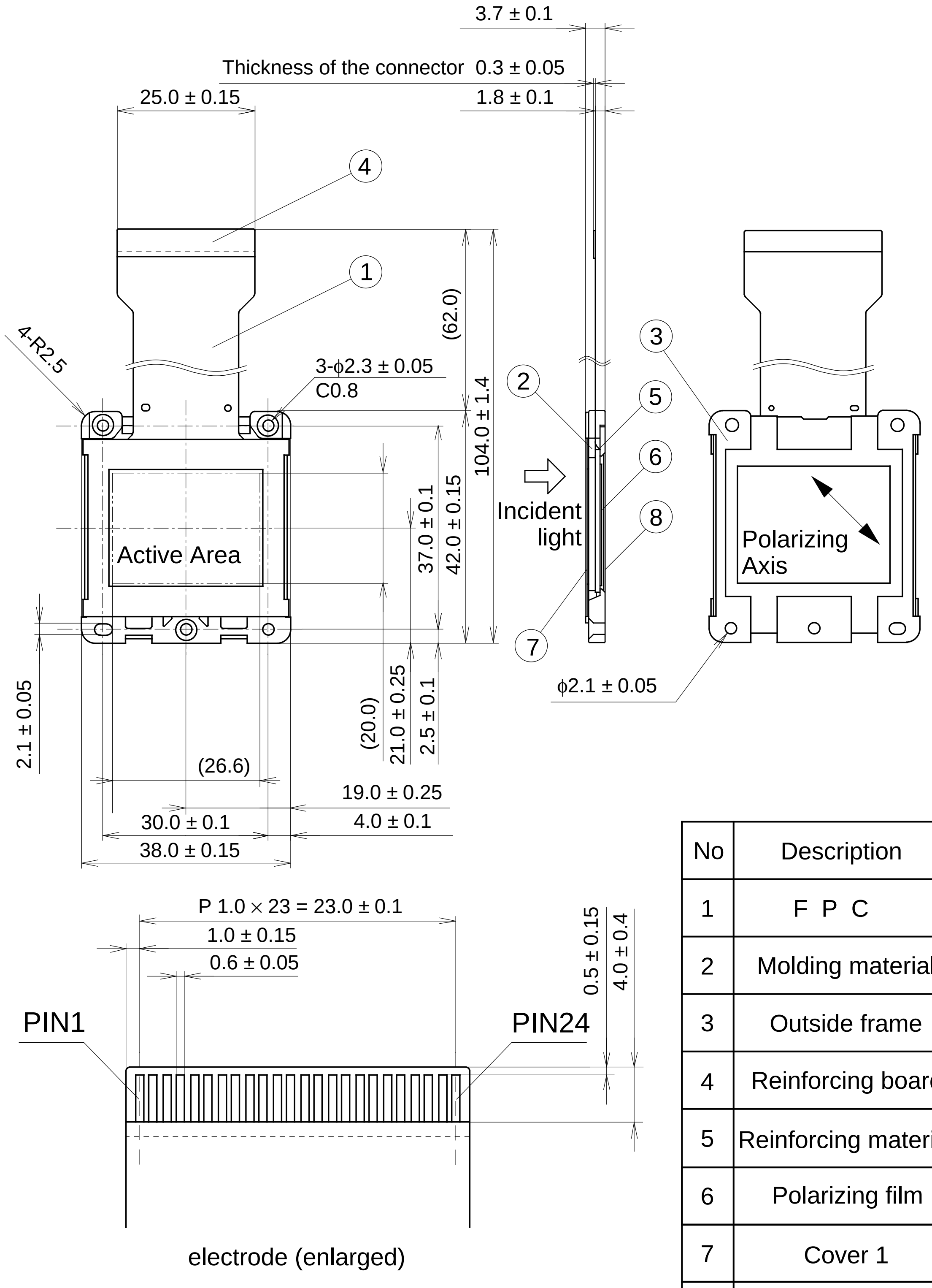
Notes on Handling

(1) Static charge prevention
Be sure to take the following protective measures. TFT-LCD panels are easily damaged by static charges.
a) Use non-chargeable gloves, or simply use bare hands.
b) Use an earth-band when handling.
c) Do not touch any electrodes of a panel.
d) Wear non-chargeable clothes and conductive shoes.
e) Install conductive mats on the working floor and working table.
f) Keep panels away from any charged materials.
g) Use ionized air to discharge the panels.

(2) Protection from dust and dirt
a) Operate in a clean environment.
b) When delivered, the panel surface (Polarizer) is covered by a protective sheet. Peel off the protective sheet carefully so as not to damage the panel.
c) Do not touch the panel surface. The surface is easily scratched. When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave a stain on the surface.
d) Use ionized air to blow dust off the panel.

(3) Other handling precautions
a) Do not twist or bend the flexible PC board especially at the connecting region because the board is easily deformed.
b) Do not drop the panel.
c) Do not twist or bend the panel or panel frame.
d) Keep the panel away from heat sources.
e) Do not dampen the panel with water or other solvents.
f) Avoid storing or using the panel at a high temperature or high humidity, which may result in panel damages.

Package Outline Unit: mm



electrode (enlarged)

The rotation angle of the active area relative to H and V is ± 1°.

No	Description
1	F P C
2	Molding material
3	Outside frame
4	Reinforcing board
5	Reinforcing material
6	Polarizing film
7	Cover 1
8	Cover 2

weight 7.6g