

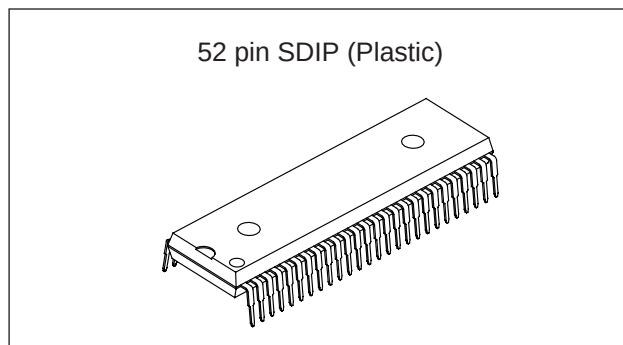
CMOS 8-bit Single Chip Microcomputer

Description

The CXP864P61 is the CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I²C bus interface, PWM output, remote control reception circuit, HSYNC counter, watchdog timer, 32kHz timer/counter besides the basic configurations of 8-bit CPU, PROM, RAM, I/O ports.

The CXP864P61 also provides a sleep function that enables to lower the power consumption.

The CXP864P61 is the PROM-incorporated version of the CXP86461 with built-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.



Structure

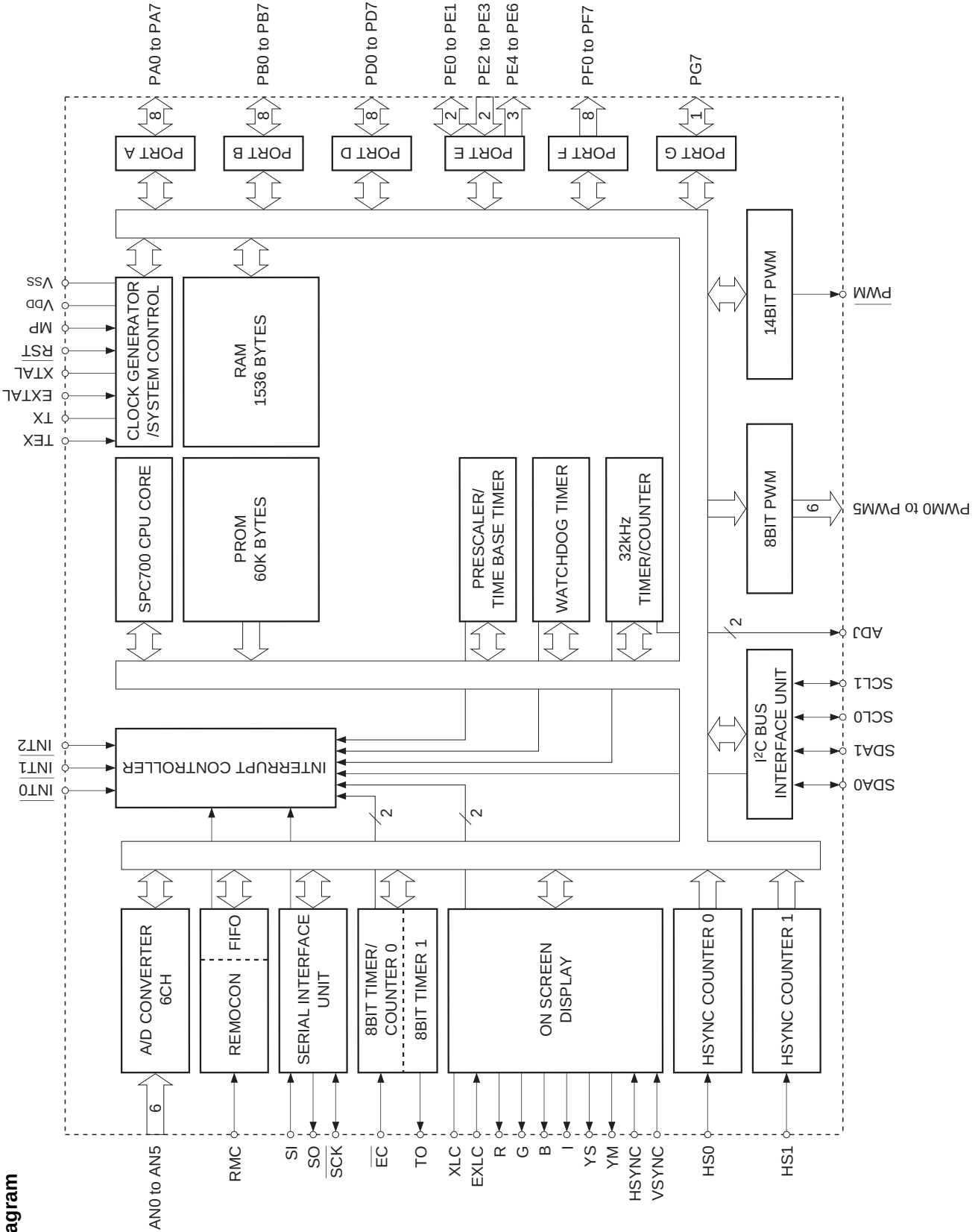
Silicon gate CMOS IC

Features

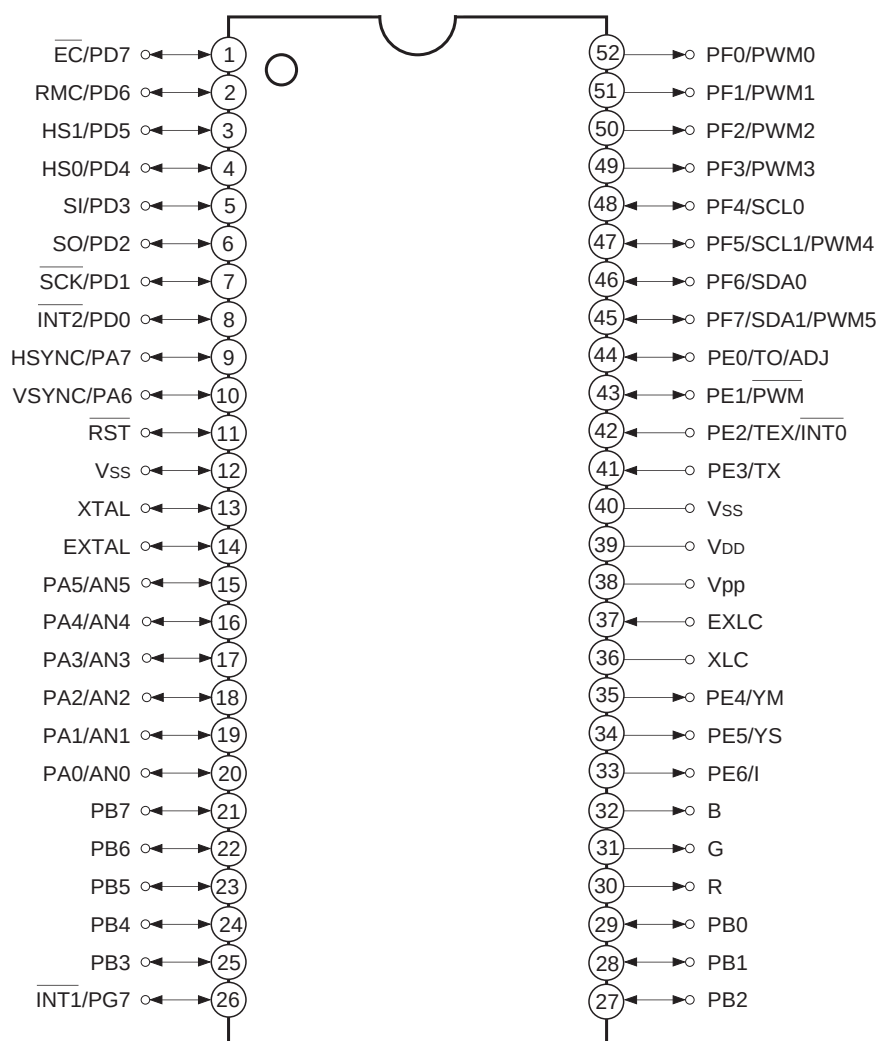
- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 122μs at 32kHz operation (2.7 to 5.5V)
- Incorporated PROM
 - 60K bytes
- Incorporated RAM
 - 1536 bytes (Excludes VRAM for on-screen display and sprite RAM)
- Peripheral functions
 - A/D converter
 - 8 bits, 6 channels, successive approximation method (Conversion time of 3.25μs at 16 MHz)
 - Serial interface
 - 8-bit clock sync type, 1 channel
 - Timer
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time-base timer
 - 32kHz timer/counter
 - On-screen display (OSD) function
 - 12 × 16 dots, 52 character types
 - 15 character colors, 2 lines × 24 characters, frame background 8 colors/ half blanking, background on full screen 15 colors/ half blanking edging/ shadowing/ rounding for every line, background with shadow for every character, double scanning, sprite OSD, 12 × 16 dots, 1 screen, 8 colors for every dot
 - I²C bus interface
 - PWM output
 - 8 bits, 8 channels
 - 14 bits, 1 channel
 - Remote control reception circuit
 - 8-bit pulse measurement counter, 6-stage FIFO
 - HSYNC counter
 - 2 channels
 - Watchdog timer
- Interruption
 - 13 factors, 13 vectors, multi-interruption possible
- Standby mode
 - Sleep
- Package
 - 52-pin plastic SDIP

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Pin Assignment (Top View)

**Note)**

1. Vpp (Pin 38) is left open.
2. Vss (Pins 12 and 40) are both connected to GND.

Pin Description

Symbol	I/O	Description	
PA0/AN0 to PA5/AN5	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Analog inputs to A/D converter. (6 pins)
PA6/VSYN	I/O/Input		OSD display vertical sync signal input.
PA7/HSYN	I/O/Input		OSD display horizontal sync signal input.
PB0 to PB7	I/O	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	
PD0/ $\overline{\text{INT2}}$	I/O/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. (8 pins)	External interruption request input. Active at the falling edge.
PD1/ $\overline{\text{SCK}}$	I/O/I/O		Serial clock I/O.
PD2/SO	I/O/Output		Serial data output.
PD3/SI	I/O/Input		Serial data input.
PD4/HS0	I/O/Input		HSYN counter (CH0) input.
PD5/HS1	I/O/Input		HSYN counter (CH1) input.
PD6/RMC	I/O/Input		Remote control reception circuit input.
PD7/ $\overline{\text{EC}}$	I/O/Input		External event input for timer/counter.
PE0/TO/ADJ	I/O/Output/ Output	(Port E) Bits 0 and 1 are I/O port; I/O can be set in a unit of single bit. Bits 2 and 3 are input port. Bits 4, 5 and 6 are output port. (7 pins)	Rectangular wave output for 8-bit timer/counter.
PE1/PWM	I/O/Output		32kHz oscillation frequency dividing output.
PE2/TEX/ $\overline{\text{INT0}}$	Input/Input/ Input		14-bit PWM output.
PE3/TX	Input/Output		Connects a crystal for 32kHz timer/counter clock oscillation. When used as an event counter, input to TEX pin and leave TX pin open.
PE4/YM	Output/Output		OSD display 6-bit output. (6 pins)
PE5/YS	Output/Output		
PE6/I	Output/Output		
B	Output		
G	Output		
R	Output		
PF0/PWM0 to PF3/PWM3	Output/Output	(Port F) 8-bit output port.	8-bit PWM output. (4 pins)
PF4/SCL0	Output/I/O	Open drain output of large current (12mA) and N channel.	I ² C bus interface transfer clock I/O. (2 pins)
PF5/SCL1/ PWM4	Output/I/O/ Output	Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive. (8 pins)	8-bit PWM output.
PF6/SDA0	Output/I/O		I ² C bus interface transfer data I/O. (2 pins)
PF7/SDA1/ PWM5	Output/I/O/ Output		8-bit PWM output.

Symbol	I/O	Description	
PG7/ $\overline{\text{INT1}}$	I/O/Input	(Port G) 1-bit I/O port. I/O can be set in a unit of single bits. (1 pin)	External interruption request input. Active at the falling edge.
EXTAL	Input	Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin.	
XTAL	Output		
$\overline{\text{RST}}$	Input	System reset; active at Low level.	
EXLC	Input	OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.	
XLC	Output		
V _{DD}		Positive power supply.	
V _{SS}		GND. Connect two V _{SS} pins to GND.	
V _{pp}		Positive power supply for incorporated-PROM writing. No connected for normal operation.	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA5/AN5 6 pins	Port A	Hi-Z
PA6/VSYNC PA7/HSYNC 2 pins	Port A	Hi-Z
PB0 to PB7 PG7/INT1 9 pins	Port B Port G	Hi-Z
PF0/PWM0 to PF3/PWM3 4 pins	Port F * 12V drive voltage Large current 12mA	Hi-Z

Pin	Circuit format	When reset
PD0/ $\overline{\text{INT2}}$ PD3/SI PD4/HS0 PD5/HS1 PD6/RMC PD7/ $\overline{\text{EC}}$ 6 pins	Port D data Port D direction "0" when reset Data bus RD (Port D) Schmitt input IP * Large current 12mA $\overline{\text{INT2}}$, SI, HS0, HS1, RMC, EC	Hi-Z
PD1/ $\overline{\text{SCK}}$ PD2/SO 2 pins	Port D data Port D direction "0" when reset Data bus RD (Port D) SCK only * Large current 12mA PD2 is not Schmitt input.	Hi-Z
PE0/TO/ADJ 1 pin	Internal reset signal Port E data "1" when reset MPX TO ADJ16K^{*1} ADJ2K^{*1} Port E function selection (Upper) Port E function selection (Lower) "00" when reset Port E direction "1" when reset Data bus RD (Port E) *1 ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output. *2 Pull-up resistors approx. 150kΩ	High level (with the resistor of pull-up transistor ON when reset)

Pin	Circuit format	When reset
PE1/ $\overline{\text{PWM}}$ 1 pin		High level
PE2/ $\overline{\text{TEX}}$ / $\overline{\text{INT0}}$ PE3/TX 2 pins		Oscillation halted Port input
PE4/YM PE5/YS PE6/I 3 pins	Writing data to output polarity register and port data register brings output to active.	Hi-Z

Pin	Circuit format	When reset
PF4/SCL0 PF5/SCL1/PWM4 PF6/SDA0 PF7/SDA1/PWM5 4 pins	Port F SCL, SDA I²C bus enable PWM4, PWM5 Port F function selection "0" when reset Port F data "1" when reset Schmitt input SCL, SDA (I²C bus circuit) * Large current 12mA BUS SW To internal I²C pins (SCL1 for SCL0)	Hi-Z
R G B 3 pins	R, G, B Output polarity "0" when reset Writing data to output polarity register brings output to active.	Hi-Z
EXLC XLC 2 pins	Oscillation control EXLC XLC OSD display clock	Oscillation halted
EXTAL XTAL 2 pins	EXTAL XTAL IP Schmitt input • Diagram shows the circuit composition during oscillation. • Feedback resistor is removed during stop mode. (This device does not enter the stop mode.)	Oscillation
$\overline{\text{RST}}$ 1 pin	Pull-up resistor Schmitt input	Low level

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	V _{pp}	−0.3 to +13.0	V	Incorporated PROM
Input voltage	V _{IN}	−0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ¹	V	
Medium drive output voltage	V _{OUTP}	−0.3 to +15.0	V	
High level output current	I _{OH}	−5	mA	
High level total output current	ΣI _{OH}	−50	mA	Total of all output pins
Low level output current	I _{OL}	15	mA	Ports excluding large current output (value per pin)
	I _{OLC}	20	mA	Large current output ports (value per pin* ²)
Low level total output current	ΣI _{OL}	130	mA	Total of all output pins
Operating temperature	T _{opr}	−10 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	400	mW	SDIP-52P-01

*¹ V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3 V.*² The large current output port is Port D (PD) and Port F (PF).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5	V	Guaranteed operation range for 1/16 frequency dividing clock or sleep mode
		2.7	5.5	V	Guaranteed operation range by TEX clock
		—	—	V	Guaranteed data hold operation range during stop* ⁵
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ¹
	V _{IHS}	0.8V _{DD}	V _{DD}	V	* ²
	V _{IHEX}	V _{DD} − 0.4	V _{DD} + 0.3	V	EXTAL pin* ³ , TEX pin* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ¹
	V _{ILS}	0	0.2V _{DD}	V	* ²
	V _{ILEX}	−0.3	0.4	V	EXTAL pin* ³ , TEX pin* ⁴
Operating temperature	T _{opr}	−10	+75	°C	

*¹ PA1 to 5, PB3 to 7, PD2, PE0, PE1, PE3, SCL0 to 1, SDA0 to 1 pins*² VSYNC, HSYNC, INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, RST, PB0, PB1, PB2 pins*³ Specifies only during external clock input.*⁴ Specifies only during external event count input.*⁵ This device does not enter the stop mode.

Electrical Characteristics

DC characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA, PB, PD, PE0 to PE1, PE4 to PE6, PG7, R, G, B	V _{DD} = 4.5V, I _{OH} = −0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = −1.2mA	3.5			V
Low level output voltage	V _{OL}	PA, PB, PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG7, R, G, B	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PD, PF	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
		PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)	V _{DD} = 4.5V, I _{OL} = 3.0mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 4.0mA			0.6	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{ILE}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.5		−40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
	I _{ILT}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.1		−10	μA
	I _{ILR}	$\overline{\text{RST}}^{*1}$		−1.5		−400	μA
I/O leakage current	I _{Iz}	PA, PB, PD, PE, PG7, R, G, B, $\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Open drain I/O leakage current (in N-ch Tr off state)	I _{LOH}	PF0 to PF3	V _{DD} = 5.5V, V _{OH} = 12.0V			50	μA
		PF4 to PF7	V _{DD} = 5.5V, V _{OH} = 5.5V			10	μA
I ² C bus switch connection impedance (in output Tr off state)	R _{BS}	SCL0: SCL1 SDA0: SDA1	V _{DD} = 4.5V V _{SCL0} = V _{SCL1} = 2.25V V _{SDA0} = V _{SDA1} = 2.25V			120	Ω
Supply current*2	I _{DD1}	V _{DD}	1/2 frequency dividing clock		25	38	mA
	V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF)						
	I _{DD2}		V _{DD} = 3.3V, 32MHz crystal oscillation (C ₁ = C ₂ = 47pF)		30	90	μA
	I _{DDS1}		Sleep mode		1.2	2.1	mA
			V _{DD} = 5.5V, 16MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DDS2}		V _{DD} = 3.3V, 32MHz crystal oscillation (C ₁ = C ₂ = 47pF)		15	38	μA
I _{DDS3}	Stop mode*3 V _{DD} = 5.5V, termination of 16MHz and 32MHz oscillation		—	—	—	μA	

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	PA, PB, PD, PE0 to PE3, R, G, B, PF, PG7, EXTAL, TEX, EXLC, $\overline{\text{RST}}$	Clock 1MHz 0V for no-measured pins		10	20	pF

*1 For $\overline{\text{RST}}$ pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

*2 When all output pins are left open. Specifies only when the OSD oscillation is halted.

*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max	Unit
System clock frequency	f _c	XTAL EXTAL	Fig. 1, Fig.2	8		16	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig.2 External clock drive	28			ns
System clock input rise and fall times	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig.2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{\text{EC}}$	Fig. 3	4t _{sys} *1			ns
Event count input clock rise and fall times	t _{ER} , t _{EF}	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	f _c	TEX TX	V _{DD} = 2.7 to 5.5 V Fig. 2 (32kHz clock applied conditions)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise and fall times	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} Indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t_{sys} (ns) = 2000/f_c (Upper 2 bits = "00"), 4000/f_c (Upper 2 bits = "01"), 16000/f_c (Upper 2 bits = "11")

Fig. 1. Clock timing

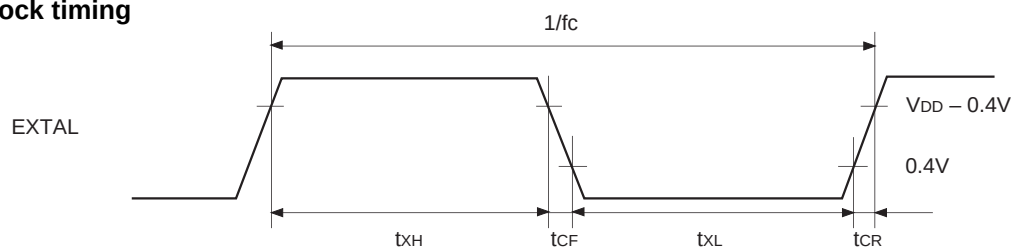


Fig.2. Clock applied conditions

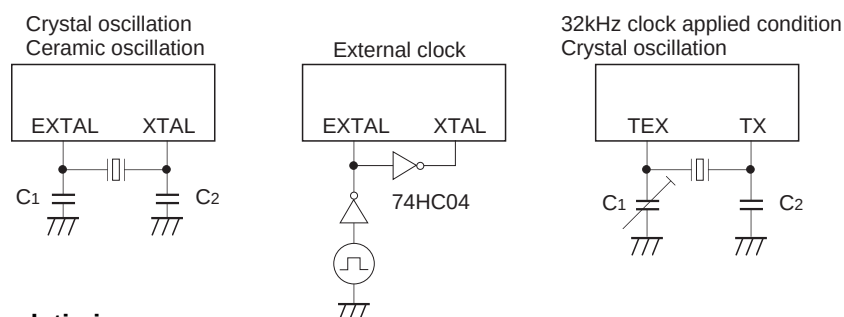
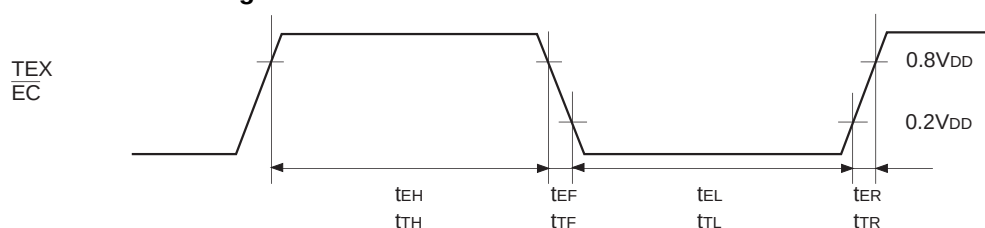


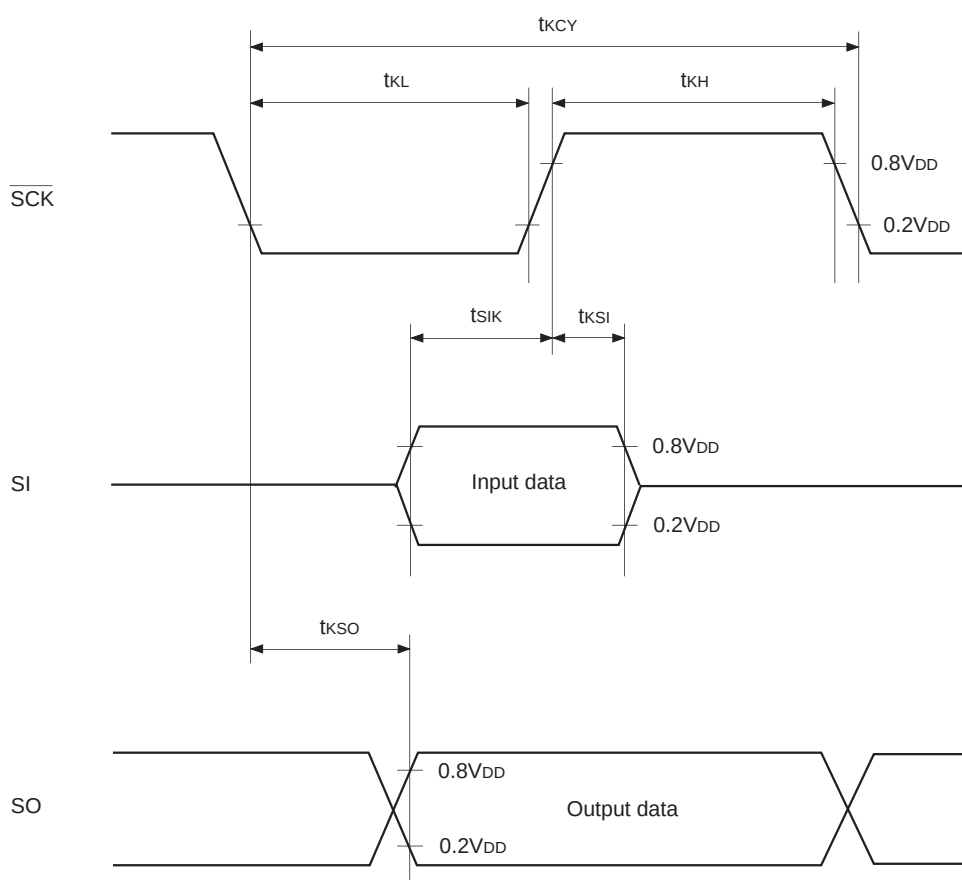
Fig. 3. Event count clock timing



(2) Serial transfer

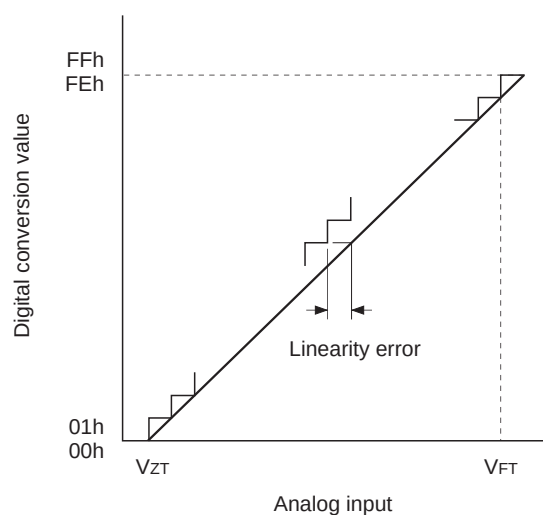
(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
$\overline{\text{SCK}}$ cycle time	t_{KCY}	$\overline{\text{SCK}}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{\text{SCK}}$ High and Low level width	t_{KH} t_{KL}	$\overline{\text{SCK}}$	$\overline{\text{SCK}}$ input mode	400		ns
			$\overline{\text{SCK}}$ output mode	4000/fc - 50		ns
SI input setup time (for $\overline{\text{SCK}} \uparrow$)	t_{SIK}	SI	$\overline{\text{SCK}}$ input mode	100		ns
			$\overline{\text{SCK}}$ output mode	200		ns
SI hold time (for $\overline{\text{SCK}} \uparrow$)	t_{KSI}	SI	$\overline{\text{SCK}}$ input mode	200		ns
			$\overline{\text{SCK}}$ output mode	100		ns
$\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time	t_{KSO}	SO	$\overline{\text{SCK}}$ input mode		200	ns
			$\overline{\text{SCK}}$ output mode		100	ns

Note) The load of $\overline{\text{SCK}}$ output mode and SO output delay time is 50pF + 1TTL.**Fig. 4. Serial transfer timing**

(3) A/D converter(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V _{DD} = 5.0V V _{SS} = 0V			±3	LSB
Zero transition voltage	V _{ZT} *1			-10	10	70	mV
Full-scale transition voltage	V _{FT} *2			4910	4970	5030	mV
Conversion time	t _{CONV}			26/f _{ADC} *3			μs
Sampling time	t _{SAMP}			6/f _{ADC} *3			μs
Analog input voltage	V _{IAN}	AN0 to AN5		0		V _{DD}	V

Fig. 5. Definitions for A/D converter terms

*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

(4) Interruption, reset input (Ta = -10 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig. 6. Interruption input timing

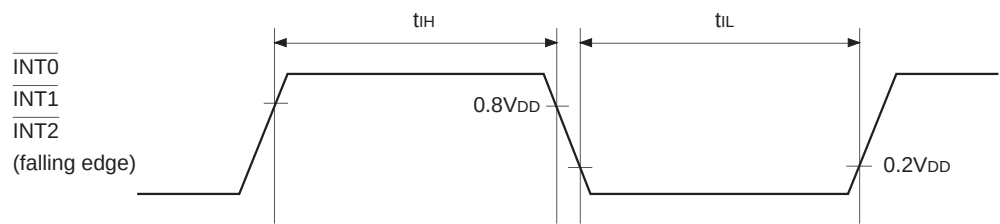
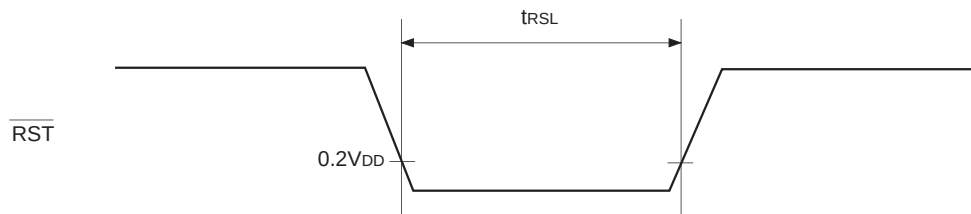


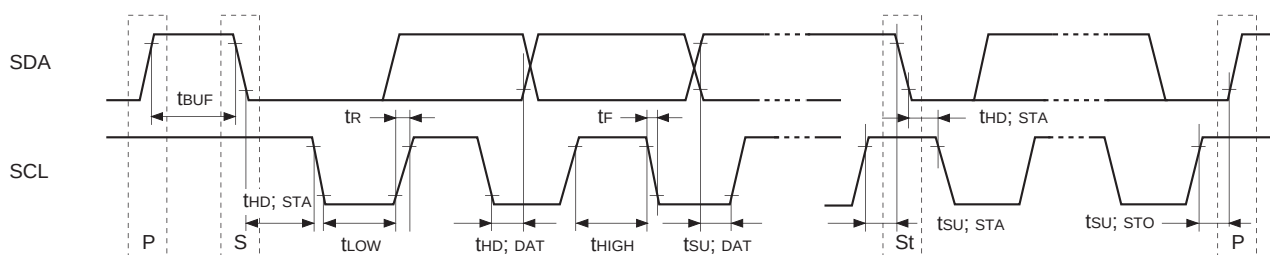
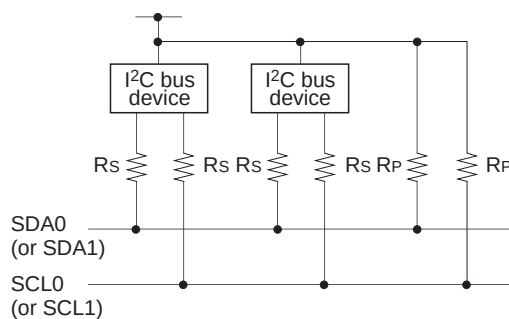
Fig. 7. $\overline{RST}$ input timing



(5) I²C bus timing(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	SCL		0	100	kHz
Bus-free time before starting transfer	t _{BUF}	SDA, SCL		4.7		μs
Hold time for starting transfer	t _{HD; STA}	SDA, SCL		4.0		μs
Clock Low level width	t _{LOW}	SCL		4.7		μs
Clock High level width	t _{HIGH}	SCL		4.0		μs
Setup time for repeated transfers	t _{SU; STA}	SDA, SCL		4.7		μs
Data hold time	t _{HD; DAT}	SDA, SCL		0*1		μs
Data setup time	t _{SU; DAT}	SDA, SCL		250		ns
SDA, SCL rise time	t _R	SDA, SCL			1	μs
SDA, SCL fall time	t _F	SDA, SCL			300	ns
Setup time for transfer completion	t _{SU; STO}	SDA, SCL		4.7		μs

*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

Fig. 8. I²C bus transfer timingFig. 9. I²C bus device recommended circuit

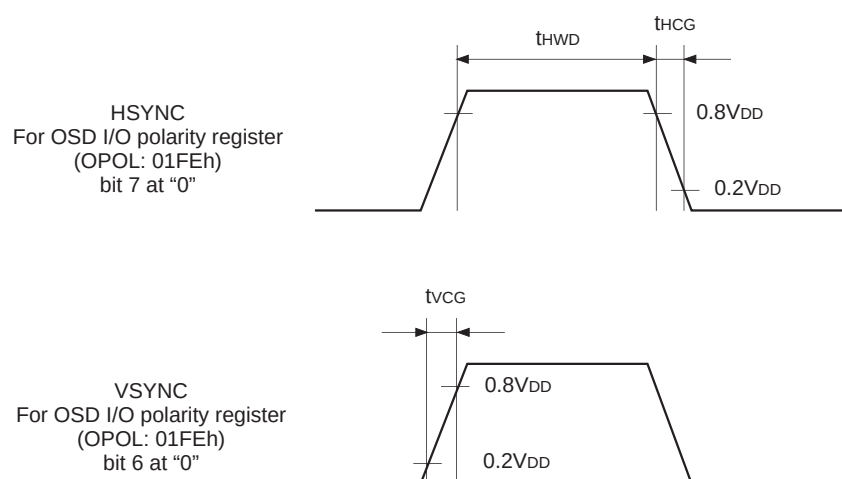
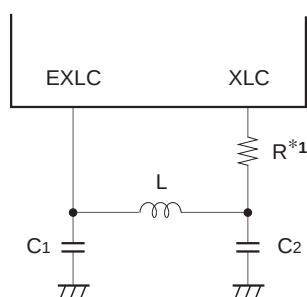
- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs = 300Ω or less) can be reduce the spike noise caused by CRT flashover.

(6) OSD timing(Ta = -10 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Max	Unit
OSD clock frequency	f _{OSC}	EXLC XLC	Fig. 11	4	30.4* ¹	MHz
HSYNC pulse width	t _{HWD}	HSYNC	Fig. 10	2		μs
HSYNC after-write rise and fall times	t _{HCG}	HSYNC	Fig. 10		200	ns
VSYNC before-write rise and fall times	t _{VCG}	VSYNC	Fig. 10		1.0	μs

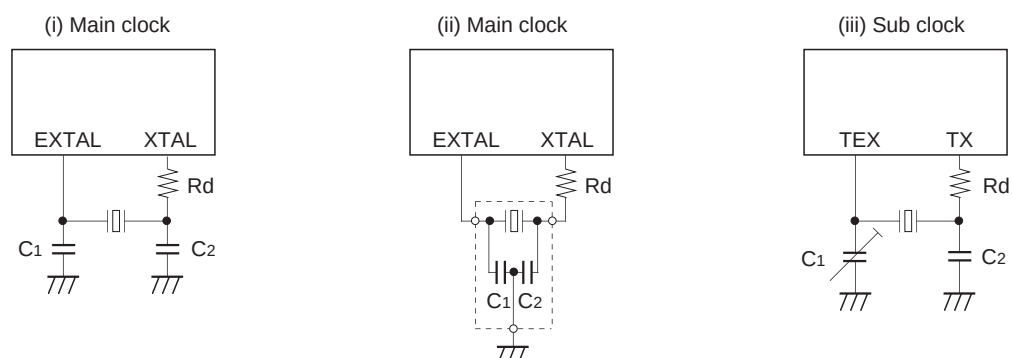
*¹ The maximum value of f_{OSC} is specified with the following equation.

$$f_{OSC} [\text{max}] \leq f_c \times 1.9$$

Fig. 10. OSD timing**Fig. 11. LC oscillation circuit connection***¹ The series resistor for XLC can reduce the frequency of occurrence of the undesired radiation.

Appendix

Fig. 12. Recommended oscillation circuit

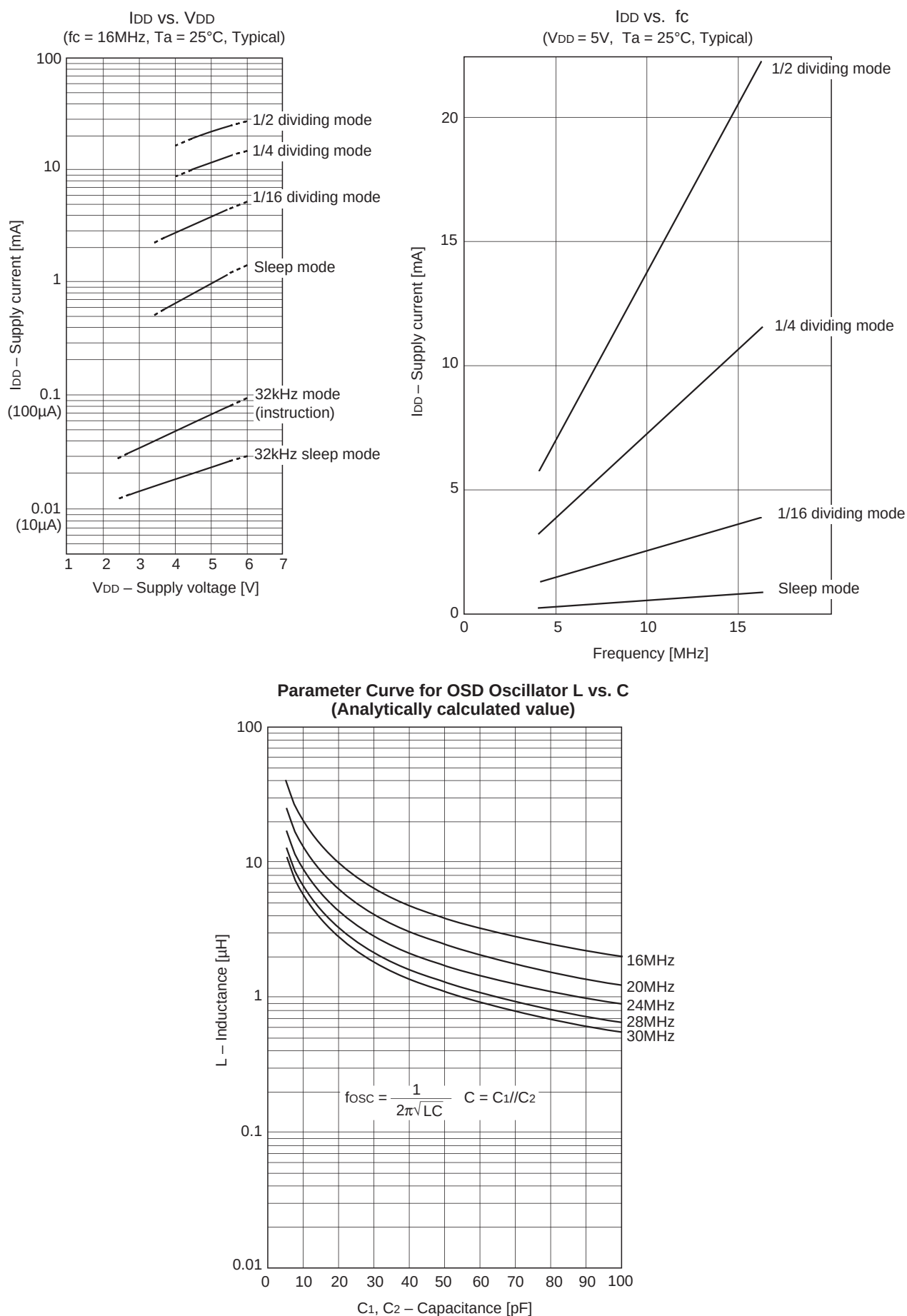


Manufacture	Model	fc (MHz)	C1 (pF)	C2 (pF)	Rd (Ω)	Circuit example	
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0 * ¹	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5		(ii)	
	CST10.0MTW*	10.0	30	30			
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CO., LTD.	HC-49/U03	8.0	18	18	330 * ¹	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0 * ¹		(iii)
		12.0	5	5			
		16.0	OPEN	OPEN			
	P3	32.768kHz	30	33	120k		

* Models with an asterisk have the built-in ground capacitance (C₁, C₂).

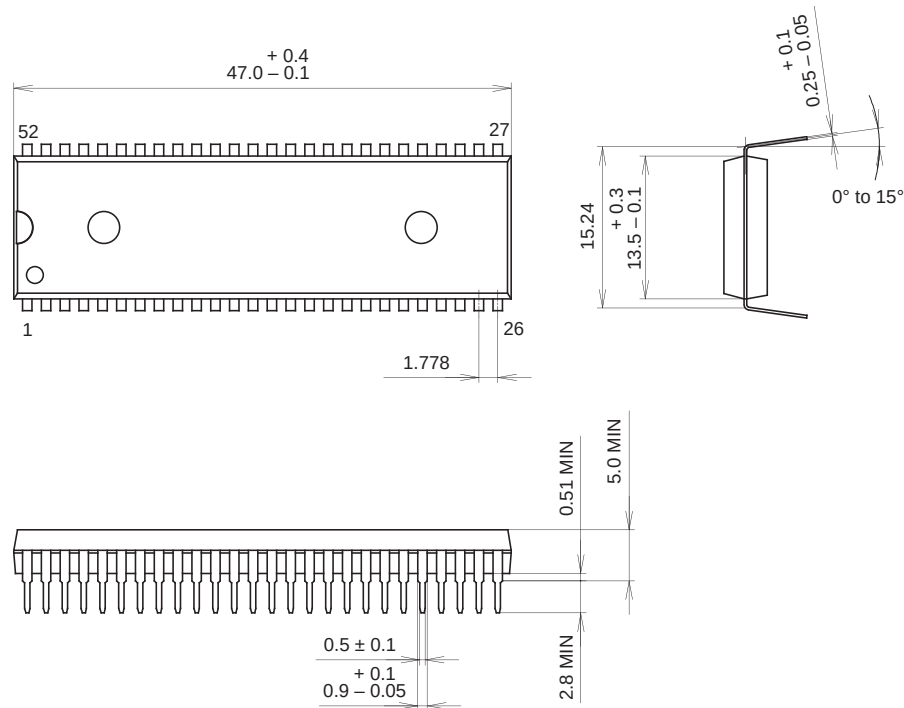
*¹ The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.

Fig. 13. Characteristic curves



Package Outline Unit: mm

52PIN SDIP (PLASTIC) 600mil



PACKAGE STRUCTURE

SONY CODE	SDIP-52P-01	PACKAGE MATERIAL	EPOXY RESIN
EIAJ CODE	SDIP052-P-0600-A	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE	_____	LEAD MATERIAL	COPPER
		PACKAGE WEIGHT	_____

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).