查询SC1164供应商

October 25, 1999

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1164/5 combines a synchronous voltage mode controller with two low-dropout linear regulators providing most of the circuitry necessary to implement three DC/DC converters for powering advanced microprocessors such as Pentium® II.

The SC1164/5 switching section features an integrated 5 bit D/A converter, pulse by pulse current limiting, integrated power good signaling, and logic compatible shutdown. The SC1164/5 switching section operates at a fixed frequency of 200kHz, providing an optimum compromise between size, efficiency and cost in the intended application areas. The integrated D/A converter provides programmability of output voltage from 2.0V to 3.5V in 100mV increments and 1.30V to 2.05V in 50mV increments with no external components.

The SC1164/5 linear sections are low dropout regulators. The SC1164 supplies 1.5V for GTL bus and 2.5V for non-GTL I/O.

For the SC1165 both LDO's are adjustable.

FEATURES

- Synchronous design, enables no heatsink solution
- 95% efficiency (switching section)
- 5 bit DAC for output programmability
- On chip power good function
- Designed for Intel Pentium® II requirements
- 1.5V, 2.5V or Adj. @ 1% for linear section

APPLICATIONS

- Pentium® II or Deschutes microprocessor supplies
- Flexible motherboards
- 1.3V to 3.5V microprocessor supplies
- Programmable triple power supplies

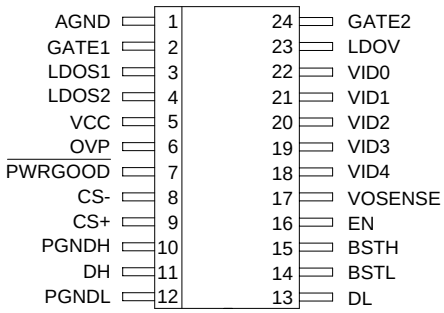
ORDERING INFORMATION

Part Number(1)	Package	Linear Voltage	Temp. Range (T_J)
SC1164CSW	SO-24	1.5V/2.5V	0° to 125°C
SC1165CSW	SO-24	Adj.	0° to 125°C

Note:
(1) Add suffix 'TR' for tape and reel.

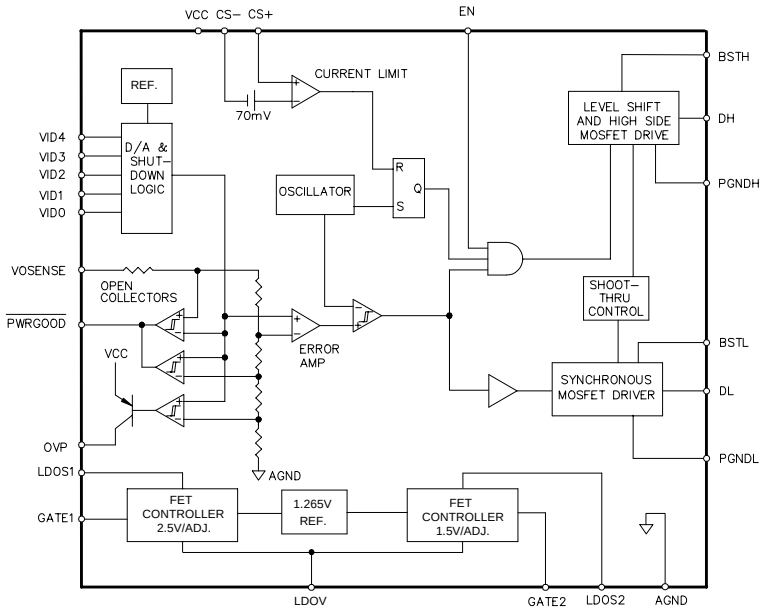
PIN CONFIGURATION

Top View



(24 Pin SOIC)

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
VCC to GND	VCC	-0.3 to +7	V
PGND to GND		± 1	V
BST to GND		-0.3 to +15	V
Operating Temperature Range	T_A	0 to +70	°C
Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 seconds	T_L	300	°C
Thermal Impedance Junction to Ambient	θ_{JA}	80	°C/W
Thermal Impedance Junction to Case	θ_{JC}	25	°C/W

ELECTRICAL CHARACTERISTICS

Unless specified: VCC = 4.75V to 5.25V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; LDOV = 11.4V to 12.6V; T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Section					
Output Voltage	I_O = 2A	See Note 1.			
Supply Voltage	VCC	4.5		7	V
Supply Current	VCC = 5.0V		8	15	mA
Load Regulation	I_O = 0.8A to 15A		1		%
Line Regulation			0.5		%
Current Limit Voltage		55	70	85	mV
Oscillator Frequency		175	200	225	kHz
Oscillator Max Duty Cycle		90	95		%
Peak DH Sink/Source Current	BSTH-DH = 4.5V, DH-PGNDH = 3V	1			A
Peak DL Sink/Source Current	BSTL-DL = 4.5V, DL-PGNDL = 3V	1			A
Output Voltage Tempco			65		ppm/°C
Gain (A_{OL})	VOSENSE to V_O		35		dB
OVP threshold voltage			120		%
OVP source current	V_{OVP} = 3.0V	10			mA
Power good threshold voltage		85		115	%
Dead time		50	100		ns
Linear Sections					
Quiescent current	LDOV = 12V			5	mA
Output Voltage (LDO1 SC1164)		2.475	2.500	2.525	V
Output Voltage (LDO2 SC1164)		1.485	1.500	1.515	V
Reference Voltage (SC1165)		1.252	1.265	1.278	V
Feedback Pin Bias Current (SC1165)				10	uA
Gain (A_{OL})	LDOS (1,2) to GATE (1,2)		90		dB
Load Regulation	I_O = 0 to 8A(2)			0.3	%
Line Regulation				0.3	%
Output Impedance			1		KΩ

Notes: (1) See Output Voltage table.
(2) In application circuit.

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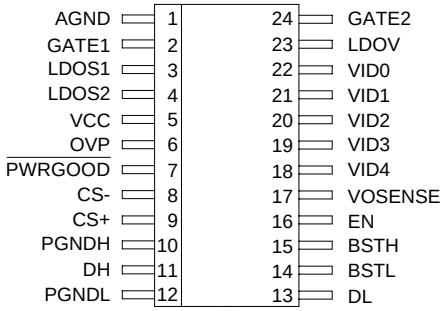
PIN DESCRIPTION

Pin	Pin Name	Pin Function
1	AGND	Small Signal Analog and Digital Ground
2	GATE1	Gate Drive Output LDO1
3	LDOS1	Sense Input for LDO1
4	LDOS2	Sense Input for LDO2
5	VCC	Input Voltage
6	OVP	High Signal out if V_O>setpoint +20%
7	$\overline{\text{PWRGOOD}}$[1]	Open collector logic output, high if V_O within 10% of setpoint
8	CS-	Current Sense Input (negative)
9	CS+	Current Sense Input (positive)
10	PGNDH	Power Ground for High Side Switch
11	DH	High Side Driver Output
12	PGNDL	Power Ground for Low Side Switch
13	DL	Low Side Driver Output
14	BSTL	Supply for Low Side Driver
15	BSTH	Supply for High Side Driver
16	EN[1]	Logic low shuts down the converter; High or open for normal operation.
17	VOSENSE	Top end of internal feedback chain
18	VID4[1]	Programming Input (MSB)
19	VID3[1]	Programming Input
20	VID2[1]	Programming Input
21	VID1[1]	Programming Input
22	VID0[1]	Programming Input (LSB)
23	LDOV	+12V for LDO section
24	GATE2	Gate Drive Output LDO2

Top View



(24 Pin SOIC)

Note:
(1) All logic level inputs and outputs are open collector TTL compatible.

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OUTPUT VOLTAGE

Unless specified: VCC = 5.00V; GND = PGND = 0V; VOSENSE = V_O; 0mV < (CS+-CS-) < 60mV; T_A = 25°C

PARAMETER	CONDITIONS	VID 43210	MIN	TYP	MAX	UNITS
Output Voltage	I_O = 2A in Application Circuit	01111	1.274	1.300	1.326	
		01110	1.323	1.350	1.377	
		01101	1.372	1.400	1.428	
		01100	1.421	1.450	1.479	
		01011	1.470	1.500	1.530	
		01010	1.527	1.550	1.573	
		01001	1.576	1.600	1.624	
		01000	1.625	1.650	1.675	
		00111	1.675	1.700	1.726	
		00110	1.724	1.750	1.776	
		00101	1.773	1.800	1.827	
		00100	1.822	1.850	1.878	
		00011	1.871	1.900	1.929	
		00010	1.921	1.950	1.979	
		00001	1.970	2.000	2.030	
		00000	2.019	2.050	2.081	
		11111	1.940	2.000	2.060	
		11110	2.058	2.100	2.142	
		11101	2.156	2.200	2.244	
		11100	2.254	2.300	2.346	
		11011	2.352	2.400	2.448	
		11010	2.450	2.500	2.550	
		11001	2.548	2.600	2.652	
		11000	2.646	2.700	2.754	
		10111	2.744	2.800	2.856	
		10110	2.842	2.900	2.958	
		10101	2.940	3.000	3.060	
		10100	3.038	3.100	3.162	
		10011	3.136	3.200	3.264	
		10010	3.234	3.300	3.366	
		10001	3.332	3.400	3.468	
		10000	3.430	3.500	3.570	

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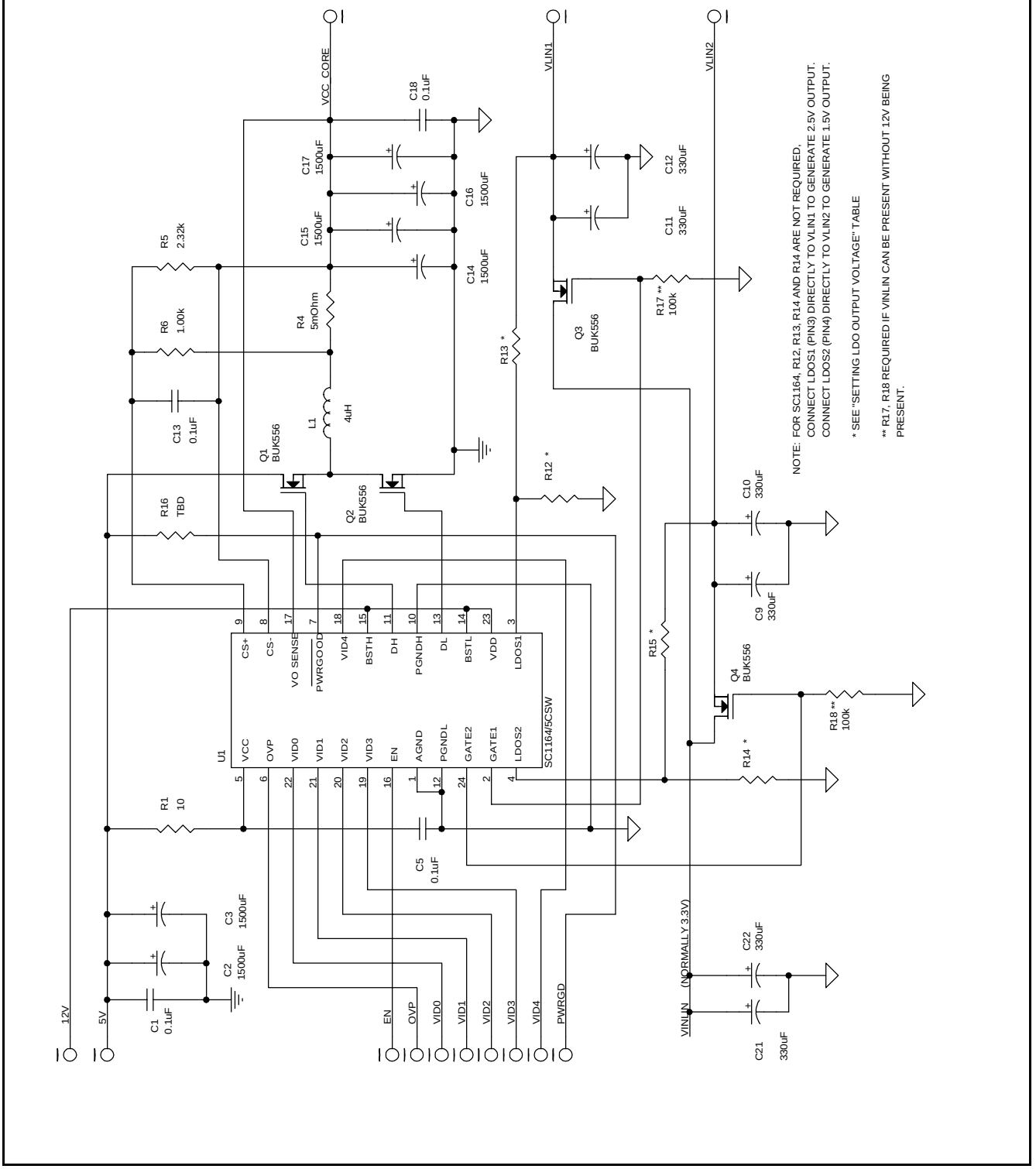
APPLICATION CIRCUIT



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MATERIALS LIST

Qty.	Reference	Part/Description	Vendor	Notes
4	C1,C5,C13,C18	0.1µF Ceramic	Various	
6	C2,C3,C14-C17	1500µF/6.3V	SANYO	MV-GX or equiv. Low ESR
6	C9-C12, C21, C22	330µF/6.3V	Various	
1	L1	4µH		8 Turns 16AWG on MICROMETALS T50-52D core
4	Q1,Q2,Q3, Q4	See notes	See notes	FET selection requires trade-off between efficiency and cost. Absolute maximum $R_{DS(ON)}$ = 22 mΩ for Q1,Q2
1	R4	5mΩ	IRC	OAR-1 Series
1	R5	2.32kΩ, 1%, 1/8W	Various	
1	R6	1kΩ, 1%, 1/8W	Various	
1	R1	10Ω, 5%, 1/8W	Various	
1	R12	1%, 1/8W	Various	See Table Below (Not required for SC1164)
1	R13	1%, 1/8W	Various	See Table Below (Not required for SC1164)
1	R14	1%, 1/8W	Various	See Table Below (Not required for SC1164)
1	R15	1%, 1/8W	Various	See Table Below (Not required for SC1164)
2	R17,R18	100kΩ, 5%,1/8W	Various	Required if Voltage is applied to the linear FET(s) without 12V applied to SC1164/5
1	U1	SC1164/5CSW	SEMTECH	

SETTING LDO OUTPUT VOLTAGE

	R_B	R_A
VOUT LDO1 (LDO2)	R12 (R14)	R13 (R15)
3.45V	105Ω	182Ω
3.30V	105Ω	169Ω
3.10V	102Ω	147Ω
2.90V	100Ω	130Ω
2.80V	100Ω	121Ω
2.50V	100Ω	97.6Ω
1.50V	100Ω	18.7Ω

$$V_{OUT} = \frac{1.265 \cdot (R_A + R_B)}{R_B} + (I_{FB} \cdot R_A)$$

Where :

I_{FB} = Feedback pin bias current

R_A = Top feedback resistor

R_B = Bottom feedback resistor

See layout diagram for clarification

R_A and R_B must be low enough so that the $(I_{FB} \cdot R_A)$ term does not cause significant error

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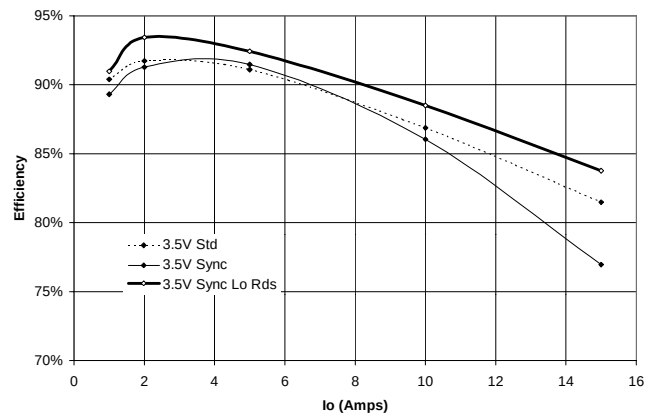
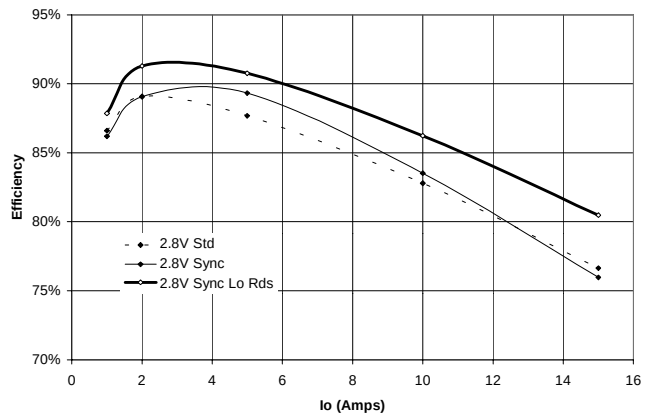
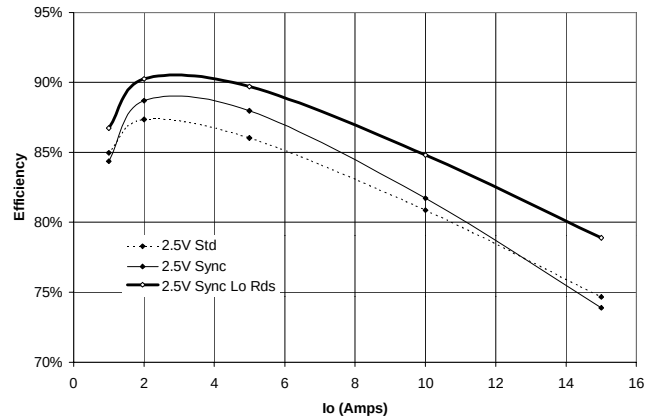


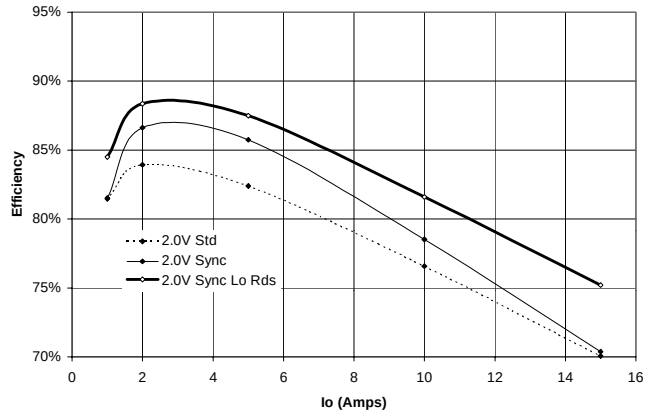
Typical Efficiency at Vo=3.5V



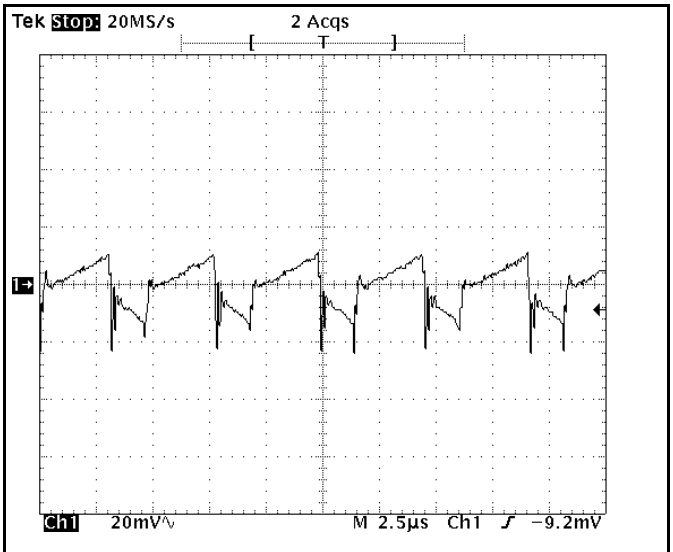
Typical Efficiency at Vo=2.8V



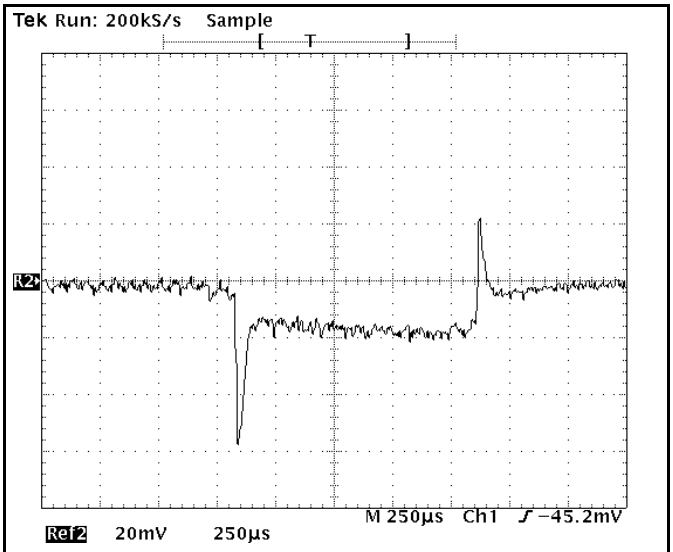
Typical Efficiency at Vo=2.5V



Typical Efficiency at Vo=2.0V



Typical Ripple, Vo=2.8V, Io=10A



Transient Response Vo=2.8V, Io=300mA to 10A

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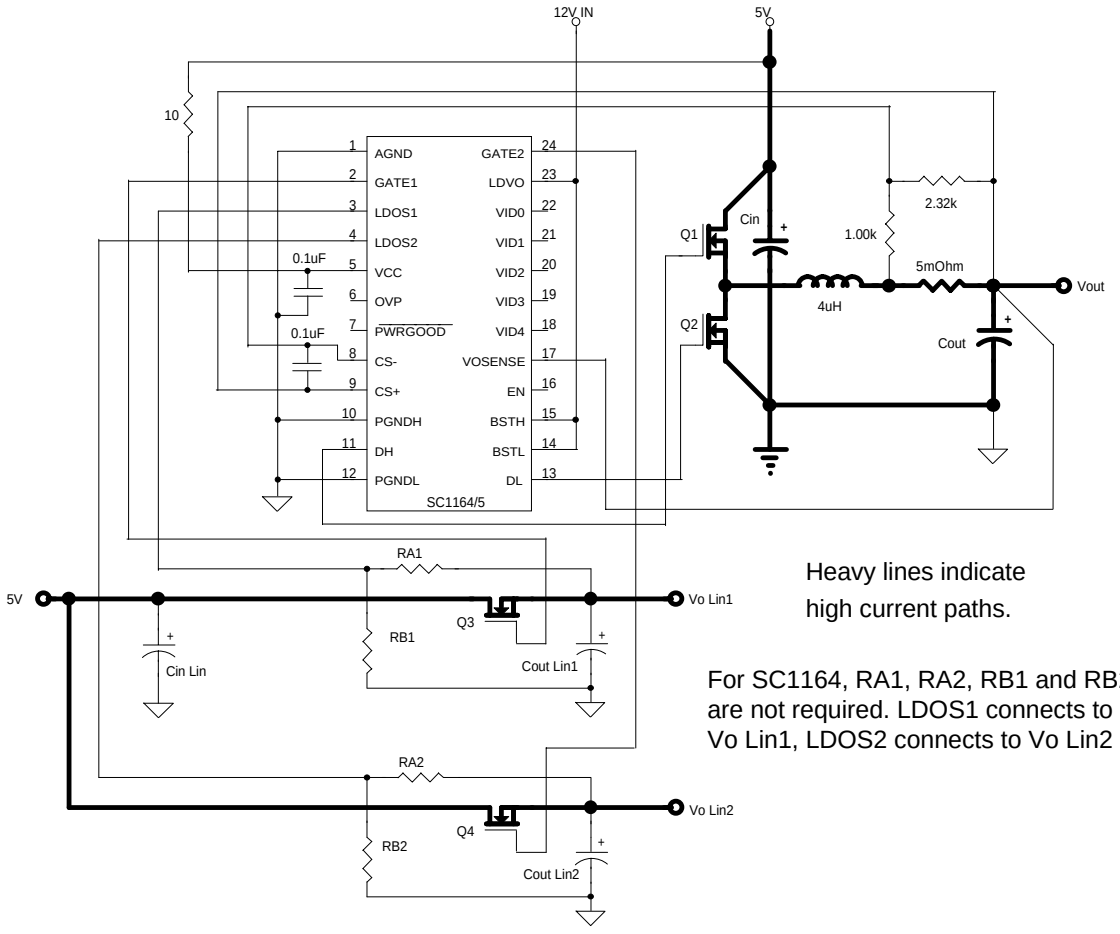
LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC1164/5 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Bottom FET (Q2) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, Q2 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.



Layout diagram for the SC1164/5

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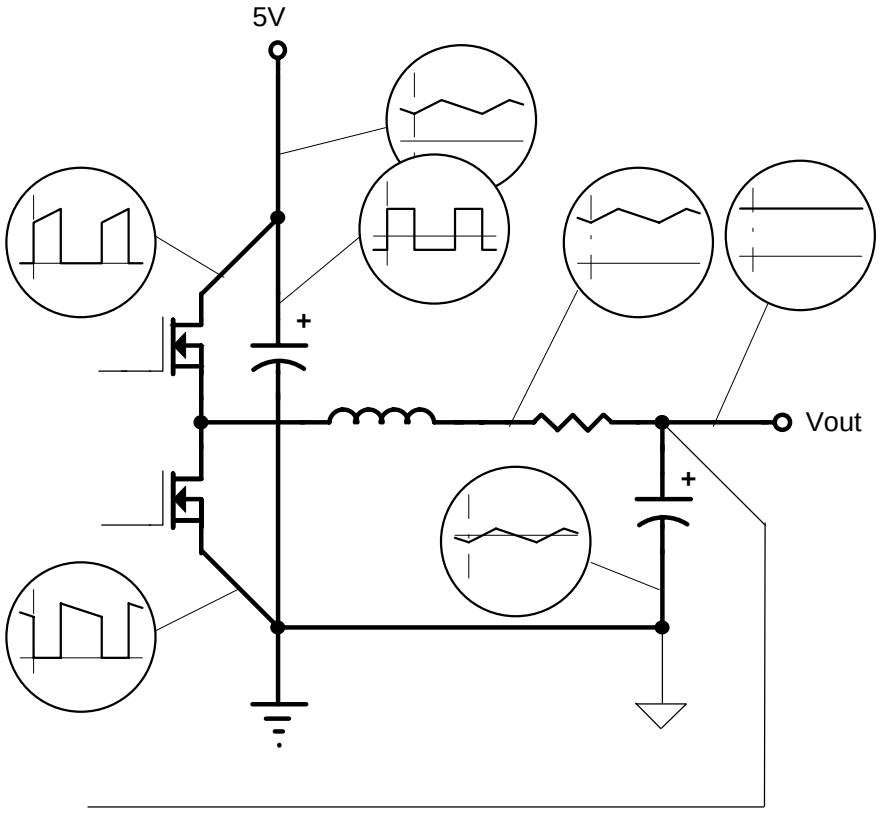
4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1164/5 is best placed over a quiet ground plane area, avoid pulse currents in the Cin, Q1, Q2 loop flowing in this area. PGNDH and PGNDL should be returned to the ground plane close to the package. The AGND pin should be connected to the ground side of (one of) the output capacitor(s). If this is not possible, the AGND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should AGND be returned to a ground inside the Cin, Q1, Q2 loop.

6) Vcc for the SC1164/5 should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to AGND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS+ and CS- on the SC1164/5 should run parallel and close to each other. The 0.1µF capacitor should be mounted as close to the CS+ and CS- pins as possible.

8) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).



Currents in various parts of the power section

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COMPONENT SELECTION

SWITCHING SECTION

OUTPUT CAPACITORS - Selection begins with the most critical component. Because of fast transient load current requirements in modern microprocessor core supplies, the output capacitors must supply all transient load current requirements until the current in the output inductor ramps up to the new level. Output capacitor ESR is therefore one of the most important criteria. The maximum ESR can be simply calculated from:

$$R_{ESR} \leq \frac{V_t}{I_t}$$

Where

V_t = Maximum transient voltage excursion

I_t = Transient current step

For example, to meet a 100mV transient limit with a 10A load step, the output capacitor ESR must be less than 10mΩ. To meet this kind of ESR level, there are three available capacitor technologies.

Technology	Each Capacitor		Qty. Rqd.	Total	
	C (µF)	ESR (mΩ)		C (µF)	ESR (mΩ)
Low ESR Tantalum	330	60	6	2000	10
OS-CON	330	25	3	990	8.3
Low ESR Aluminum	1500	44	5	7500	8.8

The choice of which to use is simply a cost/performance issue, with Low ESR Aluminum being the cheapest, but taking up the most space.

INDUCTOR - Having decided on a suitable type and value of output capacitor, the maximum allowable value of inductor can be calculated. Too large an inductor will produce a slow current ramp rate and will cause the output capacitor to supply more of the transient load current for longer - leading to an output voltage sag below the ESR excursion calculated above. The maximum inductor value may be calculated from:

$$L \leq \frac{R_{ESR}\ C}{I_t}\left(V_{IN} - V_O\right)$$

The calculated maximum inductor value assumes 100% duty cycle, so some allowance must be made. Choosing an inductor value of 50 to 75% of the calculated maximum will guarantee that the inductor current will ramp fast enough to reduce the voltage dropped across the ESR at a faster rate than the capacitor sags, hence ensuring a good recovery from transient with no additional excursions.

We must also be concerned with ripple current in the output inductor and a general rule of thumb has been to allow 10% of maximum output current as ripple current. Note that most of the output voltage ripple is produced by the inductor ripple current flowing in the output capacitor ESR. Ripple current can be calculated from:

$$I_{L_{RIPPLE}} = \frac{V_{IN}}{4 \cdot L \cdot f_{OSC}}$$

Ripple current allowance will define the minimum permitted inductor value.

POWER FETS - The FETs are chosen based on several criteria with probably the most important being power dissipation and power handling capability.

TOP FET - The power dissipation in the top FET is a combination of conduction losses, switching losses and bottom FET body diode recovery losses.

a) Conduction losses are simply calculated as:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot \delta$$

where

$$\delta = \text{duty cycle} \approx \frac{V_O}{V_{IN}}$$

b) Switching losses can be estimated by assuming a switching time, if we assume 100ns then:

$$P_{SW} = I_O \cdot V_{IN} \cdot 10^{-2}$$

or more generally,

$$P_{SW} = \frac{I_O \cdot V_{IN} \cdot (t_r + t_f) \cdot f_{OSC}}{4}$$

c) Body diode recovery losses are more difficult to estimate, but to a first approximation, it is reasonable to assume that the stored charge on the bottom FET body diode will be moved through the top FET as it starts to turn on. The resulting power dissipation in the top FET will be:

$$P_{RR} = Q_{RR} \cdot V_{IN} \cdot f_{OSC}$$

To a first order approximation, it is convenient to only consider conduction losses to determine FET suitability. For a 5V in; 2.8V out at 14.2A requirement, typical FET losses would be:

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FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
BUK556H	22	2.48	TO220
IRL2203	7.0	0.79	D^2PAK
Si4410	13.5	1.53	SO-8

BOTTOM FET - Bottom FET losses are almost entirely due to conduction. The body diode is forced into conduction at the beginning and end of the bottom switch conduction period, so when the FET turns on and off, there is very little voltage across it, resulting in low switching losses. Conduction losses for the FET can be determined by:

$$P_{COND} = I_O^2 \cdot R_{DS(on)} \cdot (1 - \delta)$$

For the example above:

FET type	$R_{DS(on)}$ (mΩ)	P_D (W)	Package
BUK556H	22	1.95	TO220
IRL2203	7.0	0.62	D^2PAK
Si4410	13.5	1.20	SO-8

Each of the package types has a characteristic thermal impedance, for the TO-220 package, thermal impedance is mostly determined by the heatsink used. For the surface mount packages on double sided FR4, 2 oz printed circuit board material, thermal impedances of 40°C/W for the D^2PAK and 80°C/W for the SO-8 are readily achievable. The corresponding temperature rise is detailed below:

	Temperature rise (°C)	
FET type	Top FET	Bottom FET
BUK556H	49.6(1)	39.0(1)
IRL2203	31.6	24.8
Si4410	122.4	96
(1) With 20°C/W Heatsink		

It is apparent that single SO-8 Si4410 are not adequate for this application, but by using parallel pairs in each position, power dissipation will be approximately halved and temperature rise reduced by a factor of 4.

INPUT CAPACITORS - since the RMS ripple current in the input capacitors may be as high as 50% of the output current, suitable capacitors must be chosen accordingly. Also, during fast load transients, there may be restrictions on input di/dt. These restrictions require useable energy storage within the converter circuitry, either as extra output capacitance or, more usually, additional input capacitors. Choosing low ESR input capacitors will help maximize ripple rating for a given size.

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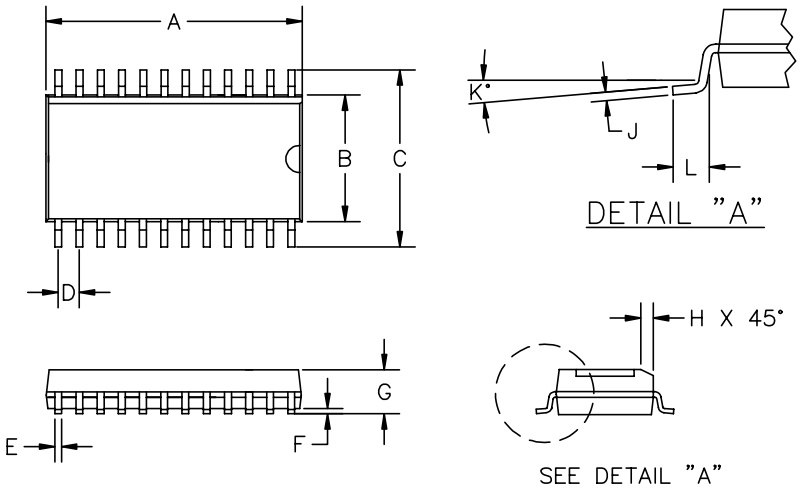
OUTLINE DRAWING - SO-24



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.5985	.6141	15.20	15.60	[2]
B	.2914	.2992	7.40	7.60	[2]
C	.394	.419	10.00	10.64	–
D	.050	BSC	1.27	BSC	–
E	.013	.020	.33	.51	–
F	.004	0.118	.10	.30	–
G	.0926	.1043	2.35	2.64	–
H	.010	.029	.25	.74	–
J	.0091	.0125	.23	.32	–
K	0°	8°	0°	8°	–
L	.016	.050	.41	1.27	–

JEDEC MS-013AD

B17104B

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTUSIONS
[1] CONTROLLING DIMENSION : MILLIMETERS.

ECN 99-667

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