Ordering number : ENN6688

CMOS IC

LC86P5632

8-Bit Single Chip Microcontroller with One-Time Programmable PROM

Preliminary

Overview

The LC86P5632 is a CMOS 8-bit single chip microcontroller with one-time PROM for the LC865600 series.
This microcontroller has the function and the pin description of the LC865600 series mask ROM version, and 32K-byte PROM.
DIP/QFP package are available for shipping as well as LC865600 series. It is suitable to set up first release, prototyping, developing and testing of set.

Features

(1) Option switching by PROM data
The option function of the LC865600 series can be specified by the PROM data.
LC86P5632 can be checked the function of the trial pieces using the mass production board.
(2) Internal one-time PROM capacity : 32768 bytes
(3) Internal RAM capacity : 512 bytes
Used PROM or RAM capacity are equal ROM or RAM capacity of mask ROM version which applies LC86P5632.

Mask ROM version	PROM capacity	RAM capacity
LC865632	32512 bytes	512 bytes
LC865628	28672 bytes	512 bytes
LC865624	24576 bytes	512 bytes
LC865620	20480 bytes	384 bytes
LC865616	16384 bytes	384 bytes
LC865612	12288 bytes	384 bytes
LC865608	8192 bytes	384 bytes

Programming service

We offers various services at nominal charges. These include the ROM writing, the ROM reading, the package stamping and the screening. Contact our representative for further information.

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

(4) Operating supply voltage : 4.5V to 6.0V
(5) Instruction cycle time : 0.98μs to 400μs
(6) Operating temperature : -30°C to +70°C
(7) The pin and the package compatible with the LC865600 series mask ROM devices
(8) Applicable mask ROM version : LC865632/ LC865628/ LC865624/LC865620/LC865616/ LC865612/ LC865608
(9) Factory shipment : DIP64S, QFP64E

Notice for use

LC86P5632 is provided for the first release and small shipping of the LC865600 series.
At using, take notice of the followings.

(1) A point of difference LC86P5632 and LC865600 series

Item	LC86P5632	LC865632/28/24/20/16/12/08
Port form at reset	Please refer "Port form at reset " on next page.	
Operation after reset releasing	The option is specified until 3ms after going to a 'H' level to the reset terminal by dgrees. The program is executed from 00H of the program counter.	The program is executed from 00H of the program counter immediately after going to a 'H' level to reset terminal.
Operating supply voltage range (VDD)	4.5V to 6.0V	2.7V to 6.0V
Total output current [∑IOAH(1)] [∑IOAH(2)]	Refer to 'electrical characteristics' on the semiconductor news.	
Power dissipation [IDDOP(1)] [IDDOP(2)] [IDDOP(3)] [IDDOP(4)]		

• A kind of the option corresponding of the LC86P5632

A kind of option	Pins, Circuits	Contents of the option
Input/output form of Input/output ports	Port 0 (Specified in a bit)	1. Input : No pull-up MOS Tr. Output : N-channel open drain 2. Input : Pull-up MOS Tr. Output : CMOS
	Port 1,2 (Specified in a bit)	1. Input : Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
	Port 3,4,5 (Specified in a bit)	1. Input : No Programmable pull-up MOS Tr. Output : N-channel open drain 2. Input : Programmable pull-up MOS Tr. Output : CMOS
Pull-up MOS Tr. Of port7	port7 (Specified in a bit)	1. Pull-up MOS Tr. not provided 2. Pull-up MOS Tr. provided * $\overline{P74}$ has on pull-up resistor option.

The port operation related the option is different at reset. Refer to the next table.

• Port form at reset

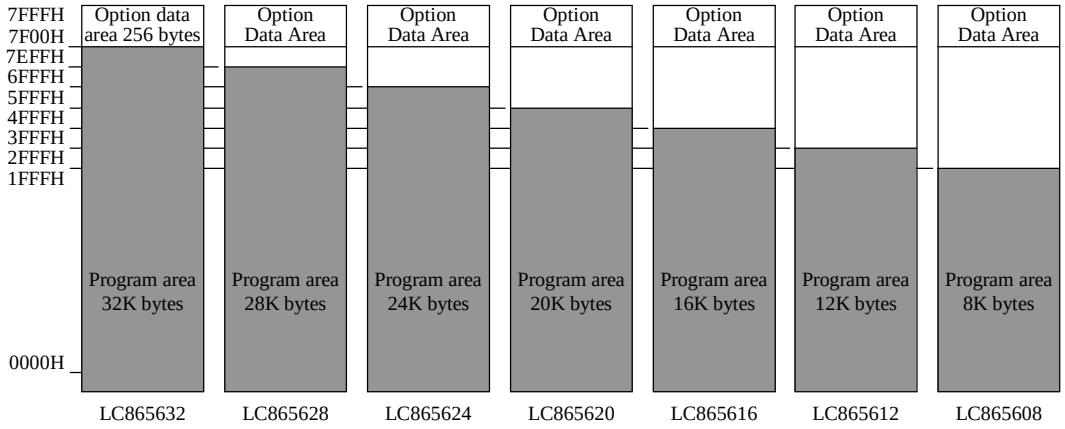
Pin	Contents of the option	LC86P5632	LC865632/28/24/20/16/12/08
P0	Input : Not pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Pull-up MOS Tr. Output : CMOS	Input mode •The pull-up MOS Tr. is not provided during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS Tr. is provided. (Output is OFF)	Input mode without pull-up MOS Tr. (Output is OFF)
P1, P2	Input : Programmable pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Programmable pull-up MOS Tr. Output : CMOS	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
P3, P4, P5	Input : Not Programmable pull-up MOS Tr. Output : N-channel open drain	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
	Input : Programmable pull-up MOS Tr. Output : CMOS	(Same as the mask version)	Input mode without pull-up MOS Tr. (Output is OFF)
P7	Pull-up MOS Tr. not provided	(Same as the mask version)	Input mode without pull-up MOS Tr.
	Pull-up MOS Tr. provided	Input mode •The pull-up MOS Tr. is not provided during reset or several hundred microseconds after releasing reset. After that, the pull-up MOS Tr. is provided.	Input mode without pull-up MOS Tr.

(2) Option

LC86P5632 uses 256 bytes which is addressed on 7F00H to 7FFFH in the program memory as option data area. This area does not affect the execution of program but the program memory capacity of LC865632 is 32512 bytes which is addressed on 0000H to 7EFFH.

The option data is created by the option specified program “SU865000.EXE”. The created option data is linked to the program area by linkage loader “L865000.EXE”.

(3) ROM space



(4) Ordering information

1. When ordering the identical mask ROM and PROM devices simultaneously.
   Provide an EPROM containing the target memory contents together with the separate order forms for each of the mask ROM and PROM versions.
2. When ordering a PROM device.
   Provide an EPROM containing the target memory contents together with an order form.

How to use

(1) Specification of option

Programming data for PROM of the LC86P5632 is required.
Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P5632.

(2) How to program for the PROM

LC86P5632 can be programmed by the EPROM programmer with attachment ; W86EP5032D, W86EP5032Q.

• Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL 1890A

• "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0000H to 7FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

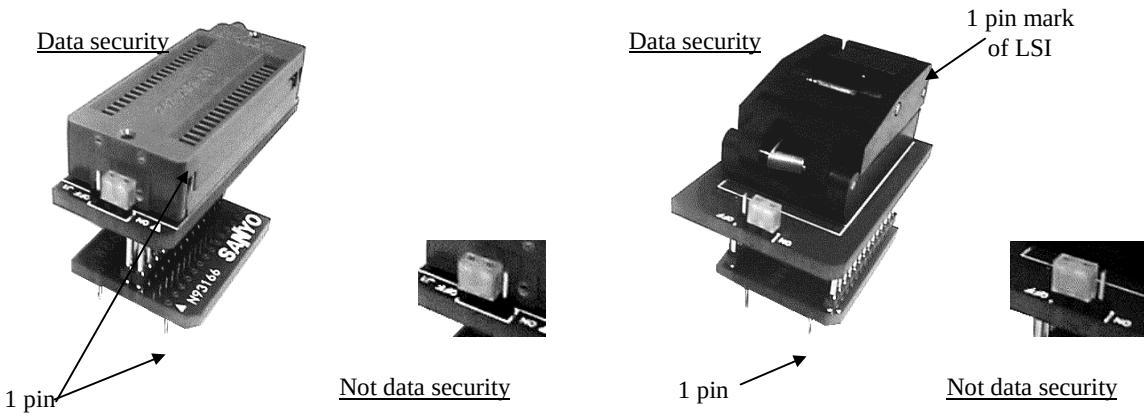
(3) How to use the data security function

"Data security" is the disabled function to read the data of the PROM.
The following is the process in order to execute the data security.

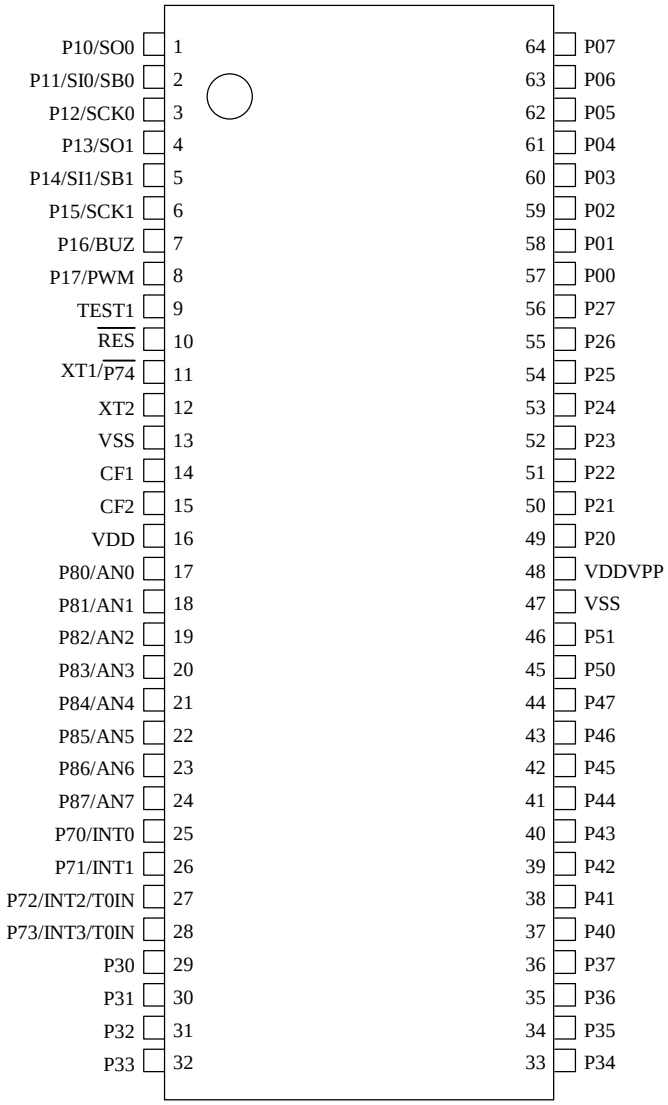
1. Set 'ON' the jumper of attachment.
2. Program again. Then EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

Notes

- Data security is not executed when the data of all address have 'FF' at the sequence 2 above.
- The programming by a sequential operation "BLANK⇒PROGRAM⇒VERIFY" cannot be executed data security at the sequence 2 above.
- Set to 'OFF' the jumper after executing the data security.



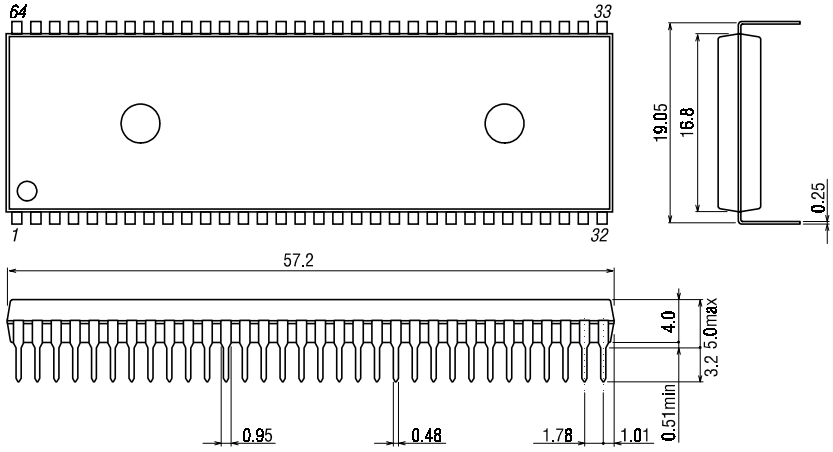
W86EP5032D W86EP5032Q



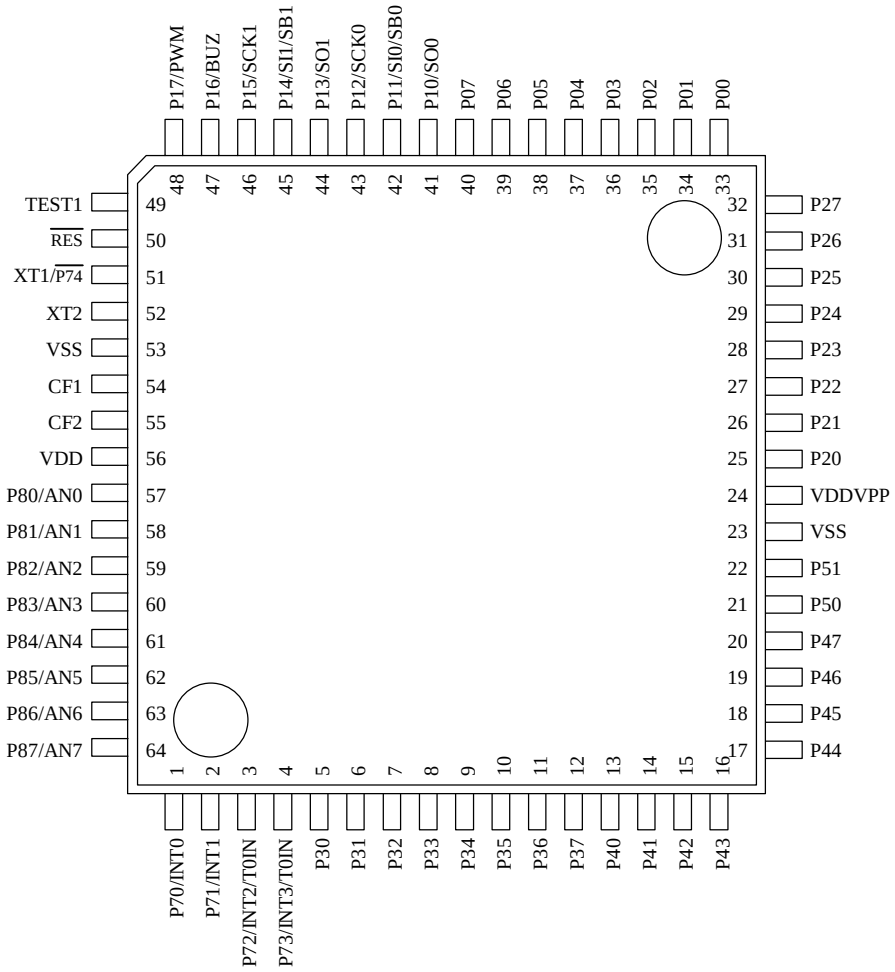
Package Dimension

(unit : mm)

3071



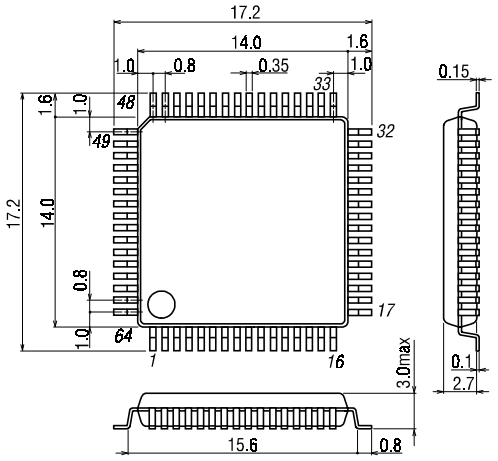
SANYO : DIP-64S(750mil)



Package Dimension

(unit : mm)

3159

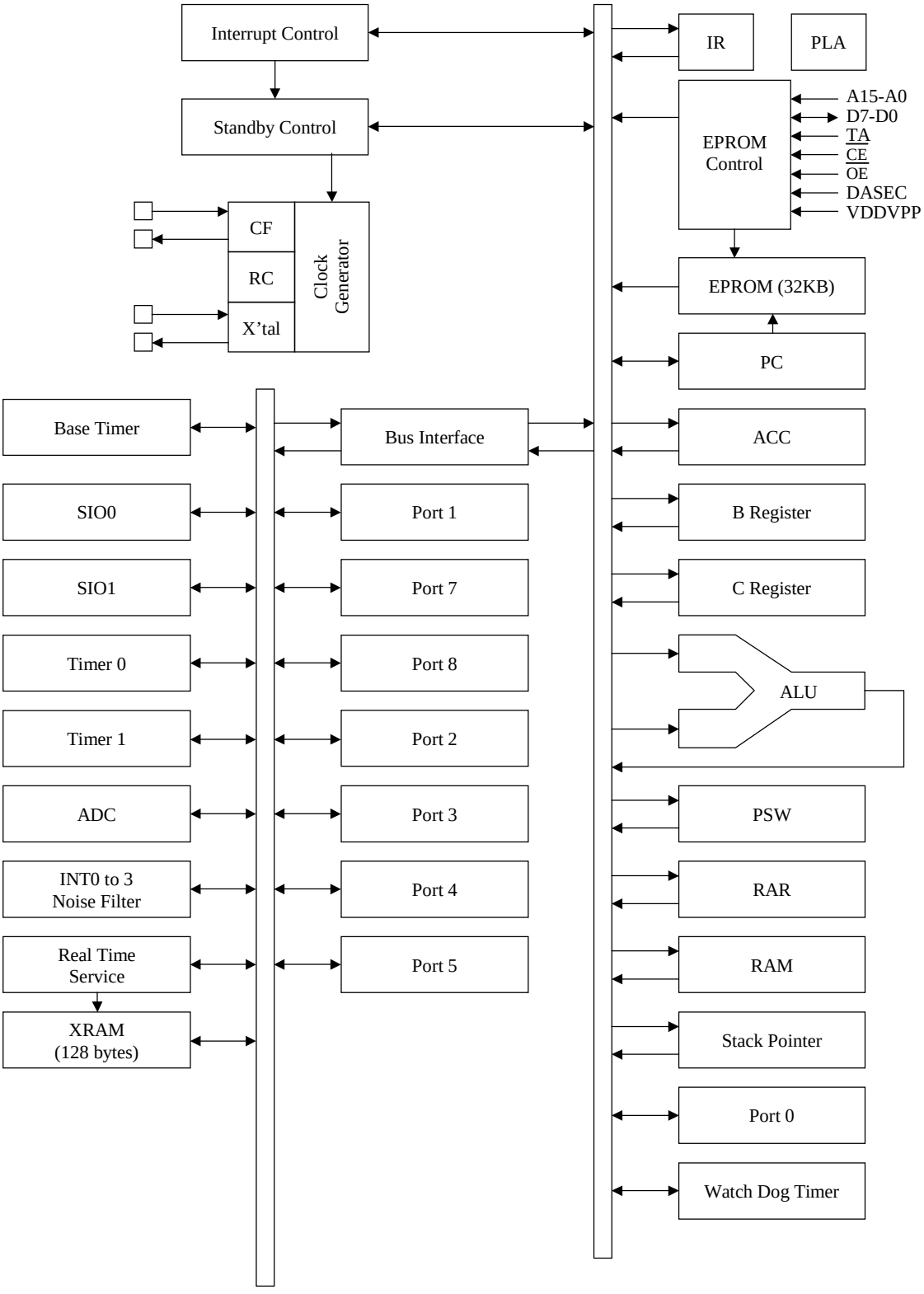


SANYO: QIP-64E

Notes

- The QFP packages should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

System Block Diagram



LC86P5632 Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Function description</th><th>Option</th><th>PROM mode</th></tr>
<tr><td>VSS</td><td>-</td><td>Power pin (-)</td><td>-</td><td>-</td></tr>
<tr><td>VDD</td><td>-</td><td>Power pin (+)</td><td>-</td><td>-</td></tr>
<tr><td>VDDVPP</td><td>-</td><td>Power pin (+)</td><td>-</td><td>Power for programming</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>•8-bit input/output port
•Input for port 0 interrupt
•Input/output in nibble units
•Input for HOLD release</td><td>•Pull-up resistor :
Provided/Not provided
•Output form :
CMOS/N-channel open drain</td><td>-</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit
•Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16 Buzzer output
P17 Timer 1 output (PWM0 output)</td><td>Output form :
CMOS/N-channel open drain</td><td>Data line
D0 to D7</td></tr>
<tr><td>PORT2
P20 to P27</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit</td><td>Output form :
CMOS/N-channel open drain</td><td></td></tr>
<tr><td>PORT3
P30 to P37</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit
•15V withstand at N-channel open drain output</td><td>Output form :
CMOS/N-channel open drain</td><td>Address input
A7 to A0</td></tr>
<tr><td>PORT4
P40 to P47</td><td>I/O</td><td>•8-bit input/output port
•Input/output can be specified in a bit unit
•15V withstand at N-channel open drain output</td><td>Output form :
CMOS/N-channel open drain</td><td>Address input
A14 to A8 (*5)
P47 : TA (*4)</td></tr>
<tr><td>PORT5
P50 to P51</td><td>I/O</td><td>•2-bit input/output port
•Input/output can be specified in a bit unit
•15V withstand at N-channel open drain output</td><td>Output form :
CMOS/N-channel open drain</td><td></td></tr>
<tr><td>PORT7

P70

P71 to $\overline{P74}$</td><td>

I/O

I</td><td>•5-bit input port
•Other pin functions
P70 : INT0 input/HOLD release/N-channel Tr. output for watchdog timer
P71 : INT1 input/HOLD release input
P72 : INT2 input/timer 0 event input
P73 : INT3 input with noise filter/timer 0 event input
$\overline{P74}$: 32.768kHz crystal oscillation terminal XT1
•Interrupt received forms, the vector addresses
<table>
<tr><th></th><th>rising</th><th>falling</th><th>rising & falling</th><th>high level</th><th>low level</th><th>vector</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>03H</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td><td>0BH</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>13H</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td><td>1BH</td></tr>
</table></td><td>•Pull-up resistor :
Provided/Not provided
(P70,71,72,73)
• $\overline{P74}$ has no pull-up resistor.</td><td>Input of PROM control signals
DASEC (*1)
$\overline{OE}$ (*2)
$\overline{CE}$ (*3)</td></tr>
</table>

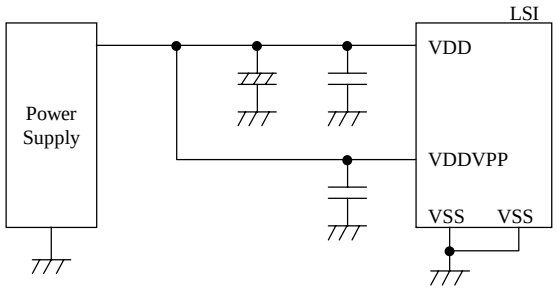
Continue.

Pin name	I/O	Function description	Option	PROM mode
PORT8 P80 to 87	I	•8-bit input port •Other function AD input port (AN7 to AN0)	-	-
$\overline{RES}$	I	Reset pin	-	-
TEST1	O	Test pin Should be left unconnected.	-	-
XT1/ $\overline{P74}$	I	•Input pin for 32.768kHz crystal oscillation •Other function : Input port $\overline{P74}$ In case of non use, connect to VDD.	-	-
XT2	O	•Output pin for 32.768kHz crystal oscillation •Other function In case of non use, should be left unconnected.	-	-
CF1	I	Input pin for the ceramic resonator oscillation	-	-
CF2	O	Output pin for the ceramic resonator oscillation	-	-

♦ All of port options can be specified in bit unit.

*1 Memory select input for data security
*2 Output enable input
*3 Chip enable input
*4 TA → PROM control signal input
*5 A14 → Address input

* Connect like the following figure to reduce noise into a VDD terminal.
Short-circuit the VDD terminal to the VDDVPP terminal.
Short-circuit the VSS terminal to the VSS terminal.



1. Absolute Maximum Ratings at VSS=0V and Ta=25°C

Parameter		Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Supply voltage		VDDMAX	VDD,VDDVPP	VDD=VDDVPP		-0.3		+7.0	V
Input voltage		VI(1)	•Ports 71,72,73, $\overline{74}$ •Port 8 • $\overline{\text{RES}}$			-0.3		VDD+0.3	
Input/Output voltage		VIO(1)	•Ports 0,1,2 •Ports 3,4,5 at CMOS output			-0.3		VDD+0.3	
		VIO(2)	Ports 3,4,5 at N-ch open drain output option			-0.3		15	
High level output current	Peak output current	IOPH(1)	•Ports 0,1,2,3,4,5	•CMOS output •At each pins		-4			mA
	Total output current	ΣIOAH(1)	Ports 0,1,2	The total of all pins		-25			
		ΣIOAH(2)	Ports 3,4,5	The total of all pins		-20			
Low level output current	Peak output current	IOPL(1)	Ports 0,1,2,3,4,5	At each pins				20	
		IOPL(2)	Port 70	At each pins				15	
	Total output current	ΣIOAL(1)	Ports 0,1,70	The total of all pins				40	
		ΣIOAL(2)	Port 2	The total of all pins				40	
		ΣIOAL(3)	Ports 3,4,5	The total of all pins				80	
Maximum power dissipation		Pdmax(1)	DIP64S	Ta=-30 to+70°C				720	mW
		Pdmax(2)	QFP64E	Ta=-30 to+70°C				420	
Operating temperature range		Topr				-30		70	°C
Storage temperature range		Tstg				-65		150	

Notes

- The QFP packages should be heat-soaked for 12 hours at 125°C immediately prior to mounting (This baking is called pre-baking).
- After pre-baking, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 24 hours.

2. Recommended Operating Range at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Operating Supply voltage	VDD(1)	VDD	0.98μs≤tCYC tCYC≤400μs		4.5		6.0	V
Hold voltage	VHD	VDD	RAMs and the registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	0.4VDD +0.9		VDD	
	VIH(2)	•Ports 1,2 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(3)	•Port 70 (Port input/interrupt) •Port 71 • $\overline{\text{RES}}$ (Schmitt)	Output N-channel Tr. OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 70 (Watchdog timer)	Output N-channel Tr. OFF	4.5 to 6.0	0.9VDD		VDD	
	VIH(5)	•Port $\overline{74}$ •Port 8	Output N-channel Tr. OFF	4.5 to 6.0	0.75VDD		VDD	
	VIH(6)	Ports 3,4,5 of CMOS output (Schmitt)	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(7)	Ports 3,4,5 of open drain output (Schmitt)	Output disable	4.5 to 6.0	0.75VDD		13.5	
Input low voltage	VIL(1)	Port 0 (Schmitt)	Output disable	4.5 to 6.0	VSS		0.2VDD	
	VIL(2)	•Ports 1,2,3,4,5 •Ports 72,73 (Schmitt)	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(3)	•Port 70 (Port input/interrupt) •Port 71 • $\overline{\text{RES}}$ (Schmitt)	N-channel Tr.OFF	4.5 to 6.0	VSS		0.25VDD	
	VIL(4)	Port 70 (Watchdog timer)	N-channel Tr.OFF	4.5 to 6.0	VSS		0.8VDD -1.0	
	VIL(5)	•Port $\overline{74}$ •Port 8	N-channel Tr.OFF	4.5 to 6.0	VSS		0.25VDD	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs
Oscillation frequency range (Note 1)	FmCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		6		MHz
	FmCF(2)	CF1, CF2	•1.5MHz (ceramic resonator oscillation) •Refer to figure 1	4.5 to 6.0		1.5		
	FmRC		RC oscillation	4.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz (crystal oscillation) •Refer to figure 2	4.5 to 6.0		32.768		kHz

Continue.

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Oscillation stabilizing time period (Note 1)	tmsCF(1)	CF1, CF2	•6MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				ms
	tmsCF(2)	CF1, CF2	•1.5MHz (ceramic resonator oscillation) •Refer to figure 3	4.5 to 6.0				
	tssXtal	XT1, XT2	•32.768kHz (crystal oscillation) ”Refer to figure 3	4.5 to 6.0				s

(Note 1) The oscillation constant is shown on table 1 and table 2.

3. Electrical Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Input high current	IIH(1)	Ports 3,4,5 at open drain output	•Output disable •VIN=13.5V (including off-leakage current of the output Tr.)	4.5 to 6.0			5	μA
	IIH(2)	•Port 0 without pull-up MOS Tr. •Ports 1,2,3,4,5	•Output disable •Pull-up MOS Tr. OFF. •VIN=VDD (including off-leakage current of the output Tr.)	4.5 to 6.0			1	
	IIH(3)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VDD	4.5 to 6.0			1	
	IIH(4)	$\overline{RES}$	VIN=VDD	4.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1,2,3,4,5 •Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leakage current of the output Tr.)	4.5 to 6.0	-1			
	IIL(2)	•Ports 70,71,72,73 without pull-up MOS Tr. •Port 8	VIN=VSS	4.5 to 6.0	-1			
	IIL(3)	$\overline{RES}$	VIN=VSS	4.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0,1,2,3,4,5 at CMOS output	IOH=-1.0mA	4.5 to 6.0	VDD-1			V
	VOH(2)		IOH=-0.1mA	4.5 to 6.0	VDD-0.5			
Output low voltage	VOL(1)	Ports 0,1,2,3,4,5	IOL=10mA	4.5 to 6.0			1.5	
	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)	Port 70	IOL=1mA	4.5 to 6.0			0.4	
	VOL(4)		IOL=0.5mA	4.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73	VOH=0.9VDD	4.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	VHIS	•Ports 0,1,2,3,4,5 •Ports 70,71,72,73 • $\overline{RES}$	Output disable	4.5 to 6.0		0.1VDD		V
Pin capacitance	CP	All pins	•f=1MHz •VIN=VSS for all unmeasured terminals. •Ta=25°C	4.5 to 6.0		10		pF

4. Serial Input/Output Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter			Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Serial clock	Input clock	Cycle	tCKCY(1)	SCK0,SCK1	Refer to figure 5	4.5 to 6.0	2			tCYC
		Low Level pulse width	tCKL(1)				1			
		High Level pulse width	tCKH(1)				1			
	Output clock	Cycle	tCKCY(2)	SCK0,SCK1	•Use pull-up resistor (1kΩ) in the open drain output. •Refer to figure 5	4.5 to 6.0	2			
		Low Level pulse width	tCKL(2)					1/2tCKCY		
		High Level pulse width	tCKH(2)					1/2tCKCY		
Serial input	Data set-up time		tICK	•SI0,SI1 •SB0,SB1	•Data set-up to SCK0,1 •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0	0.1			µs
	Data hold time		tCKI				0.1			
Serial output	Output delay time (External clock using for serial transfer clock)		tCKO(1)	•SO0,SO1 •SB0,SB1	•Use pull-up resistor (1kΩ) in the open drain output. •Data hold from SCK0,1 •Refer to figure 5	4.5 to 6.0			7/12 tCYC +0.2	
	Output delay time (Internal clock using for serial transfer clock)		tCKO(2)						1/3 tCYC +0.2	

5. Pulse Input Conditions at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
High/low level pulse width	tPIH(1) tPIL(1)	•INT0, INT1 •INT2/T0IN •INT3	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	1			tCYC
	tPIH(2) tPIL(2)	INT3 (The noise rejection clock selected to 1/1.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	2			
	tPIH(3) tPIL(3)	INT3 (The noise rejection clock selected to 1/16.)	•Interrupt acceptable •Timer0-countable	4.5 to 6.0	32			
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 6.0	200			μs

6. AD Converter Characteristics at Ta=-30°C to + 70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	VDD[V]	Ratings min.	Ratings typ.	Ratings max.	unit
Resolution	N			4.5 to 6.0		8		bit
Absolute precision (Note 2)	ET			4.5 to 6.0			±1.5	LSB
Conversion time	tCAD		AD conversion time = 16 × tCYC (ADCR2=0) (Note 3)	4.5 to 6.0	15.68 (tCYC= 0.98μs)		65.28 (tCYC= 4.08μs)	μs
			AD conversion time = 32 × tCYC (ADCR2=1) (Note 3)		31.36 (tCYC= 0.98μs)		130.56 (tCYC= 4.08μs)	
Analog input voltage range	VAIN	AN0 to AN7		4.5 to 6.0	VSS		VDD	V
Analog port input current	IAINH		VAIN=VDD	4.5 to 6.0			1	μA
	IAINL		VAIN=VSS	4.5 to 6.0	-1			

(Note 2) Absolute precision excepts the quantizing error (±1/2 LSB).
(Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				VDD[V]	min.	typ.	max.	
Current dissipation during basic operation (Note 4)	IDDOP(1)	VDD	•FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 to 6.0		13	26	mA
	IDDOP(2)		•FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 to 6.0		7	14	
	IDDOP(3)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		4	10	
	IDDOP(4)		•FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	4.5 to 6.0		4	8	

Continue.

Parameter	Symbol	Pins	Conditions		Ratings			unit
				VDD[V]	min.	typ.	max.	
Current dissipation in HALT mode (Note 4)	IDDHALT(1)		•HALT mode •FmCF=6MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 to 6.0		5	10	mA
	IDDHALT(2)		•HALT mode •FmCF=1.5MHz Ceramic resonator oscillation •FsXtal=32.768kHz crystal oscillation •System clock : CF oscillation •Internal RC oscillation stops	4.5 to 6.0		2.2	4.6	
	IDDHALT(3)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : RC oscillation	4.5 to 6.0		550	1000	μA
	IDDHALT(4)		•HALT mode FmCF=0Hz (The oscillation stops) •FsXtal=32.768kHz crystal oscillation •System clock : 32.768kHz •Internal RC oscillation stops	4.5 to 6.0		25	100	
Current dissipation in HOLD mode (Note 4)	IDDHOLD(1)	VDD	HOLD mode	4.5 to 6.0		0.05	30	
	IDDHOLD(2)			2.5 to 4.5		0.02	20	

(Note 4) The currents of the output transistors and the pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation recommended constant (main clock)

Oscillation type	Maker	Oscillator	C1	C2	Rf	Rd
12MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33pF	33pF	OPEN	560Ω
		CSA12.0MTZ	39pF	30pF	OPEN	0Ω
		CST12.0MTW	on chip		OPEN	560Ω
3MHz ceramic resonator oscillation	Murata	CSA3.00MG040	100pF	100pF	OPEN	1.5Ω
		CST3.00MGW040	on chip		OPEN	1.5Ω

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation recommended constant (sub clock)

Oscillation type	Maker	Oscillator	C3	C4
32.768kHz crystal oscillation	Kyocera	KF-38G-13P0200	18pF	18pF
	Seiko Epson	MC-306,C-002RX,32.768kHz	4pF	4pF

* Both C3 and C4 must use J rank (±5%) and CH characteristics.
(It is about the application which is not in need of high precision. Use K rank (±10%) and SL characteristics.)

(Notes) •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

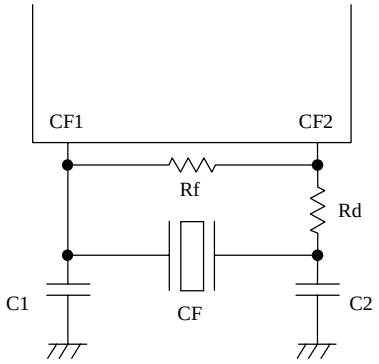


Figure 1 Main-clock circuit
Ceramic oscillation circuit

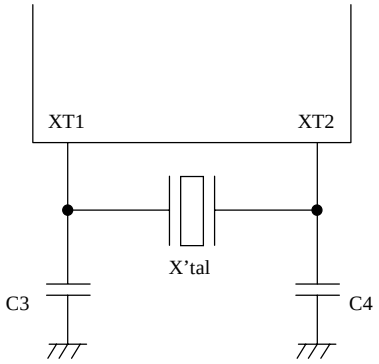


Figure 2 Sub-clock circuit
Crystal oscillation

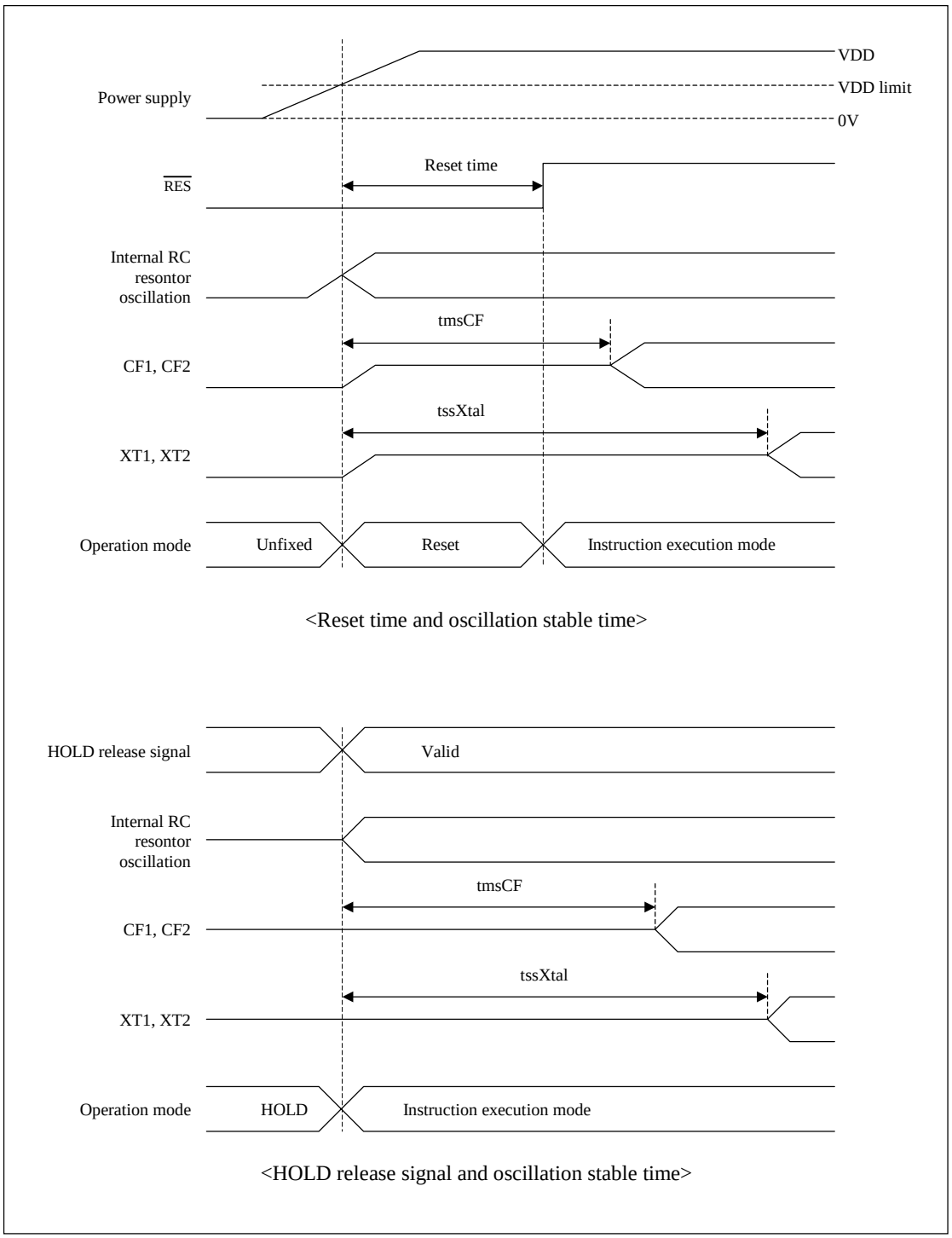
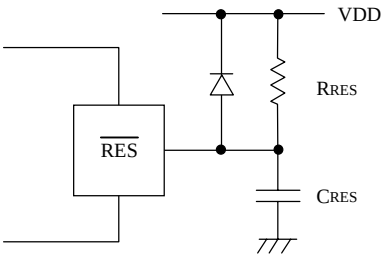
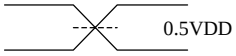


Figure 3 Oscillation stable time

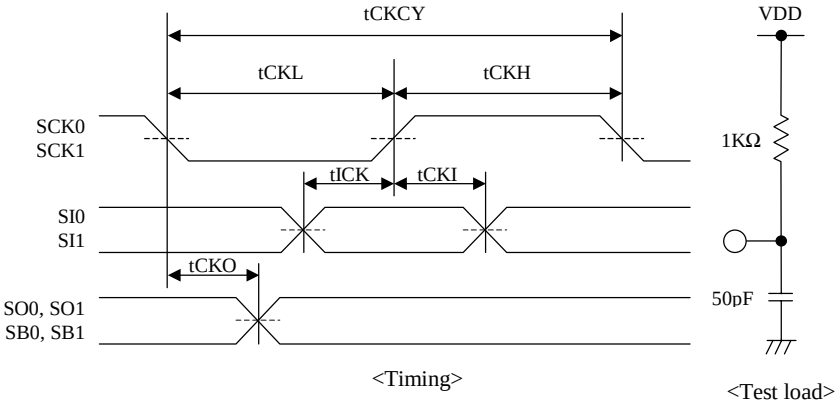


(Note) Fix the value of CRES, RRES that is sure to reset until 200μs, after Power supply has been over inferior limit of supply voltage.

Figure 4 Reset circuit



<AC timing point>



<Timing> <Test load>

Figure 5 Serial input / output test condition

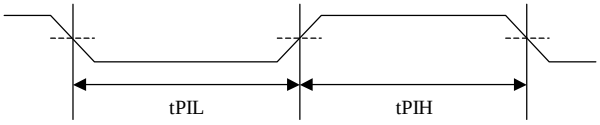


Figure 6 Pulse input timing condition

Notice for use

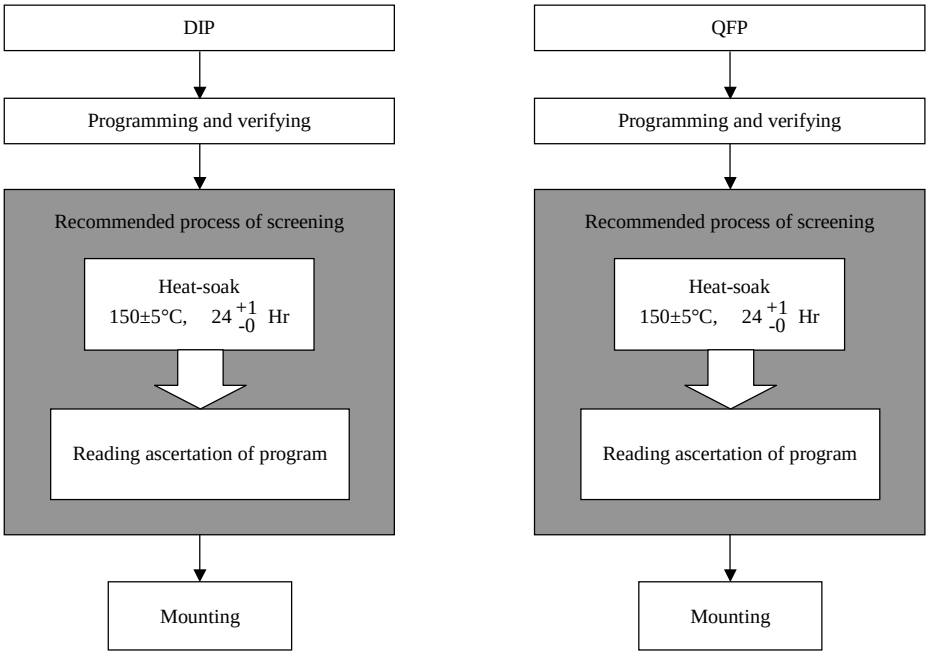
- The construction of the one-time programmable microcomputer with a blank built-in PROM makes it impossible for Sanyo to completely factory-test it before shipping. To probe reliability of the programmed devices, the screening procedure shown in the following figure should always be followed.

- It is not possible to perform a writing test on the blank PROM. 100% yield, therefore, cannot be guaranteed.

- Keeping the dry packing
  The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less.

- After opening the packing
  The preparation procedures shown in the following figure should always be followed prior to mounting the packages on the substrate. After opening the packing, a controlled environment must be maintained until soldering. The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less. Please solder within 96 hours.
  Unused devices should be kept in the dry atmosphere such as inside of desiccator or dry these up before assembling on the board.

a. Shipping with a blank PROM (Programming the data by yourself)



b. Shipping with a programmed PROM (Programming the data by Sanyo)