Ordering number: EN *5600

CMOS LSI

# LC86E4332

## 8-bit Single Chip Microcontroller

**Preliminary**

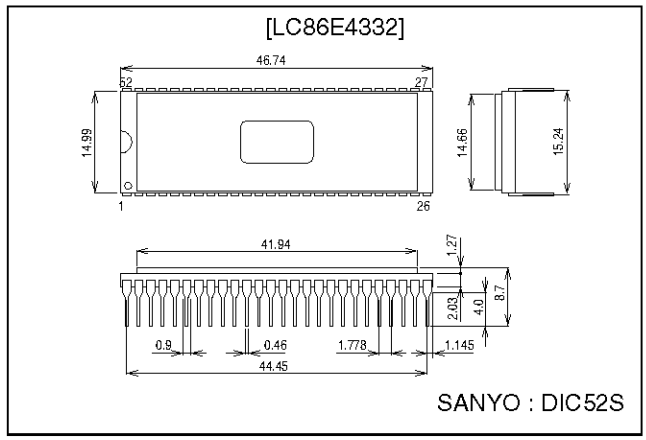
## Overview

The LC86E4332 is a CMOS 8-bit single chip microcontroller with UVEPROM for the LC864300 series.
This microcontroller has the function and the pin description of the LC864300 series mask ROM version, and the 32K-byte EPROM. The program data is rewritable. It is suitable for developing programs.

## Package Dimensions

unit : mm

### 3225-DIC52S




## Features

(1) Option switching by EPROM data
The option function of the LC864300 series can be specified by the EPROM data.
The functions of the trial pieces can be evaluated using the mass production board.
(2) Internal EPROM capacity : 32768 bytes (For program)
: 16384 × 12 bits (For character)
(3) Internal RAM capacity : 384 bytes

| Mask ROM version | PROM capacity | RAM capacity |
|---|---|---|
| LC864332 | 32512 bytes | 384 bytes |
| LC864328 | 28672 bytes | 384 bytes |
| LC864324 | 24576 bytes | 384 bytes |
| LC864320 | 20480 bytes | 384 bytes |
| LC864316 | 16384 bytes | 384 bytes |
| LC864312 | 12288 bytes | 384 bytes |

(4) Operating supply voltage : 4.5 V to 5.5 V
(5) Instruction cycle time : 0.99 µs to 40 µs
(6) Operating temperature : +10°C to +40°C
(7) The pin and the package compatible with the LC864300 series mask ROM version.
(8) Applicable mask ROM version : LC864332/LC864328/LC864324/LC864320/LC864316/LC864312
(9) Factory shipment : DIC52S

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## Notice for Use

When using, take notice of the followings.

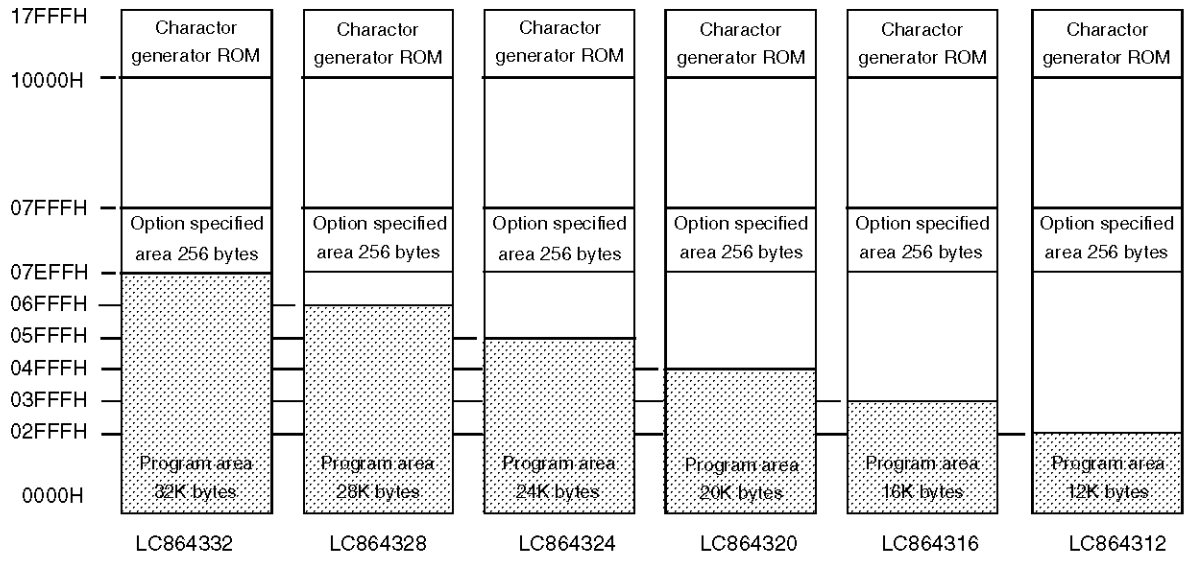
(1) Differences between the LC86E4332 and the LC864300 series

| Items | LC86E4332 | LC864332/28/24/20/16/12 |
|---|---|---|
| Operation after reset releasing | The option is specified by degrees until 3 ms after going to a 'H' level to the reset terminal. The program is executed from 00H of the program counter. | The program is executed from 00H of the program counter immediately after going to a 'H' level to the reset terminal. |
| Operating supply voltage range ($V_{DD}$) | 4.5 V to 5.5 V | 4.5 V to 5.5 V |
| Operating temperature range (Topr) | +10 to +40°C | –30 to +70°C |
| Power dissipation | Refer to 'electrical characteristics' on the semiconductor news. | |

Port configurations of LC86E4332 and LC864332/28/24/20/16/12 are identical during the reset operation.
The LC86E4332 uses the program memory area of 256 bytes from 7F00H to 7FFFH to select the options. All LC86E4332 series' options can be specified with this configuration.

(2) Option
The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

(3) ROM space
The LC86E4332 and LC864300 series use the program memory area of 256 bytes from 7F00H to 7FFFH to select the options. The program memory capacity of this series is, at most, 32512 bytes addressed on 0000H to 7EFFH.



## How to Use

(1) Create a programming data for LC86E4332
Programming data for EPROM of the LC86E4332 is required.
Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with the file converter program EVA2HEX.EXE. The HEX file is used as the programming data for the LC86E4332.

(2) How to program for the EPROM
The LC86E4332 can be programmed by the EPROM programmer with attachment W86EP4164D.
- Recommended EPROM programmer

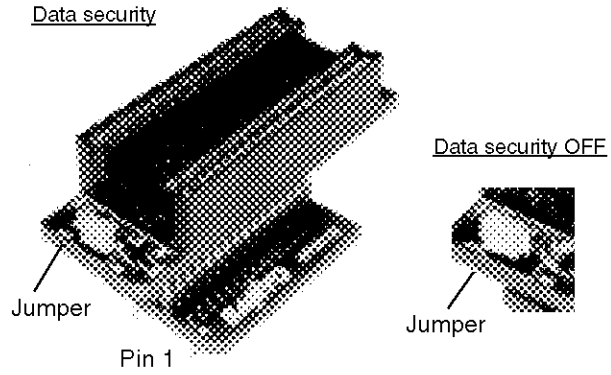
| Manufacturer | EPROM programmer |
|---|---|
| Advantest | R4945, R4944, R4943 |
| Andou | AF-9704 |
| AVAL | PKW-1100, PKW-3000 |
| Minato electronics | MODEL1890A |

- "27010 (Vpp = 12.5 V) Intel high speed programming" mode should be adopted.
- A jumper (DASEC) must be set to 'OFF' at programming.
- There are two ways to program the data of the hexa-decimal file described above into the EPROM of the LC86E4332.
  1. How to program the program and the character data individually.
     First, the hexa-decimal data of 00h to 07FFFh is programmed into the address 00h to 07FFFh of the EPROM.
     Next, write the hexa-decimal data for character addressed 10000h to 17FFFh into the address of 10000h to 17FFFh.
  2. How to program the program and the character data simultaneously.
     First, copy the program data addressed from 00h to 07FFFh into the addresses 8000h to 0FFFFh with an EPROM programmer.
     Next, write the data of 00h to 17FFFh into the EPROM of the LC86E4332.

An error will occur when the hexa-decimal data generated by the EVA2HEX program is programmed to the EPROM of the LC86E4332 directly.

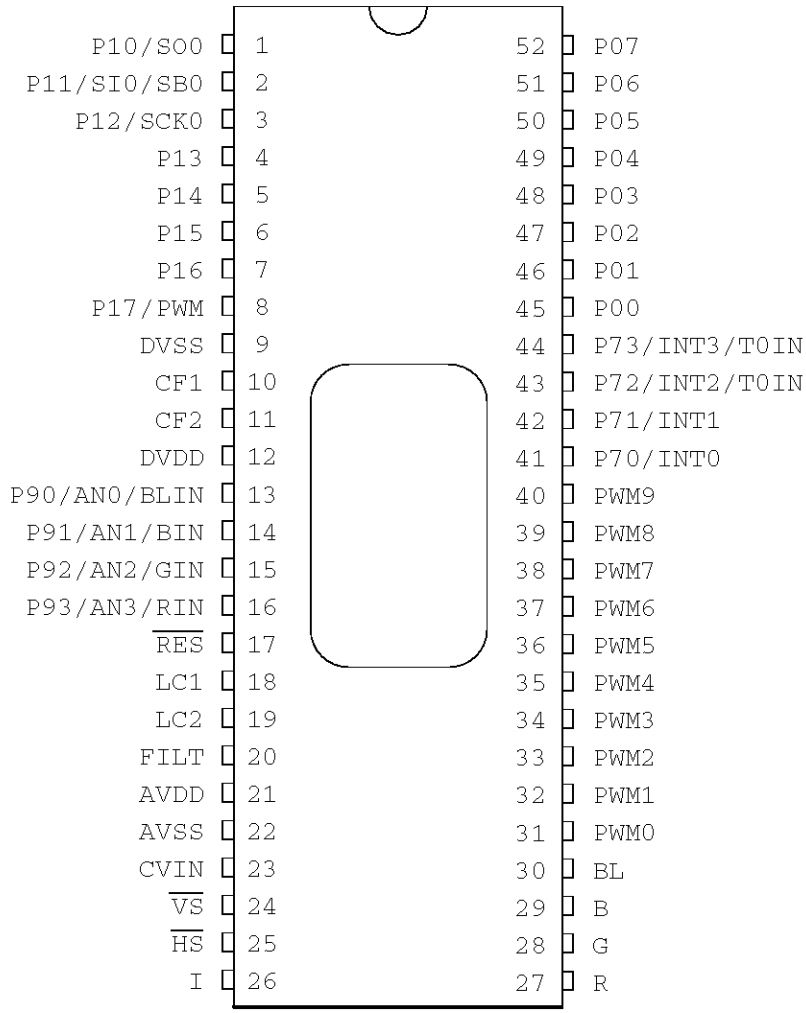
(3) How to use the data security function
"Data security" is the function to disable the EPROM data from being read out.
The following is the process in order to execute data security function.
1. Set the jumper of attachment 'ON'.
2. Program again. The EPROM programmer will display an error. The error means that the data security functions normally. It is not a trouble of the EPROM programmer or the LSI.

Notes
- Data security is not executed when the data of all address have 'FF' at sequence 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at procedure 2 above.
- Set the jumper to 'OFF' after executing the data security.



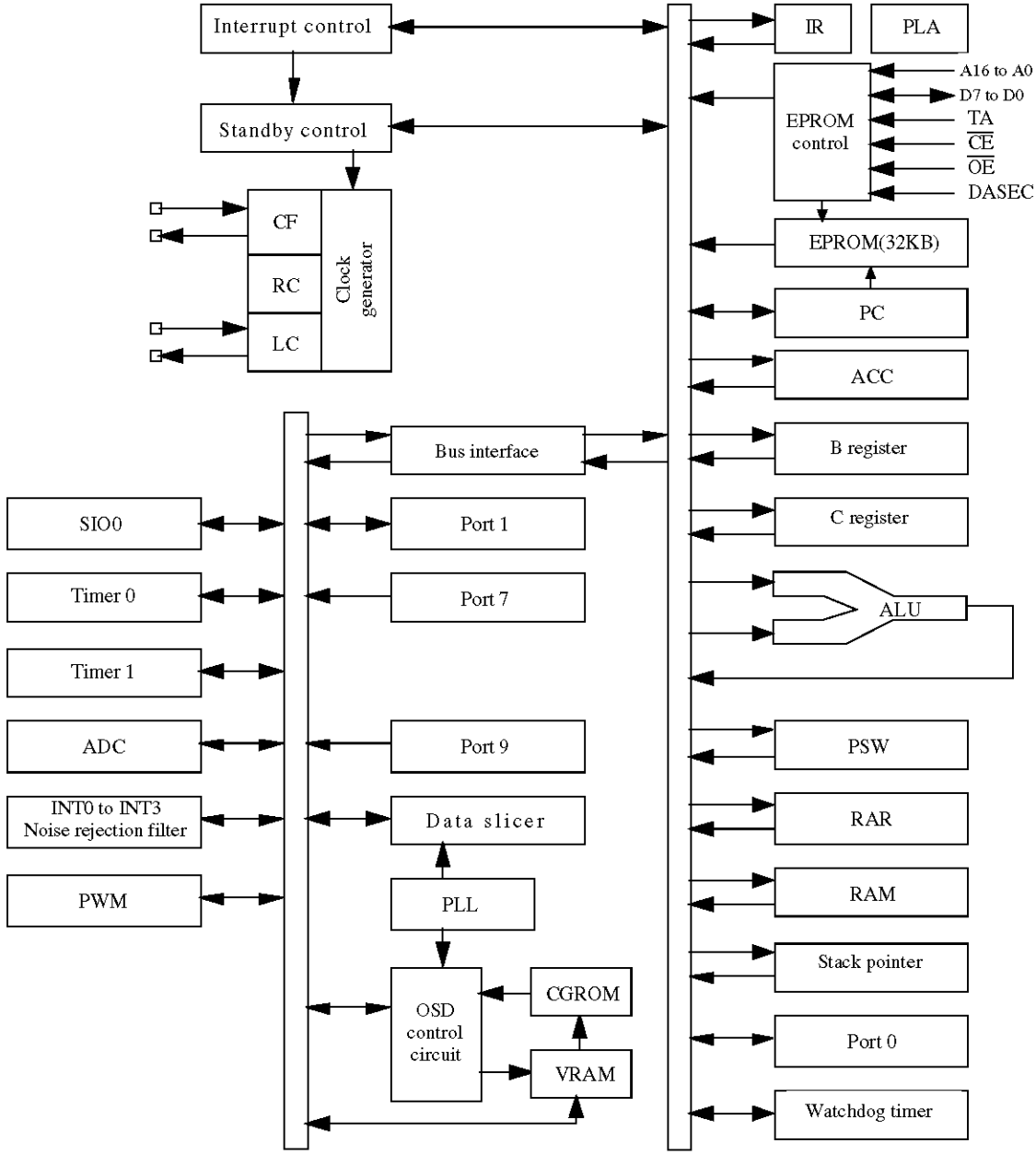

W86EP4164D

## Pin Assignment




**Top view**

## System Block Diagram



## Pin Description

- Port option can be specified by bit units.
- At port 0, 'Pull-up resistor provided' when specifying CMOS output.
  'Pull-up resistor not provided' when specifying N-ch open drain output.
- At port 1, 'Programmable pull-up resistor provided' when specifying either CMOS or N-ch open drain output.

Pin Description Table

| Pin name | Pin No. | I/O | Function description | Option | PROM mode |
|---|---|---|---|---|---|
| DVSS | 9 | — | Negative power supply for digital circuit | | |
| CF1 | 10 | I | Input terminal for ceramic resonator | | |
| CF2 | 11 | O | Output terminal for ceramic resonator | | |
| DVDD | 12 | — | Positive power supply for digital circuit | | |
| $\overline{\text{RES}}$ | 17 | I | Reset terminal | | |
| LC1 | 18 | I | LC oscillation circuit input terminal | | |
| LC2 | 19 | O | LC oscillation circuit output terminal | | |
| FILT | 20 | O | Filter terminal for PLL | | |
| AVDD | 21 | — | Positive power supply for analog circuit | | |
| AVSS | 22 | — | Negative power supply for analog circuit | | |
| CVIN | 23 | I | Video signal input terminal | | |
| $\overline{\text{VS}}$ | 24 | I | Vertical synchronization signal input terminal | | |
| $\overline{\text{HS}}$ | 25 | I | Horizontal synchronization signal input terminal | | |
| I | 26 | O | Image intensity output | | |
| R | 27 | O | Red (R) output terminal of RGB image output | | A4 (*1) |
| G | 28 | O | Green (G) output terminal of RGB image output | | A5 (*1) |
| B | 29 | O | Blue (B) output terminal of RGB image output | | A6 (*1) |
| BL | 30 | O | Fast blanking control signal<br>Switch TV image signal and caption/OSD image signal | | A7 (*1) |
| PWM0 to PWM9 | 31 to 40 | O | PWM0 to 9 output terminal<br>15 V withstand | | PWM0 to 8 :<br>A8 to A16 (*1)<br>PWM9 : "L" fixed |
| Port 0<br>P00 to P07 | 45 to 52 | I/O | 8-bit Input/output port<br>Input/output can be specified in nibble units<br>HOLD release input<br>Interrupt input | Pull-up resistor<br>Provided/not provided<br>(in bit units)<br>Output Format<br>CMOS/Nch-OD<br>(in bit units) | |
| Port 1<br>P10 to P17 | 1 to 8 | I/O | 8-bit Input/output port<br>Input/output can be specified in bit units.<br>Other function<br>P10 SIO0 data output<br>P11 SIO0 data input /bus input/output<br>P12 SIO0 clock input/output<br>P17 Timer 1 (PWM) output | Output Format<br>CMOS/Nch-OD<br>(in bit units) | D0 to D7 (*2) |

| Pin name | Pin No. | I/O | Function Description | Option | PROM mode |
|---|---|---|---|---|---|
| Port 7<br>P70<br>P71 to P73 | 41<br>42 to 44 | I/O<br>I | 4-bit input port<br>Other function<br>P70: INT0 input/HOLD release input/ Nch-transistor output for watchdog timer<br>P71: INT1 input/HOLD release input<br>P72: INT2 input/timer 0 event input<br>P73: INT3 input (noise rejection filter attached input/timer 0 event input | Pull-up resistor provided/ not provided (in bit units) | P70 : VPP (*3)<br>P71 : DASEC (*4)<br>P72 : $\overline{OE}$ (*5)<br>P73 : $\overline{CE}$ (*6) |
| Port 9<br>P90 to P93 | 13 to 16 | I | 4-bit input port<br>Other functions<br>AD converter input port (4 lines) | External RGB input | A0 to A3 (*3) |

Interrupt receiver format vector address

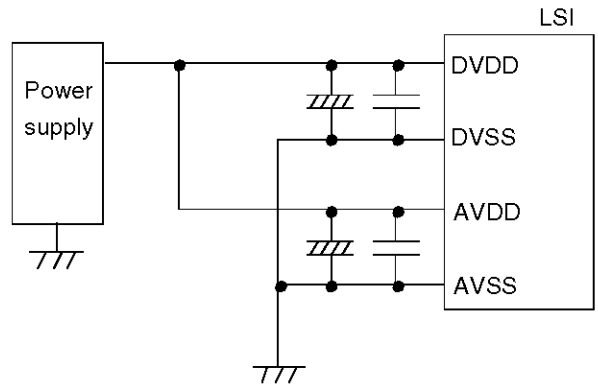
| | Rise | Fall | Rise/Fall | H level | L level | Vector |
|---|---|---|---|---|---|---|
| INT0 | enable | enable | disable | enable | enable | 03H |
| INT1 | enable | enable | disable | enable | enable | 0BH |
| INT2 | enable | enable | enable | disable | disable | 13H |
| INT3 | enable | enable | enable | disable | disable | 1BH |

*1 An → Address input
*2 Data I/O
*3 Power for programming
*4 Memory select input/output for data security
*5 Output Enable input
*6 Chip Enable input

- Port status in reset

| Terminal | I/O | Pull-up resistor state at selecting pull-up option |
|---|---|---|
| Port 0 | Input | Pull-up resistor OFF, ON after reset release |
| Port 1 | Input | Programmable pull-up resistor OFF |
| Port 7 | Input | Fixed pull-up resistor provided |

* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the mutual noise influence.



# Specifications

## 1. Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | $V_{DD}$ [V] | min | typ | max | |
| Supply voltage | | $V_{DD}$ max | DVDD, AVDD | DVDD=AVDD | | –0.3 | | +7.0 | V |
| Input voltage | | $V_I$(1) | • P71, 72, 73<br>• Port 9<br>• $\overline{RES}$,$\overline{HS}$,$\overline{VS}$,CVIN | | | –0.3 | | $V_{DD}$+0.3 | |
| Output voltage | | $V_O$(1) | R, G, B, BL, I, FILT | | | –0.3 | | $V_{DD}$+0.3 | |
| | | $V_O$(2) | PWM0 to PWM9 | | | –0.3 | | +15 | |
| Input/output voltage | | $V_{IO}$ | Ports 0, 1, P70 | | | –0.3 | | $V_{DD}$+0.3 | |
| High-level output current | Peak output current | $I_{OPH}$(1) | Ports 0, 1 | • Pull-up MOS transistor output<br>• At each pin | | –2 | | | mA |
| | | $I_{OPH}$(2) | Ports 0, 1 | • CMOS output<br>• At each pin | | –4 | | | |
| | | $I_{OPH}$(3) | R, G, B, BL, I | • CMOS output<br>• At each pin | | –5 | | | |
| | Total output current | $\Sigma I_{OAH}$(1) | Port 1 | The total of all pins | | –10 | | | |
| | | $\Sigma I_{OAH}$(2) | Port 0 | The total of all pins | | –10 | | | |
| | | $\Sigma I_{OAH}$(3) | R, G, B, BL, I | The total of all pins | | –15 | | | |
| Low-level output current | Peak output current | $I_{OPL}$(1) | Ports 0, 1 | At each pin | | | | 20 | |
| | | $I_{OPL}$(2) | P70 | At each pin | | | | 30 | |
| | | $I_{OPL}$(3) | • R, G, B, BL, I<br>• PWM0 to PWM9 | At each pin | | | | 5 | |
| | Total output currrent | $\Sigma I_{OAL}$(1) | Port 0 | The total of all pins | | | | 40 | |
| | | $\Sigma I_{OAL}$(2) | Port 1, P70 | The total of all pins | | | | 40 | |
| | | $\Sigma I_{OAL}$(3) | R, G, B, BL, I | The total of all pins | | | | 15 | |
| | | $\Sigma I_{OAL}$(4) | PWM0 to PWM9 | The total of all pins | | | | 30 | |
| Maximum power dissipation | | Pd max | DIC52S | Ta = +10 to +40°C | | | | 430 | mW |
| Operating temperature range | | Topr | | | | +10 | | +40 | °C |
| Storage temperature range | | Tstg | | | | –55 | | +125 | |

*DVSS and AVSS must be supplied the same voltage, $V_{SS}$. $V_{SS}$ = DVSS = AVSS
DVDD and AVDD must be supplied the same voltage, $V_{DD}$. $V_{DD}$ = DVDD = AVDD

## 2. Recommended Operating Range at Ta = +10°C to +40°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | | |
| Operating supply voltage range | $V_{DD}$ | DVDD, AVDD | 0.97 µs ≤ tCYC tCYC ≤ 1.02 µs | | 4.5 | | 5.5 | V | |
| Hold voltage | $V_{HD}$ | DVDD, AVDD | RAMs and the registers hold data at HOLD mode. | | 2.0 | | 5.5 | | |
| Input high-level voltage | $V_{IH}$(1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | 0.6$V_{DD}$ | | $V_{DD}$ | | |
| | $V_{IH}$(2) | • Port 1 (Schmitt)<br>• P72, 73<br>• $\overline{HS}$, $\overline{VS}$ | Output disable | 4.5 to 5.5 | 0.75$V_{DD}$ | | $V_{DD}$ | | |
| | $V_{IH}$(3) | • P70 port input / interrupt<br>• P71<br>• $\overline{RES}$ (Schmitt) | Output N-channel transistor OFF | 4.5 to 5.5 | 0.75$V_{DD}$ | | $V_{DD}$ | | |
| | $V_{IH}$(4) | • P70 Watchdog timer input | Output N-channel transistor OFF | 4.5 to 5.5 | $V_{DD}$–0.5 | | $V_{DD}$ | | |
| | $V_{IH}$(5) | Port 9 port input | | 4.5 to 5.5 | 0.7$V_{DD}$ | | $V_{DD}$ | | |
| Input low-level voltage | $V_{IL}$(1) | Port 0 (Schmitt) | Output disable | 4.5 to 5.5 | $V_{SS}$ | | 0.2$V_{DD}$ | | |
| | $V_{IL}$(2) | • Port 1 (Schmitt)<br>• P72, 73<br>• $\overline{HS}$, $\overline{VS}$<br>• Port 9 | Output disable | 4.5 to 5.5 | $V_{SS}$ | | 0.25$V_{DD}$ | | |
| | $V_{IL}$(3) | • P70 port input / interrupt<br>• P71<br>• $\overline{RES}$ (Schmitt) | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | 0.25$V_{DD}$ | | |
| | $V_{IL}$(4) | • P70 Watchdog timer input | N-channel transistor OFF | 4.5 to 5.5 | $V_{SS}$ | | 0.6$V_{DD}$ | | |
| | $V_{IL}$(5) | Port 9 port input | | 4.5 to 5.5 | $V_{SS}$ | | 0.3$V_{DD}$ | | |
| CVIN input amplitude | $V_{CVIN}$ | CVIN | | 5.0 | 1Vp-p –3dB | 1Vp-p | 1Vp-p +3dB | Vp-p | * |
| Operation cycle time | tCYC(1) | | OSD function | 4.5 to 5.5 | 0.97 | 1 | 1.02 | µs | |
| | tCYC(2) | | Except OSD function | 4.5 to 5.5 | 0.97 | | 40 | | |

* Vp-p : Peak-to-peak voltage

| Parameter | Symbol | Pins | Conditions | | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Oscillation frequency range (Note 1) | FmCF(1) | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 1. | 4.5 to 5.5 | 11.76 | 12 | 12.24 | MHz |
| | FmCF(2) | | 12.08 MHz (ceramic resonator oscillation) Refer to Figure 1. | | 11.84 | 12.08 | 12.32 | |
| | FmLC | LC1, LC2 | 14.11 MHz (LC oscillation) Refer to Figure 2. | 4.5 to 5.5 | | 14.11 | | |
| | FmRC | | RC oscillation | 4.5 to 5.5 | 0.4 | 0.8 | 3.0 | |
| Oscillation stable time period (Note 2) | tmsCF(1) | CF1, CF2 | 12 MHz (ceramic resonator oscillation) Refer to Figure 3. | 4.5 to 5.5 | | 0.02 | 0.2 | ms |
| | tmsCF(2) | | 12.08 MHz (ceramic resonator oscillation) Refer to Figure 3. | | | 0.02 | 0.2 | |

(Note 1) Refer to Table 1 and Table 2 for oscillation constant.
(Note 2) The oscillation stable time period refers to the time it takes to oscillate stably after the following conditions.
1. Applying the first supply voltage.
2. Release of the HOLD mode.
3. Release of the stopping of the main-clock oscillation.
Refer to Figure 3 for details.

## 3. Electrical Characteristics at Ta = +10°C to +40°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | $V_{DD}$ [V] | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input high-level current | $I_{IH}$(1) | • Port 1<br>• Port 0 without pull-up MOS transistor | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN}$ = $V_{DD}$<br>(including the off-leak current of the output transistor) | 4.5 to 5.5 | | | 1 | µA |
| | $I_{IH}$(2) | • Port 7 without pull-up MOS transistor<br>• Port 9<br>• $\overline{RES}$<br>• $\overline{HS}$,$\overline{VS}$ | $V_{IN}$ = $V_{DD}$ | 4.5 to 5.5 | | | 1 | |
| Input low-level current | $I_{IL}$(1) | • Port 1<br>• Port 0 without pull-up MOS transistor | • Output disable<br>• Pull-up MOS transistor OFF<br>• $V_{IN}$ = $V_{SS}$<br>(including the off-leak current of the output transistor) | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}$(2) | • Port 7 without pull-up MOS transistor<br>• Port 9 | $V_{IN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| | $I_{IL}$(3) | • $\overline{RES}$<br>• $\overline{HS}$,$\overline{VS}$ | $V_{IN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |
| Output high-level voltage | $V_{OH}$(1) | CMOS output of ports 0, 1 | $I_{OH}$ = –1.0 mA | 4.5 to 5.5 | $V_{DD}$–1 | | | V |
| | $V_{OH}$(2) | R, G, B, BL, I | $I_{OH}$ = –0.1 mA | 4.5 to 5.5 | $V_{DD}$–0.5 | | | |
| Output low-level voltage | $V_{OL}$(1) | Ports 0, 1 | $I_{OL}$ = 10 mA | 4.5 to 5.5 | | | 1.5 | |
| | $V_{OL}$(2) | Ports 0, 1 | • $I_{OL}$ = 1.6 mA<br>• The total current of the ports 0, 1 is 40 mA or less. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}$(3) | • R, G, B, BL, I | • $I_{OL}$ = 3.0 mA<br>• PWM0 to PWM9<br>• The current of any unmeasured pin is 3 mA or less. | 4.5 to 5.5 | | | 0.4 | |
| | $V_{OL}$(4) | P70 | $I_{OL}$ = 1 mA | 4.5 to 5.5 | | | 0.4 | |
| Pull-up MOS transistor resistance | Rpu | • Ports 0, 1<br>• Port 7 | $V_{OH}$ = 0.9$V_{DD}$ | 4.5 to 5.5 | 13 | 38 | 80 | kΩ |
| Output off-leakage current | $I_{OFF}$ | PWM0 to PWM9 | $V_{OUT}$ = 13.5 V | 4.5 to 5.5 | | | 5 | µA |
| Hysteresis voltage | $V_{HIS}$ | • Ports 0, 1<br>• Port 7<br>• $\overline{RES}$<br>• $\overline{HS}$,$\overline{VS}$ | Output disable | 4.5 to 5.5 | | 0.1$V_{DD}$ | | V |

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Input clamp voltage | $V_{CLMP}$ | CVIN | | 5.0 | 2.3 | 2.5 | 2.7 | V |
| Pin capacitance | CP | All pins | • f = 1 MHz<br>• Unmeasured terminals for the input are set to $V_{SS}$ level.<br>• Ta = 25°C | 4.5 to 5.5 | | 10 | | pF |

## 4. Serial Input/Output Characteristics at Ta = +10°C to +40°C, $V_{SS}$ = 0 V

| Parameter | | | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | $V_{DD}$ [V] | min | typ | max | |
| Serial clock | Input clock | Cycle | tCKCY(1) | • SCK0<br>• SCLK0 | Refer to Figure 5. | 4.5 to 5.5 | 2 | | | tCYC |
| | | Low-level pulse width | tCKL(1) | | | | 1 | | | |
| | | High-level pulse width | tCKH(1) | | | | 1 | | | |
| | Output clock | Cycle | tCKCY(2) | • SCK0<br>• SCLK0 | • Use a pull-up resistor (1 kΩ) when open drain output<br>• Refer to Figure 5. | 4.5 to 5.5 | 2 | | | |
| | | Low-level pulse width | tCKL(2) | | | | | 1/2tCKCY | | |
| | | High-level pulse width | tCKH(2) | | | | | 1/2tCKCY | | |
| Serial input | Data set-up time | | tICK | • SI0 | • Data set-up to SCK0 rising<br>• Data hold from SCK0 rising<br>• Refer to Figure 5. | 4.5 to 5.5 | 0.1 | | | µs |
| | Data hold time | | tCKI | | | 4.5 to 5.5 | 0.1 | | | |
| Serial output | Output delay time (External serial clock) | | tCKO(1) | • SO0 | • Use a pull-up resistor (1 kΩ) when open drain output<br>• Data set-up to SCK0 falling<br>• Data hold from SCK0 falling<br>• Refer to Figure 5. | 4.5 to 5.5 | | | 7/12tCYC +0.2 | µs |
| | Output delay time (Internal serial clock) | | tCKO(2) | | | 4.5 to 5.5 | | | 1/3tCYC +0.2 | |

## 5. Pulse Input Conditions at Ta = +10°C to +40°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | • INT0, INT1<br>• INT2/T0IN | • Interrupt acceptable<br>• Timer0-countable | 4.5 to 5.5 | 1 | | | tCYC |
| | tPIH(2)<br>tPIL(2) | INT3/T0IN<br>(The noise rejection clock is set to 1/1) | • Interrupt acceptable<br>• Timer0-countable | 4.5 to 5.5 | 2 | | | |
| | tPIH(3)<br>tPIL(3) | INT3/T0IN<br>(The noise rejection clock is set to 1/16) | • Interrupt acceptable<br>• Timer0-countable | 4.5 to 5.5 | 32 | | | |
| | tPIL(4) | $\overline{RES}$ | Reset acceptable | 4.5 to 5.5 | 200 | | | µs |
| | tPIH(5)<br>tPIL(5) | $\overline{HS}$, $\overline{VS}$ | Display position controllable<br>Each active edge of $\overline{HS}$, $\overline{VS}$ must be more than 1tCYC.<br>Refer to Figure 7. | 4.5 to 5.5 | 10 | | | tCYC |
| Rising/falling time | tTHL<br>tTLH | $\overline{HS}$ | Refer to Figure 7. | 4.5 to 5.5 | | | 500 | ns |
| Horizontal pull-in range | FH | $\overline{HS}$ | The monitor point in Figure 10 is 1/2 $V_{DD}$. | 4.5 to 5.5 | 15.23 | 15.73 | 16.23 | kHz |

## 6. A/D Converter Characteristics at Ta = +10°C to +40°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Resolution | N | | | 4.5 to 5.5 | | 5 | | bit |
| Absolute precision | ET | | (Note 3) | 4.5 to 5.5 | | ±1/4 | ±3/4 | LSB |
| Conversion time | tCAD | From Vref selection to when the result is output | 1 bit conversion time = 2tCYC | 4.5 to 5.5 | | 2 | | µs |
| Reference current | $I_{REF}$ | | (Regulate the ladder resistor) | 4.5 to 5.5 | | 1.0 | 2.0 | mA |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN3 | | 4.5 to 5.5 | $V_{SS}$ | | $V_{DD}$ | V |
| Analog port input current | $I_{AINH}$ | | $V_{AIN}$ = $V_{DD}$ | 4.5 to 5.5 | | | 1 | µA |
| | $I_{AINL}$ | | $V_{AIN}$ = $V_{SS}$ | 4.5 to 5.5 | –1 | | | |

(Note 3) Absolute precision excepts quantizing error (±1/2 LSB).

## 7. Current Drain Characteristics at Ta = +10°C to +40°C , $V_{SS}$ = 0 V

| Parameter | Symbol | Pins | Conditions | Ratings | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{DD}$ [V] | min | typ | max | |
| Current drain during basic operation (Note 4) | $I_{DDOP}$(1) | DVDD, AVDD | • FmCF = 12 MHz or FmCF = 12.08 MHz when ceramic resonator oscillation<br>• FmLC = 14.11 MHz when LC oscillation<br>• System clock : CF oscillation<br>• Internal RC oscillation stops | 4.5 to 5.5 | | 25 | 38 | mA |
| Current drain in HALT mode (Note 4) | $I_{DDHALT}$(1) | DVDD, AVDD | • HALT mode<br>• FmCF = 12 MHz or FmCF = 12.08 MHz when ceramic resonator oscillation<br>• FmLC = 0 Hz (when oscillation stops)<br>• System clock : CF oscillation<br>• Internal RC oscillation stops. | 4.5 to 5.5 | | 5 | 10 | mA |
| | $I_{DDHALT}$(2) | DVDD, AVDD | • HALT mode<br>• FmCF = 0 MHz (when oscillation stops)<br>• FmLC = 0 Hz (when oscillation stops)<br>• System clock : Internal RC | 4.5 to 5.5 | | 600 | 1200 | µA |
| Current drain in HOLD mode (Note 4) | $I_{DDHOLD}$ | DVDD, AVDD | • HOLD mode<br>• All oscillation stops. | 4.5 to 5.5 | | 0.05 | 20 | µA |

(Note 4) The currents to the output transistors and the pull-up MOS transistors are ignored.

| Oscillation types | Manufacturer | Oscillator | C1 | C2 |
|---|---|---|---|---|
| 12 MHz ceramic resonator oscillation | Murata | CSA12.0MTZ | 33 pF | 33 pF |
| | | CST12.0MTW | on chip | |
| | Kyocera | KBR-12.0M | 33 pF | 33 pF |
| 12.08 MHz ceramic resonator oscillation | Murata | CSA12.0MTZ021 | 33 pF | 33 pF |
| | | CST12.0MTW021 | on chip | |
| | Kyocera | KBR-12.08M | 33 pF | 33 pF |

* Both C1 and C2 must use K rank (±10%) and SL characteristics.

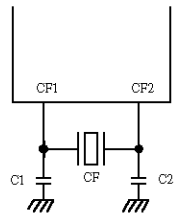
**Table 1. Ceramic Resonator Oscillation Guaranteed Constant (main-clock)**

| Oscillation types | L | C3 | C4 |
|---|---|---|---|
| 14.11 MHz LC oscillation | 4.7 µH | 33 pF | 45 pF (Trimmer) |
| | 4.7 µH ±10% (Variable) | 33 pF | 33 pF |

* See Figures 11 and 12.

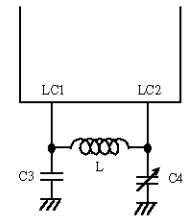
**Table 2. LC oscillation Guaranteed Constant (OSD clock)**

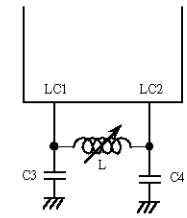
(Notes)
- Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
- If you use other oscillators herein, we provide no guarantee for the characteristics.
- Adjust the voltage of monitor point in Figure 10 to 1/2 $V_{DD}$±10% by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.




Main clock

**Figure 1 Ceramic Resonator Oscillation**




OSD clock

**Figure 2 LC Resonator Oscillation**

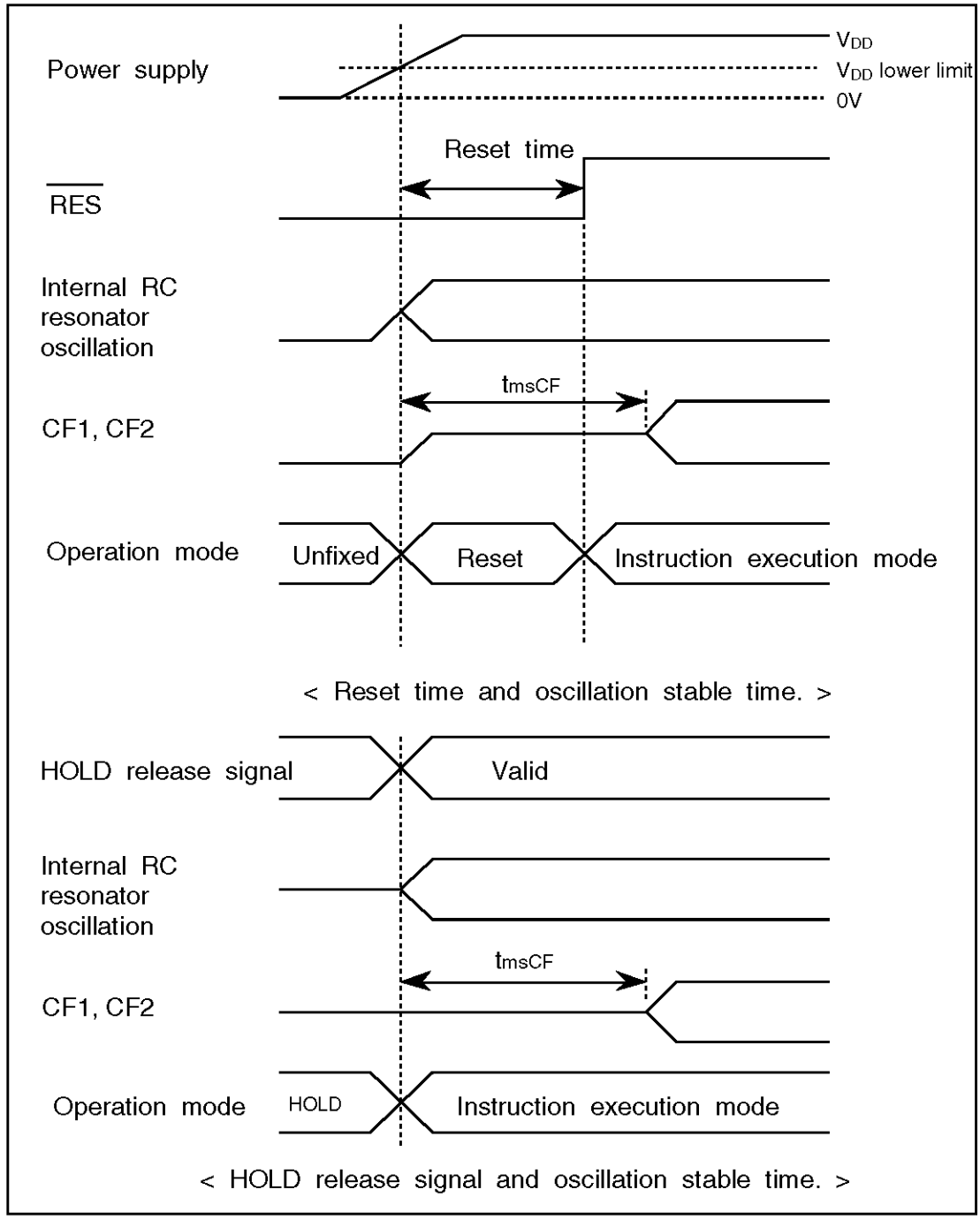
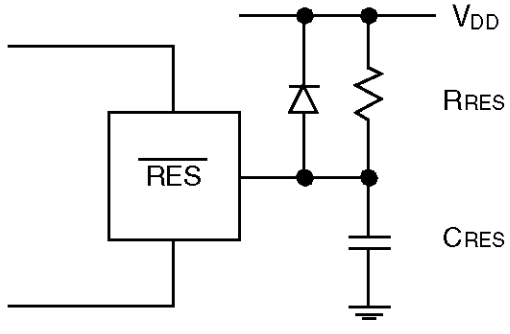



**Figure 3 Oscillation Stable Time**




(Note) Set the values of $C_{RES}$, $R_{RES}$ so that the reset time is 200 µs or longer.

**Figure 4 Reset Circuit**

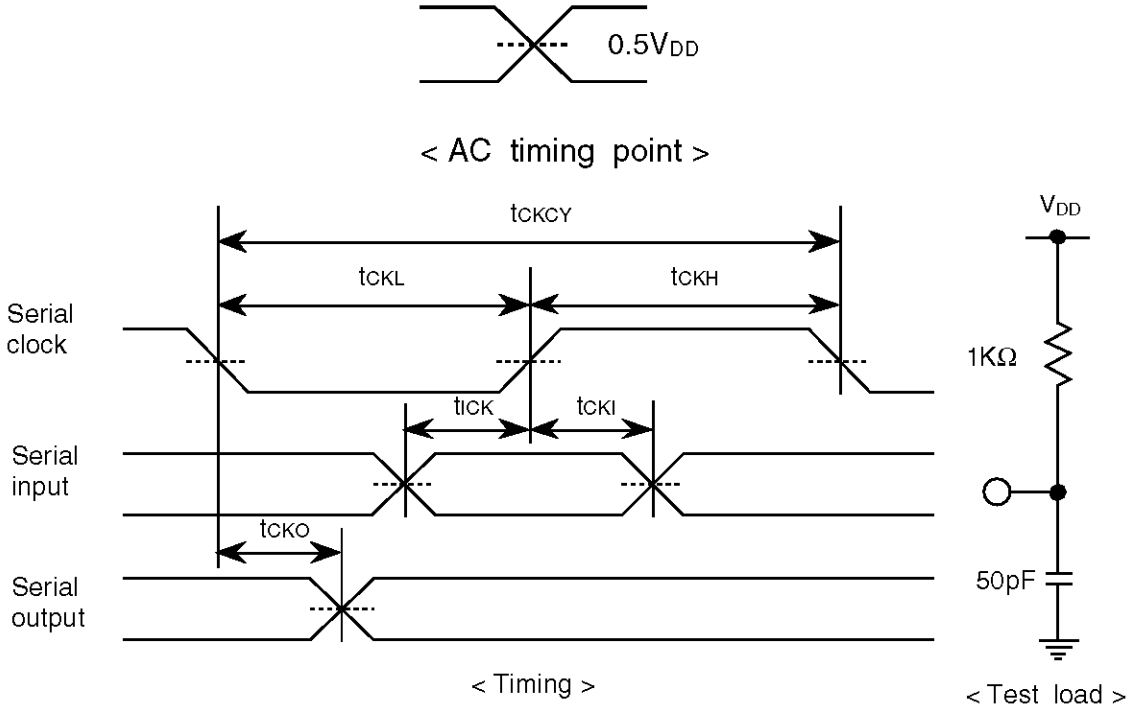



**Figure 5 Serial Input/output Test Condition**

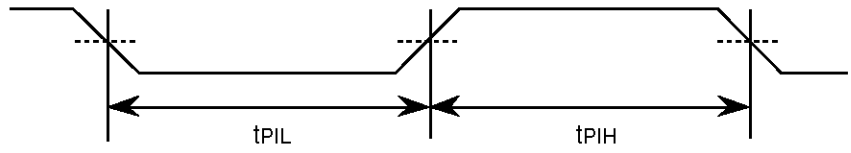
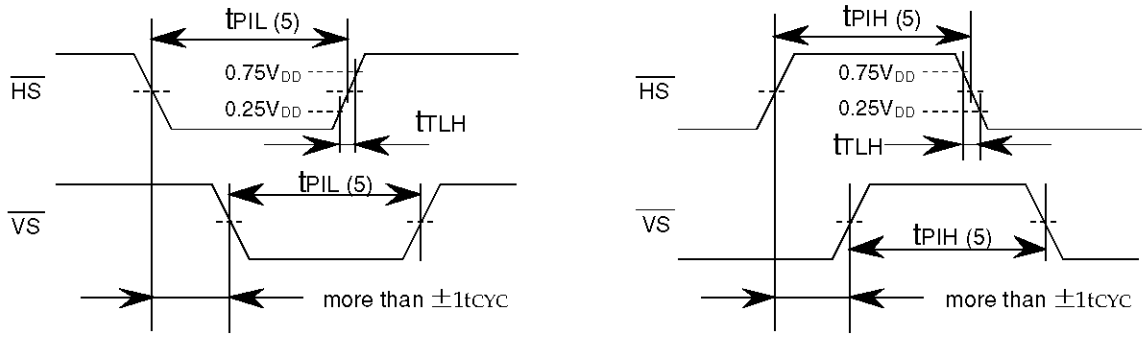



**Figure 6 Pulse Input Timing Condition - 1**




(a) In case of active low (b) In case of active high

**Figure 7 Pulse Input Timing Condition - 2**

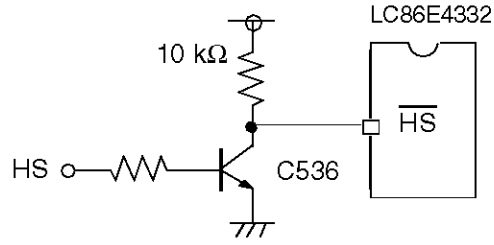



**Figure 8 Recommended Interface Circuit**

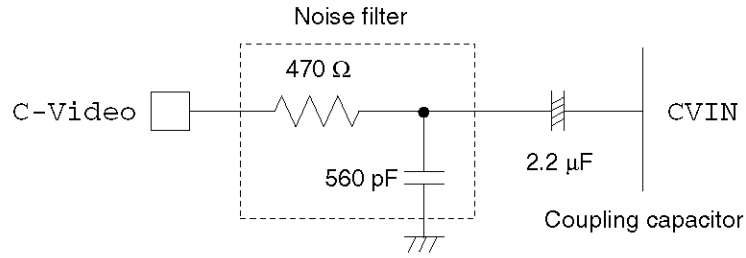



**Figure 9 CVIN Recommended Circuit**

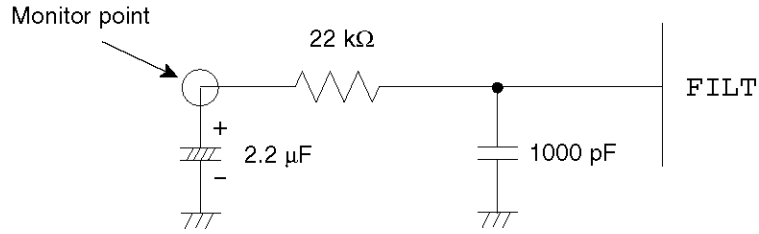



**Figure 10 FILT Recommended Circuit**

(Note) • Place the parts connected FILT terminal as close to the FILT as possible with the shortest pattern length on the board.

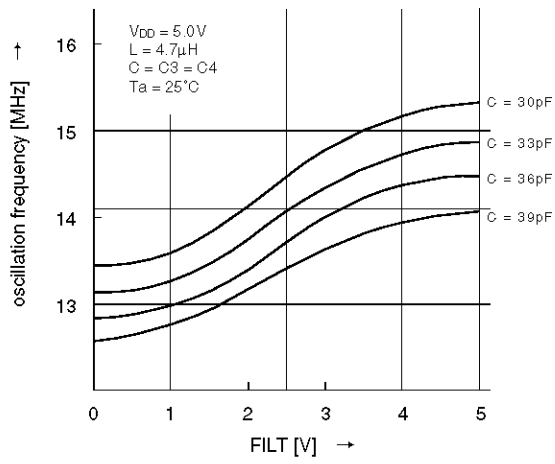



**Figure 11 FILT-LC Oscillation Frequency(1)**

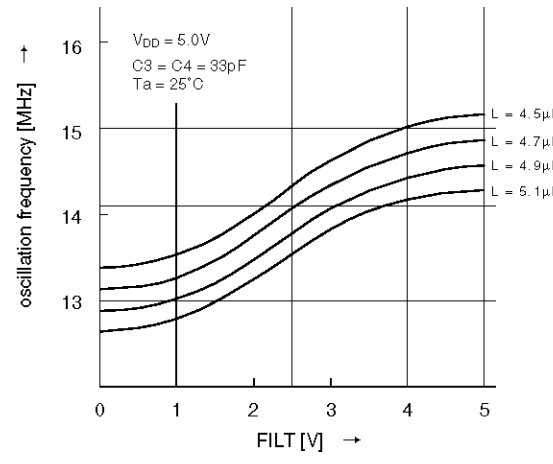



**Figure 12 FILT-LC Oscillation Frequency(2)**