



LC72133M, 72133V

PLL Frequency Synthesizer for Electronic Tuning



Overview

The LC72133M and LC72133V are a phase-locked loop frequency synthesizer LSI circuits for use in radio tuners. It supports low-voltage (2.7 to 3.6 V) operation and can implement high-performance AM/FM tuners easily.

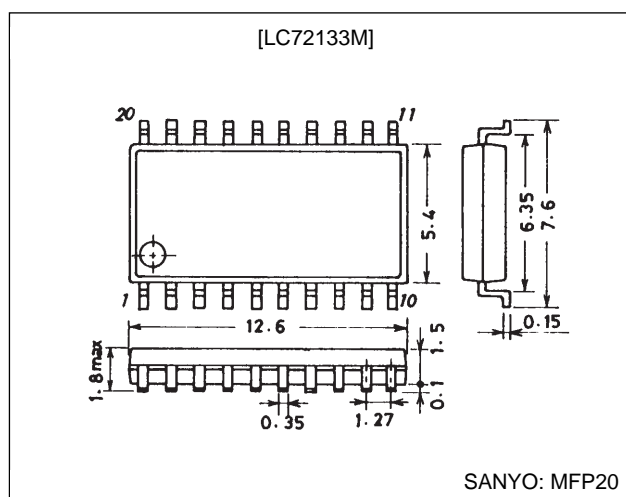
Functions

- High speed programmable dividers
 - FMIN: 10 to 120 MHzpulse swallower (built-in divide-by-two prescaler), $V_{DD} \geq 2.7$ V
 - 10 to 130 MHzpulse swallower (built-in divide-by-two prescaler), $V_{DD} \geq 3.0$ V
 - AMIN: 2 to 40 MHzpulse swallower
 - 0.5 to 10 MHzdirect division
- IF counter
 - IFIN: 0.4 to 12 MHzAM/FM IF counter
- Reference frequencies
 - Twelve selectable frequencies (4.5 or 7.2 MHz crystal)
 - 1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50 and 100 kHz
- Phase comparator
 - Dead zone control
 - Unlock detection circuit
 - Deadlock clear circuit
- Built-in MOS transistor for forming an active low-pass filter
- I/O ports
 - Dedicated output ports: 4
 - Input or output ports: 2
 - Support clock time base output
- Serial data I/O
 - Support CCB format communication with the system controller.
- Operating ranges
 - Supply voltage.....2.7 to 3.6 V
 - Operating temperature.....-20 to +70°C
- Package
 - MFP20
 - SSOP20

Package Dimensions

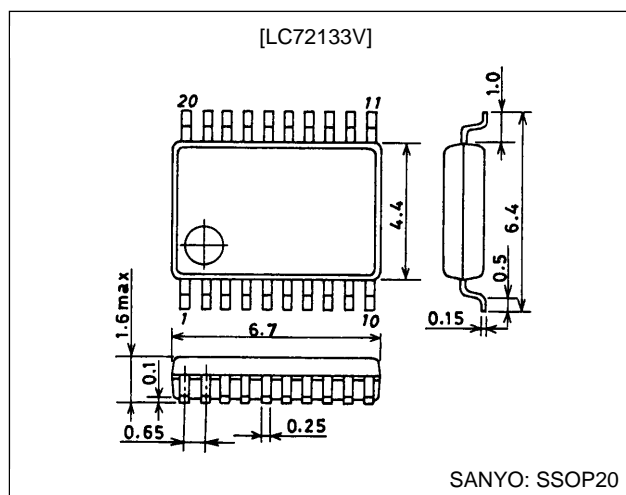
unit: mm

3036B-MFP20



unit: mm

3179A-SSOP20



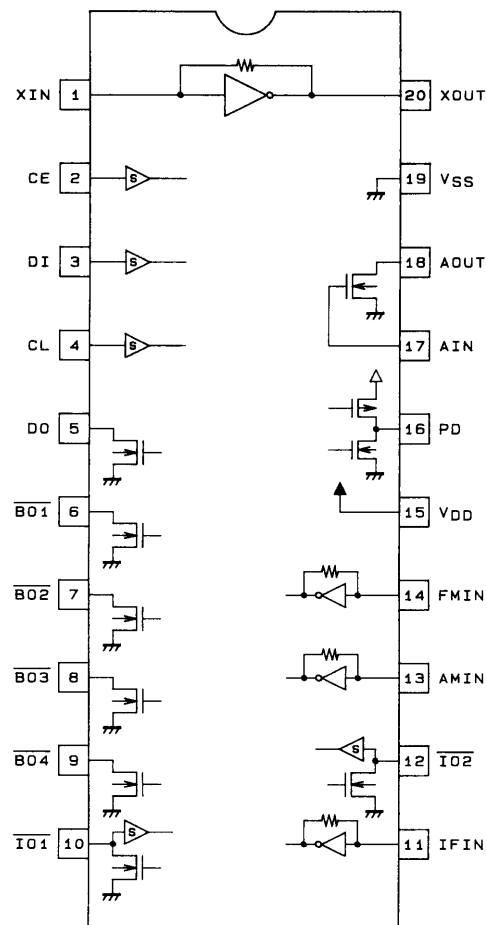
- CCB is a trademark of SANYO ELECTRIC CO., LTD.
- CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.

SANYO Electric Co.,Ltd. Semiconductor Business Headquarters

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22897HA (OT)/63196HA (OT) No. 5427-1/22

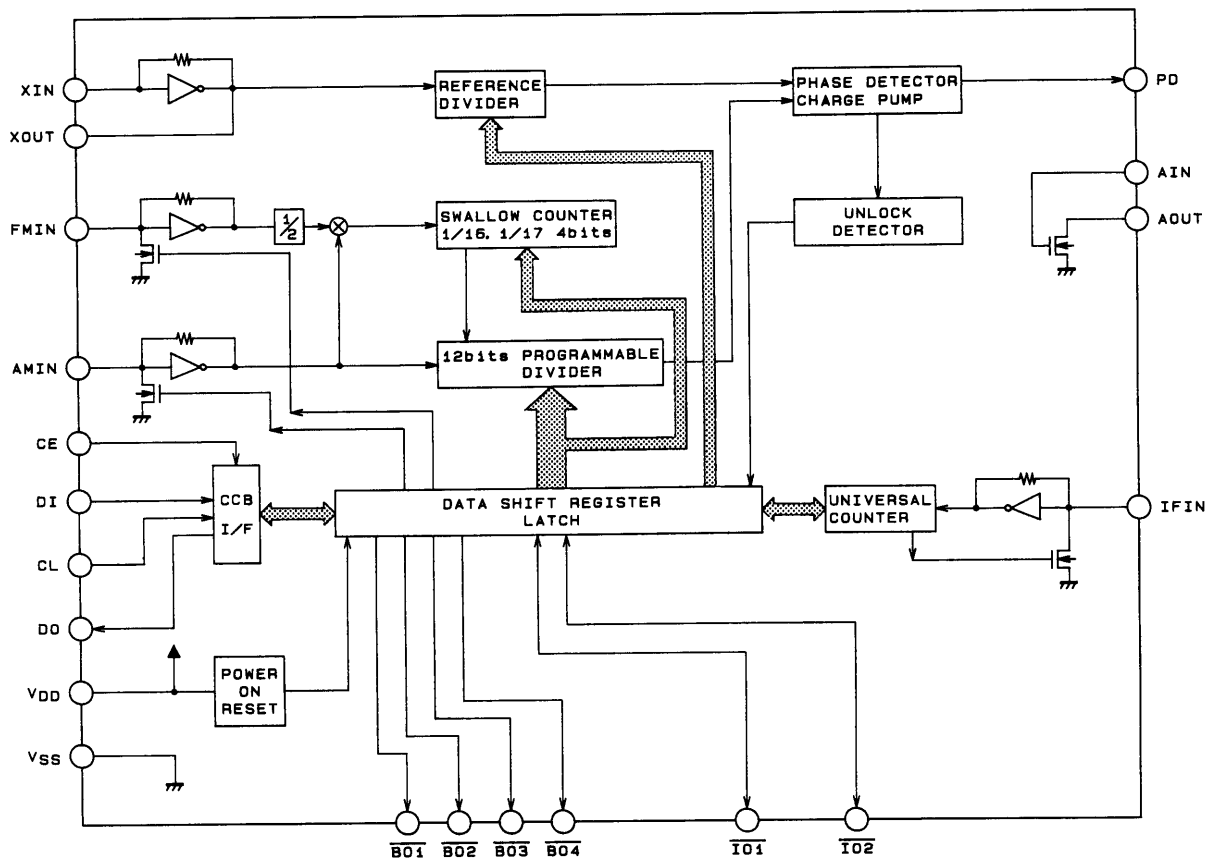
Pin Assignment



Block Diagram

Top view

A02596



A02697

Specifications

Absolute Maximum Ratings at Ta = 25°C, VSS = 0 V

Parameter	Symbol	Pins	Ratings	Unit
Supply voltage	V _{DD} max	V _{DD}	−0.3 to +5.5	V
Maximum input voltage	V _{IN1} max	CE, CL, DI, AIN	−0.3 to +5.5	V
	V _{IN2} max	XIN, FMIN, AMIN, IFIN	−0.3 to V _{DD} + 0.3	V
	V _{IN3} max	IO1, IO2	−0.3 to +15	V
Maximum output voltage	V _{O1} max	DO	−0.3 to +5.5	V
	V _{O2} max	XOUT, PD	−0.3 to V _{DD} + 0.3	V
	V _{O3} max	BO1 to BO4, IO1, IO2, AOUT	−0.3 to +15	V
Maximum output current	I _{O1} max	BO1	0 to 3.0	mA
	I _{O2} max	AOUT, DO	0 to 6.0	mA
	I _{O3} max	BO2 to BO4, IO1, IO2	0 to 6.0	mA
Allowable power dissipation	Pd max	Ta ≤ 70°C: LC72133M	180	mW
		Ta ≤ 70°C: LC72133V	160	mW
Operating temperature	T _{opr}		−20 to +70	°C
Storage temperature	T _{stg}		−40 to +125	°C

Allowable Operating Ranges at Ta = −20 to +70°C, VSS = 0 V

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Supply voltage	V _{DD}	V _{DD}		2.7		3.6	V
Input high-level voltage	V _{IH1}	CE, CL, DI		0.7 V _{DD}		5.5	V
	V _{IH2}	IO1, IO2		0.7 V _{DD}		13	V
Input low-level voltage	V _{IL}	CE, CL, DI, IO1, IO2		0		0.3 V _{DD}	V
Output voltage	V _{O1}	DO		0		5.5	V
	V _{O2}	BO1 to BO4, IO1, IO2, AOUT		0		13	V
Input frequency	f _{IN1}	XIN	V _{IN1}	1		8	MHz
	f _{IN2-1}	FMIN	V _{IN2-1}	10		90	MHz
	f _{IN2-2}	FMIN	V _{IN2-2}	10		120	MHz
	f _{IN2-3}	FMIN	V _{IN2-1} , V _{DD} ≥ 3.0 V	10		130	MHz
	f _{IN3}	AMIN	V _{IN3} , SNS = 1	2		40	MHz
	f _{IN4}	AMIN	V _{IN4} , SNS = 0	0.5		10	MHz
	f _{IN5}	IFIN	V _{IN5}	0.4		12	MHz
Input amplitude	V _{IN1}	XIN	f _{IN1}	400		900	mVrms
	V _{IN2-1}	FMIN	f _{IN2-1} , f _{IN2-3}	70		900	mVrms
	V _{IN2-2}	FMIN	f _{IN2-2}	100		900	mVrms
	V _{IN3}	AMIN	f _{IN3} , SNS = 1	70		900	mVrms
	V _{IN4}	AMIN	f _{IN4} , SNS = 0	70		900	mVrms
	V _{IN5-1}	IFIN	f _{IN5} , IFS = 1	70		900	mVrms
	V _{IN5-2}	IFIN	f _{IN6} , IFS = 0	100		900	mVrms
Supported crystals	Xtal	XIN, XOUT	*	4.0		8.0	MHz

Note: * Recommended crystal oscillator CI values:

CI ≤ 120Ω (For a 4.5 MHz crystal)

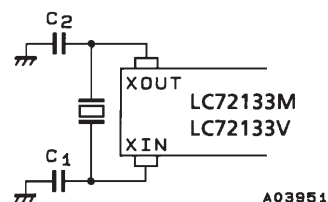
CI ≤ 70Ω (For a 7.2 MHz crystal)

<Sample Oscillator Circuit>

Crystal oscillator: HC-49/U (manufactured by Kinseki, Ltd.), CL = 12 pF

C1 = C2 = 15 pF

The circuit constants for the crystal oscillator circuit depend on the crystal used, the printed circuit board pattern, and other items. Therefore we recommend consulting with the manufacturer of the crystal for evaluation and reliability.

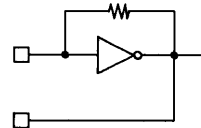
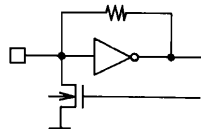
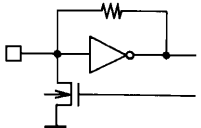
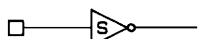
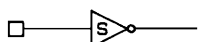

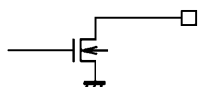


LC72133M, 72133V

Electrical Characteristics for the Allowable Operating Ranges at Ta = -20 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Built-in feedback resistance	Rf1	XIN			1.0		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	AMIN			500		kΩ
	Rf4	IFIN			250		kΩ
Built-in pull-down resistor	Rpd1	FMIN			200		kΩ
	Rpd2	AMIN			200		kΩ
Hysteresis	V _{HIS}	CE, CL, DI, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$			0.1 V _{DD}		V
Output high level voltage	V _{OH1}	PD	I _O = -1 mA	V _{DD} - 1.0			V
Output low level voltage	V _{OL1}	PD	I _O = 1 mA			1.0	V
	V _{OL2}	$\overline{\text{BO1}}$	I _O = 0.5 mA			0.6	V
			I _O = 1 mA			1.2	V
	V _{OL3}	DO	I _O = 1 mA			0.25	V
			I _O = 3 mA			0.75	V
	V _{OL4}	$\overline{\text{BO2}}$ to $\overline{\text{BO4}}$, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	I _O = 1 mA			0.25	V
			I _O = 5 mA			1.25	V
	V _{OL5}	AOUT	I _O = 1 mA, AIN = 1.3 V			0.5	V
Input high level current	I _{IH1}	CE, CL, DI	V _I = 5.5 V			5.0	μA
	I _{IH2}	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V _I = 13 V			5.0	μA
	I _{IH3}	XIN	V _I = V _{DD}	1.3		8	μA
	I _{IH4}	FMIN, AMIN	V _I = V _{DD}	2.7		15	μA
	I _{IH5}	IFIN	V _I = V _{DD}	5.4		30	μA
	I _{IH6}	AIN	V _I = 5.5 V			200	nA
Input low level current	I _{IL1}	CE, CL, DI	V _I = 0 V			5.0	μA
	I _{IL2}	$\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V _I = 0 V			5.0	μA
	I _{IL3}	XIN	V _I = 0 V	1.3		8	μA
	I _{IL4}	FMIN, AMIN	V _I = 0 V	2.7		15	μA
	I _{IL5}	IFIN	V _I = 0 V	5.4		30	μA
	I _{IL6}	AIN	V _I = 0 V			200	nA
Output off leakage current	I _{OFF1}	$\overline{\text{BO1}}$ to $\overline{\text{BO4}}$, AOUT, $\overline{\text{IO1}}$, $\overline{\text{IO2}}$	V _O = 13 V			5.0	μA
	I _{OFF2}	DO	V _O = 5.5 V			5.0	μA
High level three-state off leakage current	I _{OFFH}	PD	V _O = V _{DD}		0.01	200	nA
Low level three-state off leakage current	I _{OFFL}	PD	V _O = 0 V		0.01	200	nA
Input capacitance	C _{IN}	FMIN			6		pF
Current drain	I _{DD1}	V _{DD}	Xtal = 7.2 MHz, f _{IN2} = 130 MHz, V _{IN2} = 70 mVrms		2	5	mA
	I _{DD2}	V _{DD}	PLL block stopped (PLL INHIBIT), Xtal oscillator operating (Xtal = 7.2 MHz)		0.3		mA
	I _{DD3}	V _{DD}	PLL block stopped Xtal oscillator stopped			30	μA

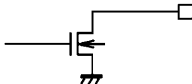
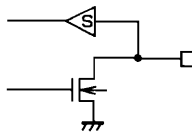
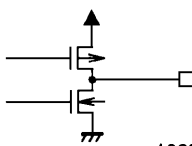
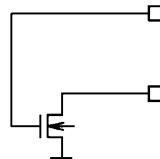
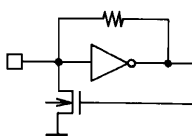
Pin Functions

Symbol	Pin No.	Type	Functions	Circuit configuration															
XIN XOUT	1 20	Xtal OSC	<ul style="list-style-type: none">Crystal resonator connection (4.5/7.2 MHz)	 A02598															
FMIN	14	Local oscillator signal input	<ul style="list-style-type: none">FMIN is selected when the serial data input DVS bit is set to 1.The input frequency range is from 10 to 130 MHz.The input signal passes through the internal divide-by-two prescaler and is input to the swallow counter.The divisor can be in the range 272 to 65535. However, since the signal has passed through the divide-by-two prescaler, the actual divisor is twice the set value. <table border="1"><thead><tr><th rowspan="2">Operating conditions</th><th colspan="3">FMIN input frequency</th></tr><tr><th>10 to 90 MHz</th><th>10 to 120 MHz</th><th>10 to 130 MHz</th></tr></thead><tbody><tr><td>Operating power-supply voltage</td><td>2.7 to 3.6 V</td><td>2.7 to 3.6 V</td><td>3.0 to 3.6 V</td></tr><tr><td>Operating input levels</td><td>70 to 900 mVrms</td><td>100 to 900 mVrms</td><td>70 to 900 mVrms</td></tr></tbody></table>	Operating conditions	FMIN input frequency			10 to 90 MHz	10 to 120 MHz	10 to 130 MHz	Operating power-supply voltage	2.7 to 3.6 V	2.7 to 3.6 V	3.0 to 3.6 V	Operating input levels	70 to 900 mVrms	100 to 900 mVrms	70 to 900 mVrms	 A02599
Operating conditions	FMIN input frequency																		
	10 to 90 MHz	10 to 120 MHz	10 to 130 MHz																
Operating power-supply voltage	2.7 to 3.6 V	2.7 to 3.6 V	3.0 to 3.6 V																
Operating input levels	70 to 900 mVrms	100 to 900 mVrms	70 to 900 mVrms																
AMIN	13	Local oscillator signal input	<ul style="list-style-type: none">AMIN is selected when the serial data input DVS bit is set to 0.When the serial data input SNS bit is set to 1:<ul style="list-style-type: none">The input frequency range is 2 to 40 MHz.The signal is directly input to the swallow counter.The divisor can be in the range 272 to 65535, and the divisor used will be the value set.When the serial data input SNS bit is set to 0:<ul style="list-style-type: none">The input frequency range is 0.5 to 10 MHz.The signal is directly input to a 12-bit programmable divider.The divisor can be in the range 4 to 4095, and the divisor used will be the value set.	 A02599															
CE	2	Chip enable	Set this pin high when inputting (DI) or outputting (DO) serial data.	 A02600															
CL	4	Clock	<ul style="list-style-type: none">Used as the synchronization clock when inputting (DI) or outputting (DO) serial data.	 A02600															
DI	3	Data input	<ul style="list-style-type: none">Inputs serial data transferred from the controller to the LC72133.	 A02600															
DO	5	Data output	<ul style="list-style-type: none">Outputs serial data transferred from the LC72133 to the controller.The content of the output data is determined by the serial data DOC0 to DOC2.	 A02601															
V _{DD}	15	Power supply	<ul style="list-style-type: none">The LC72133 power supply pin (V_{DD} = 2.7 to 3.6 V)The power on reset circuit operates when power is first applied.																

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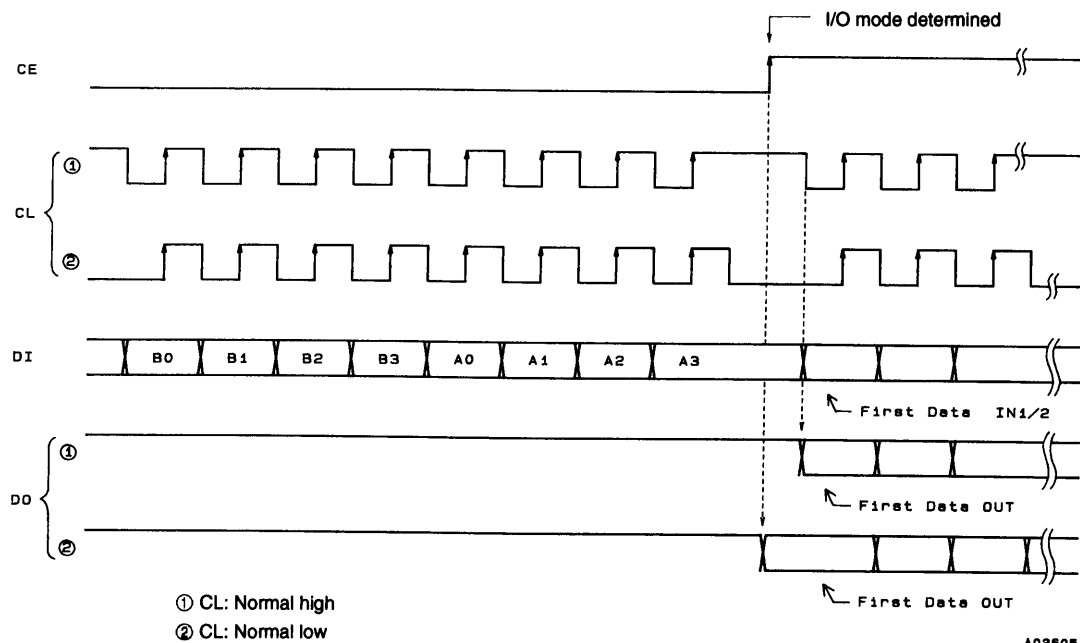
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Symbol	Pin No.	Type	Functions	Circuit configuration
V _{SS}	19	Ground	<ul style="list-style-type: none"> The LC72133 ground 	—
$\overline{\text{BO1}}$ $\overline{\text{BO2}}$ $\overline{\text{BO3}}$ $\overline{\text{BO4}}$	6 7 8 9	Output port	<ul style="list-style-type: none"> Dedicated output pins The output states are determined by $\overline{\text{BO1}}$ to $\overline{\text{BO4}}$ bits in the serial data. Data: 0 = open, 1 = low A time base signal (8 Hz) can be output from the $\overline{\text{BO1}}$ pin. (When the serial data TBC bit is set to 1.) Care is required when using the $\overline{\text{BO1}}$ pin, since it has a higher on impedance than the other output ports (pins $\overline{\text{BO2}}$ to $\overline{\text{BO4}}$). The data = 0 (open) state is selected after the power-on reset. 	 A02601
$\overline{\text{IO1}}$ $\overline{\text{IO2}}$	10 12	I/O port	<ul style="list-style-type: none"> I/O dual-use pins The direction (input or output) is determined by bits IOC1 and IOC2 in the serial data. Data: 0 = input port, 1 = output port When specified for use as input ports: The state of the input pin is transmitted to the controller over the DO pin. Input state: low = 0 data value high = 1 data value When specified for use as output ports: The output states are determined by the IO1 and IO2 bits in the serial data. Data: 0 = open, 1 = low These pins function as input pins following a power on reset. 	 A02602
PD	16	Charge pump output	<ul style="list-style-type: none"> PLL charge pump output When the frequency generated by dividing the local oscillator frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high impedance state when the frequencies match. 	 A02603
AIN AOUT	17 18	LPF amplifier transistor	<ul style="list-style-type: none"> The n-channel MOS transistor used for the PLL active low-pass filter. 	 A02604
IFIN	11	IF counter	<ul style="list-style-type: none"> Accepts an input in the frequency range 0.4 to 12 MHz. The input signal is directly transmitted to the IF counter. The result is output starting the MSB of the IF counter using the DO pin. Four measurement periods are supported: 4, 8, 32, and 64 ms. 	 A02599

Serial Data I/O Methods

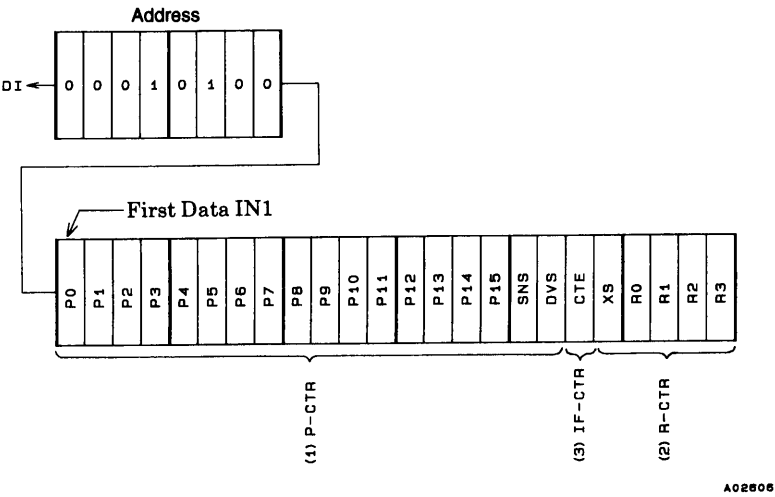
The LC72133 inputs and outputs data using the Sanyo CCB (computer control bus) audio LSI serial bus format. This LSI adopts an 8-bit address format CCB.

	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
1	IN1 (82)	0	0	0	1	0	1	0	0	<ul style="list-style-type: none"> Control data input mode (serial data input) 24 data bits are input. See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.
2	IN2 (92)	1	0	0	1	0	1	0	0	<ul style="list-style-type: none"> Control data input mode (serial data input) 24 data bits are input. See the "DI Control Data (serial data input) Structure" item for details on the meaning of the input data.
3	OUT (A2)	0	1	0	1	0	1	0	0	Data output mode (serial data output) <ul style="list-style-type: none"> The number of bits output is equal to the number of clock cycles. See the "DO Output Data (Serial Data Output) Structure" item for details on the meaning of the output data.

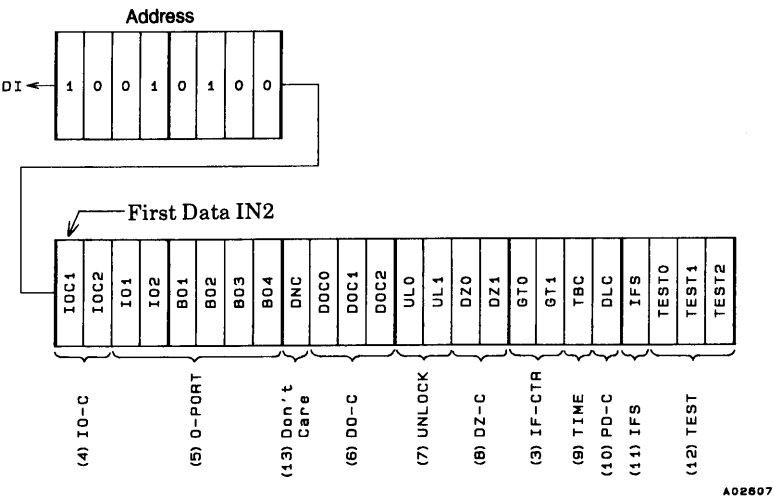


1. DI Control Data (Serial Data Input) Structure

- IN1 Mode



- IN2 Mode



2. DI Control Data Functions

No.	Control block/data	Functions	Related data																																				
(1)	Programmable divider data P0 to P15 DVS, SNS	<ul style="list-style-type: none">Data that sets the programmable divider. A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS. (*: don't care) <table><tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr><tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr><tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr><tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr></table> <p>Note: P0 to P3 are ignored when P4 is the LSB.</p> <ul style="list-style-type: none">Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the input frequency range. (*: don't care) <table><tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr><tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 130 MHz</td></tr><tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40 MHz</td></tr><tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10 MHz</td></tr></table> <p>Note: See the "Programmable Divider" item for more information.</p>	DVS	SNS	LSB	Divisor setting (N)	Actual divisor	1	*	P0	272 to 65535	Twice the value of the setting	0	1	P0	272 to 65535	The value of the setting	0	0	P4	4 to 4095	The value of the setting	DVS	SNS	Input pin	Input frequency range	1	*	FMIN	10 to 130 MHz	0	1	AMIN	2 to 40 MHz	0	0	AMIN	0.5 to 10 MHz	
DVS	SNS	LSB	Divisor setting (N)	Actual divisor																																			
1	*	P0	272 to 65535	Twice the value of the setting																																			
0	1	P0	272 to 65535	The value of the setting																																			
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DVS	SNS	Input pin	Input frequency range																																				
1	*	FMIN	10 to 130 MHz																																				
0	1	AMIN	2 to 40 MHz																																				
0	0	AMIN	0.5 to 10 MHz																																				
(2)	Reference divider data R0 to R3 																																						

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No.	Control block/data	Functions	Related data																																																																																									
(6)	DO pin control data DOC0, DOC1, DOC2	<div>• Data that determines the DO pin output</div> <table><tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin state</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr><tr><td>0</td><td>1</td><td>0</td><td>end-UC*1</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr><tr><td>1</td><td>0</td><td>1</td><td>The $\overline{\text{IO1}}$ pin state*2</td></tr><tr><td>1</td><td>1</td><td>0</td><td>The $\overline{\text{IO2}}$ pin state*2</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr></table> <p>The open state is selected after the power-on reset.</p> <p>Note: 1. end-UC: Check for IF counter measurement completion</p> <div></div> <div><p>① Counter start ② Counter complete ③ CE: high</p><p>▲02508</p></div> <div><p>① When end-UC is set and the IF counter is started (i.e., when CTE is changed from zero to one), the DO pin automatically goes to the open state.</p><p>② When the IF counter measurement completes, the DO pin goes low to indicate the measurement completion state.</p><p>③ Depending on serial data I/O (CE: high) the DO pin goes to the open state.</p><p>2. Goes to the open state if the I/O pin is specified to be an output port.</p></div> <p>Caution: The state of the DO pin during a data input period (an IN1 or IN2 mode period with CE high) will be open, regardless of the state of the DO control data (DOC0 to DOC2). Also, the DO pin during a data output period (an OUT mode period with CE high) will output the contents of the internal DO serial data in synchronization with the CL pin signal, regardless of the state of the DO control data (DOC0 to DOC2).</p> <div>UL0, UL1, CTE, IOC1, IOC2</div>	DOC2	DOC1	DOC0	DO pin state	0	0	0	Open	0	0	1	Low when the unlock state is detected	0	1	0	end-UC*1	0	1	1	Open	1	0	0	Open	1	0	1	The $\overline{\text{IO1}}$ pin state*2	1	1	0	The $\overline{\text{IO2}}$ pin state*2	1	1	1	Open	(7)	Unlock detection data UL0, UL1	<div>• Selects the phase error (øE) detection width for checking PLL lock. A phase error in excess of the specified detection width is seen as an unlocked state.</div> <table><tr><th>UL1</th><th>UL0</th><th>øE detection width</th><th>Detector output</th></tr><tr><td>0</td><td>0</td><td>Stopped</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>øE is output directly</td></tr><tr><td>1</td><td>0</td><td>±0.55 μs</td><td>øE is extended by 1 to 2 ms</td></tr><tr><td>1</td><td>1</td><td>±1.11</td><td>øE is extended by 1 to 2 ms</td></tr></table> <p>Note: In the unlocked state the DO pin goes low and the UL bit in the serial data becomes zero.</p> <div>DOC0, DOC1, DOC2</div>	UL1	UL0	øE detection width	Detector output	0	0	Stopped	Open	0	1	0	øE is output directly	1	0	±0.55 μs	øE is extended by 1 to 2 ms	1	1	±1.11	øE is extended by 1 to 2 ms	(8)	Phase comparator control data DZ0, DZ1	<div>• Controls the phase comparator dead zone.</div> <table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table> <p>Dead zone widths: DZA < DZB < DZC < DZD</p> <div></div>	DZ1	DZ0	Dead zone mode	0	0	DZA	0	1	DZB	1	0	DZC	1	1	DZD	(9)	Clock time base TBC	Setting TBC to one causes an 8 Hz, 40% duty clock time base signal to be output from the BO1 pin. (BO1 data is invalid in this mode.)	BO1	(10)	Charge pump control data DLC	<div>• Forcibly controls the charge pump output.</div> <table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal operation</td></tr><tr><td>1</td><td>Forced low</td></tr></table> <p>Note: If deadlock occurs due to the VCO control voltage (Vtune) going to zero and the VCO oscillator stopping, deadlock can be cleared by forcing the charge pump output to low and setting Vtune to VCC. (This is the deadlock clearing circuit.)</p> <div></div>	DLC	Charge pump output	0	Normal operation	1	Forced low
DOC2	DOC1	DOC0	DO pin state																																																																																									
0	0	0	Open																																																																																									
0	0	1	Low when the unlock state is detected																																																																																									
0	1	0	end-UC*1																																																																																									
0	1	1	Open																																																																																									
1	0	0	Open																																																																																									
1	0	1	The $\overline{\text{IO1}}$ pin state*2																																																																																									
1	1	0	The $\overline{\text{IO2}}$ pin state*2																																																																																									
1	1	1	Open																																																																																									
UL1	UL0	øE detection width	Detector output																																																																																									
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DZ1	DZ0	Dead zone mode																																																																																										
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0	1	DZB																																																																																										
1	0	DZC																																																																																										
1	1	DZD																																																																																										
DLC	Charge pump output																																																																																											
0	Normal operation																																																																																											
1	Forced low																																																																																											

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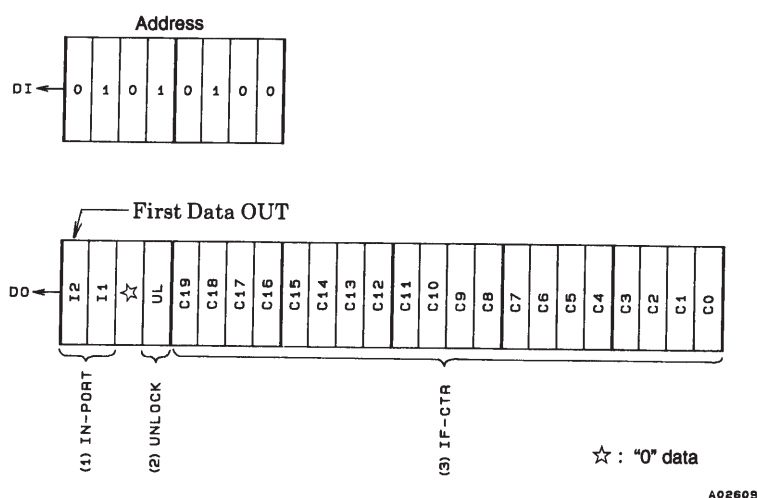
LC72133M, 72133V

Continued from preceding page.

No.	Control block/data	Functions	Related data
(11)	IF counter control data IFS	<ul style="list-style-type: none"> Note that if this value is set to zero the system enters input sensitivity degradation mode, and the sensitivity is reduced to 10 to 30 mV rms. * See the "IF Counter Operation" item for details. 	
(12)	LSI test data TEST 0 to TEST 2	<ul style="list-style-type: none"> LSI test data TEST0 TEST1 TEST2 These values must all be set to 0. These test data are set to 0 automatically after the power-on reset. 	
(13)	DNC	Don't care. This data must be set to 0.	

3. DO Output Data (Serial Data Output)

- OUT Mode

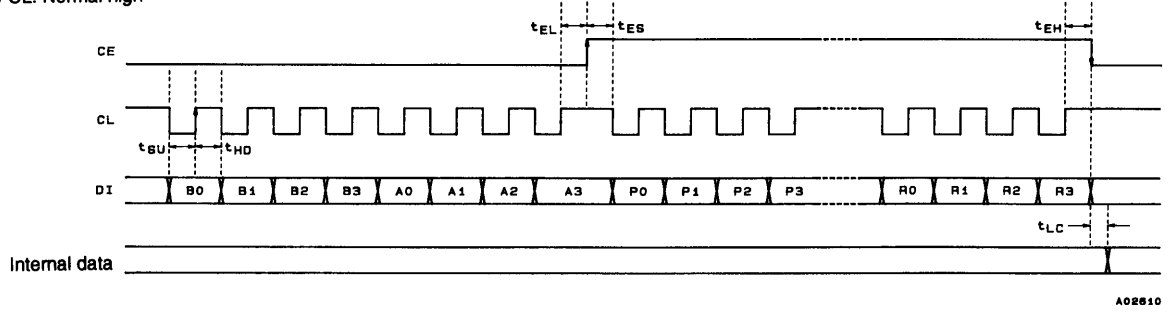


4. DO Output Data

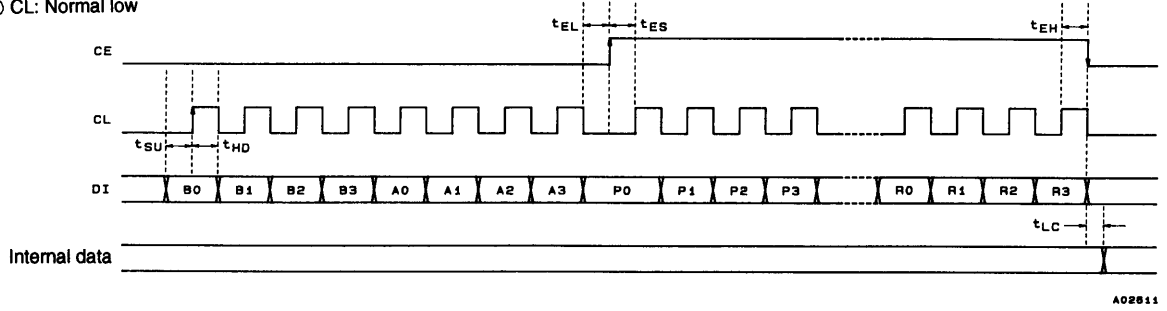
No.	Control block/data	Functions	Related data
(1)	I/O port data I2, I1	<ul style="list-style-type: none"> Latched from the pin states of the $\overline{IO1}$ and $\overline{IO2}$ I/O ports. These values follow the pin states regardless of the input or output setting. Data is latched at the point where the circuit enters data output mode (OUT mode). I1 ← $\overline{IO1}$ pin state } High: 1 I2 ← $\overline{IO2}$ pin state } Low: 0 	IOC1, IOC2
(2)	PLL unlock data UL	<ul style="list-style-type: none"> Latched from the state of the unlock detection circuit. UL ← 0: Unlocked UL ← 1: Locked or detection stopped mode 	UL0, UL1
(3)	IF counter binary data C19 to C0	<ul style="list-style-type: none"> Latched from the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter 	CTE, GT0, GT1

5. Serial Data Input (IN1/IN2) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75 \mu s$, $t_{LC} < 0.75 \mu s$

① CL: Normal high

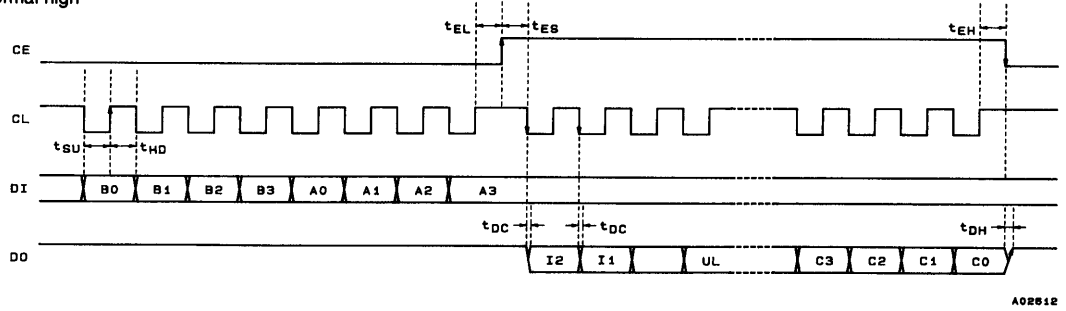


② CL: Normal low

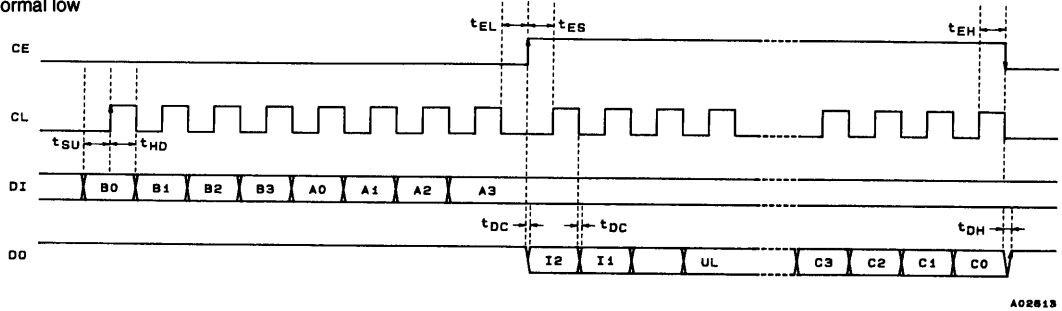


6. Serial Data Output (OUT) t_{SU} , t_{HD} , t_{EL} , t_{ES} , $t_{EH} \geq 0.75 \mu s$, t_{DC} , $t_{DH} < 0.35 \mu s$

① CL: Normal high

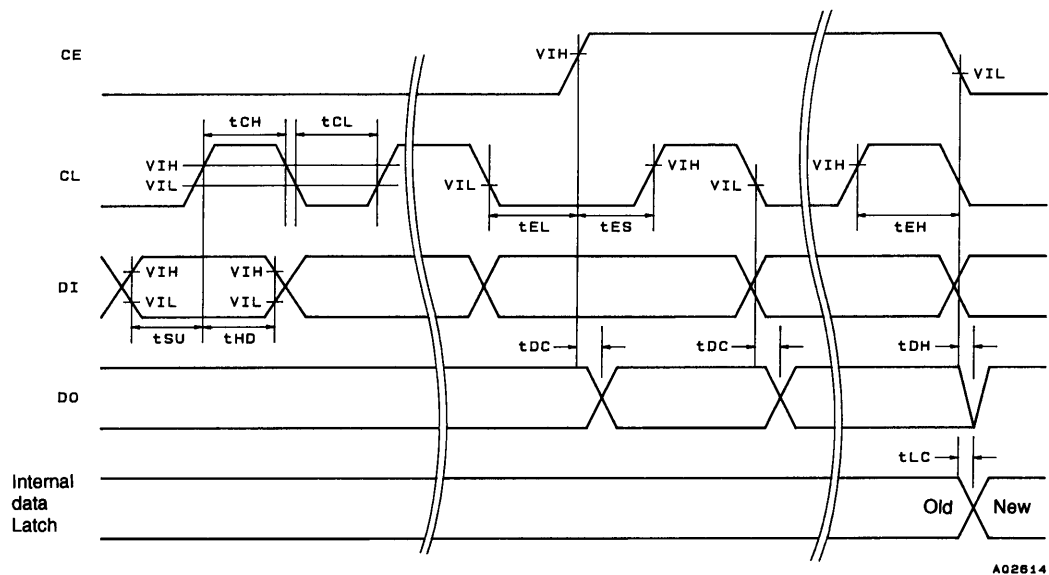


② CL: Normal low

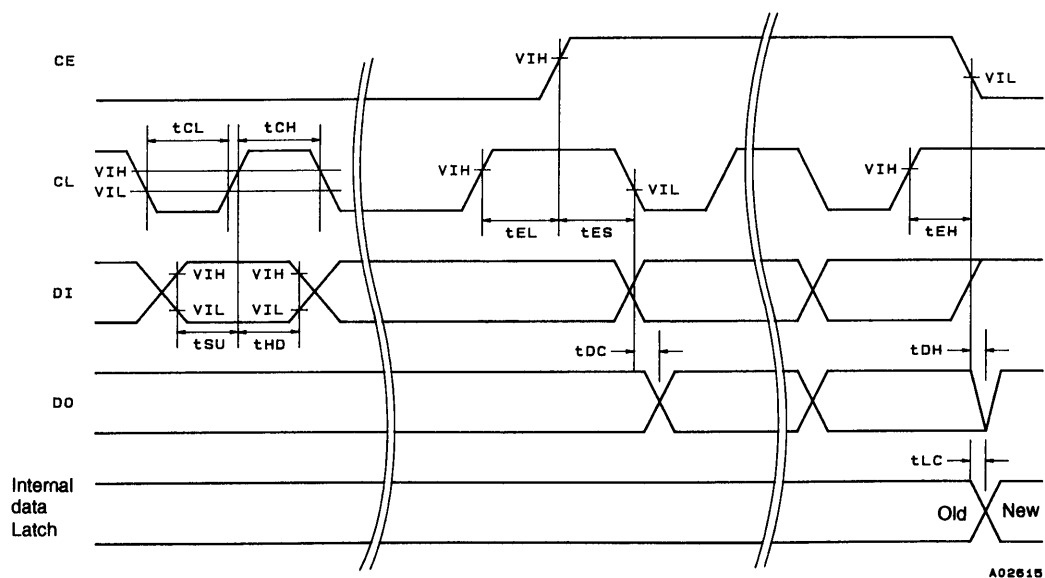


Note: Since the DO pin is an n-channel open-drain circuit, the time for the data to change (t_{DC} and t_{DH}) will differ depending on the value of the pull-up resistor and printed circuit, board capacitance.

7. Serial Data Timing



When stopped with CL low

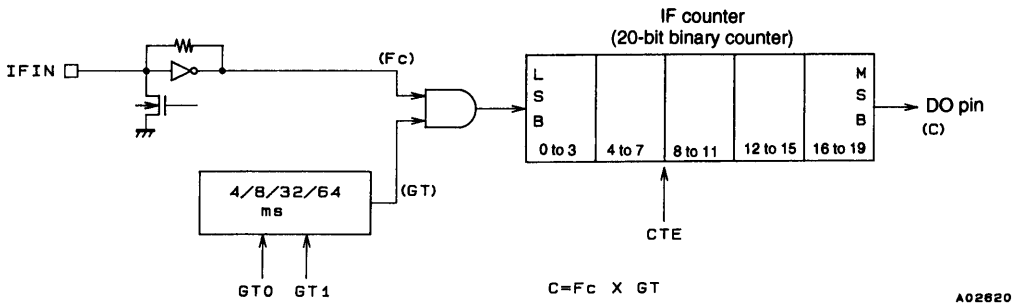


When stopped with CL high

Parameter	Symbol	Pins	Conditions	min	typ	max	Unit
Data setup time	t _{SU}	DI, CL		0.75			μs
Data hold time	t _{HD}	DI, CL		0.75			μs
Clock low-level time	t _{CL}	CL		0.75			μs
Clock high-level time	t _{CH}	CL		0.75			μs
CE wait time	t _{EL}	CE, CL		0.75			μs
CE setup time	t _{ES}	CE, CL		0.75			μs
CE hold time	t _{EH}	CE, CL		0.75			μs
Data latch change time	t _{LC}					0.75	μs
Data output time	t _{DC}	DO, CL	Differs depending on the value of the pull-up resistor and the printed circuit board capacitances.			0.35	μs
	t _{DH}	DO, CE					

IF Counter Structure

The LC72133 IF counter is a 20-bit binary counter. The result, i.e., the counter's MSB, can be read serially from the DO pin.



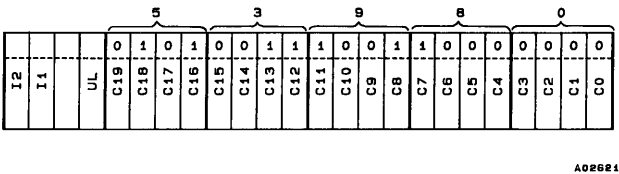
GT1	GT0	Measurement time	
		Measurement period (GT) (ms)	Wait time (twu) (ms)
0	0	4	3 to 4
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

The IF frequency (Fc) is measured by determining how many pulses were input to an IF counter in a specified measurement period, GT.

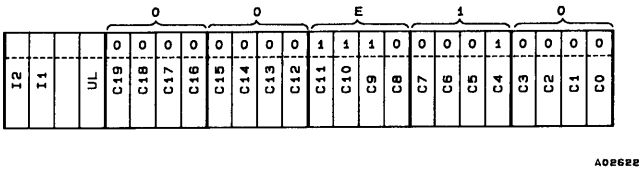
$$F_c = \frac{C}{GT} \quad (C = F_c \times GT) \quad C: \text{Count value (number of pulses)}$$

1. IF Counter Frequency Calculation Examples

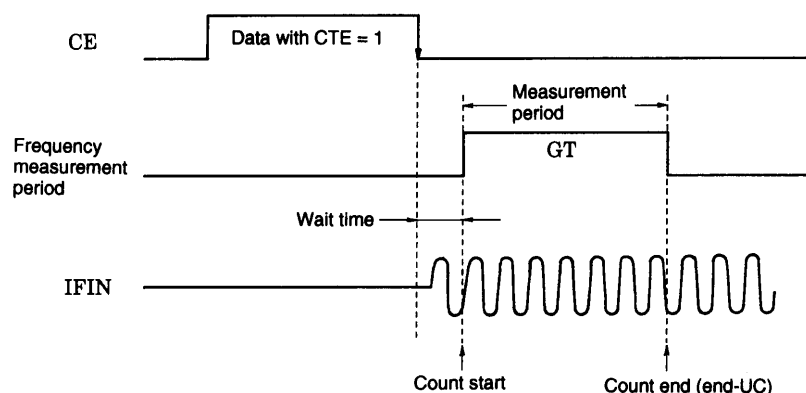
- When the measurement period (GT) is 32 ms, the count (C) is 53980 hexadecimal (342400 decimal):
IF frequency (Fc) = 342400 ÷ 32 ms = 10.7 MHz



- When the measurement period (GT) is 8 ms, the count (C) is E10 hexadecimal (3600 decimal):
IF frequency (Fc) = 3600 ÷ 8 ms = 450 kHz



2. IF Counter Operation



A02623

Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0.

The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the LC72133 when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF counter at the end of the measurement period must be read out during the period that CTE is 1. This is because the IF counter is reset when CTE is set to 0.

Note: When operating the IF counter, the control microprocessor must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output and execute an IF count operation. Autosearch techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

IFIN minimum input sensitivity standard

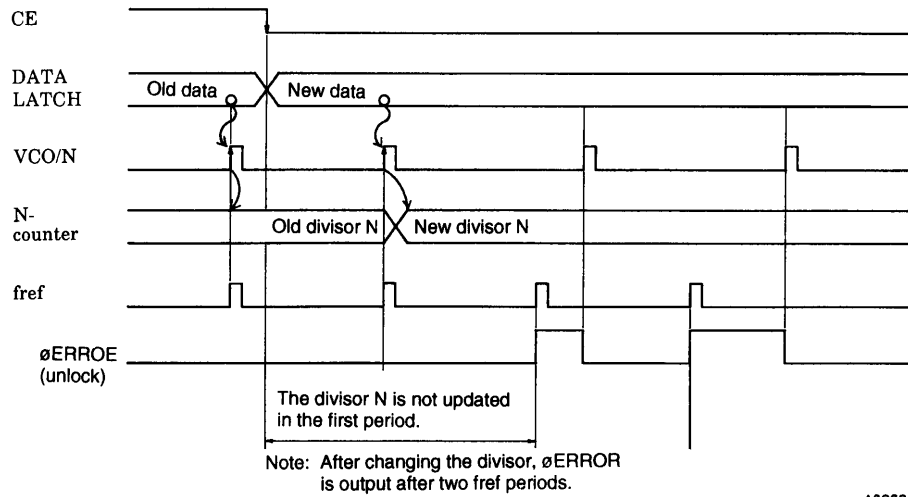
IFS	f (MHz)		
	$0.4 \leq f < 0.5$	$0.5 \leq f < 8$	$8 \leq f \leq 12$
1: Normal mode	70 mVrms (0.5 to 5 mVrms)	70 mVrms	70 mVrms (2 to 10 mVrms)
0: Degradation mode	100 mVrms (10 to 15 mVrms)	100 mVrms	100 mVrms (30 to 50 mVrms)

Note: Values in parentheses are actual performance values presented as reference data.

Unlock Detection Timing

1. Unlock Detection Determination Timing

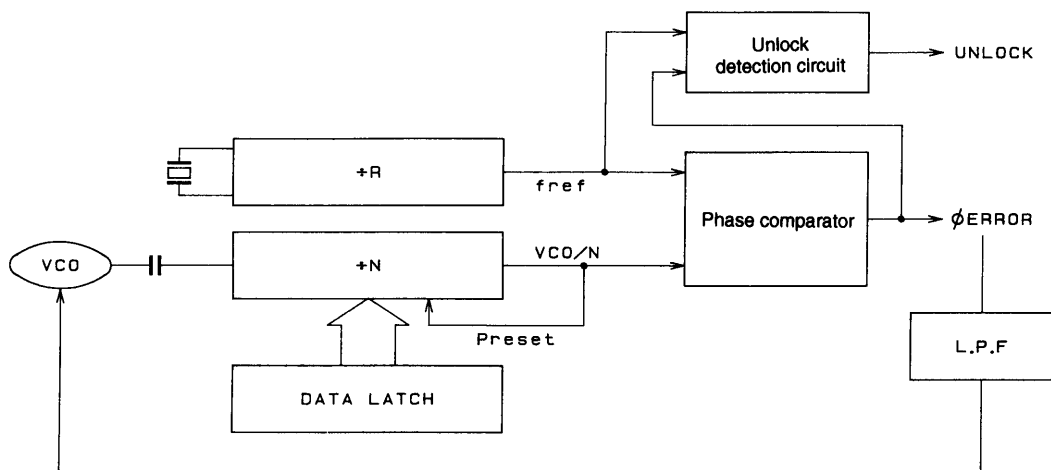
Unlocked state detection is performed in the reference frequency (f_{ref}) period (interval). Therefore, in principle, unlock determination requires a time longer than the period of the reference frequency. However, immediately after changing the divisor N (frequency) unlock detection must be performed after waiting at least two periods of the reference frequency.



A02624

Figure 1 Unlocked State Detection Timing

For example, if f_{ref} is 1 kHz, i.e., the period is 1 ms, after changing the divisor N, the system must wait at least 2 ms before checking for the unlocked state.



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Figure 2 Circuit Structure

2. Unlock Detection Software

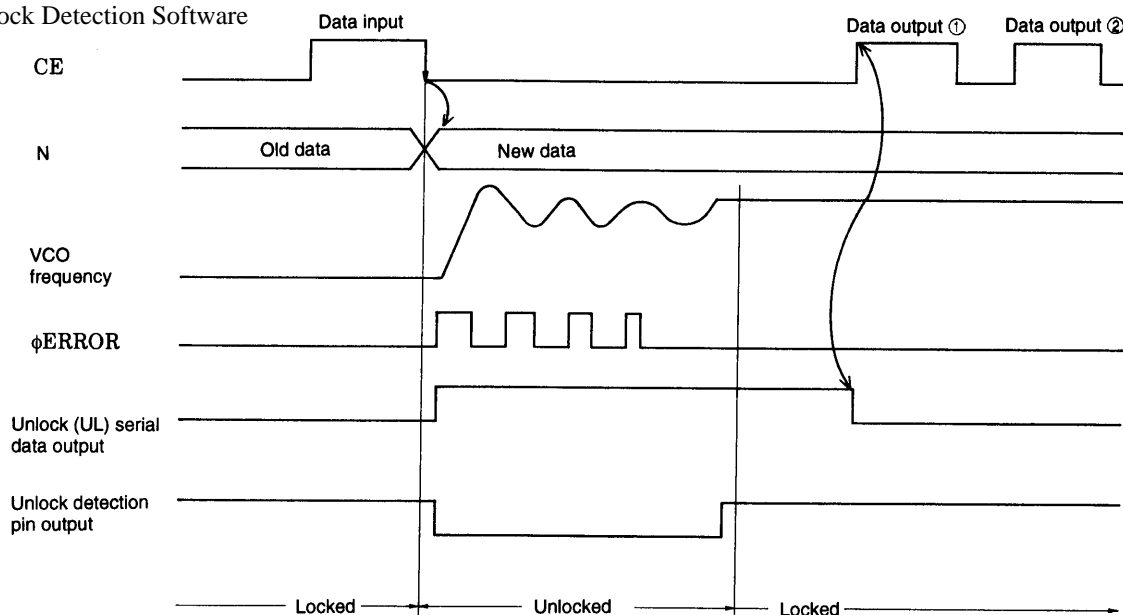


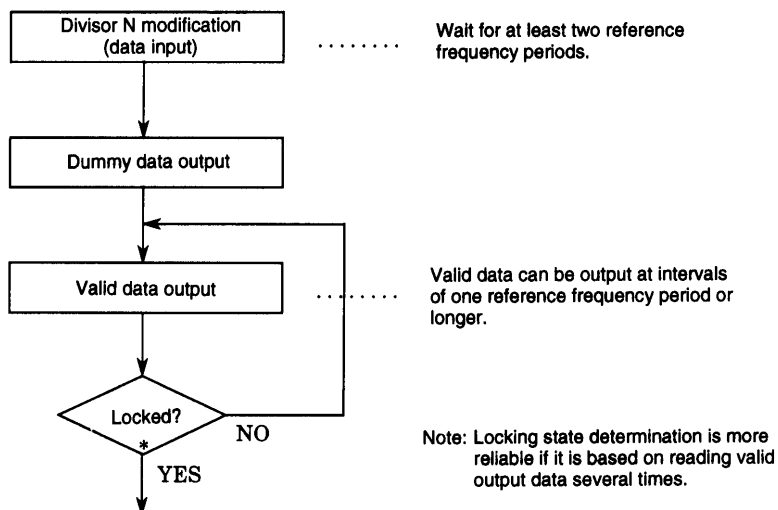
Figure 3

A02626

3. Unlocked State Data Output Using Serial Data Output

In the LC72133, once an unlocked state occurs, the unlocked state serial data (UL) will not be reset until a data input (or output) operation is performed. At the data output ① point in Figure 3, although the VCO frequency has stabilized (locked), since no data output has been performed since the divisor N was changed the unlocked state data remains in the unlocked state. As a result, even though the frequency has stabilized (locked), the system remains (from the standpoint of the data) in the unlocked state.

Therefore, the unlocked state data acquired at data output ①, which occurs immediately after the divisor N was changed, should be treated as a dummy data output and ignored. The second data output (data output ②) and following outputs are valid data.



Locked State Determination Flowchart

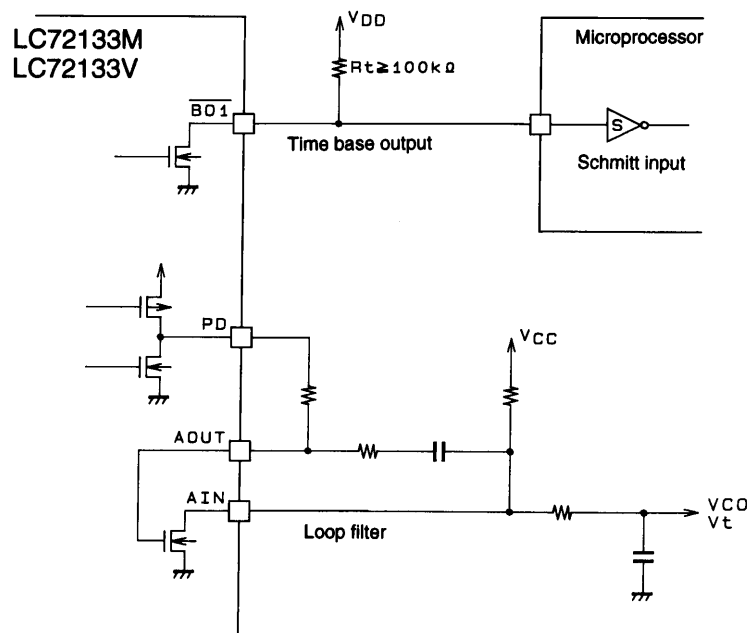
4. Directly Outputting Unlocked State Data from the DO Pin (Set by the DO pin control data)

Since the locking state (high = locked, low = unlocked) is output directly from the DO pin, the dummy data processing described in section 3 above is not required. After changing the divisor N, the locking state can be checked after waiting at least two reference frequency periods.

Clock Time Base Usage Notes

The pull-up resistor used on the clock time base output pin ($\overline{BO1}$) should be at least 100 k Ω . Also, to prevent chattering we recommend using a Schmitt input at the controller (microprocessor) that receives this signal.

This is to prevent degrading the VCO C/N characteristics when a loop filter is formed using the built-in low-pass filter transistor. Since the clock time base output pin and the low-pass filter have a common ground internal to the IC, it is necessary to minimize the time base output pin current fluctuations and to suppress their influence on the low-pass filter.



Other Items

1. Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	- -0 s
0	1	DZB	ON/ON	-0 s
1	0	DZC	OFF/OFF	+0 s
1	1	DZD	OFF/OFF	+ +0 s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

- Side band generation due to reference frequency leakage
- Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/N ratio in excess of 90 to 100 dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

Dead Zone

The phase comparator compares f_p to a reference frequency (f_r) as shown in Figure 4. Although the characteristics of this circuit (see Figure 5) are such that the output voltage is proportional to the phase difference ϕ (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularly-priced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

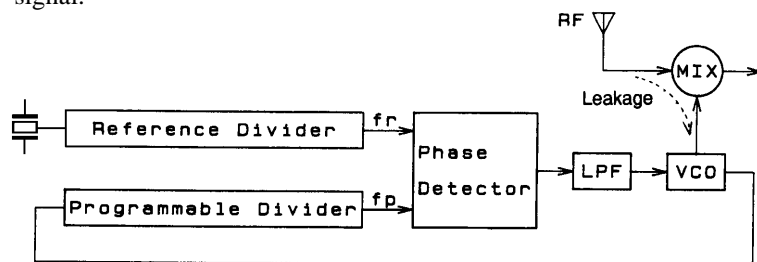
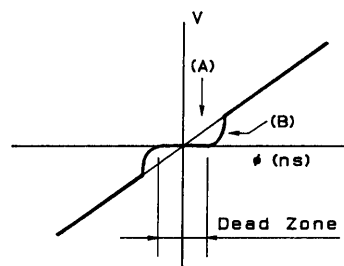


Figure 4

A02930



A02931

Figure 5

2. Notes on the FMIN, AMIN, and IFIN Pins

Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100 pF is desirable. In particular, if a capacitance of 1000 pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

3. Notes on IF Counting → SD must be used in conjunction with the IF counting time

When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can stop at points where there is no signal due to leakage output from the IF counter buffer.

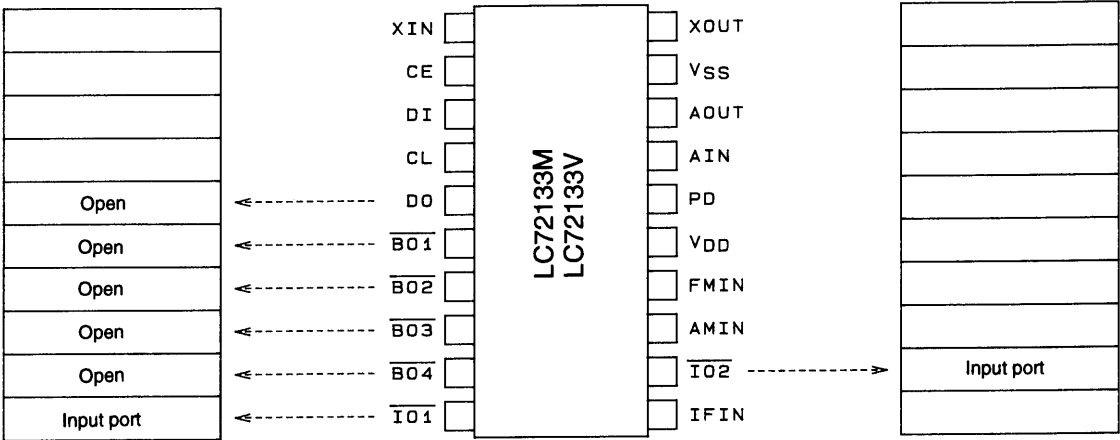
4. DO Pin Usage Techniques

In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

5. Power Supply Pins

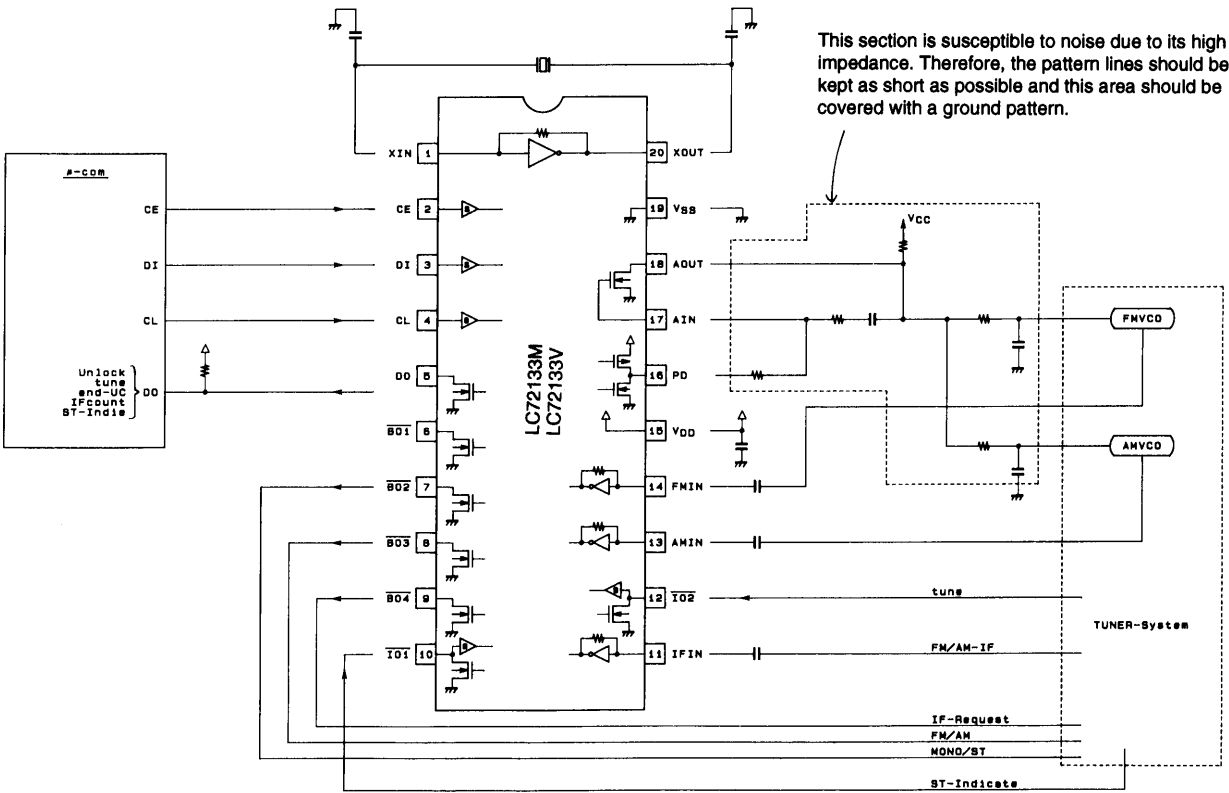
A capacitor of at least 2000 pF must be inserted between the power supply V_{DD} and V_{SS} pins for noise exclusion. This capacitor must be placed as close as possible to the V_{DD} and V_{SS} pins.

Pin States After the Power ON Reset



A02628

Application System Example



A02629

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