

4Gb B-die DDR3 SDRAM

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

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1. Ordering Information

[Table 1] Samsung 4Gb DDR3 B-die ordering information table

Organization	DDR3-1066 (7-7-7)	DDR3-1333 (9-9-9) ⁴	DDR3-1600 (11-11-11) ³	DDR3-1866 (13-13-13) ²	Package
1Gx4	K4B4G0446B-HCF8	K4B4G0446B-HCH9	K4B4G0446B-HCK0	K4B4G0446B-HCMA	78 FBGA
512Mx8	K4B4G0846B-HCF8	K4B4G0846B-HCH9	K4B4G0846B-HCK0	K4B4G0846B-HCMA	78 FBGA

NOTE :

1. Speed bin is in order of CL-tRCD-tRP.
2. Backward compatible to DDR3-1600(11-11-11), DDR3-1333(9-9-9), DDR3-1066(7-7-7)
3. Backward compatible to DDR3-1333(9-9-9), DDR3-1066(7-7-7)
4. Backward compatible to DDR3-1066(7-7-7)

2. Key Features

[Table 2] 4Gb DDR3 B-die Speed bins

Speed	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
	6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	
tCK(min)	2.5	1.875	1.5	1.25	1.07	ns
CAS Latency	6	7	9	11	13	nCK
tRCD(min)	15	13.125	13.5	13.75	13.91	ns
tRP(min)	15	13.125	13.5	13.75	13.91	ns
tRAS(min)	37.5	37.5	36	35	34	ns
tRC(min)	52.5	50.625	49.5	48.75	47.91	ns

- JEDEC standard 1.5V ± 0.075V Power Supply
- V_{DDQ} = 1.5V ± 0.075V
- 400 MHz f_{CK} for 800Mb/sec/pin, 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin, 900MHz f_{CK} for 1866Mb/sec/pin
- 8 Banks
- Programmable CAS Latency(posted CAS): 5,6,7,8,9,10,11,12,13
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600) and 9(DDR3-1866)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95 °C
- Asynchronous Reset
- Package : 78 balls FBGA - x4/x8
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-free

The 4Gb DDR3 SDRAM B-die is organized as a 128Mbit x 4 I/Os x 8banks or 64Mbit x 8 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866Mb/sec/pin (DDR3-1866) for general applications.

The chip is designed to comply with the following key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset .

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. The DDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V V_{DDQ}.

The 4Gb DDR3 B-die device is available in 78ball FBGAs(x4/x8).

NOTE : 1. This data sheet is an abstract of full DDR3 specification and does not cover the common features which are described in "DDR3 SDRAM Device Operation & Timing Diagram".

2. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

3. Package pinout/Mechanical Dimension & Addressing

3.1 x4 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	V _{SS}	V _{DD}	NC				NC	V _{SS}	V _{DD}	A
B	V _{SS}	V _{SSQ}	DQ0				DM	V _{SSQ}	V _{DDQ}	B
C	V _{DDQ}	DQ2	DQS				DQ1	DQ3	V _{SSQ}	C
D	V _{SSQ}	NC	$\overline{\text{DQS}}$				V _{DD}	V _{SS}	V _{SSQ}	D
E	V _{REFDQ}	V _{DDQ}	NC				NC	NC	V _{DDQ}	E
F	NC	V _{SS}	$\overline{\text{RAS}}$				CK	V _{SS}	NC	F
G	ODT	V _{DD}	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	V _{DD}	CKE	G
H	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	H
J	V _{SS}	BA0	BA2				A15	V _{REFCA}	V _{SS}	J
K	V _{DD}	A3	A0				A12/BC	BA1	V _{DD}	K
L	V _{SS}	A5	A2				A1	A4	V _{SS}	L
M	V _{DD}	A7	A9				A11	A6	V _{DD}	M
N	V _{SS}	$\overline{\text{RESET}}$	A13				A14	A8	V _{SS}	N

Ball Locations (x4)

- Populated ball
- + Ball not populated

Top view
(See the balls through the package)

	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	●	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	●
M	●	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	●

3.2 x8 Package Pinout (Top view) : 78ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	V _{SS}	V _{DD}	NC				NU/TDQS	V _{SS}	V _{DD}	A
B	V _{SS}	V _{SSQ}	DQ0				DM/TDQS	V _{SSQ}	V _{DDQ}	B
C	V _{DDQ}	DQ2	DQS				DQ1	DQ3	V _{SSQ}	C
D	V _{SSQ}	DQ6	DQS				V _{DD}	V _{SS}	V _{SSQ}	D
E	V _{REFDQ}	V _{DDQ}	DQ4				DQ7	DQ5	V _{DDQ}	E
F	NC	V _{SS}	RAS				CK	V _{SS}	NC	F
G	ODT	V _{DD}	CAS				CK	V _{DD}	CKE	G
H	NC	CS	WE				A10/AP	ZQ	NC	H
J	V _{SS}	BA0	BA2				A15	V _{REFCA}	V _{SS}	J
K	V _{DD}	A3	A0				A12/BC	BA1	V _{DD}	K
L	V _{SS}	A5	A2				A1	A4	V _{SS}	L
M	V _{DD}	A7	A9				A11	A6	V _{DD}	M
N	V _{SS}	RESET	A13				A14	A8	V _{SS}	N

Ball Locations (x8)

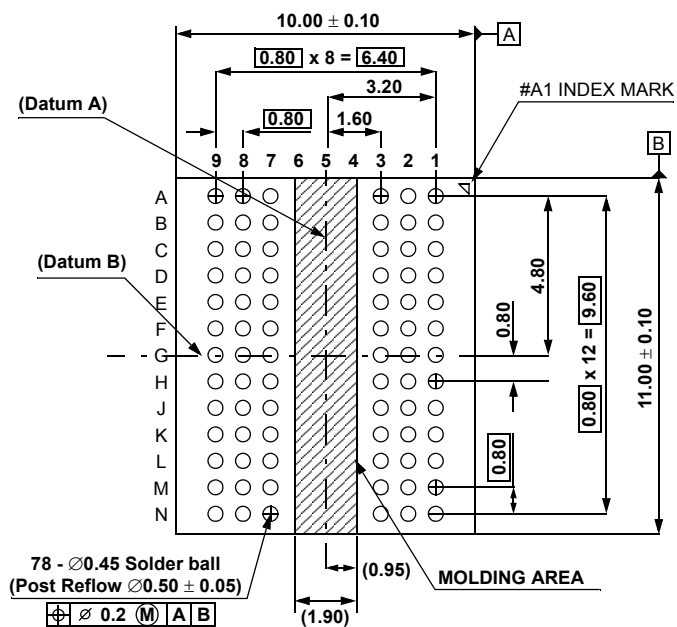
- Populated ball
+ Ball not populated

Top view
(See the balls through the package)

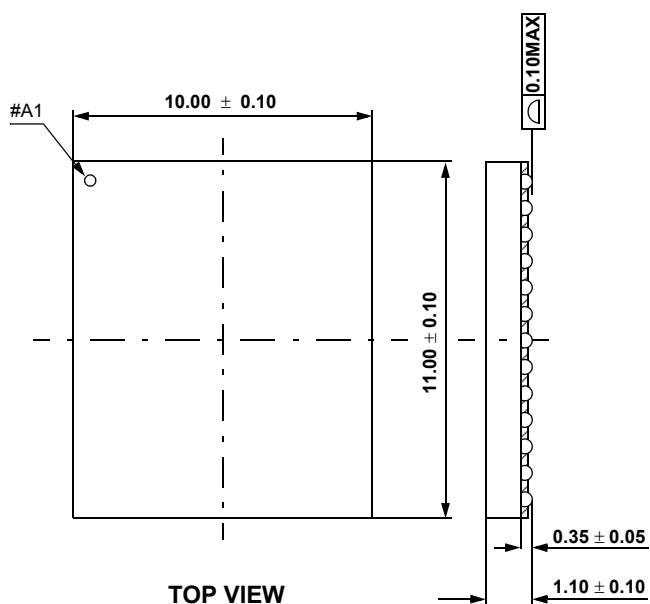
	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	●	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	●
M	●	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	●

3.3 FBGA Package Dimension (x4/x8)

Units : Millimeters



BOTTOM VIEW



TOP VIEW

4. Input/Output Functional Description

[Table 3] Input/Output function description

Symbol	Type	Function
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$. Output (read) data is referenced to the crossings of CK and $\overline{\text{CK}}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{\text{CS}}$	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ and DM/TDQS, $\overline{\text{DM/TDQS}}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{\text{TDQS}}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{\text{BC}}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Autoprecharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{\text{BC}}$	Input	Burst Chop: A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} , i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus.
DQS, ($\overline{\text{DQS}}$)	Input/Output	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL: corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL and DQSU are paired with differential signals $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ and $\overline{\text{DQSU}}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, ($\overline{\text{TDQS}}$)	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/ $\overline{\text{DQS}}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11=0 in MR1.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5V +/- 0.075V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5V +/- 0.075V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE : Input only pins (BA0-BA2, A0-A15, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, ODT and $\overline{\text{RESET}}$) do not supply termination.

5. DDR3 SDRAM Addressing

1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₃	A ₀ - A ₁₃	A ₀ - A ₁₂
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ /BC	A ₁₂ /BC	A ₁₂ /BC
Page size ^{*1}	1 KB	1 KB	2 KB

2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₄	A ₀ - A ₁₄	A ₀ - A ₁₃
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ /BC	A ₁₂ /BC	A ₁₂ /BC
Page size ^{*1}	1 KB	1 KB	2 KB

4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₅	A ₀ - A ₁₅	A ₀ - A ₁₄
Column Address	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉	A ₀ - A ₉
BC switch on the fly	A ₁₂ /BC	A ₁₂ /BC	A ₁₂ /BC
Page size ^{*1}	1 KB	1 KB	2 KB

8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Bank	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A ₁₀ /AP	A ₁₀ /AP	A ₁₀ /AP
Row Address	A ₀ - A ₁₅	A ₀ - A ₁₅	A ₀ - A ₁₅
Column Address	A ₀ - A ₉ , A ₁₁ , A ₁₃	A ₀ - A ₉ , A ₁₁	A ₀ - A ₉
BC switch on the fly	A ₁₂ /BC	A ₁₂ /BC	A ₁₂ /BC
Page size ^{*1}	2 KB	2 KB	2 KB

NOTE 1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.

Page size is per bank, calculated as follows: $\text{page size} = 2^{\text{COLBITS}} \times \text{ORG} \div 8$
 where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

6. Absolute Maximum Ratings

6.1 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE :

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC standard.
- V_{DD} and V_{DDQ} must be within 300mV of each other at all times; and V_{REF} must be not greater than $0.6 \times V_{DDQ}$. When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

6.2 DRAM Component Operating Temperature Range

[Table 5] Temperature Range

Symbol	Parameter	rating	Unit	NOTE
T_{OPER}	Operating Temperature Range	0 to 95	°C	1, 2, 3

NOTE :

- Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
- Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the refresh interval t_{REFI} to 3.9us.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_b and MR2 A7 = 1_b), in this case I_{DD6} current can be increased around 10~20% than normal Temperature range.

7. AC & DC Operating Conditions

7.1 Recommended DC operating Conditions (SSTL_1.5)

[Table 6] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

NOTE :

- Under all conditions V_{DDQ} must be less than or equal to V_{DD} .
- V_{DDQ} tracks with V_{DD} . AC parameters are measured with V_{DD} and V_{DDQ} tied together.

8. AC & DC Input Measurement Levels

8.1 AC & DC Logic input levels for single-ended signals

[Table 7] Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		DDR3-1866		Unit	NOTE
		Min.	Max.	Min.	Max.		
$V_{IH,CA}(DC100)$	DC input logic high	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	mV	1,5
$V_{IL,CA}(DC100)$	DC input logic low	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	mV	1,6
$V_{IH,CA}(AC175)$	AC input logic high	$V_{REF} + 175$	Note 2	-	-	mV	1,2,7
$V_{IL,CA}(AC175)$	AC input logic low	Note 2	$V_{REF} - 175$	-	-	mV	1,2,8
$V_{IH,CA}(AC150)$	AC input logic high	$V_{REF} + 150$	Note 2	-	-	mV	1,2,7
$V_{IL,CA}(AC150)$	AC input logic low	Note 2	$V_{REF} - 150$	-	-	mV	1,2,8
$V_{IH,CA}(AC135)$	AC input logic high	-	-	$V_{REF} + 135$	Note 2	mV	1,2,7
$V_{IL,CA}(AC135)$	AC input logic low	-	-	Note 2	$V_{REF} - 135$	mV	1,2,8
$V_{IH,CA}(AC125)$	AC input logic high	-	-	$V_{REF} + 125$	Note 2	mV	1,2,7
$V_{IL,CA}(AC125)$	AC input logic low	-	-	Note 2	$V_{REF} - 125$	mV	1,2,8
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3,4

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFCA}(DC)$
- See 'Overshoot/Undershoot Specification' on page 19.
- The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF}(DC)$ by more than $\pm 1\% V_{DD}$ (for reference : approx. $\pm 15mV$)
- For reference : approx. $V_{DD}/2 \pm 15mV$
- $V_{IH}(dc)$ is used as a simplified symbol for $V_{IH,CA}(DC100)$
- $V_{IL}(dc)$ is used as a simplified symbol for $V_{IL,CA}(DC100)$
- $V_{IH}(ac)$ is used as a simplified symbol for $V_{IH,CA}(AC175)$ and $V_{IH,CA}(AC150)$; $V_{IH,CA}(AC175)$ value is used when $V_{REF} + 175mV$ is referenced and $V_{IH,CA}(AC150)$ value is used when $V_{REF} + 150mV$ is referenced.
- $V_{IL}(ac)$ is used as a simplified symbol for $V_{IL,CA}(AC175)$ and $V_{IL,CA}(AC150)$; $V_{IL,CA}(AC175)$ value is used when $V_{REF} - 175mV$ is referenced and $V_{IL,CA}(AC150)$ value is used when $V_{REF} - 150mV$ is referenced.

[Table 8] Single-ended AC & DC input levels for DQ and DM

Symbol	Parameter	DDR3-800/1066		DDR3-1333/1600		DDR3-1866		Unit	NOTE
		Min.	Max.	Min.	Max.	Min.	Max.		
$V_{IH,DQ}(DC100)$	DC input logic high	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	$V_{REF} + 100$	V_{DD}	mV	1,5
$V_{IL,DQ}(DC100)$	DC input logic low	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	V_{SS}	$V_{REF} - 100$	mV	1,6
$V_{IH,DQ}(AC175)$	AC input logic high	$V_{REF} + 175$	NOTE 2	-	-	-	-	mV	1,2,7
$V_{IL,DQ}(AC175)$	AC input logic low	NOTE 2	$V_{REF} - 175$	-	-	-	-	mV	1,2,8
$V_{IH,DQ}(AC150)$	AC input logic high	$V_{REF} + 150$	NOTE 2	$V_{REF} + 150$	NOTE 2	-	-	mV	1,2,7
$V_{IL,DQ}(AC150)$	AC input logic low	NOTE 2	$V_{REF} - 150$	NOTE 2	$V_{REF} - 150$	-	-	mV	1,2,8
$V_{IH,DQ}(AC135)$	AC input logic high	-	-	-	-	$V_{REF} + 135$	NOTE 2	mV	1,2,7
$V_{IL,DQ}(AC135)$	AC input logic low	-	-	-	-	NOTE 2	$V_{REF} - 135$	mV	1,2,8
$V_{REFDQ}(DC)$	Reference Voltage for DQ, DM inputs	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	$0.49 \cdot V_{DD}$	$0.51 \cdot V_{DD}$	V	3,4

NOTE :

- For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFDQ}(DC)$
- See 'Overshoot/Undershoot Specification' on page 19.
- The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF}(DC)$ by more than $\pm 1\% V_{DD}$ (for reference : approx. $\pm 15mV$)
- For reference : approx. $V_{DD}/2 \pm 15mV$
- $V_{IH}(dc)$ is used as a simplified symbol for $V_{IH,DQ}(DC100)$
- $V_{IL}(dc)$ is used as a simplified symbol for $V_{IL,DQ}(DC100)$
- $V_{IH}(ac)$ is used as a simplified symbol for $V_{IH,DQ}(AC175)$, $V_{IH,DQ}(AC150)$; $V_{IH,DQ}(AC175)$ value is used when $V_{REF} + 175mV$ is referenced, $V_{IH,DQ}(AC150)$ value is used when $V_{REF} + 150mV$ is referenced.
- $V_{IL}(ac)$ is used as a simplified symbol for $V_{IL,DQ}(AC175)$, $V_{IL,DQ}(AC150)$; $V_{IL,DQ}(AC175)$ value is used when $V_{REF} - 175mV$ is referenced, $V_{IL,DQ}(AC150)$ value is used when $V_{REF} - 150mV$ is referenced.

8.2 V_{REF} Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 7 on page 12. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than $\pm 1\% V_{DD}$.

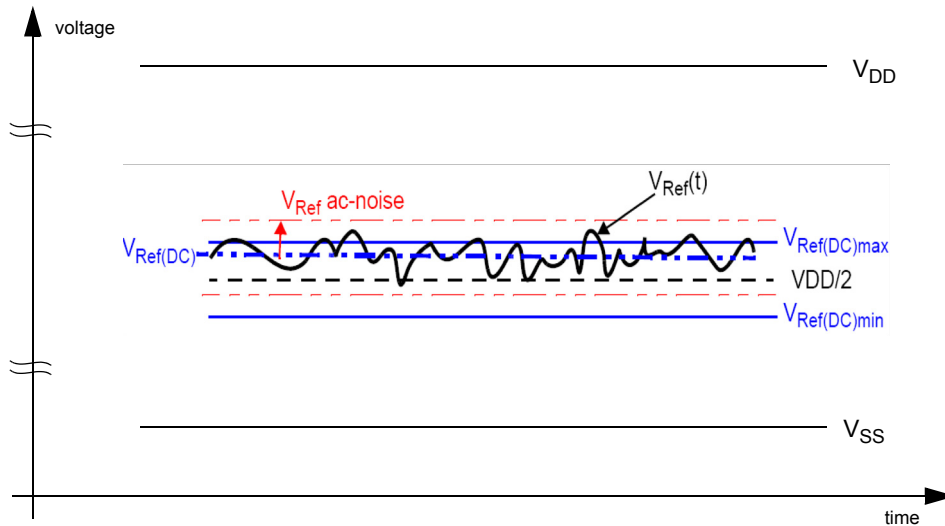


Figure 1. Illustration of $V_{REF}(DC)$ tolerance and V_{REF} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF} .

" V_{REF} " shall be understood as $V_{REF}(DC)$, as defined in Figure 1.

This clarifies, that dc-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} ac-noise. Timing and voltage effects due to ac-noise on V_{REF} up to the specified limit ($\pm 1\%$ of V_{DD}) are included in DRAM timings and their associated deratings.

8.3 AC & DC Logic Input Levels for Differential Signals

8.3.1 Differential signals definition

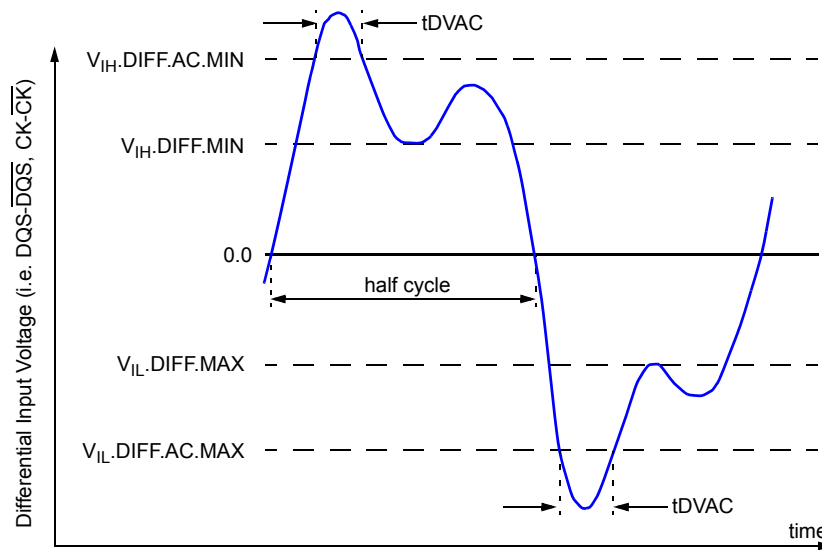


Figure 2. Definition of differential ac-swing and "time above ac level" tDVAC

8.3.2 Differential swing requirement for clock (CK - $\overline{\text{CK}}$) and strobe (DQS - $\overline{\text{DQS}}$)

[Table 9] Differential AC & DC Input Levels

Symbol	Parameter	DDR3-800/1066/1333/1600/1866		unit	NOTE
		min	max		
V_{IHdiff}	differential input high	+0.2	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.2	V	1
$V_{IHdiff}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

- NOTE :**
- Used to define a differential signal slew-rate.
 - for CK - $\overline{\text{CK}}$ use $V_{IH}/V_{IL}(AC)$ of ADD/CMD and V_{REFCA} ; for DQS - $\overline{\text{DQS}}$, DQSL - $\overline{\text{DQSL}}$, DQSU - $\overline{\text{DQSU}}$ use $V_{IH}/V_{IL}(AC)$ of DQs and V_{REFDQ} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
 - These values are not defined, however they single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "overshoot and Undershoot Specification"

[Table 10] Allowed time before ringback (tDVAC) for CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$

Slew Rate [V/ns]	tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 350mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 300mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 270mV$		tDVAC [ps] @ $ V_{IH/Ldiff}(AC) = 250mV$	
	min	max	min	max	min	max	min	max
> 4.0	75	-	175	-	TBD	-	TBD	-
4.0	57	-	170	-	TBD	-	TBD	-
3.0	50	-	167	-	TBD	-	TBD	-
2.0	38	-	163	-	TBD	-	TBD	-
1.8	34	-	162	-	TBD	-	TBD	-
1.6	29	-	161	-	TBD	-	TBD	-
1.4	22	-	159	-	TBD	-	TBD	-
1.2	13	-	155	-	TBD	-	TBD	-
1.0	0	-	150	-	TBD	-	TBD	-
< 1.0	0	-	150	-	TBD	-	TBD	-

8.3.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, or $\overline{\text{DQSU}}$) has also to comply with certain requirements for single-ended signals.

CK and $\overline{\text{CK}}$ have to approximately reach $V_{\text{SEHmin}} / V_{\text{SELmax}}$ [approximately equal to the ac-levels $\{V_{\text{IH}}(\text{AC}) / V_{\text{IL}}(\text{AC})\}$ for ADD/CMD signals] in every half-cycle.

DQS, DQSL, DQSU, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$ have to reach $V_{\text{SEHmin}} / V_{\text{SELmax}}$ [approximately the ac-levels $\{V_{\text{IH}}(\text{AC}) / V_{\text{IL}}(\text{AC})\}$ for DQ signals] in every half-cycle proceeding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if $V_{\text{IH150}}(\text{AC})/V_{\text{IL150}}(\text{AC})$ is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{\text{CK}}$.

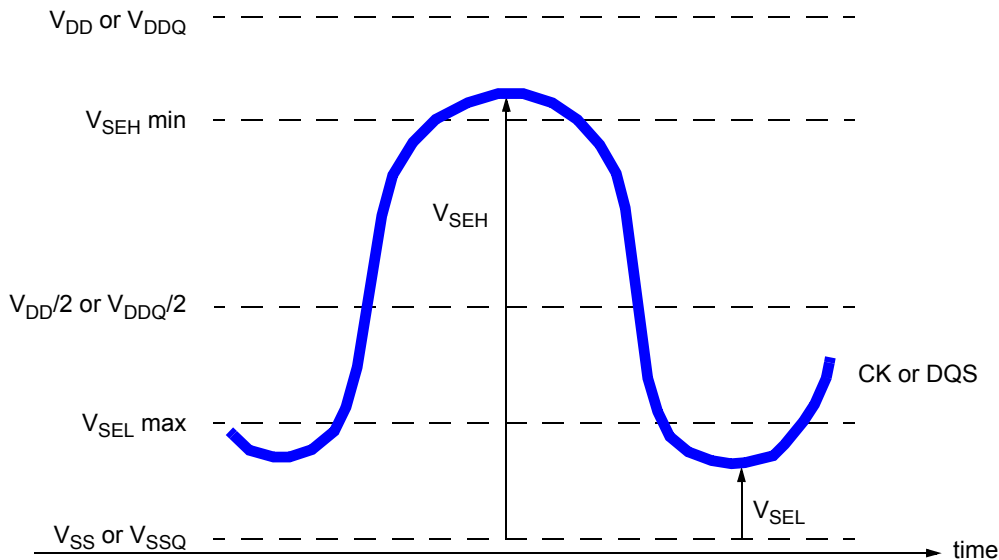


Figure 3. Single-ended requirement for differential signals

Note that while ADD/CMD and DQ signal requirements are with respect to V_{REF} , the single-ended components of differential signals have a requirement with respect to $V_{\text{DD}}/2$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SELmax} , V_{SEHmin} has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 11] Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{\text{CK}}$, $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, or $\overline{\text{DQSU}}$

Symbol	Parameter	DDR3-1066/1333/1600/1866		Unit	NOTE
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	$(V_{\text{DD}}/2)+0.175$	NOTE3	V	1, 2
	Single-ended high-level for CK, $\overline{\text{CK}}$	$(V_{\text{DD}}/2)+0.175$	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for strobes	NOTE3	$(V_{\text{DD}}/2)-0.175$	V	1, 2
	Single-ended low-level for CK, $\overline{\text{CK}}$	NOTE3	$(V_{\text{DD}}/2)-0.175$	V	1, 2

NOTE :

- For CK, $\overline{\text{CK}}$ use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of ADD/CMD; for strobes (DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$) use $V_{\text{IH}}/V_{\text{IL}}(\text{AC})$ of DQs.
- $V_{\text{IH}}(\text{AC})/V_{\text{IL}}(\text{AC})$ for DQs is based on V_{REFDQ} ; $V_{\text{IH}}(\text{AC})/V_{\text{IL}}(\text{AC})$ for ADD/CMD is based on V_{REFCA} ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
- These values are not defined, however the single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits ($V_{\text{IH}}(\text{DC})$ max, $V_{\text{IL}}(\text{DC})$ min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specification"

8.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid level between of V_{DD} and V_{SS} .

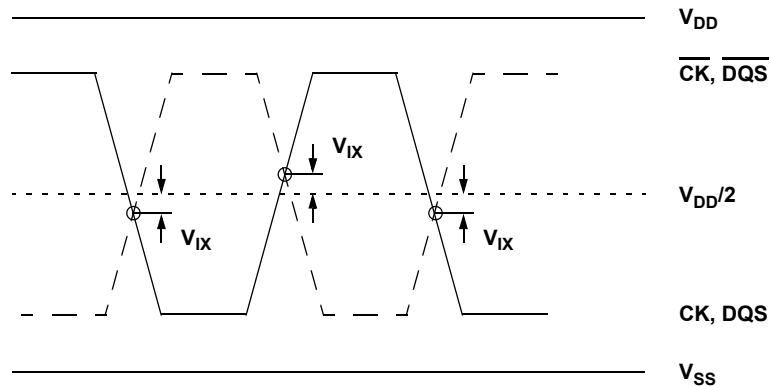


Figure 4. VIX Definition

[Table 12] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800/1066/1333/1600/1866		Unit	NOTE
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, $\overline{\text{CK}}$	-150	150	mV	
		-175	175	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, $\overline{\text{DQS}}$	-150	150	mV	

NOTE :

- Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{\text{CK}}$ are monotonic, have a single-ended swing V_{SEL} / V_{SEH} of at least $V_{DD}/2 \pm 250$ mV, and the differential slew rate of CK- $\overline{\text{CK}}$ is larger than 3 V/ ns. Refer to Table 11 on page 15 for V_{SEL} and V_{SEH} standard values.
- The relation between V_{IX} Min/Max and V_{SEL}/V_{SEH} should satisfy following.
 $(V_{DD}/2) + V_{IX}(\text{Min}) - V_{SEL} \geq 25\text{mV}$
 $V_{SEH} - ((V_{DD}/2) + V_{IX}(\text{Max})) \geq 25\text{mV}$

8.5 Slew rate definition for Differential Input Signals

See 14.3 "Address/Command Setup, Hold and Derating :" on page 48 for single-ended slew rate definitions for address and command signals.
 See 14.4 "Data Setup, Hold and Slew Rate Derating :" on page 54 for single-ended slew rate definitions for data signals.

8.6 Slew rate definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) are defined and measured as shown in Table 13 and Figure 5.

[Table 13] Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\Delta T_{Rdiff}}$
Differential input slew rate for falling edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\Delta T_{Fdiff}}$

NOTE :

The differential signal (i.e. CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$) must be linear between these thresholds.

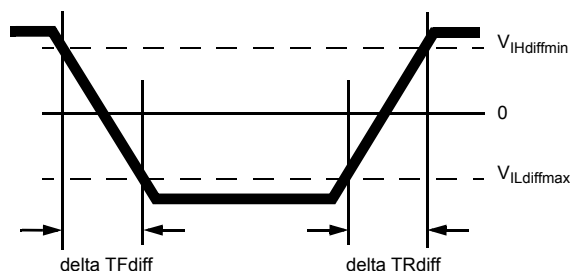


Figure 5. Differential Input Slew Rate definition for DQS, $\overline{\text{DQS}}$, and CK, $\overline{\text{CK}}$

9. AC & DC Output Measurement Levels

9.1 Single-ended AC & DC Output Levels

[Table 14] Single-ended AC & DC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600/1866	Units	NOTE
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC output low measurement level (for output SR)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

NOTE : 1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$.

9.2 Differential AC & DC Output Levels

[Table 15] Differential AC & DC output levels

Symbol	Parameter	DDR3-800/1066/1333/1600/1866	Units	NOTE
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	$+0.2 \times V_{DDQ}$	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	$-0.2 \times V_{DDQ}$	V	1

NOTE : 1. The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

9.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single ended signals as shown in Table 16 and Figure 6.

[Table 16] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TRse}$
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TFse}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 17] Single-ended output slew rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	2.5	5 ¹⁾	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

se : Single-ended Signals

For Ron = RZQ/7 setting

NOTE : 1) In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

- Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
- Case_2 is defined for a single DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

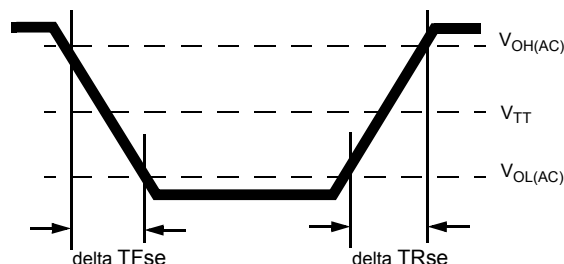


Figure 6. Single-ended Output Slew Rate Definition

9.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OHdiff}(AC)$ for differential signals as shown in Table 18 and Figure 7.

[Table 18] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$\frac{V_{OHdiff}(AC) - V_{OLdiff}(AC)}{\Delta TR_{diff}}$
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$\frac{V_{OHdiff}(AC) - V_{OLdiff}(AC)}{\Delta TF_{diff}}$

NOTE : Output slew rate is verified by design and characterization, and may not be subject to production test.

[Table 19] Differential output slew rate

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	5	10	5	10	5	10	5	10	5	12	V/ns

Description : SR : Slew Rate

Q : Query Output (like in DQ, which stands for Data-in, Query-Output)

diff : Differential Signals

For Ron = RZQ/7 setting

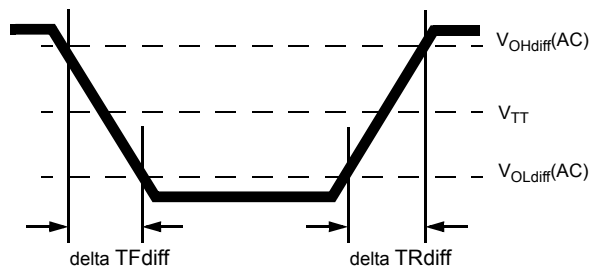


Figure 7. Differential Output Slew Rate Definition

9.5 Reference Load for AC Timing and Output Slew Rate

Figure 8 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

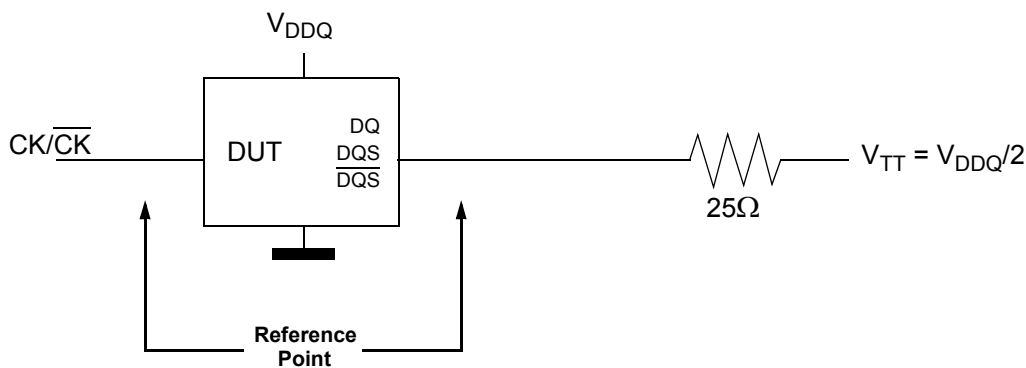


Figure 8. Reference Load for AC Timing and Output Slew Rate

9.6 Overshoot/Undershoot Specification

9.6.1 Address and Control Overshoot and Undershoot specifications

[Table 20] AC overshoot/undershoot specification for Address and Control pins (A0-A12, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT)

Parameter	Specification					Unit
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	
Maximum peak amplitude allowed for overshoot area (See Figure 9)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum peak amplitude allowed for undershoot area (See Figure 9)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum overshoot area above V_{DD} (See Figure 9)	0.67V-ns	0.5V-ns	0.4V-ns	0.33V-ns	0.28V-ns	V-ns
Maximum undershoot area below V_{SS} (See Figure 9)	0.67V-ns	0.5V-ns	0.4V-ns	0.33V-ns	0.28V-ns	V-ns

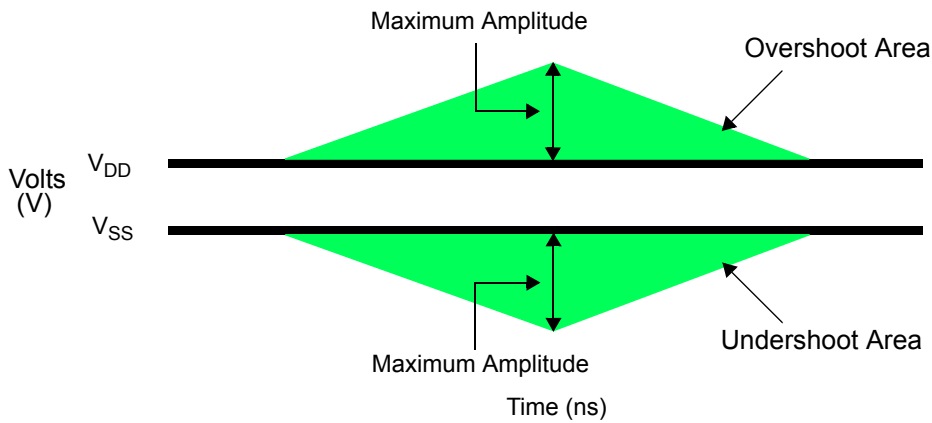


Figure 9. Address and Control Overshoot and Undershoot Definition

9.6.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

[Table 21] AC overshoot/undershoot specification for Clock, Data, Strobe and Mask (DQ, DQS, $\overline{DQS}$, DM, CK, $\overline{CK}$)

Parameter	Specification					Unit
	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	
Maximum peak amplitude allowed for overshoot area (See Figure 10)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum peak amplitude allowed for undershoot area (See Figure 10)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum overshoot area above V_{DDQ} (See Figure 10)	0.25V-ns	0.19V-ns	0.15V-ns	0.13V-ns	0.11V-ns	V-ns
Maximum undershoot area below V_{SSQ} (See Figure 10)	0.25V-ns	0.19V-ns	0.15V-ns	0.13V-ns	0.11V-ns	V-ns

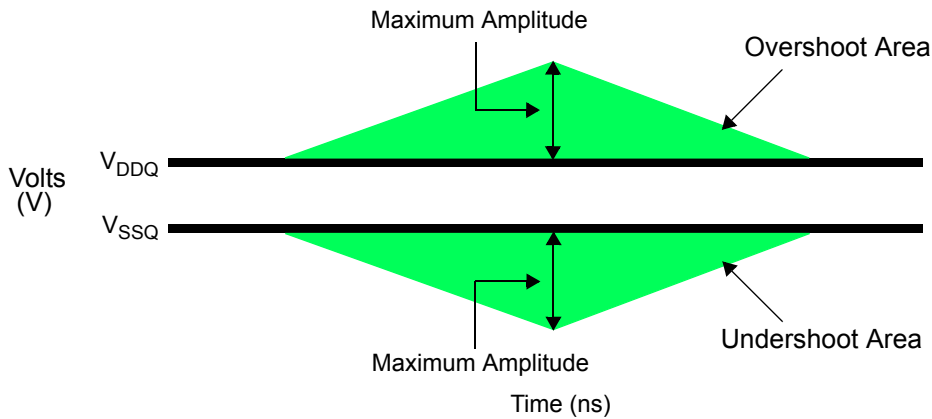


Figure 10. Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

9.7 34ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown below. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:

$$RON_{34} = RZQ/7 \text{ (Nominal 34.3ohms +/- 10% with nominal RZQ=240ohm)}$$

The individual Pull-up and Pull-down resistors (RONpu and RONpd) are defined as follows

$$RON_{pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RON_{pd} \text{ is turned off}$$

$$RON_{pd} = \frac{V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RON_{pu} \text{ is turned off}$$

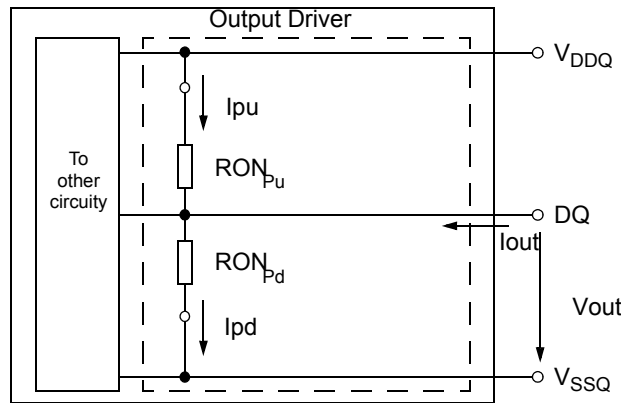


Figure 11. Output Driver : Definition of Voltages and Currents

[Table 22] Output Driver DC Electrical Characteristics, assuming RZQ=240ohms ;
entire operating temperature range ; after proper ZQ calibration

RONnom	Resistor	Vout	Min	Nom	Max	Units	NOTE
34Ohms	RON34pd	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/7	1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
	RON34pu	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.1		1,2,3
40Ohms	RON40pd	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.1	RZQ/6	1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
	RON40pu	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.4		1,2,3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1		1,2,3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.1		1,2,3
Mismatch between Pull-up and Pull-down, MMpupd		$V_{OMdc} = 0.5 \times V_{DDQ}$	-10		10	%	1,2,4

NOTE :

- The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
- The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
- Pull-down and pull-up output driver impedance are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$
- Measurement definition for mismatch between pull-up and pull-down, MMpupd: Measure RONpu and RONpd. both at $0.5 \times V_{DDQ}$:

$$MMpupd = \frac{RON_{pu} - RON_{pd}}{RON_{nom}} \times 100$$

9.7.1 Output Drive Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table 23 and Table 24.

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$

* dR_{ONdT} and dR_{ONdV} are not subject to production test but are verified by design and characterization

[Table 23] Output Driver Sensitivity Definition

	Min	Max	Units
$RONPU@V_{OHDC}$	$0.6 - dR_{ONdTH} * \Delta T - dR_{ONdVH} * \Delta V $	$1.1 + dR_{ONdTH} * \Delta T + dR_{ONdVH} * \Delta V $	RZQ/7
$RON@V_{OMDC}$	$0.9 - dR_{ONdTM} * \Delta T - dR_{ONdVM} * \Delta V $	$1.1 + dR_{ONdTM} * \Delta T + dR_{ONdVM} * \Delta V $	RZQ/7
$RONPD@VOLDC$	$0.6 - dR_{ONdTL} * \Delta T - dR_{ONdVL} * \Delta V $	$1.1 + dR_{ONdTL} * \Delta T + dR_{ONdVL} * \Delta V $	RZQ/7

[Table 24] Output Driver Voltage and Temperature Sensitivity

Speed Bin	DDR3-800/1066/1333		DDR3-1600/1866		Units
	Min	Max	Min	Max	
dR_{ONdTM}	0	1.5	0	1.5	%/°C
dR_{ONdVM}	0	0.15	0	0.13	%/mV
dR_{ONdTL}	0	1.5	0	1.5	%/°C
dR_{ONdVL}	0	0.15	0	0.13	%/mV
dR_{ONdTH}	0	1.5	0	1.5	%/°C
dR_{ONdVH}	0	0.15	0	0.13	%/mV

9.8 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register.

ODT is applied to the DQ, DM, DQS/DQS and TDQS, TDQS (x8 devices only) pins.

A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTT_{pu} and RTT_{pd}) are defined as follows :

$$RTT_{pu} = \frac{V_{DDQ} - V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RTT_{pd} \text{ is turned off}$$

$$RTT_{pd} = \frac{V_{OUT}}{|I_{out}|} \quad \text{under the condition that } RTT_{pu} \text{ is turned off}$$

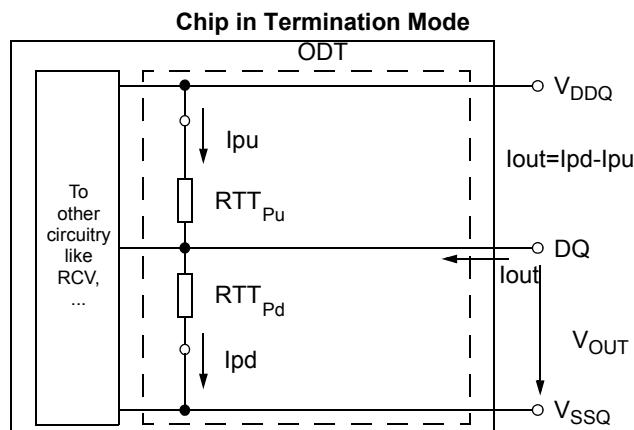


Figure 12. On-Die Termination : Definition of Voltages and Currents

9.8.1 ODT DC Electrical Characteristics

Table 25 provides an overview of the ODT DC electrical characteristics. The values for $RTT_{60pd120}$, $RTT_{60pu120}$, $RTT_{120pd240}$, $RTT_{120pu240}$, RTT_{40pd80} , RTT_{40pu80} , RTT_{30pd60} , RTT_{30pu60} , RTT_{20pd40} , RTT_{20pu40} are not specification requirements, but can be used as design guide lines:

[Table 25] ODT DC Electrical Characteristics, assuming $RZQ=240\Omega \pm 1\%$ entire operating temperature range; after proper ZQ calibration

MR1 (A9,A6,A2)	RTT	RESISTOR	Vout	Min	Nom	Max	Unit	NOTE
(0,1,0)	120 ohm	RTT _{120pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ}	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ}	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ}	1,2,3,4
		RTT _{120pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ}	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ}	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ}	1,2,3,4
		RTT ₁₂₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /2	1,2,5
(0,0,1)	60 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /2	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /2	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /2	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /2	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /2	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /2	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /4	1,2,5
(0,1,1)	40 ohm	RTT _{40pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /3	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /3	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /3	1,2,3,4
		RTT _{40pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /3	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /3	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /3	1,2,3,4
		RTT ₄₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /6	1,2,5
(1,0,1)	30 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /4	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /4	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /4	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /4	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /4	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /4	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /8	1,2,5
(1,0,0)	20 ohm	RTT _{60pd240}	V _{OL} (DC) 0.2XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /6	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /6	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /6	1,2,3,4
		RTT _{60pu240}	V _{OL} (DC) 0.2XV _{DDQ}	0.9	1.0	1.4	R _{ZQ} /6	1,2,3,4
			0.5XV _{DDQ}	0.9	1.0	1.1	R _{ZQ} /6	1,2,3,4
			V _{OH} (DC) 0.8XV _{DDQ}	0.6	1.0	1.1	R _{ZQ} /6	1,2,3,4
		RTT ₆₀	V _{IL} (AC) to V _{IH} (AC)	0.9	1.0	1.6	R _{ZQ} /12	1,2,5
Deviation of V _M w.r.t V _{DDQ} /2, ΔVM				-5		5	%	1,2,5,6

NOTE :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5XV_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2XV_{DDQ}$ and $0.8XV_{DDQ}$.
4. Not a specification requirement, but a design guide line
5. Measurement definition for RTT:
Apply $V_{IH}(AC)$ to pin under test and measure current $I(V_{IH}(AC))$, then apply $V_{IL}(AC)$ to pin under test and measure current $I(V_{IL}(AC))$ respectively

$$RTT = \frac{V_{IH}(AC) - V_{IL}(AC)}{I(V_{IH}(AC)) - I(V_{IL}(AC))}$$

6. Measurement definition for V_M and ΔV_M : Measure voltage (V_M) at test pin (midpoint) with no load

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1 \right) \times 100$$

9.8.2 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to table below

$\Delta T = T - T(@\text{calibration})$; $\Delta V = V_{DDQ} - V_{DDQ}(@\text{calibration})$; $V_{DD} = V_{DDQ}$

[Table 26] ODT Sensitivity Definition

	Min	Max	Units
RTT	$0.9 - dR_{TTdT} * \Delta T - dR_{TTdV} * \Delta V $	$1.6 + dR_{TTdT} * \Delta T + dR_{TTdV} * \Delta V $	RZQ/2,4,6,8,12

[Table 27] ODT Voltage and Temperature Sensitivity

	Min	Max	Units
dR_{TTdT}	0	1.5	%/°C
dR_{TTdV}	0	0.15	%/mV

NOTE : These parameters may not be subject to production test. They are verified by design and characterization.

9.9 ODT Timing Definitions

9.9.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 13.

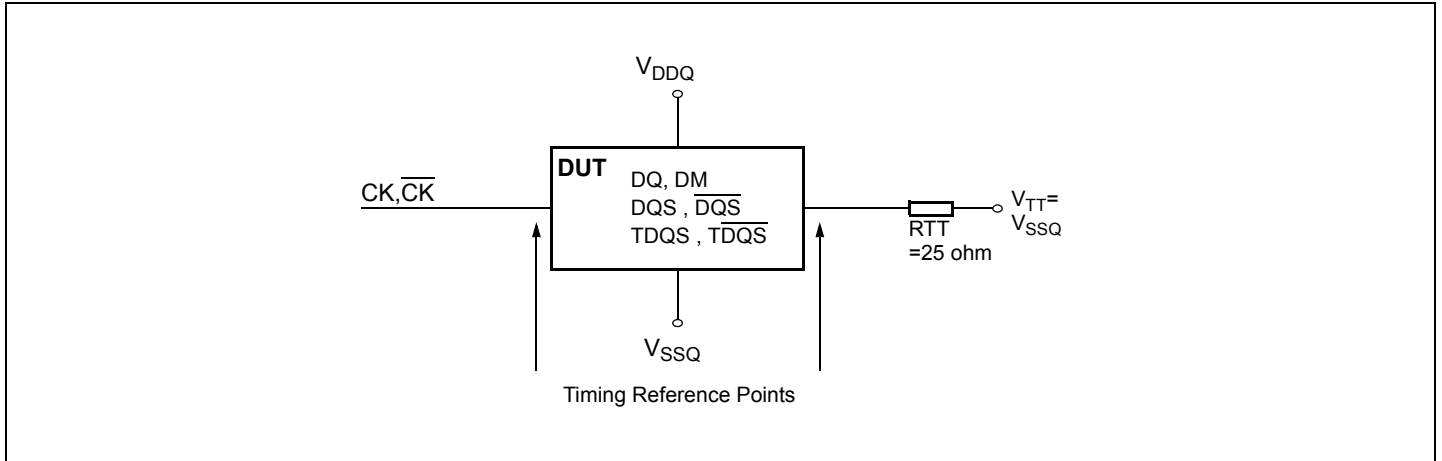


Figure 13. ODT Timing Reference Load

9.9.2 ODT Timing Definitions

Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in Table 28 and subsequent figures. Measurement reference settings are provided in Table 29.

[Table 28] ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 14
tAONPD	Rising edge of CK - $\overline{\text{CK}}$ with ODT being first registered high	Extrapolated point at V_{SSQ}	Figure 15
tAOF	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLoff	End point: Extrapolated point at $V_{\text{RTT_Nom}}$	Figure 16
tAOFPD	Rising edge of CK - $\overline{\text{CK}}$ with ODT being first registered low	End point: Extrapolated point at $V_{\text{RTT_Nom}}$	Figure 17
tADC	Rising edge of CK - $\overline{\text{CK}}$ defined by the end point of ODTLcwn, ODTLcwn4 of ODTLcwn8	End point: Extrapolated point at $V_{\text{RTT_Wr}}$ and $V_{\text{RTT_Nom}}$ respectively	Figure 18

[Table 29] Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V _{sw1} [V]	V _{sw2} [V]	NOTE
tAON	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAONPD	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAOF	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tAOFPD	$R_{\text{ZQ}}/4$	NA	0.05	0.10	
	$R_{\text{ZQ}}/12$	NA	0.10	0.20	
tADC	$R_{\text{ZQ}}/12$	$R_{\text{ZQ}}/2$	0.20	0.30	

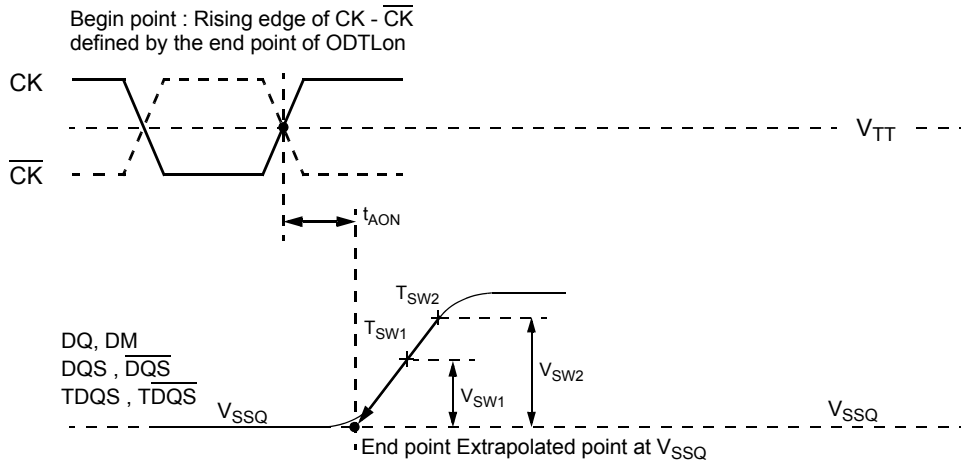


Figure 14. Definition of t_{AON}

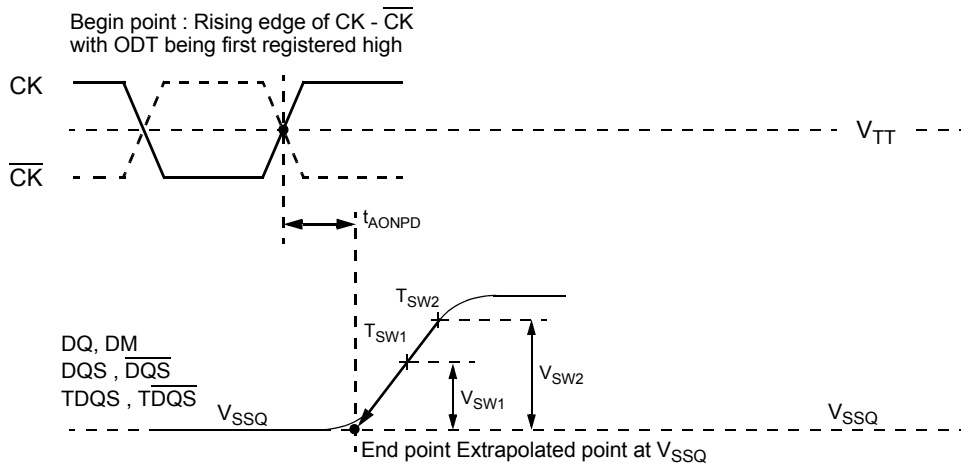


Figure 15. Definition of t_{AONPD}

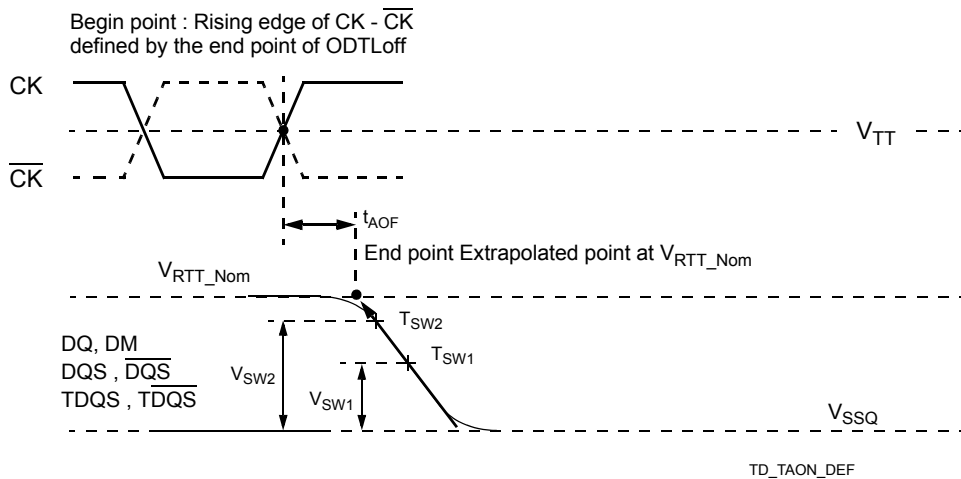


Figure 16. Definition of t_{AOF}

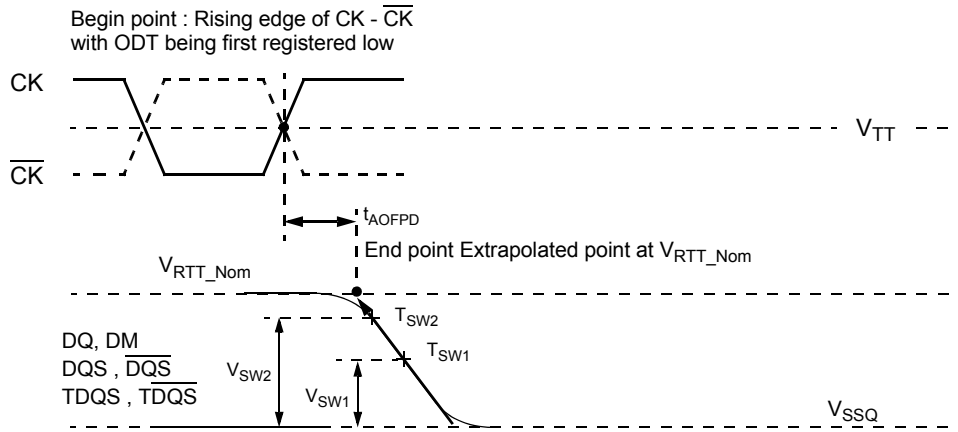


Figure 17. Definition of t_{AOFDP}

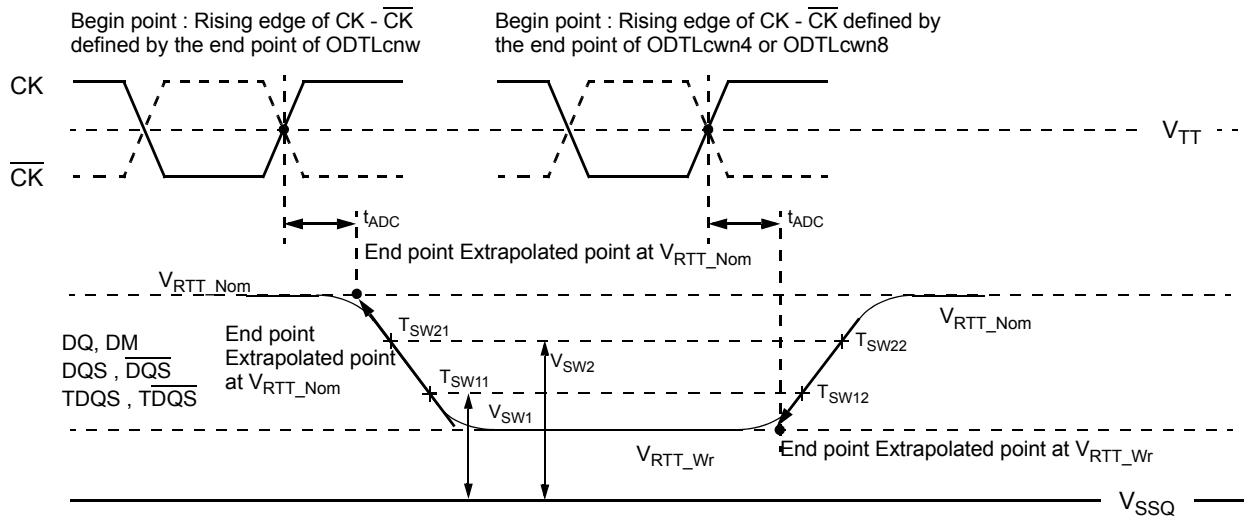


Figure 18. Definition of t_{ADC}

10. IDD Current Measure Method

10.1 IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 19 shows the setup and test load for IDD and IDDQ measurements.

- **IDD currents** (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all V_{DD} balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.

- **IDDQ currents** (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all V_{DDQ} balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Attention : IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 20. In DRAM module application, IDDQ cannot be measured separately since V_{DD} and V_{DDQ} are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply :

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC}(max)$.

- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC}(min)$.

- "FLOATING" is defined as inputs are $V_{REF} = V_{DD} / 2$.

- "Timing used for IDD and IDDQ Measured - Loop Patterns" are provided in Table 30

- "Basic IDD and IDDQ Measurement Conditions" are described in Table 31

- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 32 on page 31 through Table 39.

- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting

RON = RZQ/7 (34 Ohm in MR1);

Qoff = 0B (Output Buffer enabled in MR1);

RTT_Nom = RZQ/6 (40 Ohm in MR1);

RTT_Wr = RZQ/2 (120 Ohm in MR2);

TDQS Feature disabled in MR1

- **Attention** : The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Define $\underline{D} = \{CS, RAS, CAS, WE\} := \{HIGH, LOW, LOW, LOW\}$

- Define $\underline{D} = \{CS, RAS, CAS, WE\} := \{HIGH, HIGH, HIGH, HIGH\}$

- RESET Stable time is : During a Cold Boot RESET (Initialization), current reading is valid once power is stable and RESET has been LOW for 1ms;
During Warm Boot RESET(while operating), current reading is valid after RESET has been LOW for 200ns + tRFC

[Table 30] Timing used for IDD and IDDQ Measured - Loop Patterns

Parameter	Bin	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	Unit
		6-6-6	7-7-7	9-9-9	11-11-11	13-13-13	
tCKmin(IDD)		2.5	1.875	1.5	1.25	1.07	ns
CL(IDD)		6	7	9	11	13	nCK
tRCDmin(IDD)		6	7	9	11	13	nCK
tRCmin(IDD)		21	27	33	39	45	nCK
tRASmin(IDD)		15	20	24	28	32	nCK
tRPmin(IDD)		6	7	9	11	13	nCK
tFAW(IDD)	x4/x8	16	20	20	24	26	nCK
	x16	20	27	30	32	33	nCK
tRRD(IDD)	x4/x8	4	4	4	5	5	nCK
	x16	4	6	5	6	6	nCK
tRFC(IDD) - 512Mb		36	48	60	72	85	nCK
tRFC(IDD) - 1Gb		44	59	74	88	103	nCK
tRFC(IDD) - 2Gb		64	86	107	128	150	nCK
tRFC(IDD) - 4Gb		104	139	174	208	243	nCK
tRFC(IDD) - 8Gb		140	187	234	280	328	nCK

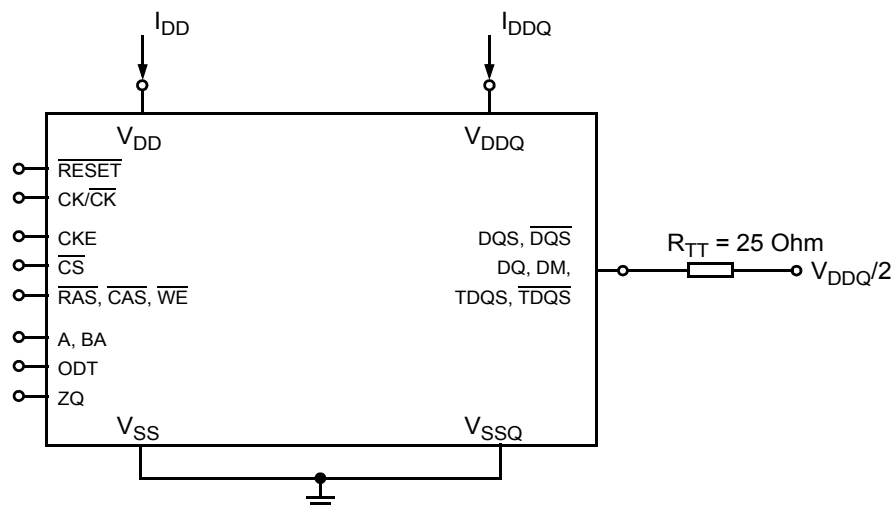


Figure 19. Measurement Setup and Test Load for IDD and IDDQ Measurements

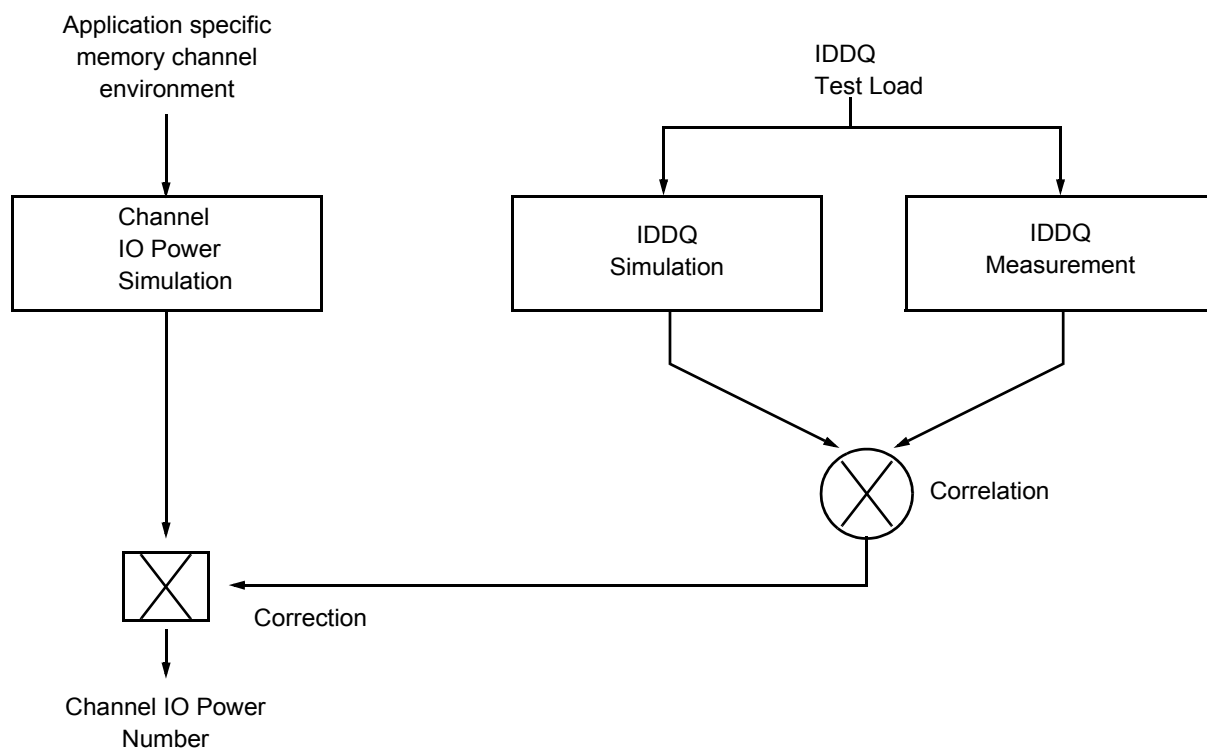


Figure 20. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 31] Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD0	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 32 on page 31 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 32); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 32
IDD1	Operating One Bank Active-Read-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling according to Table 33 on page 32 ; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 33); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 33
IDD2N	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 34 on page 32 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 34
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 35 on page 33 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: toggling according to Table 35 ; Pattern Details: see Table 35
IDDQ2NT	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2P0	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pre-charge Power Down Mode: Slow Exit ³⁾
IDD2P1	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pre-charge Power Down Mode: Fast Exit ³⁾
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 34 on page 32 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 34
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 36 on page 33 ; Data IO: seamless read data burst with different data between one burst and the next one according to Table 36 ; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7 on page 12); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 36
IDDQ4R	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 37 on page 34 ; Data IO: seamless write data burst with different data between one burst and the next one according to Table 37; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 37); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at HIGH; Pattern Details: see Table 37
IDD5B	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 38 on page 34 ; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nRFC (see Table 38); Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 38
IDD6	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled ⁴⁾ ; Self-Refresh Temperature Range (SRT): Normal ⁵⁾ ; CKE: Low; External clock: Off; CK and $\overline{\text{CK}}$: LOW; CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: 0; $\overline{\text{CS}}$, Command, Address, Bank Address, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: FLOATING

[Table 31] Basic IDD and IDDQ Measurement Conditions

Symbol	Description
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 30 on page 27 ; BL: 8 ¹⁾ ; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 39 on page 35 ; Data IO: read data bursts with different data between one burst and the next one according to Table 39 ; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 39 ; Output Buffer and RTT: Enabled in Mode Registers ²⁾ ; ODT Signal: stable at 0; Pattern Details: see Table 39
IDD8	RESET Low Current RESET : Low; External clock : off; CK and CK : LOW; CKE : FLOATING ; CS, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING

NOTE :

- 1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
- 2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
- 3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
- 4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
- 5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
- 6) Read Burst type : Nibble Sequential, set MR0 A[3]=0B

[Table 32] IDD0 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC + 0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3, 4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	
			...	repeat 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

- DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

[Table 33] IDD1 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC + 3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary												
			1*nRC + nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,..., 4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC + nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,..., 4 until 2 * nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 34] IDD2 and IDD3N Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-27	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

NOTE :

- DM must be driven Low all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
- DQ signals are MID-LEVEL.

[Table 35] IDD2NT and IDDQ2NT Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	D	1	0	0	0	0	0	00	0	0	0	0	-
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-27	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

NOTE :

1. DM must be driven Low all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

2. DQ signals are MID-LEVEL.

[Table 36] IDD4R and IDDQ4R Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}, \overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}, \overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.

2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 37] IDD4W Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
		5	5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	F	0	-
			1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1											
			2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2											
			3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3											
			4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4											
			5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5											
			6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6											
			7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7											

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to WR Commands, otherwise MID-LEVEL.
 2. Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

[Table 38] IDD5B Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	1	0	REF	0	0	0	1	0	0	00	0	0	0	0	-
			1,2	D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC - 1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

NOTE :

1. DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are MID-LEVEL.
 2. DQ signals are MID-LEVEL.

[Table 39] IDD7 Measurement - Loop Pattern¹⁾

CK/CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ²⁾
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2*nRRD-1												
		2	2 * nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3 * nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4 * nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2*nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2*nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2*nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2*nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2*nFAW + 2*nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3*nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4*nFAW - 1, if necessary												

NOTE :

- DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
- Burst Sequence driven on each DQ signal by Read Command. Outside burst operation. DQ signals are MID-LEVEL.

11. 4Gb DDR3 SDRAM B-die IDD Specification Table

[Table 40] IDD Specification for 4Gb DDR3 B-die

Symbol	1Gx4 (K4B4G0446B)				Unit	NOTE
	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866		
	7-7-7	9-9-9	11-11-11	13-13-13		
IDD0	40	40	45	TBD	mA	
IDD1	50	50	55	TBD	mA	
IDD2P0(slow exit)	15	15	15	TBD	mA	
IDD2P1(fast exit)	15	15	15	TBD	mA	
IDD2N	20	20	20	TBD	mA	
IDD2NT	20	25	25	TBD	mA	
IDDQ2NT	40	40	40	TBD	mA	
IDD2Q	20	20	20	TBD	mA	
IDD3P	20	20	20	TBD	mA	
IDD3N	30	30	30	TBD	mA	
IDD4R	65	75	85	TBD	mA	
IDDQ4R	35	35	35	TBD	mA	
IDD4W	70	80	95	TBD	mA	
IDD5B	120	145	145	TBD	mA	
IDD6	15	15	15	TBD	mA	
IDD7	130	160	165	TBD	mA	
IDD8	15	15	15	TBD	mA	

Symbol	512Mx8 (K4B4G0846B)				Unit	NOTE
	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866		
	7-7-7	9-9-9	11-11-11	13-13-13		
IDD0	40	40	45	TBD	mA	
IDD1	50	50	55	TBD	mA	
IDD2P0(slow exit)	15	15	15	TBD	mA	
IDD2P1(fast exit)	15	15	15	TBD	mA	
IDD2N	20	20	20	TBD	mA	
IDD2NT	20	25	25	TBD	mA	
IDDQ2NT	70	70	70	TBD	mA	
IDD2Q	20	20	20	TBD	mA	
IDD3P	20	20	20	TBD	mA	
IDD3N	30	30	30	TBD	mA	
IDD4R	70	85	100	TBD	mA	
IDDQ4R	50	50	50	TBD	mA	
IDD4W	75	90	110	TBD	mA	
IDD5B	120	145	145	TBD	mA	
IDD6	15	15	15	TBD	mA	
IDD7	130	170	175	TBD	mA	
IDD8	15	15	15	TBD	mA	

12. Input/Output Capacitance

[Table 41] Input/Output Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	CIO	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.3	1.4	2.2	pF	1,2,3
Input capacitance (CK and $\overline{\text{CK}}$)	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF	2,3
Input capacitance delta (CK and $\overline{\text{CK}}$)	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	0.75	1.2	pF	2,3,6
Input capacitance delta (DQS and $\overline{\text{DQS}}$)	CDDQS	0	0.2	0	0.2	0	0.15	0	0.15	0	0.15	pF	2,3,5
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-only pins)	CDI_ADD_CMD	-0.5	0.5	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	-	3	pF	2, 3, 12

- NOTE :**
- Although the DM, TDQS and $\overline{\text{TDQS}}$ pins have different functions, the loading matches DQ and DQS
 - This parameter is not subject to production test. It is verified by design and characterization.
The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{DD} , V_{DDQ} , V_{SS} , V_{SSQ} applied and all other pins floating (except the pin under test, CKE, $\overline{\text{RESET}}$ and ODT as necessary). $V_{DD}=V_{DDQ}=1.5V$, $V_{BIAS}=V_{DD}/2$ and on-die termination off.
 - This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
 - Absolute value of CCK- $\overline{\text{CCK}}$
 - Absolute value of CIO(DQS)-CIO($\overline{\text{DQS}}$)
 - CI applies to ODT, $\overline{\text{CS}}$, CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
 - CDI_CTRL applies to ODT, $\overline{\text{CS}}$ and CKE
 - CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI($\overline{\text{CLK}}$))
 - CDI_ADD_CMD applies to A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$
 - CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI($\overline{\text{CLK}}$))
 - CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO($\overline{\text{DQS}}$))
 - Maximum external load capacitance on ZQ pin: 5pF

13. Electrical Characteristics and AC timing for DDR3-800 to DDR3-1866

13.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR3 SDRAM device.

13.1.1 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left(\sum_{j=1}^N tCK_j \right) / N \quad N=200$$

13.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

13.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$\left(\sum_{j=1}^N tCH_j \right) / N \times tCK(avg) \quad N=200 \quad \left(\sum_{j=1}^N tCL_j \right) / N \times tCK(avg) \quad N=200$$

13.1.4 Definition for note for tJIT(per), tJIT(per, lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). tJIT(per) = min/max of {tCK_i-tCK(avg) where i=1 to 200}

tJIT(per) defines the single period jitter when the DLL is already locked.

tJIT(per, lck) uses the same definition for single period jitter, during the DLL locking period only.

tJIT(per) and tJIT(per, lck) are not subject to production test.

13.1.5 Definition for tJIT(cc), tJIT(cc, lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of {tCK_{i+1}-tCK_i}

tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.

tJIT(cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.

tJIT(cc) and tJIT(cc, lck) are not subject to production test.

13.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

13.2 Refresh Parameters by Device Density

[Table 42] Refresh parameters by device density

Parameter	Symbol	1Gb	2Gb	4Gb	8Gb	Units	NOTE
All Bank Refresh to active/refresh cmd time	tRFC	110	160	260	350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T _{CASE} ≤ 85 °C	7.8	7.8	7.8	μs	
		85 °C < T _{CASE} ≤ 95 °C	3.9	3.9	3.9	μs	1

NOTE :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

13.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

DDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

[Table 43] DDR3-800 Speed Bins

Speed			DDR3-800		Units	NOTE
CL-nRCD-nRP			6 - 6 - 6			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15	20	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	15	-	ns	
ACT to ACT or REF command period		tRC	52.5	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,10,11
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3
Supported CL Settings			5,6		nCK	
Supported CWL Settings			5		nCK	

[Table 44] DR3-1066 Speed Bins

Speed			DDR3-1066		Units	NOTE
CL-nRCD-nRP			7 - 7 - 7			
Parameter	Symbol	min	max			
Internal read command to first data		tAA	13.125	20	ns	
ACT to internal read or write delay time		tRCD	13.125	-	ns	
PRE command period		tRP	13.125	-	ns	
ACT to ACT or REF command period		tRC	50.625	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,5,10,11
	CWL = 6	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,5
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,9
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3
Supported CL Settings			5,6,7,8		nCK	
Supported CWL Settings			5,6		nCK	

[Table 45] DDR3-1333 Speed Bins

Speed			DDR3-1333		Units	NOTE
CL-nRCD-nRP			9 -9 - 9			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.5 (13.125) ⁹	20		ns	
ACT to internal read or write delay time	tRCD	13.5 (13.125) ⁹	-		ns	
PRE command period	tRP	13.5 (13.125) ⁹	-		ns	
ACT to ACT or REF command period	tRC	49.5 (49.125) ⁹	-		ns	
ACT to PRE command period		tRAS	36	9*tREFI	ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,6,10,11
	CWL = 6,7	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,6
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,9
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3
Supported CL Settings			5,6,7,8,9		nCK	
Supported CWL Settings			5,6,7		nCK	

[Table 46] DDR3-1600 Speed Bins

Speed			DDR3-1600		Units	NOTE
CL-nRCD-nRP			11-11-11			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.75 (13.125) ⁹	20	ns		
ACT to internal read or write delay time	tRCD	13.75 (13.125) ⁹	-	ns		
PRE command period	tRP	13.75 (13.125) ⁹	-	ns		
ACT to ACT or REF command period	tRC	48.75 (48.125) ⁹	-	ns		
ACT to PRE command period	tRAS	35	9*tREFI	ns		
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,7,10,11
	CWL = 6,7,8	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,7
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 7, 8	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,7
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,4,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,7
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
Supported CL Settings			5,6,7,8,9,10,11		nCK	
Supported CWL Settings			5,6,7,8		nCK	

[Table 47] DDR3-1866 Speed Bins

Speed			DDR3-1866		Units	NOTE
CL-nRCD-nRP			13-13-13			
Parameter	Symbol	min	max			
Internal read command to first data	tAA	13.91 (13.125) ¹²	20		ns	
ACT to internal read or write delay time	tRCD	13.91 (13.125) ¹²	-		ns	
PRE command period	tRP	13.91 (13.125) ¹²	-		ns	
ACT to ACT or REF command period	tRC	47.91 (47.125) ¹²	-		ns	
ACT to PRE command period	tRAS	34	9*tREFI		ns	
CL = 5	CWL = 5	tCK(AVG)	3.0	3.3	ns	1,2,3,4,8,10,11
	CWL = 6,7,8,9	tCK(AVG)	Reserved		ns	4
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,8
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	2.5	ns	1,2,3,4,8
	CWL = 7,8,9	tCK(AVG)	Reserved		ns	4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,8
	CWL = 7	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CWL = 8,9	tCK(AVG)	Reserved		ns	4
CL = 9	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	4
CL = 10	CWL = 5,6	tCK(AVG)	Reserved		ns	4
	CWL = 7	tCK(AVG)	1.5	<1.875	ns	1,2,3,8
	CWL = 8	tCK(AVG)	Reserved		ns	1,2,3,4,8
CL = 11	CWL = 5,6,7	tCK(AVG)	Reserved		ns	4
	CWL = 8	tCK(AVG)	1.25	1.5	ns	1,2,3,4,8
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 12	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	tCK(AVG)	Reserved		ns	4
	CWL = 9	tCK(AVG)	1.07	<1.25	ns	1,2,3,9
Supported CL Settings			5,6,7,8,9,10,11,13		nCK	
Supported CWL Settings			5,6,7,8,9		nCK	

13.3.1 Speed Bin Table Notes

Absolute Specification (T_{OPER} ; $V_{\text{DDQ}} = V_{\text{DD}} = 1.5\text{V} \pm 0.075\text{V}$);

NOTE :

1. The CL setting and CWL setting result in $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ and $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ requirements. When making a selection of $t_{\text{CK}}(\text{AVG})$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{\text{CK}}(\text{AVG})$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating $\text{CL} [\text{nCK}] = t_{\text{AA}} [\text{ns}] / t_{\text{CK}}(\text{AVG}) [\text{ns}]$, rounding up to the next "Supported CL".
3. $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ limits: Calculate $t_{\text{CK}}(\text{AVG}) = t_{\text{AA}}_{\text{MAX}} / \text{CL}_{\text{SELECTED}}$ and round the resulting $t_{\text{CK}}(\text{AVG})$ down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ corresponding to CL SELECTED.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. For devices supporting optional downshift to CL=7 and CL=9, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RP}}$ min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte 16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-1866(CL13) devices supporting downshift to DDR3-1600(CL11) or DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for t_{AAmin} (Byte16), t_{RCDmin} (Byte 18), and t_{RPmin} (Byte 20). DDR3-1600 devices supporting down binning to DDR3-1333 or DDR3-1066 should program 13.125ns in SPD byte for t_{AAmin} (Byte 16), t_{RCDmin} (Byte 18) and t_{RPmin} (Byte 20). Once t_{RP} (Byte 20) is programmed to 13.125ns, t_{RCmin} (Byte 21,23) also should be programmed accordingly. For example, 49.125ns, ($t_{\text{RASmin}} + t_{\text{RPmin}} = 36\text{ns} + 13.125\text{ns}$) for DDR3-1333 and 48.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 35\text{ns} + 13.125\text{ns}$) for DDR3-1600.
10. DDR3 800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.
11. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
12. For devices supporting optional down binning to CL=11, CL=9 and CL=7, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RPmin}}$ must be 13.125ns. SPD setting must be programmed to match. For example, DDR3-1866 devices supporting down binning to DDR3-1600 or DDR3-1333 or 1066 should program 13.125ns in SPD bytes for t_{AAmin} (byte16), t_{RCDmin} (Byte18) and t_{RPmin} (byte20). Once t_{RP} (Byte20) is programmed to 13.125ns, t_{RCmin} (Byte21,23) also should be programmed accordingly. For example, 47.125ns ($t_{\text{RASmin}} + t_{\text{RPmin}} = 34\text{ns} + 13.125\text{ns}$)

14. Timing Parameters by Speed Grade

[Table 48] Timing Parameters by Speed Bins for DDR3-800 to DDR3-1333 (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table						ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-100	100	-90	90	-80	80	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-90	90	-80	80	-70	70	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	180		160		140		ps	
Cumulative error across 2 cycles	tERR(2per)	- 147	147	- 132	132	- 118	118	ps	
Cumulative error across 3 cycles	tERR(3per)	- 175	175	- 157	157	- 140	140	ps	
Cumulative error across 4 cycles	tERR(4per)	- 194	194	- 175	175	- 155	155	ps	
Cumulative error across 5 cycles	tERR(5per)	- 209	209	- 188	188	- 168	168	ps	
Cumulative error across 6 cycles	tERR(6per)	- 222	222	- 200	200	- 177	177	ps	
Cumulative error across 7 cycles	tERR(7per)	- 232	232	- 209	209	- 186	186	ps	
Cumulative error across 8 cycles	tERR(8per)	- 241	241	- 217	217	- 193	193	ps	
Cumulative error across 9 cycles	tERR(9per)	- 249	249	- 224	224	- 200	200	ps	
Cumulative error across 10 cycles	tERR(10per)	- 257	257	- 231	231	- 205	205	ps	
Cumulative error across 11 cycles	tERR(11per)	- 263	263	- 237	237	- 210	210	ps	
Cumulative error across 12 cycles	tERR(12per)	- 269	269	- 242	242	- 215	215	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max						ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)	26
Data Timing									
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps	13
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-800	400	-600	300	-500	250	ps	13,14, f
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	400	-	300	-	250	ps	13,14, f
Data setup time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels	tDS(base) AC175	75	-	25	-	-	-	ps	d, 17
	tDS(base) AC150	125	-	75	-	30	-	ps	d, 17
Data hold time to DQS, $\overline{DQS}$ referenced to $V_{IH}(DC)V_{IL}(DC)$ levels	tDH(base) DC100	150	-	100	-	65	-	ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	ps	28
Data Strobe Timing									
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	NOTE 19	0.9	NOTE 19	0.9	NOTE 19	tCK	13, 19, g
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	NOTE 11	0.3	NOTE 11	0.3	NOTE 11	tCK	11, 13, b
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.38	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	tDQSCK	-400	400	-300	300	-255	255	ps	13,f
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-800	400	-600	300	-500	250	ps	13,14,f
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	400	-	300	-	250	ps	12,13,14
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)	c
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32
DQS, $\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)	c, 32

[Table 48] Timing Parameters by Speed Bins for DDR3-800 to DDR3-1333 (Cont.)

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
CAS to CAS command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 42						ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-	max (4nCK,6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,10ns)	-	max (4nCK,10ns)	-	max (4nCK,7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	ns	e
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIS(base) AC175	200	-	125	-	65	-	ps	b,16
	tIS(base) AC150	200 + 150	-	125 + 150	-	65+125	-	ps	b,16,27
Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{DC}) / V_{IL}(\text{DC})$ levels	tIH(base) DC100	275	-	200	-	140	-	ps	b,16
Control & Address Input pulse width for each input	tIPW	900	-	780	-	620	-	ps	28
Calibration Timing									
Power-up and RESET calibration time	tZQinitl	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CK HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CK low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

[Table 48] Timing Parameters by Speed Bins for DDR3-800 to DDR3-1333

Speed		DDR3-800		DDR3-1066		DDR3-1333		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Pre-charge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK, 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL +4+WR +1	-	WL +4+WR+1	-	WL +4+WR+1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timing									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing									
First DQS/DQS rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	tCK	3
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	tWLS	325	-	245	-	195	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

[Table 49] Timing Parameters by Speed Bins for DDR3-1600, DDR3-1866 (Cont.)

Speed		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Clock Timing							
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	ns	6
Average Clock Period	tCK(avg)	See Speed Bins Table				ps	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-60	60	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-50	50	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		120		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		100		ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	-88	88	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	-105	105	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	-117	117	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	-126	126	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	-133	133	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	-139	139	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	-145	145	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	-150	150	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	-154	154	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	-158	158	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	-161	161	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max				ps	24
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	tCK(avg)	25
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	tCK(avg)	26
Data Timing							
DQS, $\overline{\text{DQS}}$ to DQ skew, per group, per access	tDQSQ	-	100	-	85	ps	13
DQ output hold time from DQS, $\overline{\text{DQS}}$	tQH	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, $\overline{\text{CK}}$	tLZ(DQ)	-450	225	-390	195	ps	13,14, f
DQ high-impedance time from CK, $\overline{\text{CK}}$	tHZ(DQ)	-	225	-	195	ps	13,14, f
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (AC)V _{IL} (AC) levels	tDS(base) AC150	10	-	-	-	ps	d, 17
	tDS(base) AC135	-	-	0	-	ps	d, 17
Data hold time to DQS, $\overline{\text{DQS}}$ referenced to V _{IH} (DC)V _{IL} (DC) levels	tDH(base) DC100	45	-	20	-	ps	d, 17
DQ and DM Input pulse width for each input	tDIPW	360	-	320	-	ps	28
Data Strobe Timing							
DQS, $\overline{\text{DQS}}$ differential READ Preamble	tRPRE	0.9	NOTE 19	0.9	NOTE 19	tCK	13, 19, g
DQS, $\overline{\text{DQS}}$ differential READ Postamble	tRPST	0.3	NOTE 11	0.3	NOTE 11	tCK	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	tQSH	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential output low time	tQSL	0.4	-	0.4	-	tCK(avg)	13, g
DQS, $\overline{\text{DQS}}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK	
DQS, $\overline{\text{DQS}}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	tDQSCCK	-225	225	-195	195	ps	13,f
DQS, $\overline{\text{DQS}}$ low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	ps	13,14,f
DQS, $\overline{\text{DQS}}$ high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	ps	12,13,14
DQS, $\overline{\text{DQS}}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK	29, 31
DQS, $\overline{\text{DQS}}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK	30, 31
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	-0.27	0.27	-0.27	0.27	tCK(avg)	c
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.9	NOTE 19	0.18	-	tCK(avg)	c, 32
DQS, $\overline{\text{DQS}}$ falling edge hold time to CK, $\overline{\text{CK}}$ rising edge	tDSH	0.3	NOTE 11	0.18	-	tCK(avg)	c, 32

[Table 49] Timing Parameters by Speed Bins for DDR3-1600, DDR3-1866 (Cont.)

Speed		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Command and Address Timing							
DLL locking time	tDLLK	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		e,18
WRITE recovery time	tWR	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK,15ns)	-	max (12nCK,15ns)	-		
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)			WR + roundup (tRP / tCK(AVG))		nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin" on page 42				ns	e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK,6ns)	-	max (4nCK, 5ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK,7.5ns)	-	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	tFAW	30	-	27	-	ns	e
Four activate window for 2KB page size	tFAW	40	-	35	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{AC}) / V_{IL}(\text{AC})$ levels	tIS(base) AC175	45	-	-	-	ps	b,16
	tIS(base) AC150	170	-	-	-	ps	b,16
	tIS(base) AC135	-	-	65	-	ps	b,16
	tIS(base) AC125	-	-	150	-	ps	b,16,27
Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to $V_{IH}(\text{DC}) / V_{IL}(\text{DC})$ levels	tIH(base) DC100	120	-	100	-	ps	b,16
Control & Address Input pulse width for each input	tIPW	560	-	535	-	ps	28
Calibration Timing							
Power-up and RESET calibration time	tZQinitl	512	-	max(512nCK,640ns)	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	max(256nCK,320ns)	-	nCK	
Normal operation short calibration time	tZQCS	64	-	max(64nCK,80ns)	-	nCK	23
Reset Timing							
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC + 10ns)	-	max(5nCK, tRFC + 10ns)	-		
Self Refresh Timing							
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC + 10ns)	-	max(5nCK,tRFC + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-		

[Table 49] Timing Parameters by Speed Bins for DDR3-1600, DDR3-1866

Speed		DDR3-1600		DDR3-1866		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX		
Power Down Timing							
Exit Power Down with DLL on to any valid command;Exit Pre-charge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK,6ns)	-	max(3nCK,6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max(10nCK,24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK,5ns)	-	max(3nCK,5ns)	-		
Command pass disable delay	tCPDED	1	-	2	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK	15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(tWR/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-		20,21
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-		
ODT Timing							
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns	
RTT turn-on	tAON	-225	225	-195	195	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)	8,f
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)	f
Write Leveling Timing							
First DQS/ $\overline{\text{DQS}}$ rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	tCK	3
DQS/ $\overline{\text{DQS}}$ delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	tCK	3
Write leveling setup time from rising CK, $\overline{\text{CK}}$ crossing to rising DQS, $\overline{\text{DQS}}$ crossing	tWLS	165	-	140	-	ps	
Write leveling hold time from rising DQS, $\overline{\text{DQS}}$ crossing to rising CK, $\overline{\text{CK}}$ crossing	tWLH	165	-	140	-	ps	
Write leveling output delay	tWLO	0	7.5	0	7.5	ns	
Write leveling output error	tWLOE	0	2	0	2	ns	

14.1 Jitter Notes

- Specific Note a** Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.
- Specific Note b** These parameters are measured from a command/address signal (CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/ $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note c** These parameters are measured from a data strobe signal (DQS(L/U), $\overline{\text{DQS}}$ (L/U)) crossing to its respective clock signal (CK, $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note d** These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{\text{DQS}}$ (L/U)) crossing.
- Specific Note e** For these parameters, the DDR3 SDRAM device supports tPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.
- Specific Note f** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 ≤ m ≤ 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 ≤ n ≤ 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 ≤ n ≤ 12.
- Specific Note g** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

14.2 Timing Parameter Notes

- Actual value dependant upon measurement level definitions which are TBD.
- Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
- The max values are system dependent.
- WR as programmed in mode register
- Value must be rounded-up to next higher integer value
- There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
- For definition of RTT turn-on time tAON see "Device Operation & Timing Diagram Datasheet"
- For definition of RTT turn-off time tAOF see "Device Operation & Timing Diagram Datasheet".
- tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
- WR in clock cycles as programmed in MR0
- The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See "Device Operation & Timing Diagram Datasheet".
- Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
- Value is only valid for RON34
- Single ended signal parameter. Refer to chapter 8 and chapter 9 for definition and measurement method.
- tREFI depends on T_{OPER}
- tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, $V_{REF}(DC) = V_{REF}DQ(DC)$. For input only pins except RESET, $V_{REF}(DC) = V_{REF}CA(DC)$. See "Address/Command Setup, Hold and Derating ." on page 52. .
- tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, $V_{REF}(DC) = V_{REF}DQ(DC)$. For input only pins except RESET, $V_{REF}(DC) = V_{REF}CA(DC)$. See "Data Setup, Hold and Slew Rate Derating ." on page 59.
- Start of internal write transaction is defined as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
- The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation & Timing Diagram Datasheet"
- CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
- Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation & Timing Diagram Datasheet".
- Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
- One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128ms$$

- n = from 13 cycles to 50 cycles. This row defines 38 parameters.
- tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
- tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
- The tIS(base) AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 125 ps for DDR3-800/1066 or 100ps for DDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV - 150 mV) / 1 V/ns].
- Pulse width of a input signal is defined as the width between the first crossing of $V_{REF}(DC)$ and the consecutive crossing of $V_{REF}(DC)$
- tDQSL describes the instantaneous differential input low pulse width on DQS- $\overline{DQS}$, as measured from one falling edge to the next consecutive rising edge.
- tDQSH describes the instantaneous differential input high pulse width on DQS- $\overline{DQS}$, as measured from one rising edge to the next consecutive falling edge.
- tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
- tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
- The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for DDR3-1866 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV - 125mV) / 1 V/ns].

14.3 Address/Command Setup, Hold and Derating :

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 50) to the ΔtIS and ΔtIH derating value (see Table 51) respectively.

Example: tIS (total setup time) = tIS(base) + ΔtIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IH}(AC)_{min}$. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IL}(AC)_{max}$. If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF}(DC)$ to ac region', use nominal slew rate for derating value (see Figure 21). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF}(DC)$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 23).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(DC)_{max}$ and the first crossing of $V_{REF}(DC)$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}(DC)_{min}$ and the first crossing of $V_{REF}(DC)$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF}(DC)$ region', use nominal slew rate for derating value (see Figure 22). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF}(DC)$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF}(DC)$ level is used for derating value (see Figure 24).

For a valid transition the input signal has to remain above/below $V_{IH/IL}(AC)$ for some time tVAC (see Table 55).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}(AC)$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}(AC)$.

For slew rates in between the values listed in Table 51, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

[Table 50] ADD/CMD Setup and Hold Base-Values for 1V/ns

[ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	reference
tIS(base) AC175	200	125	65	45	-	$V_{IH/L}(AC)$
tIS(base) AC150	350	275	190	170	-	$V_{IH/L}(AC)$
tIS(base)-AC135	-	-	-	-	65	$V_{IH/L}(AC)$
tIS(base)-AC125	-	-	-	-	150	$V_{IH/L}(AC)$
tIH(base)-DC100	275	200	140	120	100	$V_{IH/L}(DC)$

NOTE :

- AC/DC referenced for 1V/ns Address/Command slew rate and 2 V/ns differential CK-CK slew rate
- The tIS(base)-AC150 specifications are adjusted from the tIS(base) AC175 specification by adding an additional 125ps for DDR3-800/1066 or 100ps for DDR3-1333/1600 of derating to accommodate for the lower alternate threshold of 150mV and another 25ps to account for the earlier reference point [(175mV-150mV)/1 V/ns]
- The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75ps for DDR3-1866 and 65ps for DDR3-2133 to accommodate for the lower alternate threshold of 125mV and another 10ps to account for the earlier reference point [(135mV-125mV)/1V/ns].

[Table 51] Derating values DDR3-800/1066/1333/1600 tIS/tIH-AC/DC based AC175 Threshold

$\Delta t_{IS}, \Delta t_{IH}$ Derating [ps] AC/DC based Alternate AC175 Threshold -> $V_{IH}(AC) = V_{REF}(DC) + 175mV$, $V_{IL}(AC) = V_{REF}(DC) - 175mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}	Δt_{IS}	Δt_{IH}
CMD/ ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10	

[Table 52] Derating values DDR3-800/1066/1333/1600 tIS/tIH-AC/DC based - Alternate AC150 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC150 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 150mV, V_{IL}(AC) = V_{REF}(DC) - 150mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

[Table 53] Derating values DDR3-1866 tIS/tIH-AC/DC based Alternate AC135 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 135mV, V_{IL}(AC) = V_{REF}(DC) - 135mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	68	50	68	50	68	50	76	58	84	66	92	74	100	84	108	100
	1.5	45	34	45	34	45	34	53	42	61	50	69	58	77	68	85	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-4	2	-4	2	-4	10	4	18	12	26	20	34	30	42	46
	0.8	3	-10	3	-10	3	-10	11	-2	19	6	27	14	35	24	43	40
	0.7	6	-16	6	-16	6	-16	14	-8	22	0	30	8	38	18	46	34
	0.6	9	-26	9	-26	9	-26	17	-18	25	-10	33	-2	41	8	49	24
	0.5	5	-40	5	-40	5	-40	13	-32	21	-24	29	-16	37	-6	45	10
	0.4	-3	-60	-3	-60	-3	-60	6	-52	14	-44	22	-36	30	-26	38	-10

[Table 54] Derating values DDR3-1866 tIS/tIH-AC/DC based - Alternate AC125 Threshold

$\Delta tIS, \Delta tIH$ Derating [ps] AC/DC based Alternate AC125 Threshold $\rightarrow V_{IH}(AC) = V_{REF}(DC) + 125mV, V_{IL}(AC) = V_{REF}(DC) - 125mV$																	
		CLK,CLK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	63	50	63	50	63	50	71	58	79	66	87	74	95	84	103	100
	1.5	42	34	42	34	42	34	50	42	58	50	66	58	74	68	82	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	4	-4	4	-4	4	-4	12	4	20	12	28	20	36	30	44	46
	0.8	6	-10	6	-10	6	-10	14	-2	22	6	30	14	38	24	46	40
	0.7	11	-16	11	-16	11	-16	19	-8	27	0	35	8	43	18	51	34
	0.6	16	-26	16	-26	16	-26	24	-18	32	-10	40	-2	48	8	56	24
	0.5	15	-40	15	-40	15	-40	23	-32	31	-24	39	-16	47	-6	55	10
	0.4	13	-60	13	-60	13	-60	21	-52	29	-44	37	-36	45	-26	53	-10

[Table 55] Required time t_{VAC} above $V_{IH}(AC)$ (blow $V_{IL}(AC)$) for valid transition

Slew Rate[V/ns]	t_{VAC} @175mV [ps]		t_{VAC} @150mV [ps]		t_{VAC} @135mV [ps]		t_{VAC} @125mV [ps]	
	min	max	min	max	min	max	min	max
>2.0	75	-	175	-	TBD	-	TBD	-
2.0	57	-	170	-	TBD	-	TBD	-
1.5	50	-	167	-	TBD	-	TBD	-
1.0	38	-	163	-	TBD	-	TBD	-
0.9	34	-	162	-	TBD	-	TBD	-
0.8	29	-	161	-	TBD	-	TBD	-
0.7	22	-	159	-	TBD	-	TBD	-
0.6	13	-	155	-	TBD	-	TBD	-
0.5	0	-	150	-	TBD	-	TBD	-
< 0.5	0	-	150	-	TBD	-	TBD	-

NOTE : Clock and Strobe are drawn on a different time scale.

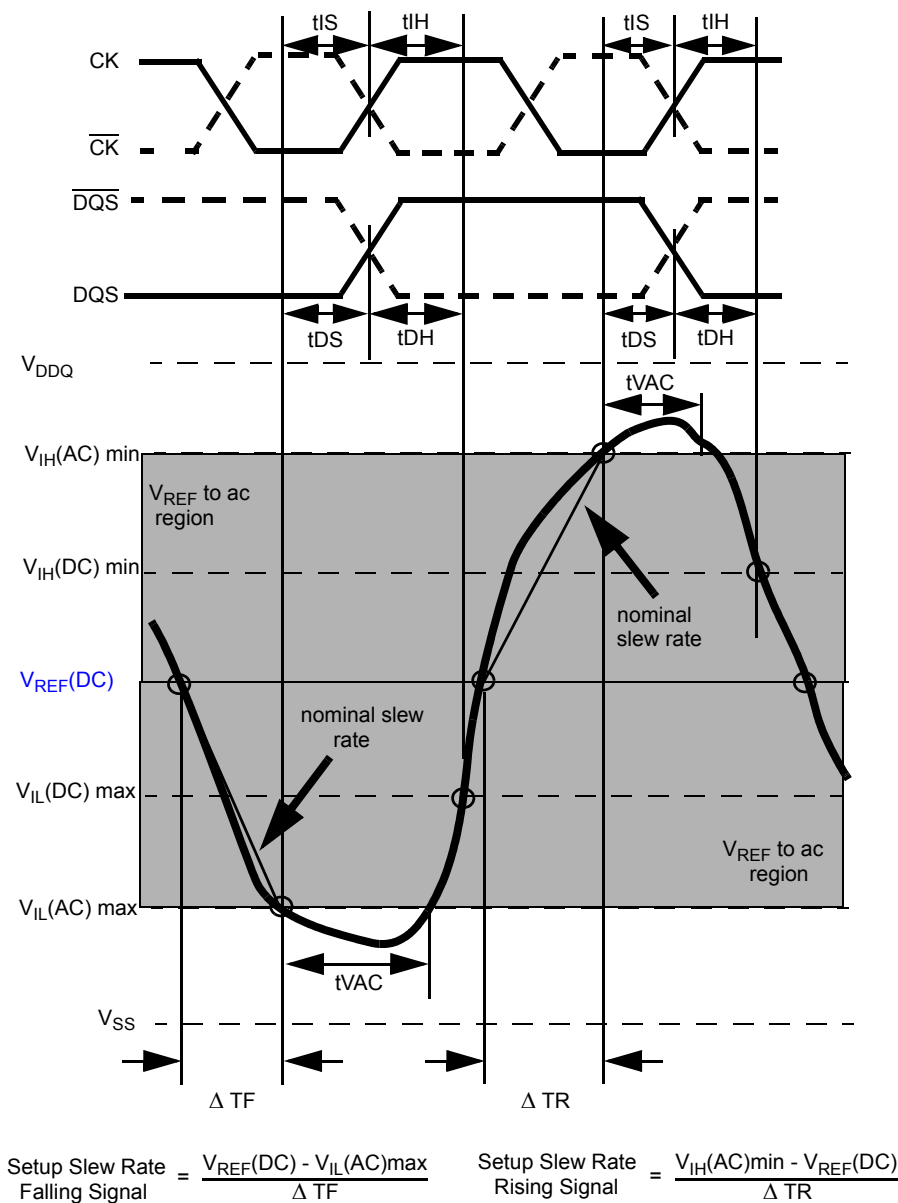


Figure 21. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

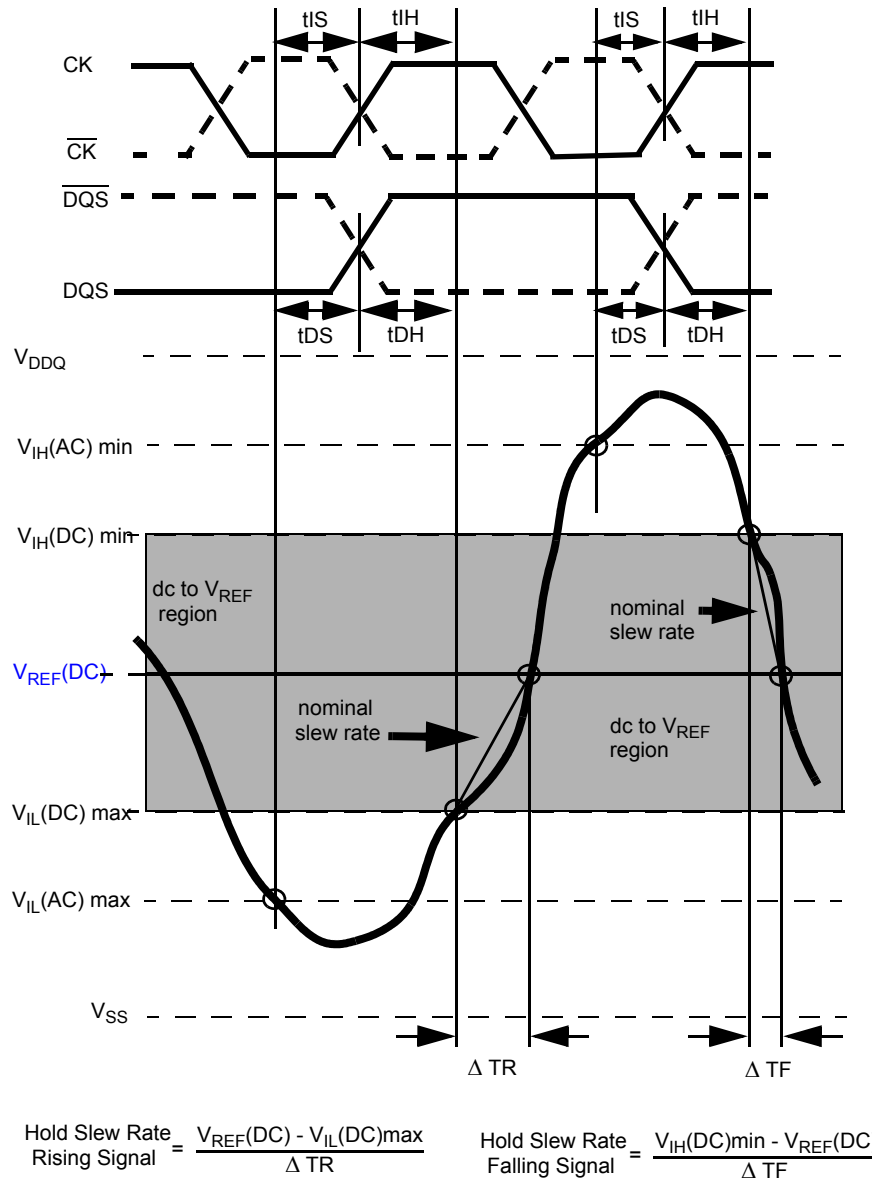


Figure 22. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

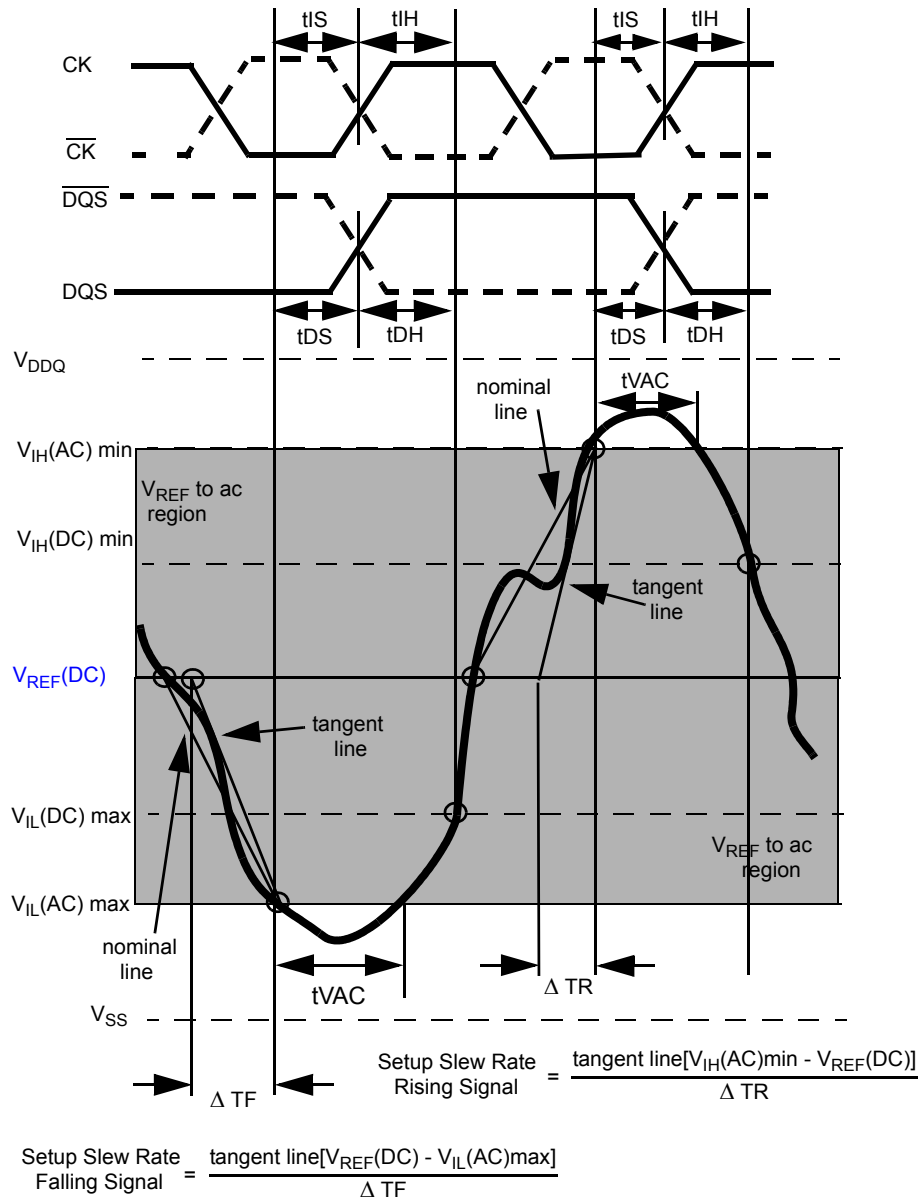


Figure 23. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

NOTE :Clock and Strobe are drawn on a different time scale.

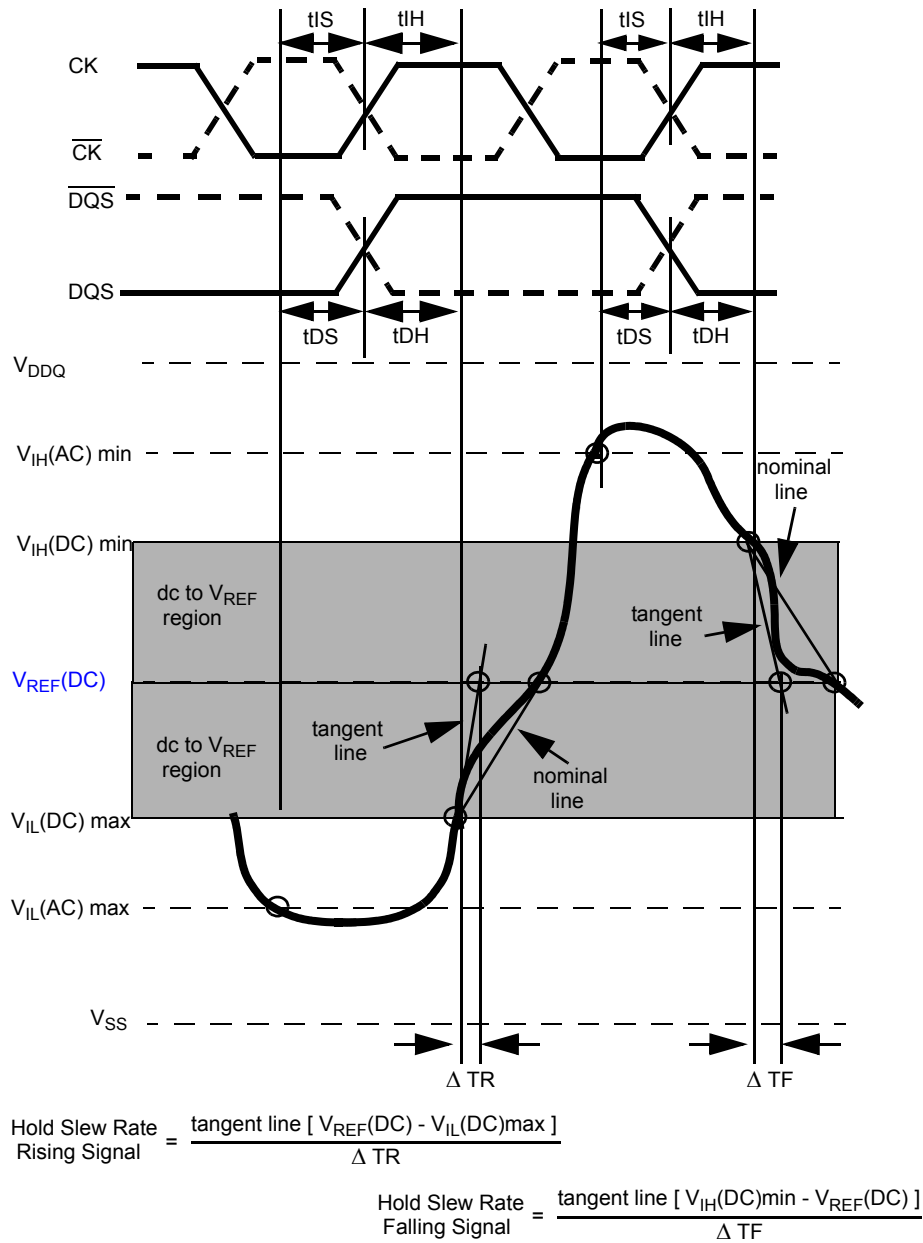


Figure 24. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)

14.4 Data Setup, Hold and Slew Rate Derating :

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 56) to the ΔtDS and ΔtDH (see Table 55) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS .

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IH}(AC)_{min}$.

Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}(DC)$ and the first crossing of $V_{IL}(AC)_{max}$ (see Figure 25). If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF}(DC)$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF}(DC)$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 27).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}(DC)_{max}$ and the first crossing of $V_{REF}(DC)$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}(DC)_{min}$ and the first crossing of $V_{REF}(DC)$ (see Figure). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF}(DC)$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF}(DC)$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF}(DC)$ level is used for derating value (see Figure 28).

For a valid transition the input signal has to remain above/below $V_{IH/IL}(AC)$ for some time tVAC (see Table 56).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}(AC)$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}(AC)$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

[Table 56] Data Setup and Hold Base-Values

[ps]	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	reference
tDS(base) AC175	75	25	-	-	-	$V_{IH/IL}(AC)$
tDS(base) AC150	125	75	30	10	-	$V_{IH/IL}(AC)$
tDS(base) AC135	-	-	-	-	0	$V_{IH/IL}(AC)$
tDH(base) DC100	150	100	65	45	20	$V_{IH/IL}(DC)$

NOTE : AC/DC referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

[Table 57] Derating values DDR3-800/1066 tDS/tDH - (AC175)

$\Delta tDS, \Delta tDH$ Derating in [ps] AC/DC based ¹																	
		DQS,DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DDR3 - 800/ 1066	DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-
		1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-
		1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-
		0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-
		0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-
		0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29
		0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23
		0.5	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	6	10
		0.4	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 58] Derating values for DDR3-800/1066/1333/1600 tDS/tDH - (AC150)

$\Delta tDS, \Delta tDH$ Derating in [ps] AC/DC based ¹																	
		DQS,DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
	1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
	0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
	0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
	0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
	0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 59] Derating values for DDR3-1866 tDS/tDH - (AC135)

Δt_{DS} , Δt_{DH} Derating in [ps] AC/DC based ¹																	
DQS, DQS Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew rate V/ns	2.0	68	50	68	50	68	50	-	-	-	-	-	-	-	-	-	-
	1.5	45	34	45	34	45	34	53	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-4	2	-4	10	4	18	12	26	20	-	-	-	-
	0.8	-	-	-	-	3	-10	11	-2	19	6	27	14	35	24	-	-
	0.7	-	-	-	-	-	-	14	-8	22	0	30	8	38	18	46	34
	0.6	-	-	-	-	-	-	-	-	25	-10	33	-2	41	8	49	24
	0.5	-	-	-	-	-	-	-	-	-	-	29	-16	37	-6	45	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-26	38	-10

NOTE : 1. Cell contents shaded in red are defined as 'not supported'.

[Table 60] Required time t_{VAC} above $V_{IH}(AC)$ (below $V_{IL}(AC)$) for valid transition

Slew Rate[V/ns]	t_{VAC} [ps] DDR3-1066 (AC175)		t_{VAC} [ps] DDR3-1066/1333/1600 (AC150)		t_{VAC} [ps] DDR3-1866 (AC135)	
	min	max	min	max	min	max
>2.0	75	-	175	-	TBD	-
2.0	57	-	170	-	TBD	-
1.5	50	-	167	-	TBD	-
1.0	38	-	163	-	TBD	-
0.9	34	-	162	-	TBD	-
0.8	29	-	161	-	TBD	-
0.7	22	-	159	-	TBD	-
0.6	13	-	155	-	TBD	-
0.5	0	-	155	-	TBD	-
<0.5	0	-	150	-	TBD	-

NOTE : Clock and Strobe are drawn on a different time scale.

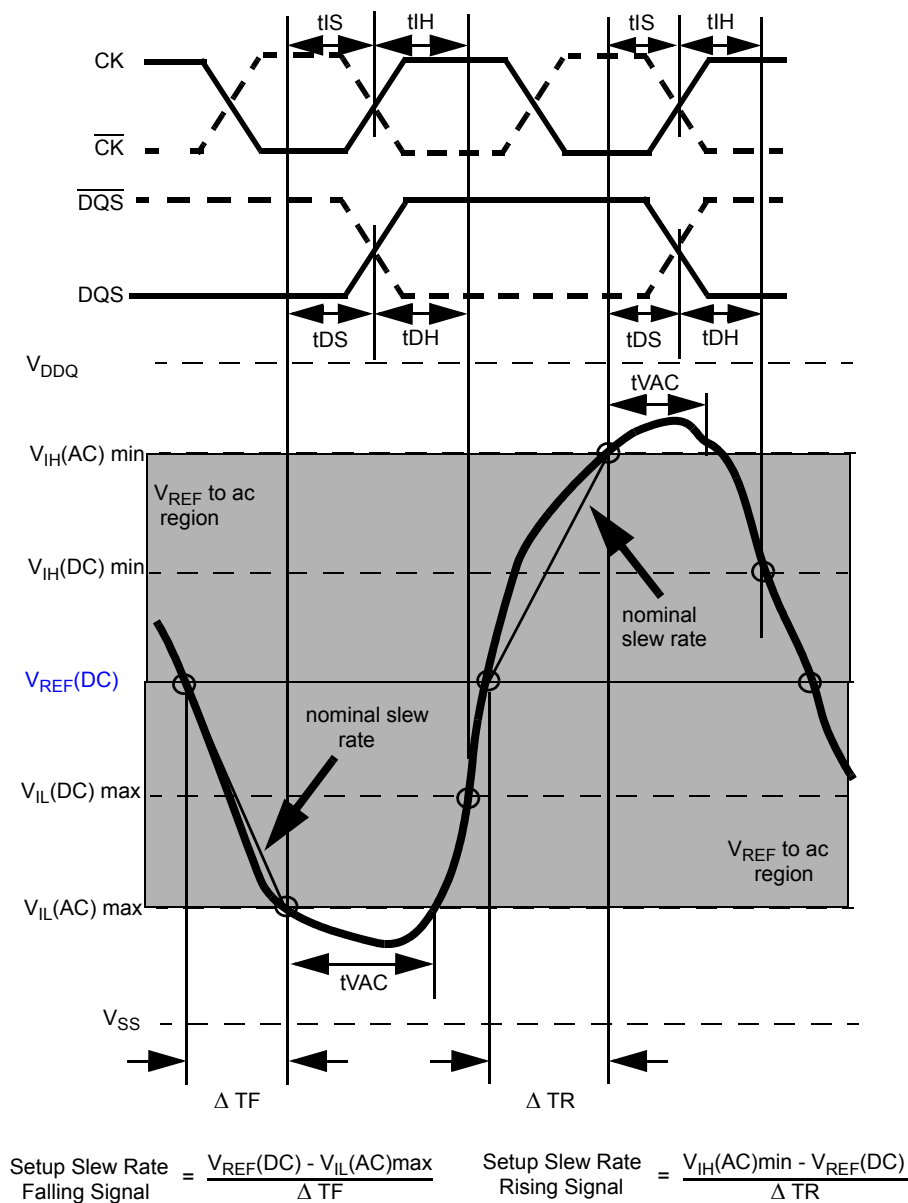


Figure 25. Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

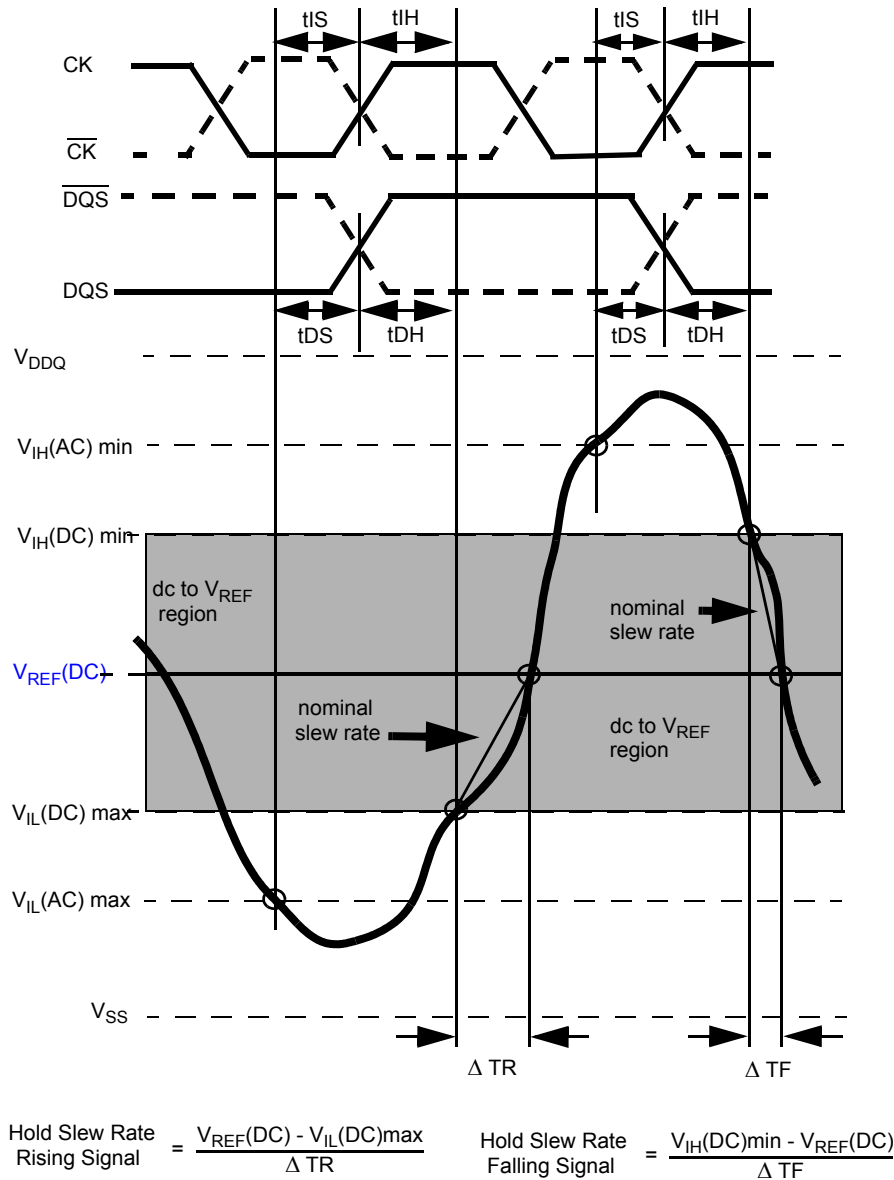


Figure 26. Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

NOTE :Clock and Strobe are drawn on a different time scale.

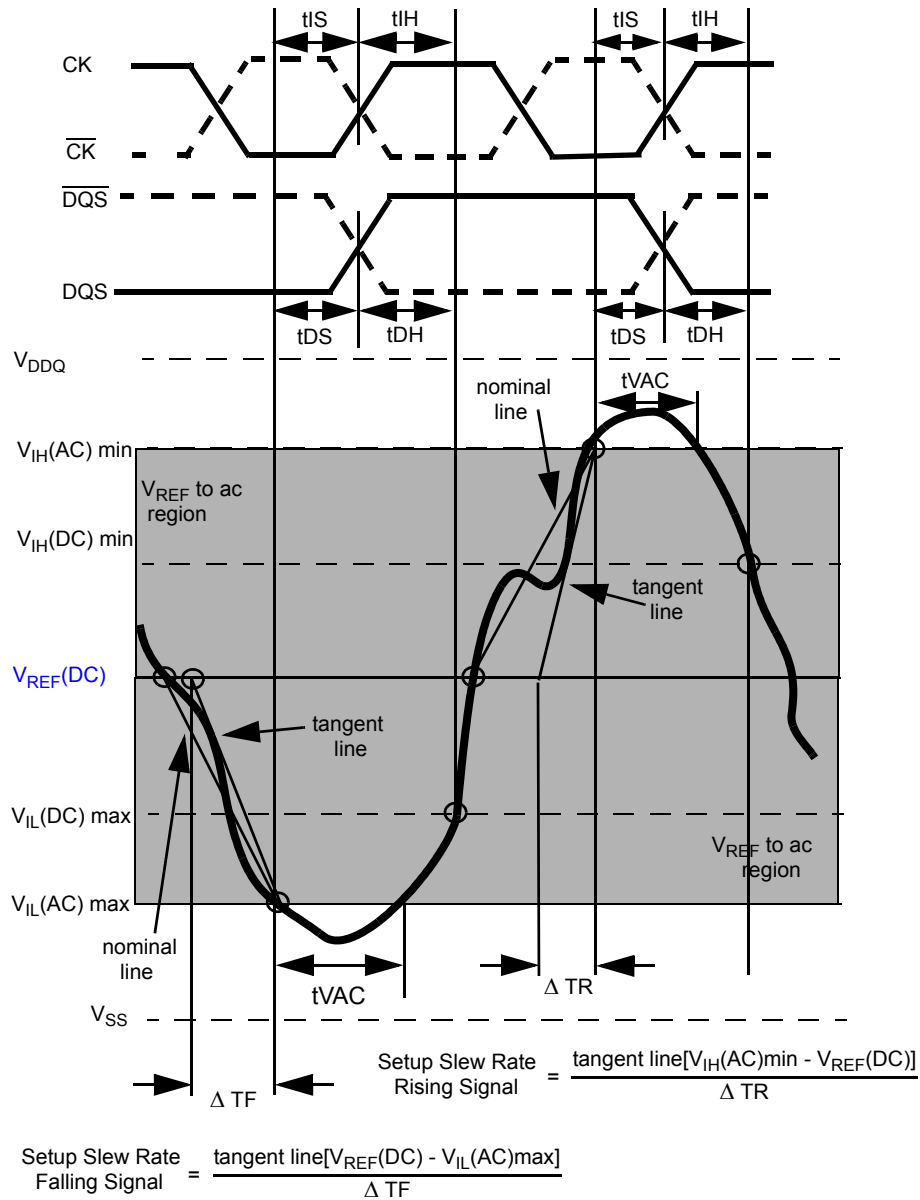


Figure 27. Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock)

NOTE :Clock and Strobe are drawn on a different time scale.

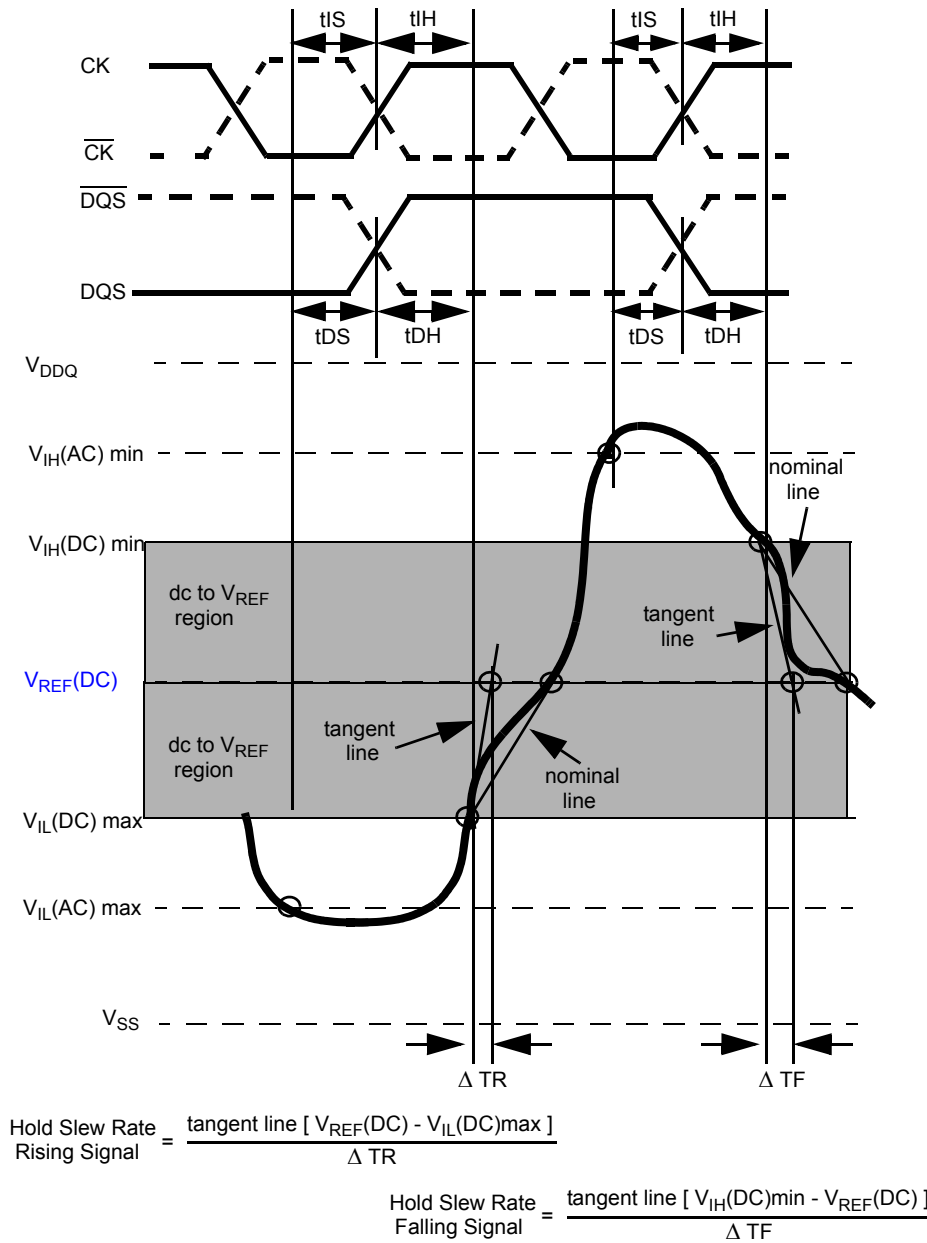


Figure 28. Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock)