



# Virtex™-E 1.8 V Field Programmable Gate Arrays

DS022-1 (v2.2) November 9, 2001

Preliminary Product Specification

## Features

- Fast, High-Density 1.8 V FPGA Family
  - Densities from 58 k to 4 M system gates
  - 130 MHz internal performance (four LUT levels)
  - Designed for low-power operation
  - PCI compliant 3.3 V, 32/64-bit, 33/ 66-MHz
- Highly Flexible SelectI/O+™ Technology
  - Supports 20 high-performance interface standards
  - Up to 804 singled-ended I/Os or 344 differential I/O pairs for an aggregate bandwidth of > 100 Gb/s
- Differential Signalling Support
  - LVDS (622 Mb/s), BLVDS (Bus LVDS), LVPECL
  - Differential I/O signals can be input, output, or I/O
  - Compatible with standard differential devices
  - LVPECL and LVDS clock inputs for 300+ MHz clocks
- Proprietary High-Performance SelectLink™ Technology
  - Double Data Rate (DDR) to Virtex-E link
  - Web-based HDL generation methodology
- Sophisticated SelectRAM+™ Memory Hierarchy
  - 1 Mb of internal configurable distributed RAM
  - Up to 832 Kb of synchronous internal block RAM
  - True Dual-Port™ BlockRAM capability
  - Memory bandwidth up to 1.66 Tb/s (equivalent bandwidth of over 100 RAMBUS channels)
  - Designed for high-performance Interfaces to External Memories
  - 200 MHz ZBT\* SRAMs
  - 200 Mb/s DDR SDRAMs
  - Supported by free Synthesizable reference design
- High-Performance Built-In Clock Management Circuitry
  - Eight fully digital Delay-Locked Loops (DLLs)
  - Digitally-Synthesized 50% duty cycle for Double Data Rate (DDR) Applications
  - Clock Multiply and Divide
  - Zero-delay conversion of high-speed LVPECL/LVDS clocks to any I/O standard
- Flexible Architecture Balances Speed and Density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input function
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensor diode
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Further compile time reduction of 50%
  - Internet Team Design (ITD) tool ideal for million-plus gate density designs
  - Wide selection of PC and workstation platforms
- SRAM-Based In-System Configuration
  - Unlimited re-programmability
- Advanced Packaging Options
  - 0.8 mm Chip-scale
  - 1.0 mm BGA
  - 1.27 mm BGA
  - HQ/PQ
- 0.18 µm 6-Layer Metal Process
- 100% Factory Tested

\* ZBT is a trademark of Integrated Device Technology, Inc.

Table 1: Virtex-E Field-Programmable Gate Array Family Members

| Device   | System Gates | Logic Gates | CLB Array | Logic Cells | Differential I/O Pairs | User I/O | BlockRAM Bits | Distributed RAM Bits |
|----------|--------------|-------------|-----------|-------------|------------------------|----------|---------------|----------------------|
| XCV50E   | 71,693       | 20,736      | 16 x 24   | 1,728       | 83                     | 176      | 65,536        | 24,576               |
| XCV100E  | 128,236      | 32,400      | 20 x 30   | 2,700       | 83                     | 196      | 81,920        | 38,400               |
| XCV200E  | 306,393      | 63,504      | 28 x 42   | 5,292       | 119                    | 284      | 114,688       | 75,264               |
| XCV300E  | 411,955      | 82,944      | 32 x 48   | 6,912       | 137                    | 316      | 131,072       | 98,304               |
| XCV400E  | 569,952      | 129,600     | 40 x 60   | 10,800      | 183                    | 404      | 163,840       | 153,600              |
| XCV600E  | 985,882      | 186,624     | 48 x 72   | 15,552      | 247                    | 512      | 294,912       | 221,184              |
| XCV1000E | 1,569,178    | 331,776     | 64 x 96   | 27,648      | 281                    | 660      | 393,216       | 393,216              |
| XCV1600E | 2,188,742    | 419,904     | 72 x 108  | 34,992      | 344                    | 724      | 589,824       | 497,664              |
| XCV2000E | 2,541,952    | 518,400     | 80 x 120  | 43,200      | 344                    | 804      | 655,360       | 614,400              |
| XCV2600E | 3,263,755    | 685,584     | 92 x 138  | 57,132      | 344                    | 804      | 753,664       | 812,544              |
| XCV3200E | 4,074,387    | 876,096     | 104 x 156 | 73,008      | 344                    | 804      | 851,968       | 1,038,336            |

## Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

$V_{CCINT}$ , the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18  $\mu$ m design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100  $\Omega$  resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by  $V_{CCINT}$ . With Virtex-E devices, the LVTTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage  $V_{CCO}$ .

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

## General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18  $\mu$ m CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

## Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

## Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: Performance for Common Circuit Functions

| Function                | Bits    | Virtex-E (-7) |
|-------------------------|---------|---------------|
| Register-to-Register    |         |               |
| Adder                   | 16      | 4.3 ns        |
|                         | 64      | 6.3 ns        |
| Pipelined Multiplier    | 8 x 8   | 4.4 ns        |
|                         | 16 x 16 | 5.1 ns        |
| Address Decoder         | 16      | 3.8 ns        |
|                         | 64      | 5.5 ns        |
| 16:1 Multiplexer        |         | 4.6 ns        |
| Parity Tree             | 9       | 3.5 ns        |
|                         | 18      | 4.3 ns        |
|                         | 36      | 5.9 ns        |
| Chip-to-Chip            |         |               |
| HSTL Class IV           |         |               |
| LVTTTL, 16mA, fast slew |         |               |
| LVDS                    |         |               |
| LVPECL                  |         |               |

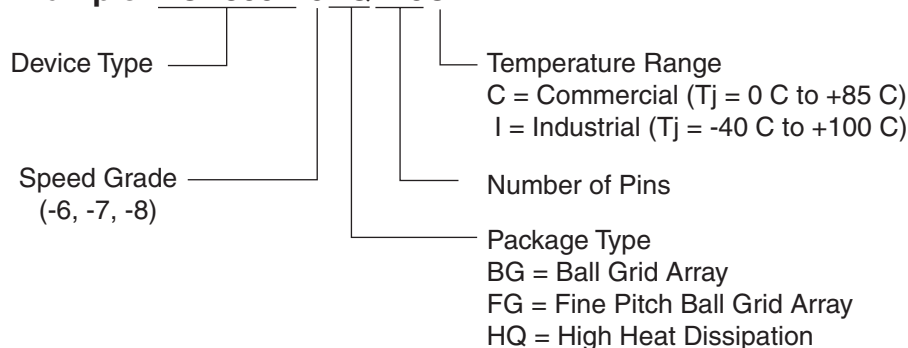
## Virtex-E Device/Package Combinations and Maximum I/O

Table 3: Virtex-E Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)

|        | XCV<br>50E | XCV<br>100E | XCV<br>200E | XCV<br>300E | XCV<br>400E | XCV<br>600E | XCV<br>1000E | XCV<br>1600E | XCV<br>2000E | XCV<br>2600E | XCV<br>3200E |
|--------|------------|-------------|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|--------------|
| CS144  | 94         | 94          | 94          |             |             |             |              |              |              |              |              |
| PQ240  | 158        | 158         | 158         | 158         | 158         |             |              |              |              |              |              |
| HQ240  |            |             |             |             |             | 158         | 158          |              |              |              |              |
| BG352  |            | 196         | 260         | 260         |             |             |              |              |              |              |              |
| BG432  |            |             |             | 316         | 316         | 316         |              |              |              |              |              |
| BG560  |            |             |             |             | 404         | 404         | 404          | 404          | 404          |              |              |
| FG256  | 176        | 176         | 176         | 176         |             |             |              |              |              |              |              |
| FG456  |            |             | 284         | 312         |             |             |              |              |              |              |              |
| FG676  |            |             |             |             | 404         | 444         |              |              |              |              |              |
| FG680  |            |             |             |             |             | 512         | 512          | 512          | 512          |              |              |
| FG860  |            |             |             |             |             |             | 660          | 660          | 660          |              |              |
| FG900  |            |             |             |             |             | 512         | 660          | 700          |              |              |              |
| FG1156 |            |             |             |             |             |             | 660          | 724          | 804          | 804          | 804          |

## Virtex-E Ordering Information

### Example: XCV300E-6PQ240C



DS022\_043\_072000

Figure 1: Ordering Information

## Revision History

The following table shows the revision history for this document.

| Date    | Version | Revision  |
|---------|---------|---|
| 12/7/99 | 1.0     | Initial Xilinx release.   |
| 1/10/00 | 1.1     | Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.   |
| 1/28/00 | 1.2     | Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T <sub>BYP</sub> values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.  |
| 2/29/00 | 1.3     | Updated pinout tables, V <sub>CC</sub> page 20, and corrected Figure 20.  |
| 5/23/00 | 1.4     | Correction to table on p. 22.   |
| 7/10/00 | 1.5     | <ul style="list-style-type: none"> <li>Numerous minor edits.</li> <li>Data sheet upgraded to Preliminary.</li> <li>Preview -8 numbers added to <b>Virtex-E Electrical Characteristics</b> tables.</li> </ul>  |
| 8/1/00  | 1.6     | <ul style="list-style-type: none"> <li>Reformatted entire document to follow new style guidelines.</li> <li>Changed speed grade values in tables on pages 35-37.</li> </ul>   |
| 9/20/00 | 1.7     | <ul style="list-style-type: none"> <li>Min values added to <b>Virtex-E Electrical Characteristics</b> tables.</li> <li>XCV2600E and XCV3200E numbers added to <b>Virtex-E Electrical Characteristics</b> tables (Module 3).</li> <li>Corrected user I/O count for XCV100E device in Table 1 (Module 1).</li> <li>Changed several pins to "No Connect in the XCV100E" and removed duplicate V<sub>CCINT</sub> pins in Table ~ (Module 4).</li> <li>Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4).</li> <li>Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4).</li> <li>Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".</li> </ul> |

| Date     | Version | Revision  |
|----------|---------|---|
| 11/20/00 | 1.8     | <ul style="list-style-type: none"> <li>Upgraded speed grade -8 numbers in <b>Virtex-E Electrical Characteristics</b> tables to Preliminary.</li> <li>Updated minimums in Table 13 and added notes to Table 14.</li> <li>Added to note 2 to <b>Absolute Maximum Ratings</b>.</li> <li>Changed speed grade -8 numbers for <math>T_{SHCKO32}</math>, <math>T_{REG}</math>, <math>T_{BCCS}</math>, and <math>T_{ICKOF}</math></li> <li>Changed all minimum hold times to –0.4 under <b>Global Clock Setup and Hold for LVTTL Standard, with DLL</b>.</li> <li>Revised maximum <math>T_{DLLPW}</math> in -6 speed grade for <b>DLL Timing Parameters</b>.</li> <li>Changed GCLK0 to BA22 for FG860 package in Table 46.</li> </ul> |
| 2/12/01  | 1.9     | <ul style="list-style-type: none"> <li>Revised footnote for Table 14.</li> <li>Added numbers to <b>Virtex-E Electrical Characteristics</b> tables for XCV1000E and XCV2000E devices.</li> <li>Updated Table 27 and Table 78 to include values for XCV400E and XCV600E devices.</li> <li>Revised Table 62 to include pinout information for the XCV400E and XCV600E devices in the BG560 package.</li> <li>Updated footnotes 1 and 2 for Table 76 to include XCV2600E and XCV3200E devices.</li> </ul>   |
| 4/2/01   | 2.0     | <ul style="list-style-type: none"> <li>Updated numerous values in <b>Virtex-E Switching Characteristics</b> tables.</li> <li>Converted data sheet to modularized format. See the <b>Virtex-E Data Sheet</b> section.</li> </ul>   |
| 10/25/01 | 2.1     | <ul style="list-style-type: none"> <li>Updated the <b>Virtex-E Device/Package Combinations and Maximum I/O</b> table to show XCV3200E in the FG1156 package.</li> </ul>   |
| 11/09/01 | 2.2     | <ul style="list-style-type: none"> <li>Minor edits.</li> </ul>  |

## Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:  
**Introduction and Ordering Information (Module 1)**
- DS022-2, Virtex-E 1.8V FPGAs:  
[Functional Description \(Module 2\)](#)
- DS022-3, Virtex-E 1.8V FPGAs:  
[DC and Switching Characteristics \(Module 3\)](#)
- DS022-4, Virtex-E 1.8V FPGAs:  
[Pinout Tables \(Module 4\)](#)