4 Megabit Module XM28C040 512K x 8 Bit

5 Volt, Byte Alterable E²PROM

TYPICAL FEATURES

- **High Density 4 Megabit (512K x 8) Module**
- **Access Time of 200ns at –55°C to +125°C**
- **Base Memory Component: Xicor X28C010**
- **Pinout Conforms to JEDEC Standard for 4 Megabit E²PROM**
- **Fast Write Cycle Times**
  - **—256 Byte Page Write**
- **Early End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit Polling**
- **Software Data Protection**
- **Three Temperature Ranges**
  - **—Commercial: 0°C to +75°C**
  - **—Industrial: –40° to +85°C**
  - **—Military: –55° to +125°C**
- **High Rel Modules all Components are MIL-STD-883 Compliant**
- **Endurance: 100,000 Cycles**

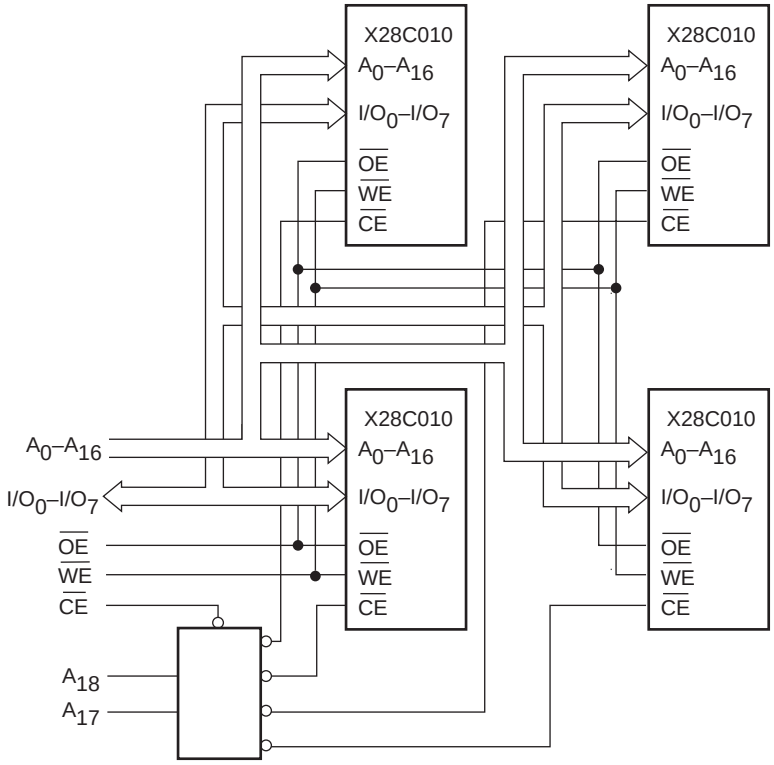
DESCRIPTION

The XM28C040 is a high density 4 Megabit E²PROM comprised of four X28C010's mounted on a co-fired multilayered ceramic substrate. Individual components are 100% tested prior to assembly in module form and then 100% tested after assembly.

The XM28C040 is configured 512K x 8 bit. The module supports a 256-byte page write operation. This combined with $\overline{\text{DATA}}$ Polling or Toggle Bit Polling, effectively provides a 39µs/byte write cycle, enabling the entire array to be rewritten in 10 seconds.

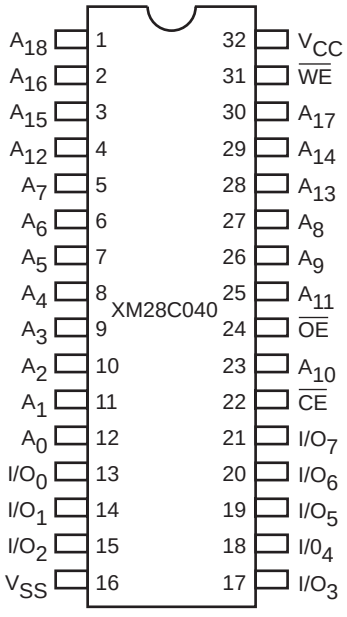
The XM28C040 provides the same high endurance and data retention as the X28C010.

FUNCTIONAL DIAGRAM



3873 FHD F01

PIN CONFIGURATION



3873 FHD F02

PIN DESCRIPTIONS

Addresses (A_0–A_{18})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the XM28C040 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the XM28C040.

PIN NAMES

Symbol	Description
A_0–A_{18}	Address Inputs
I/O_0–I/O_8	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

3873 PGM T01

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The XM28C040 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms (see Note 4).

Page Write Operation

The page write feature of the XM28C040 allows the entire memory to be written in 10 seconds. Page write allows two to 256 bytes of data to be consecutively written to the XM28C040 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_8 through A_{18}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

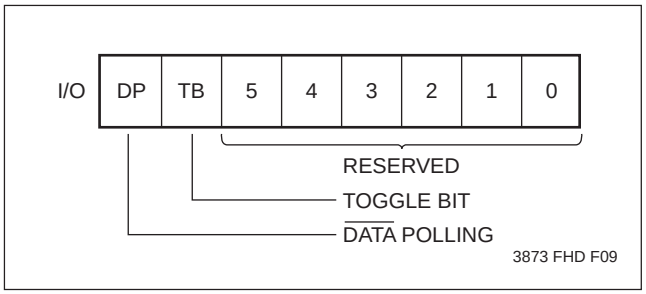
The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 255 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The XM28C040 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

$\overline{DATA}$ Polling (I/O_7)

Figure 1. Status Bit Assignment



The XM28C040 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28C040, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28C040 is in the protected state and an illegal write operation is attempted, $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The XM28C040 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from “1” to “0” and “0” to “1” on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

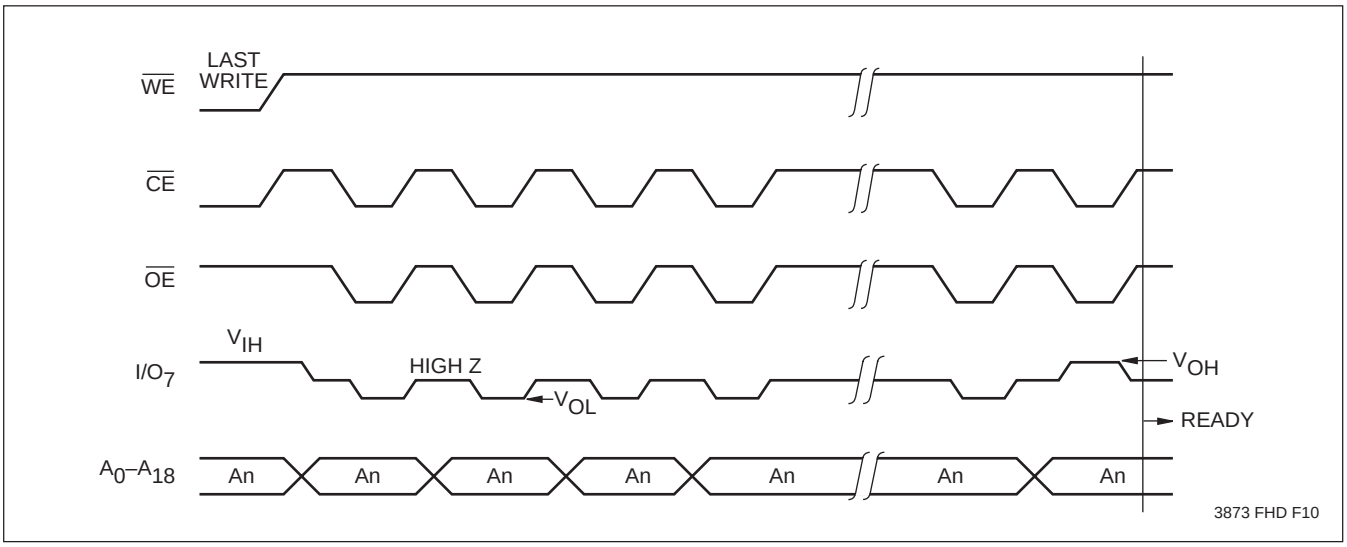
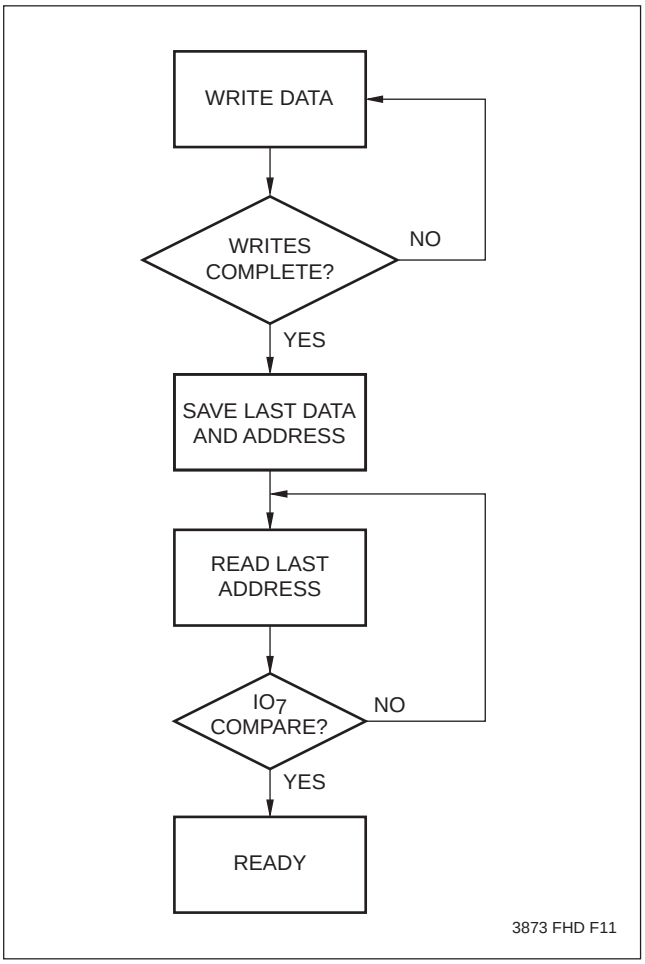


Figure 3. $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the XM28C040. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

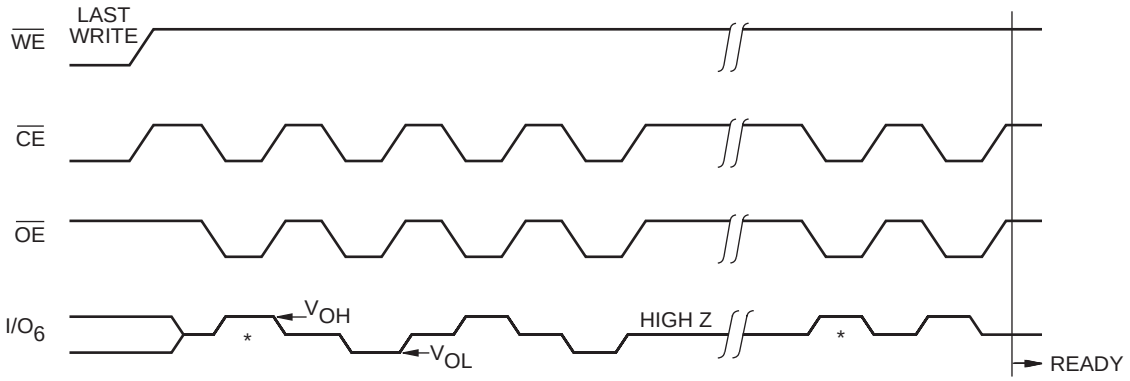
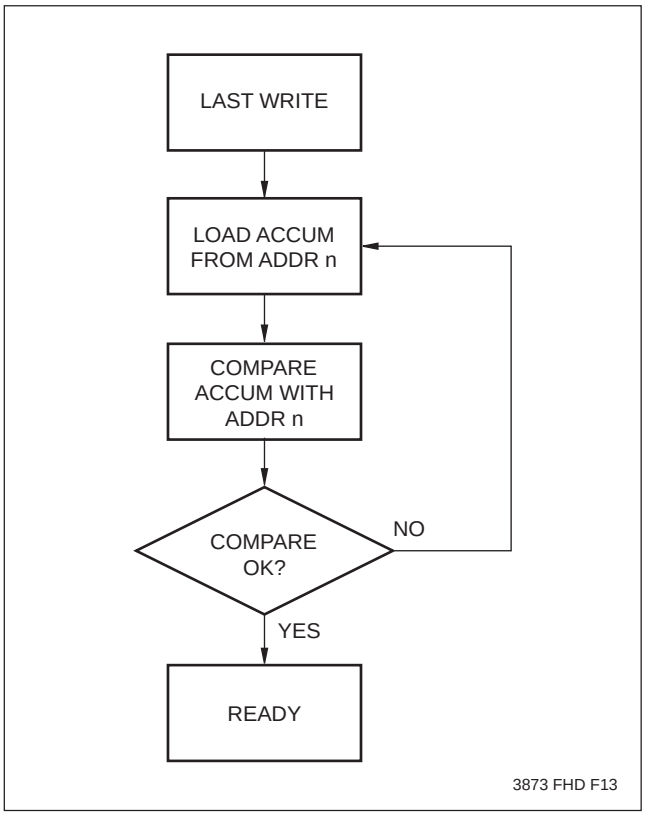


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple XM28C040 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The XM28C040 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤ 3V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-up and power-down.

SOFTWARE DATA PROTECTION

The XM28C040 does provide the Software Data Protection (SDP) feature.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode, data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

SOFTWARE COMMAND SEQUENCE

A_{17} and A_{18} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

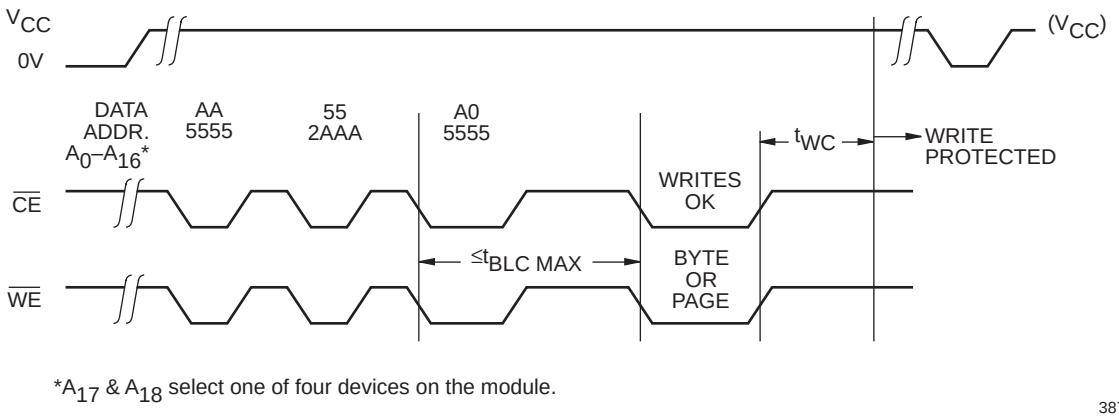
Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit, the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to 256 bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

SOFTWARE DATA PROTECTION

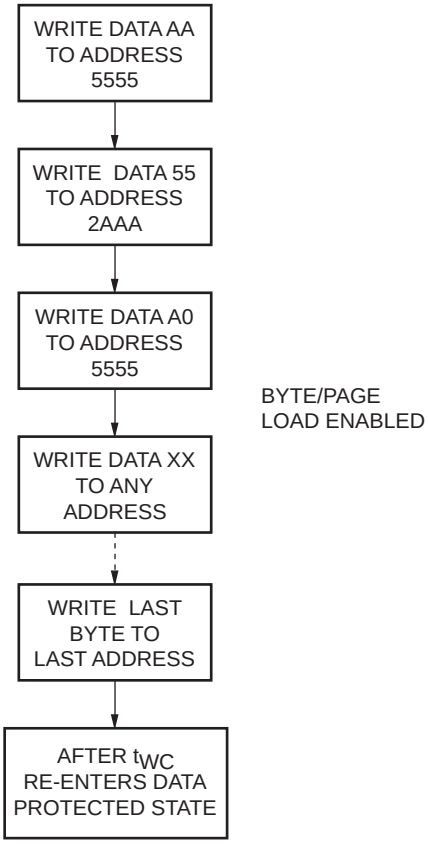
Figure 6. Timing Sequence—Byte or Page Write



*A_{17} & A_{18} select one of four devices on the module.

3873 FHD F14

Figure 7. Write Sequence for Software Data Protection

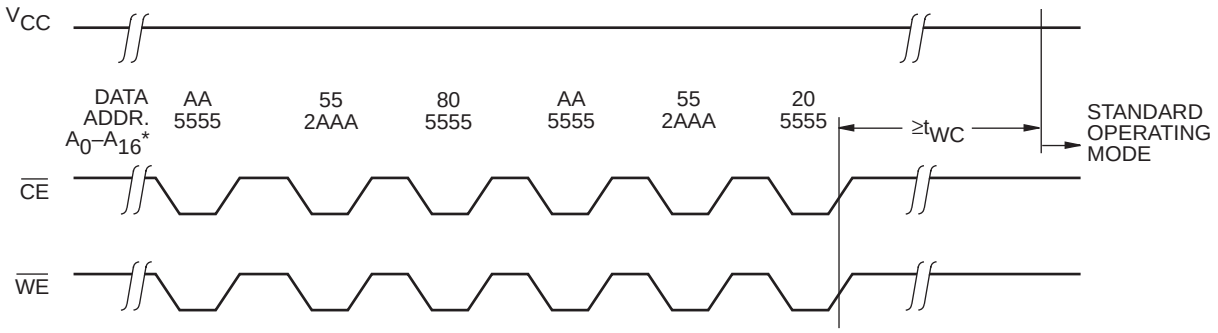


3873 FHD F15

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

RESETTING SOFTWARE DATA PROTECTION

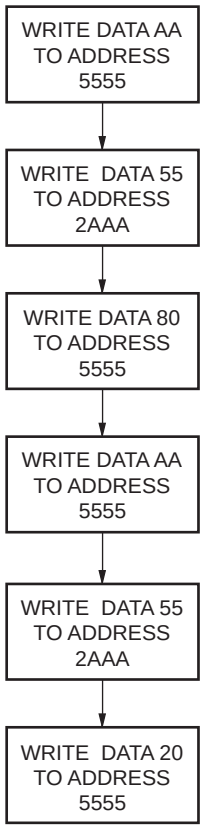
Figure 8. Reset Software Data Protection Timing Sequence



*A_{17} & A_{18} select one of four devices on the module.

3873 FHD F16

Figure 9. Software Sequence to Deactivate Software Data Protection



3873 FHD F17

In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

SYSTEM CONSIDERATIONS

Because the XM28C040 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C040 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be place between V_{CC} and V_{SS} for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 seconds) ..... 300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

XM28C040 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		80	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5MHz
I_{SB}	V_{CC} Current (Standby)		5	mA	$\overline{CE}$, A_{17}, A_{18} = V_{CC} –0.3V All other inputs = V_{IH} All I/Os = OPEN
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}	Input LOW Voltage	–1	0.8	V	
V_{IH}	Input HIGH Voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = –400µA

3873 PGM T02.2

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-up to Initiation of Read Operation	100	ms
t_{PUW}(2)	Power-up to Initiation of Write Operation	5	ms

3873 PGM T03

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	50	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	50	pF	V_{IN} = 0V

3873 PGM T04.1

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

3873 PGM T05.1

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

3873 PGM T06

A.C. CHARACTERISTICS

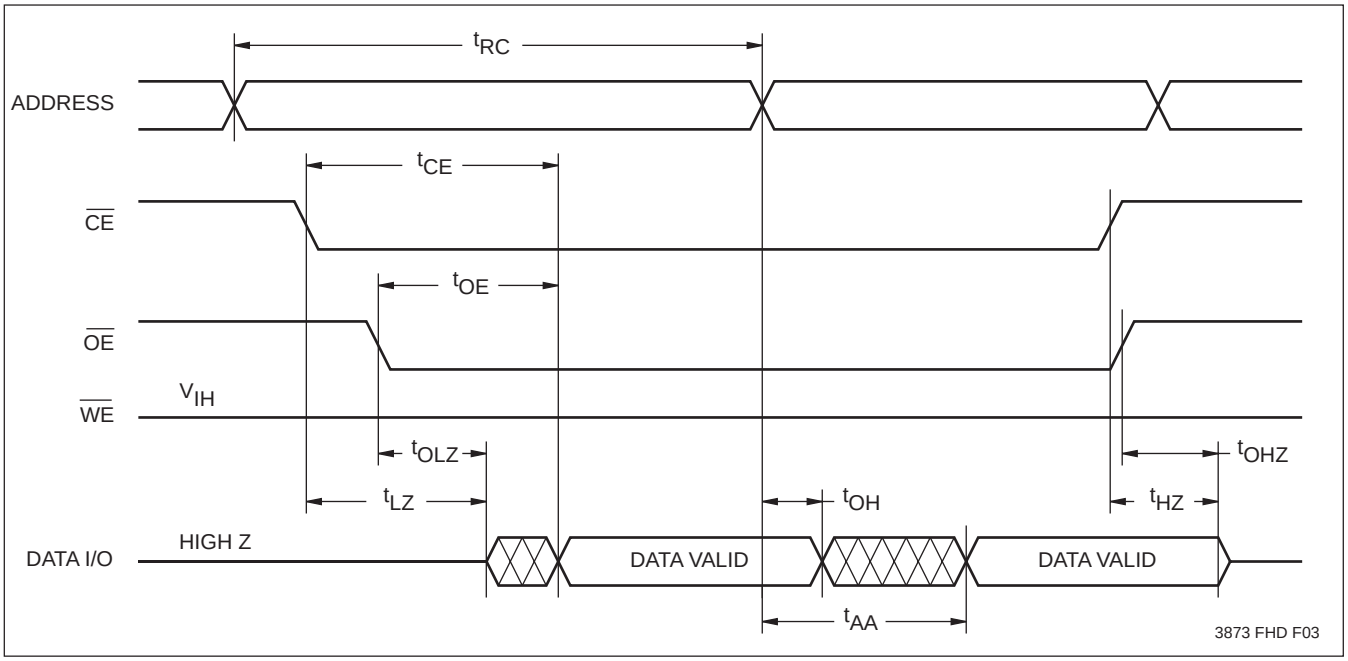
XM28C040 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C040M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

		XM28C040-20		XM28C040-25		XM28C040		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		80		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		100		100		100	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		100		100		100	ns
t_{OH}	Output Hold From Address Change	0		0		0		ns

3873 PGM T07

Read Cycle



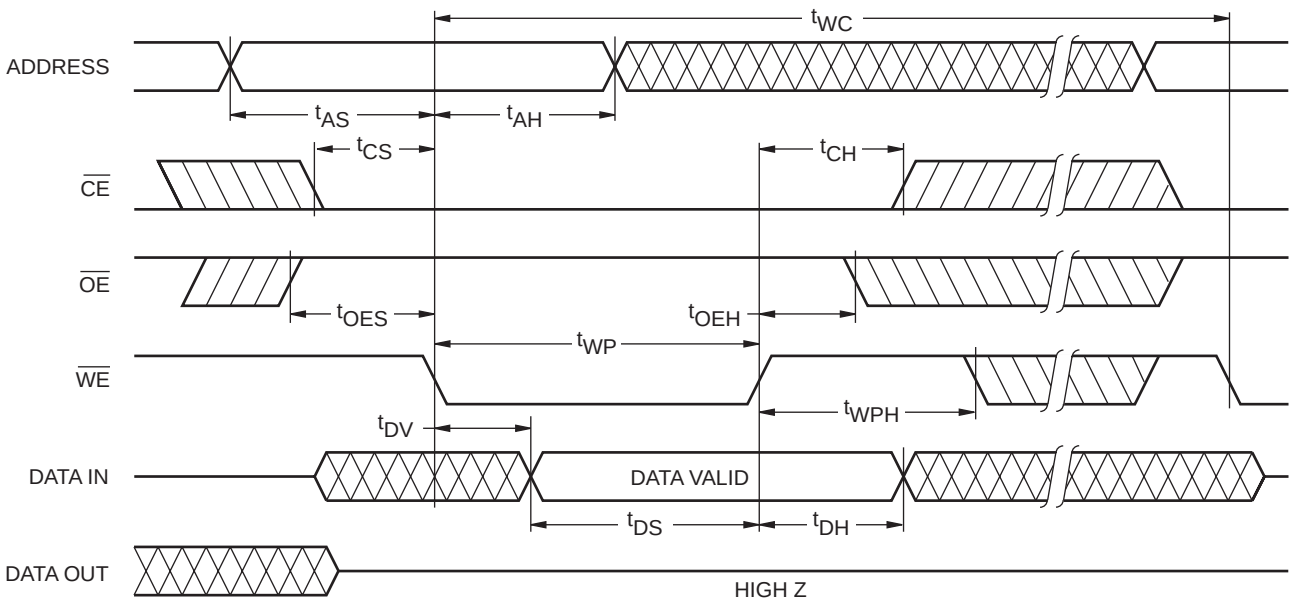
Note: (3) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	$\overline{WE}$ Controlled Write		$\overline{CE}$ Controlled Write (4)		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	125		125		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	$\overline{CE}$ Pulse Width	125		100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		35		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		125		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		100		ns
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	10		35		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	0.3	100	0.3	100	µs

3873 PGM T08.1

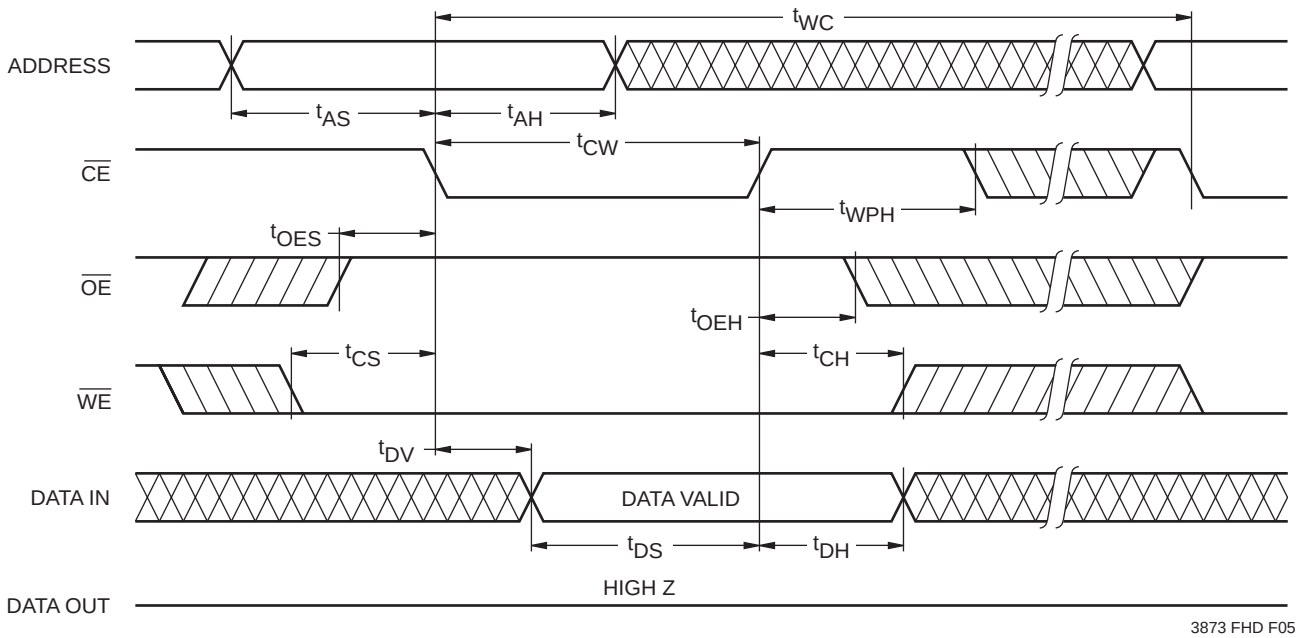
$\overline{WE}$ Controlled Write Cycle



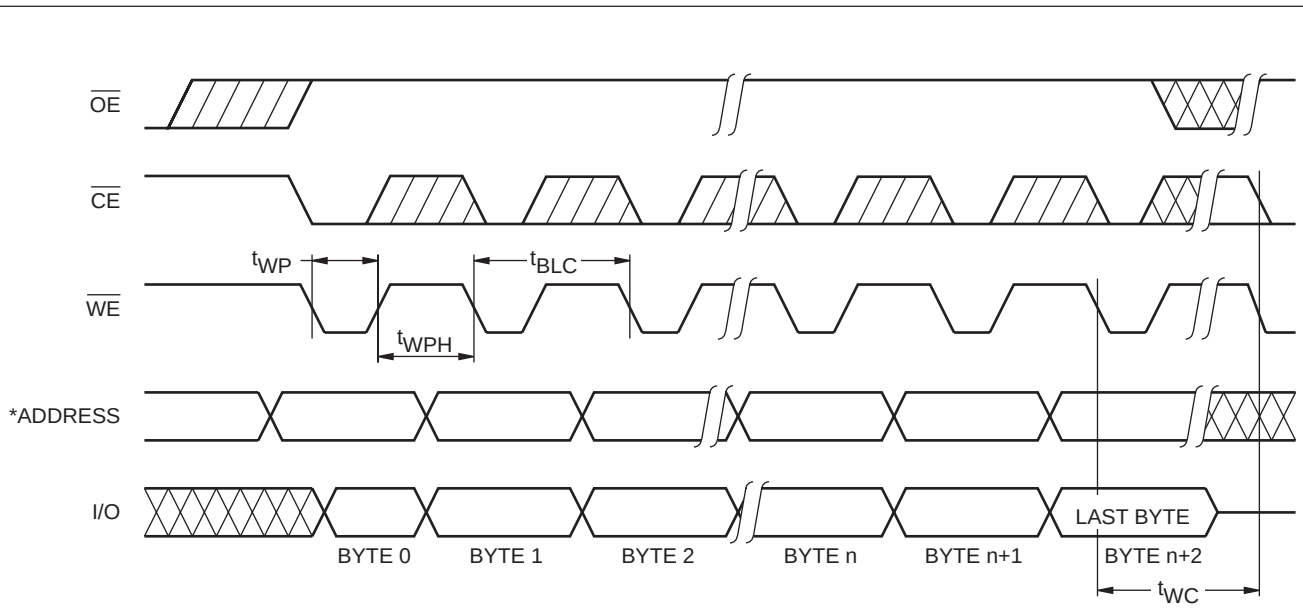
3873 FHD F04

Note: (4) Due to the inclusion of the decoder IC on board the module the $\overline{WE}$ and $\overline{CE}$ write controlled timings will vary. When utilizing the $\overline{CE}$ controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a $\overline{WE}$ controlled write operation $\overline{CE}$ must be a minimum 125ns to accommodate the additional setup time required.

$\overline{CE}$ Controlled Write Cycle

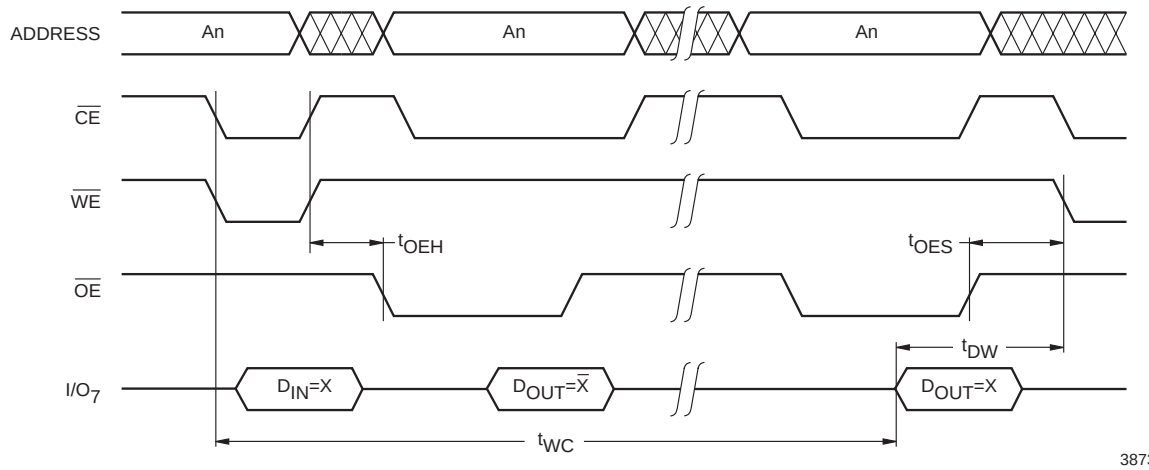


Page Write Cycle



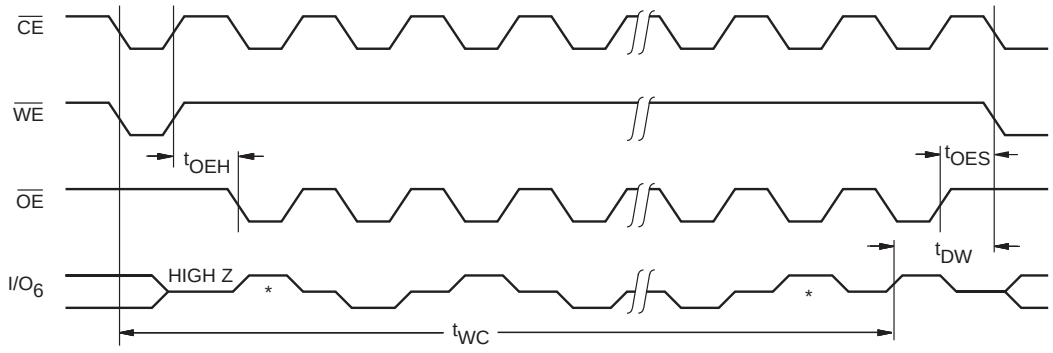
*For each successive write within the page write operation, A_7–A_{18} should be the same or writes to an unknown address could occur.

$\overline{\text{DATA}}$ Polling Timing Diagram



3873 FHD F07

Toggle Bit Timing Diagram



* Starting and ending state of I/O_6 will vary, depending upon actual t_{WC}.

3873 FHD F08

MultiPlane Architecture

The design of the XM28C040 has implemented a multiplane architecture. That is, there are four independent 128K x 8 memory spaces or planes, each selected by its own chip enable input via the on-board decoder chip. This architecture can be utilized in a number of ways.

Separate Data and Program Memory Spaces

The multiplane concept allows the system to write to one plane of the module and still be able to read (continue executing code) from the module, utilizing any plane not performing a write operation.

This concept of separate data and program spaces can be expanded by providing a simple off-module circuit that will disable writes to predetermined portions of memory. A very basic version is shown in the Functional Diagram. Whenever A_{18} is HIGH, the $\overline{WE}$ input is forced HIGH, write protecting one half the module. This half would be reserved for read only program store while the other half would be available for read and write data store.

Expanded Sequential Page Lengths

A standard system implementation would be decoding externally the module's chip enable and then wiring each address of the module to its corresponding address line in the system. This would effectively provide the system a memory organized as four separate memory planes with a sequential page address space of 256 bytes.

In an application such as data logging, the most efficient method of logging the data is in a sequential manner. If the data come in bursts that exceed 256 bytes in length a longer page might be desirable. By swapping address lines externally the effective page length can be expanded to 1024 bytes. Refer to the table below for a matrix illustrating the various page length options.

TABLE 1. ADDRESS TRANSLATION MATRIX

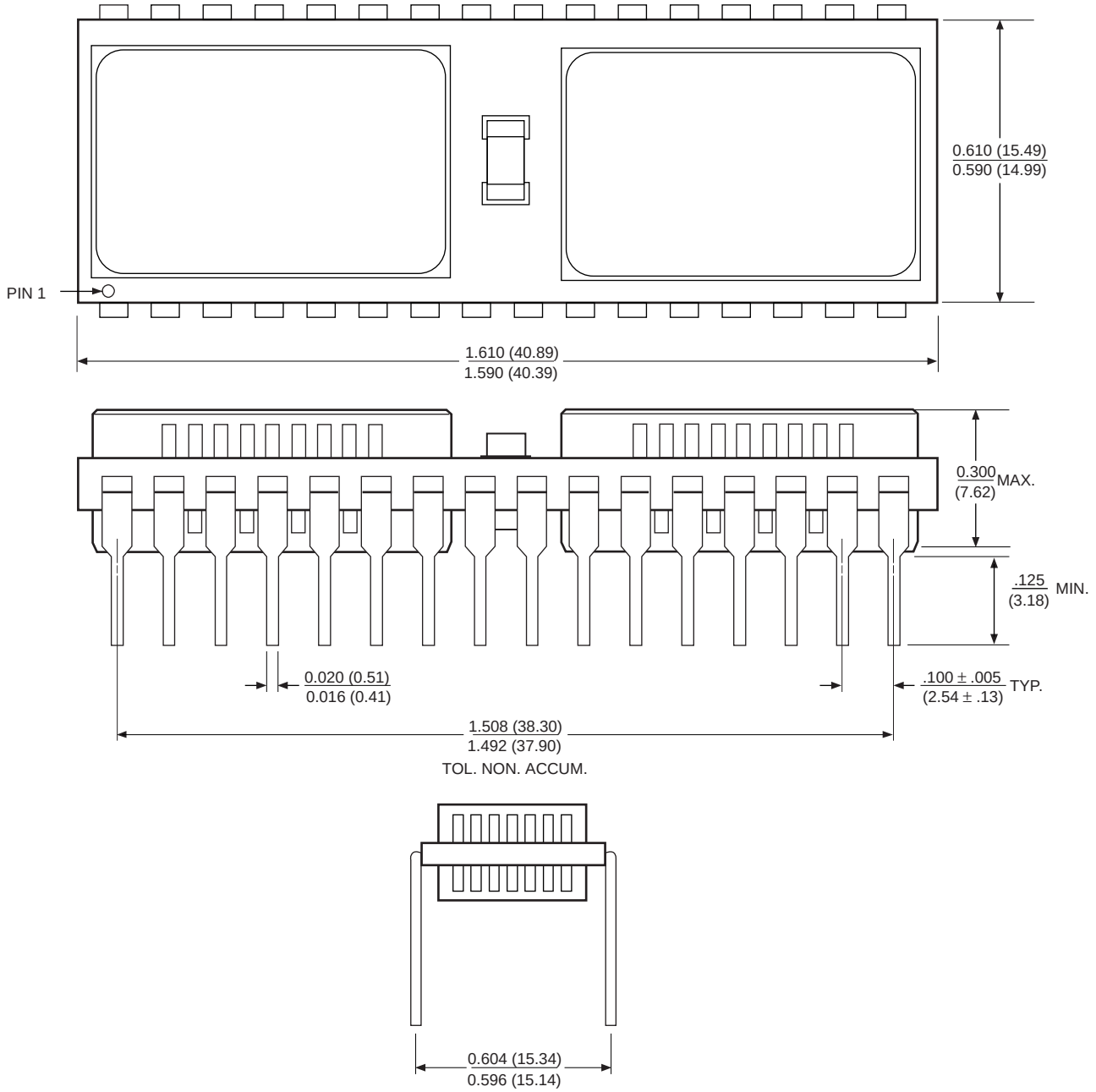
	Module Address Inputs				Page Size	Effective No. of Planes
	A_0-A_7	A_8-A_{16}	A17	A_{18}		
System Address Lines	A0-A7	A8-A16	A17	A18	256	4
	A0-A7	A9-A17	A8	A18	512	2
	A0-A7	A10-A18	A8	A9	1024	1

3873 PGM T09

Note: The user should be aware the overall I_{CC} of the module will increase as more individual components on the module are activated.

PACKAGING INFORMATION

32-PIN DUAL-IN-LINE MODULE USING
STRETCHED CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

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ORDERING INFORMATION
XM28C040: 512K X 8 CMOS E^{2}PROM Module