Winbond Electronics Corp.

4-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W741L240 is a high-performance 4-bit microcontroller (μC) that provides an LCD driver. The device contains a 4-bit ALU, a 8-bit timers, a divider, a 24 × 4 LCD driver, and three 4-bit I/O ports. There are also three interrupt sources and 8-level subroutine nesting for interrupt applications. The W741L240 operates on low voltage and very low current and has two power reduction modes, hold mode and stop mode, which help to minimize power dissipation.

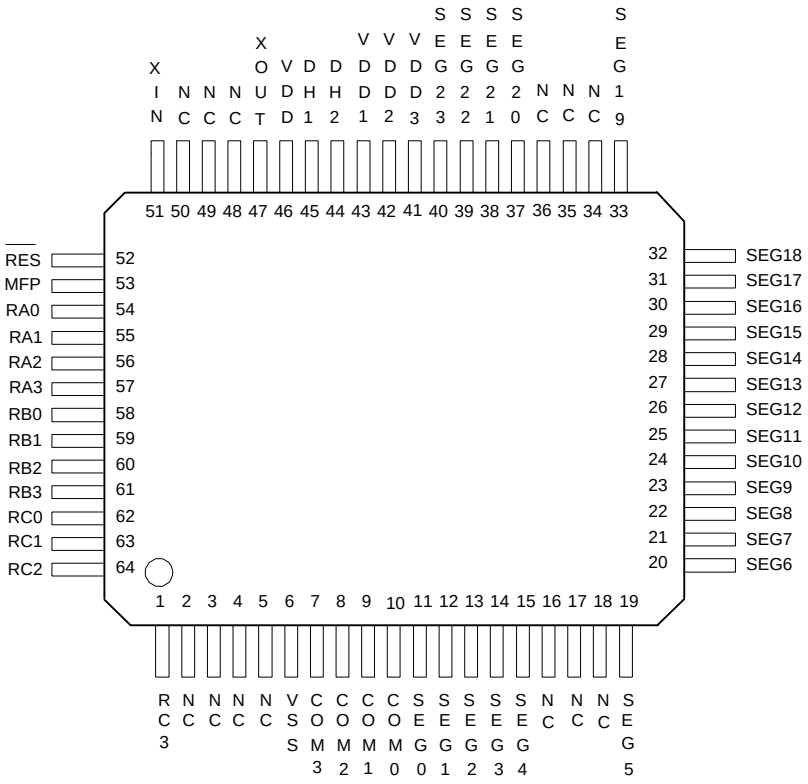
The W741L240 is suitable for caculators, simple watches and clocks, multiple I/O products, keyboard controllers, speech synthesis LSI controllers, and other products.

FEATURES

- Operating voltage: 1.2V to 1.8V (LCD drive voltage: 3.0 or 4.5V)
- Crystal/RC oscillation circuit selectable by code option for system clock
- Crystal oscillator: 32.768 KHz only
- RC oscillator: 1 MHz (maximum)
  - High-frequency (400 KHz to 1 MHz) or low-frequency (below 400 KHz) oscillation option must be determined by the code option.
  - In RC mode, attention must be paid to the high/low frequency oscillation option, because the LCD driver frequency is related to this option.
- Memory
  - 2048 × 16 bit program ROM (shared with 2K × 4 bit look-up table)
  - 64 × 4 bit data RAM (shared with 16 working registers)
  - 24 × 4 LCD data RAM
- 13 input/output pins
  - Ports for input only: 1 port/4 pins
  - Input/output ports: 2 ports/8 pins
  - MFP output pin: 1 pin (MFP)
- Power-down mode
  - Hold function: no operation (except for oscillator)
  - Stop function: no operation (including oscillator)
- Three types of interrupts
  - Two internal interrupts (Divider 0, Timer 1)
  - One external interrupts (Port RC)
- LCD driver output
  - 24 segment × 4 common
  - Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias) driving mode can be selected

- MFP output pin
  - Output is software selectable as modulating or nonmodulating frequency
  - Works as frequency output specified by Timer 1
- Built-in 14-bit clock frequency divider circuit
- One built-in 8-bit programmable countdown timers
  - Timer 1: Offers auto-reload function and one of two internal clock frequencies (FOSC or FOSC/64) can be selected (output through MFP pin)
- Built-in 18/14-bit watchdog timer selectable for system reset
- Powerful instruction set: 100 instructions
- 8-level subroutine (include interrupt) nesting
- Up to 4 μS instruction cycle (with 1 MHz operating frequency)
- Packaged in 64-pin QFP

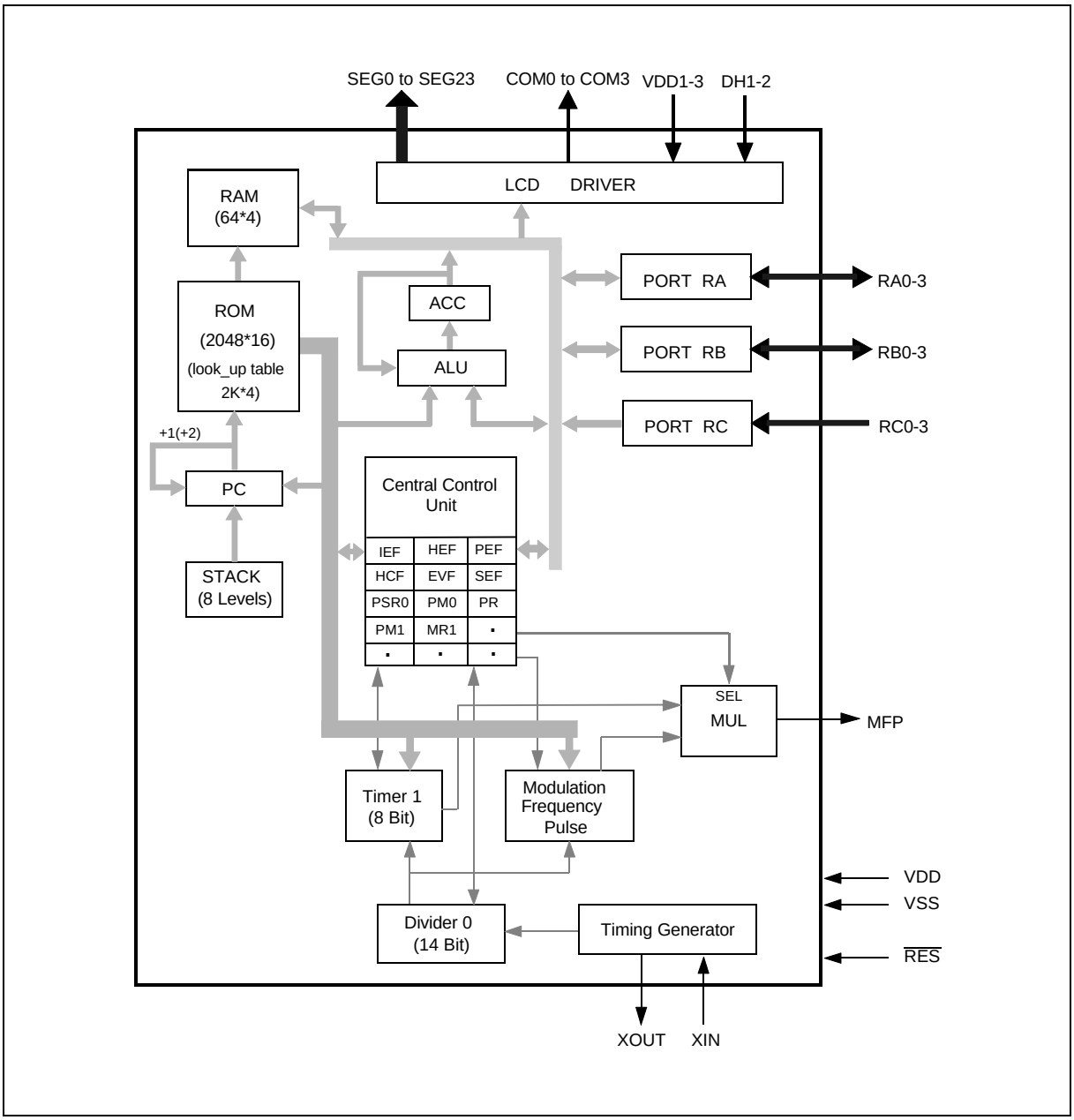
PIN CONFIGURATION



PIN DESCRIPTION

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>FUNCTION</th></tr>
<tr><td>XIN</td><td>I</td><td>Input pin for oscillator.
Connected to crystal or resistor to generate system clock by code option.</td></tr>
<tr><td>XOUT</td><td>O</td><td>Output pin for oscillator.
Connected to crystal or resistor to generate system clock by code option.</td></tr>
<tr><td>RA0–RA3</td><td>I/O</td><td>Input/Output port.
Input/output mode specified by port mode 1 register (PM1).</td></tr>
<tr><td>RB0–RB3</td><td>I/O</td><td>Input/Output port.
Input/output mode specified by port mode 2 register (PM2).</td></tr>
<tr><td>RC0–RC3</td><td>I</td><td>4-bit port for input only.
Each pin has an independent interrupt capability.</td></tr>
<tr><td>MFP</td><td>O</td><td>Output pin only.
This pin can output modulating or nonmodulating frequency, or Timer 1 clock output specified by mode register 1 (MR1).</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>System reset pin with pull-high resistor.</td></tr>
<tr><td>SEG0–SEG23</td><td>O</td><td>LCD segment output pins.
Also can be used as DC output ports specified by code option.</td></tr>
<tr><td>COM0–COM3</td><td>O</td><td>LCD common signal output pins.
<table>
<tr><th></th><th>Static</th><th>1/2 Duty</th><th>1/3 Duty</th><th>1/4 Duty</th></tr>
<tr><td>COM0</td><td>Used</td><td>Used</td><td>Used</td><td>Used</td></tr>
<tr><td>COM1</td><td>Not Used</td><td>Used</td><td>Used</td><td>Used</td></tr>
<tr><td>COM2</td><td>Not Used</td><td>Not Used</td><td>Used</td><td>Used</td></tr>
<tr><td>COM3</td><td>Not Used</td><td>Not Used</td><td>Not Used</td><td>Used</td></tr>
</table>
The LCD alternating frequency can be selected by code option.</td></tr>
<tr><td>DH1, DH2</td><td>I</td><td>Connection terminals for voltage doubler (halver) capacitor.</td></tr>
<tr><td>V_{DD1}, V_{DD2}, V_{DD3}</td><td>I</td><td>Positive (+) supply voltage terminal.
Refer to Functional Description.</td></tr>
<tr><td>V_{DD}</td><td>I</td><td>Positive power supply (+).</td></tr>
<tr><td>V_{SS}</td><td>I</td><td>Negative power supply (-).</td></tr>
</table>

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Program Counter (PC)

Organized as an 11-bit binary counter (PC0 to PC10), the program counter generates the addresses of the 2048 × 16 on-chip ROM containing the program instruction words. When jump or subroutine call instructions or interrupt or initial reset conditions are to be executed, the address corresponding to the instruction will be loaded into the program counter. The format used is shown below.

ITEM	ADDRESS	INTERRUPT PRIORITY
Initial Reset	000H	-
INT 0 (Divider 0)	004H	1st
INT 2 (Port RC)	00CH	2nd
INT 7 (Timer 1)	020H	3rd
JP Instruction	XXXH	-
Subroutine Call	XXXH	-

Stack Register (STACK)

The stack register is organized as 11 bits × 8 levels (first-in, last-out). When either a call subroutine or an interrupt is executed, the program counter will be pushed onto the stack register automatically. At the end of a call subroutine or an interrupt service subroutine, the RTN instruction must be executed to pop the contents of the stack register into the program counter. When the stack register is pushed over the eighth level, the contents of the first level will be lost. In other words, the stack register is always eight levels deep.

Program Memory (ROM)

The read-only memory (ROM) is used to store program codes; the look-up table is arranged as 2048 × 4 bits. The first three quarters of ROM (000H to 5FFH) are used to store instruction codes only, but the last quarter (600H to 7FFH) can store both instruction codes and the look-up table. Each look-up table element is composed of 4 bits, so the look-up table can be addressed up to 2048 elements. There are two registers (TABL and TABH) to be used in look-up table addressing and they are controlled by MOV TABH, R and MOV TABL, R instructions. When the instruction MOVC R is executed, the contents of the look-up table location address specified by TABH, TABL and ACC will be read and transfered to the data RAM. Refer to the instruction table for more details. The organization of the program memory is shown in Figure 1.

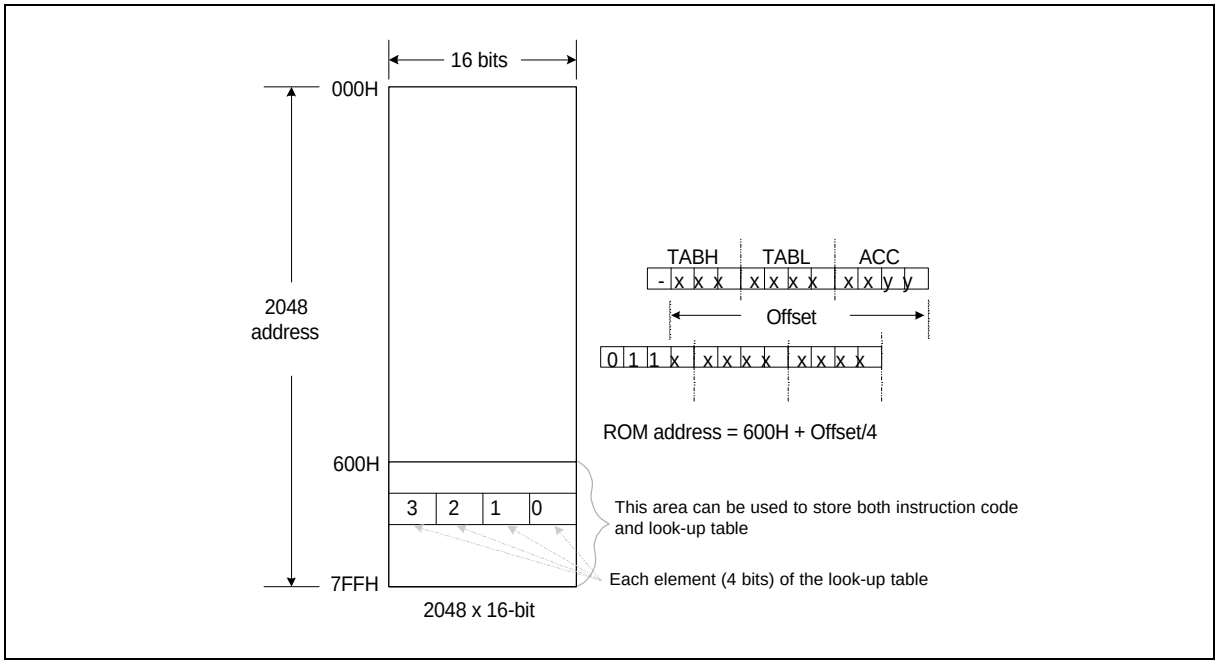


Figure 1. Program Memory Organization

Data Memory (RAM)

1. Architecture

The static data memory (RAM) used to store data is arranged as 64 × 4 bits. The data memory can be addressed directly or indirectly. The organization of the data memory is shown in Figure 2.

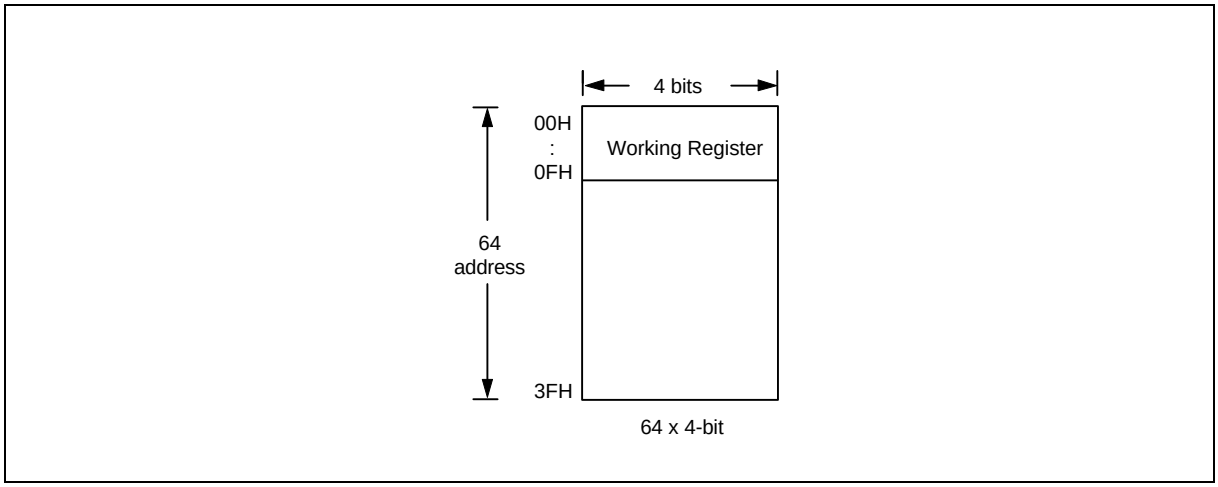


Figure 2. Data Memory Organization

The first sixteen addresses (00H to 0FH) in the data memory are known as the working registers (WR). The other data memory is used as general memory and cannot operate directly with immediate data. The relationship between data memory locations and the page register (PAGE) in indirect addressing mode is described in the next section.

2. Page Register (PAGE)

The page register is organized as a 4-bit binary register. The bit descriptions are as follows:

	3	2	1	0
PAGE	–	–	R/W	R/W

Note: R/W means read/write available.

Bit 3 and Bit2 are reserved.

Bit 1, Bit 0 are indirect addressing mode preselect bits:

00 = Page 0 (00H–0FH) 01 = Page 1 (10H–1FH)
10 = Page 2 (20H–2FH) 11 = Page 3 (30H–3FH)

Accumulator (ACC)

The accumulator (ACC) is a 4-bit register used to hold results from the ALU and transfer data between the memory, I/O ports, and registers.

Arithmetic and Logic Unit (ALU)

This is a circuit which performs arithmetic and logic operations. The ALU provides the following functions:

- Logic operations: ANL, XRL, ORL
- Branch decisions: JB0, JB1, JB2, JB3, JNZ, JZ, JC, JNC
- Shift operations: SHRC, RRC, SHLC, RLC
- Binary additions/subtractions: ADC, SBC, ADD, SUB, DEC, INC

After any of the above instructions are executed, the status of the carry flag (CF) and zero flag (ZF) is stored in the internal registers. CF can be read out by executing MOVA R, CF.

Clock Generator

The W741L240 provides a crystal or RC oscillation circuit selected by option codes to generate the system clock through external connections. If a crystal oscillator is used, a crystal must be connected to XIN and XOUT, and the capacitor must be connected if an accurate frequency is needed. When a crystal oscillator is used, only low-frequency clock (32 KHz) can be selected for the system clock by means of option codes. If the RC oscillator is used, a resistor in the range of 20 KΩ to 1.6 MΩ must be connected to XIN and XOUT, as shown in Figure 3. The system clock frequency range is from 32 KHz to 1 MHz. One machine cycle consists of a four-phase system clock sequence and can run up to 4 μS with a 1 MHz system clock.

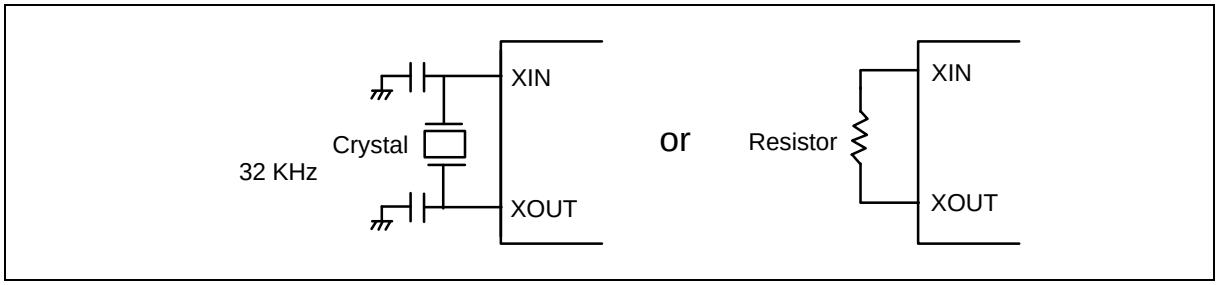


Figure 3. Oscillator Configuration

Divider 0

Divider 0 is organized as a 14-bit binary up-counter designed to generate periodic interrupts, as shown in Figure 4. When the system starts, the divider is incremented by each system clock (FOSC). When an overflow occurs, the divider event flag is set to 1 (EVF.0 = 1). Then, if the divider interrupt enable flag has been set (IEF.0 = 1), the interrupt is executed, while if the hold release enable flag has been set (HEF.0 = 1), the hold state is terminated. In addition, the 4 MSB of the divider can be reset by executing the CLR DIVR0 instruction.

Watchdog Timer (WDT)

The watchdog timer (WDT) is organized as a 4-bit up counter and is designed to protect the program from unknown errors. The WDT is enable when the corresponding option code bit of the WDT is set to 1. If the WDT overflows, the chip will be reset. At initial reset, the input clock of the WDT is FOSC/1024. The input clock of the WDT can be switched to FOSC/16384 (or FOSC/1024) by executing the SET PMF, #08H (or CLR PMF, #08H) instruction. The contents of the WDT can be reset by the instruction CLR WDT. In normal operation, the application program must reset WDT before it overflows. A WDT overflow indicates that the operation is not under control and the chip will be reset. The WDT minimun overflow period is 468.75 mS when the system clock (FOSC) is 32 KHz and WDT clock input is FOSC/1024. When the corresponding option code bit of the WDT is set to 0, the WDT function is disabled. The organization of the Divider0 and watchdog timer is shown in Figure 4.

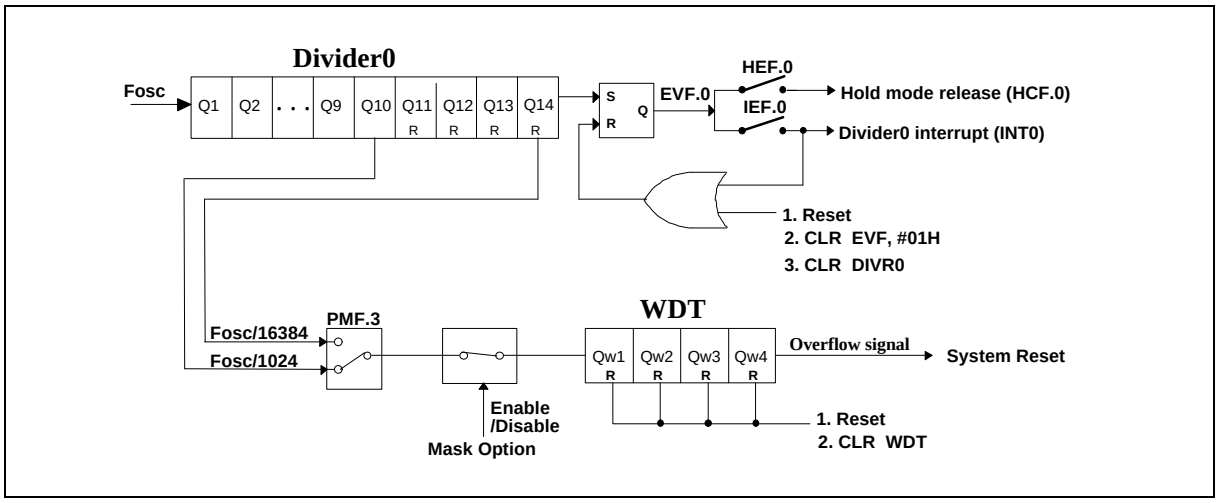


Figure 4. Organization of Divider 0 and Watchdog Timer

Timer/Counter

Timer 1 (TM1)

Timer 1 (TM1) is also a programmable 8-bit binary down counter, as shown in Figure 5. Timer 1 can be used as a counter to output an arbitrary frequency to the MFP pin. The input clock of Timer 1 can be one of two sources: FOSC/64, or FOSC. The source can be selected by setting bit 0 of mode register 1 (MR1). At initial reset, the Timer 1 clock input is FOSC. When the MOV TM1L, R or MOV TM1H, R instruction is executed, the specified data are loaded into the auto-reload buffer and the TM1 down-counting will be disabled (i.e. MR1.3 is reset to 0). If the bit 3 of MR1 is set (MR1.3 = 1), the contents of the auto-reload buffer will be loaded into the TM1 down counter, Timer 1 starts to down count, and the event flag 7 is reset (EVF.7 = 0). When the timer decrements to FFH, it will generate an underflow (EVF.7 = 1) and be auto-reloaded with the specified data, after which it will

continue to count down. An interrupt is executed if the interrupt enable flag 7 has been set to 1 (IEF.7 = 1), and the hold state is terminated if the hold mode release enable flag 7 is set to 1 (HEF.7 = 1). The specified frequency of Timer 1 can be delivered to the MFP output pin by programming bit 2 of MR1. Bit 3 of MR1 can be used to make Timer 1 stop or start counting.

If the Timer 1 clock input is F_T, then:

Desired Timer 1 interval = (preset value +1) / F_T

Desired frequency for MFP output pin = $F_T \div$ (preset value + 1) $\div$ 2 (Hz)

Preset value: Decimal number of Timer 1 preset value, and

F_{OSC}: Clock oscillation frequency

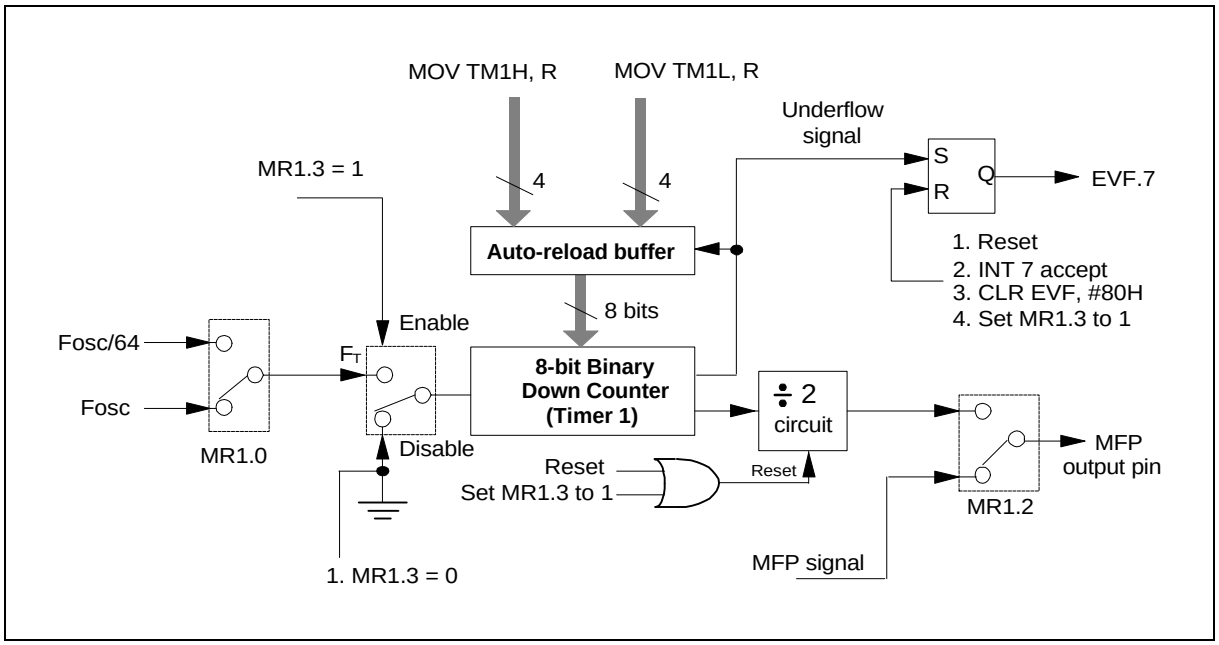


Figure 5. Organization of Timer 1

For example, when F_T equals 32768 Hz, depending on the preset value of TM1, the MFP pin will output a single tone signal in the tone frequency range from 64 Hz to 16384 Hz. The relation between the tone frequency and the preset value of TM1 is shown in the table below.

		3			4			5		
		Tone frequency	TM1 preset value & MFP frequency		Tone frequency	TM1 preset value & MFP frequency		Tone frequency	TM1 preset value & MFP frequency	
TONE	C	130.81	7CH	131.07	261.63	3EH	260.06	523.25	1EH	528.51
	C#	138.59	75H	138.84	277.18	3AH	277.69	554.37	1CH	564.96
	D	146.83	6FH	146.28	293.66	37H	292.57	587.33	1BH	585.14
	D#	155.56	68H	156.03	311.13	34H	309.13	622.25	19H	630.15
	E	164.81	62H	165.49	329.63	31H	327.68	659.26	18H	655.36
	F	174.61	5DH	174.30	349.23	2EH	372.36	698.46	16H	712.34
	F#	185.00	58H	184.09	369.99	2BH	390.09	739.99	15H	744.72
	G	196.00	53H	195.04	392.00	29H	420.10	783.99	14H	780.19
	G#	207.65	4EH	207.39	415.30	26H	443.81	830.61	13H	819.20
	A	220.00	49H	221.40	**440.00**	**24H**	**442.81**	880.00	12H	862.84
	A#	233.08	45H	234.05	466.16	22H	468.11	932.23	11H	910.22
	B	246.94	41H	248.24	493.88	20H	496.48	987.77	10H	963.76

Note: Central tone is A4 (440 Hz).

Mode Register 1 (MR1)

Mode Register 1 is organized as a 4-bit binary register (MR1.0 to MR1.3). MR1 can be used to control the operation of Timer 1. The bit descriptions are as follows:

	3	2	1	0
MR1	W	W	–	W

Note: W means write only.

Bit 0 = 0 The internal fundamental frequency of Timer 1 is FOSC.
= 1 The internal fundamental frequency of Timer 1 is FOSC/64.

Bit 1 Reserved

Bit 2 = 0 The specified waveform of the MFP generator is delivered at the MFP output pin.
= 1 The specified frequency of Timer 1 is delivered at the MFP output pin.

Bit 3 = 0 Timer 1 stops down-counting.
= 1 Timer 1 starts down-counting.

Interrupts

The W741L240 provides two internal interrupt sources (Divider 0, Timer 1) and one external interrupt sources (port RC). Vector addresses for each of the interrupts are located in the range of program memory (ROM) addresses 004H to 020H. The flags IEF, PEF, and EVF are used to control the interrupts. When EVF is set to "1" by hardware and the corresponding bits of IEF and PEF have been set by software, an interrupt is generated. When an interrupt occurs, all of the interrupts are inhibited until the EN INT or MOV IEF, #I instruction is invoked. The interrupts can also be disabled by executing the DIS INT instruction. When an interrupt is generated in hold mode, the hold mode will be released momentarily and the interrupt subroutine will be executed. After the RTN instruction is executed in an interrupt subroutine, the μC will enter hold mode again. The operation flow chart is shown in Figure 7. The control diagram is shown below.

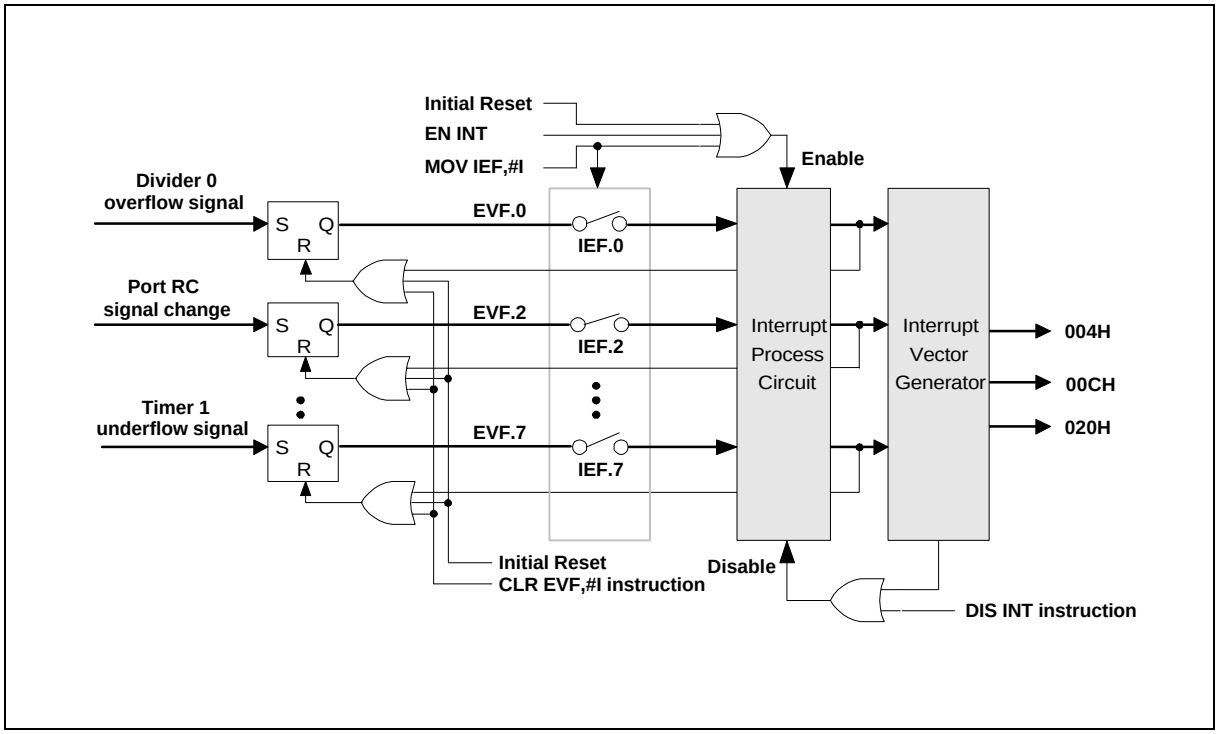


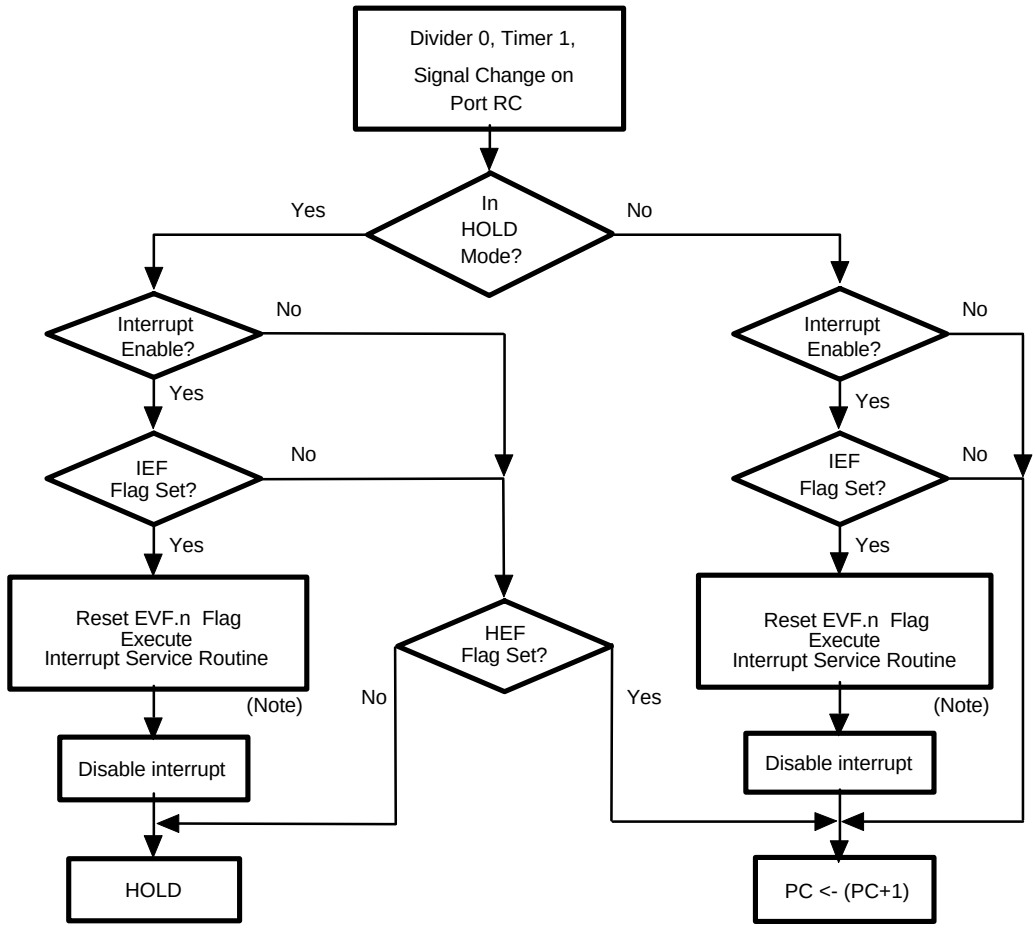
Figure 6. Interrupt Event Control Diagram

Stop Mode Operation

In stop mode, all operations of the μC cease (including the operation of the oscillator). The μC enters stop mode when the STOP instruction is executed and exits stop mode when an external trigger is activated (by a falling signal on the RC port). When the designated signal is accepted, the μC awakens and executes the next instruction (if the corresponding bits of IEF and PEF have been set, It will enter the interrupt service routine after stop mode released). To prevent erroneous execution, the NOP instruction should follow the STOP command.

Hold Mode Operation

In hold mode, all operations of the µC cease, except for the operation of the oscillator, timer, and LCD driver. The µC enters hold mode when the HOLD instruction is executed. The hold mode can be released in one of three ways: by the action of Timer 1, Divider 0, or the RC port. Before the device enters the hold mode, the HEF, PEF, and IEF flags must be set to define the hold mode release conditions. For more details, refer to the instruction-set table and the following flow chart.



Note : The bit of EVF corresponding to the interrupt request signal will be reset.

Figure 7. Hold Mode and Interrupt Operation Flow Chart

Hold Mode Release Enable Flag (HEF)

The hold mode release enable flag is organized as an 8-bit binary register (HEF.0 to HEF.7). The HEF is used to control the hold mode release conditions. It is controlled by the MOV HEF, #I instruction. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
HEF	w	–	–	–	–	w	–	w

Note: W means write only.

HEF.0 = 1 Overflow from Divider 0 causes hold mode to be released.

HEF.1 Reserved

HEF.2 = 1 Signal change at port RC causes hold mode to be released.

HEF.3, 4 Reserved

HEF.5, 6 Reserved

HEF.7 = 1 Underflow from Timer 1 causes hold mode to be released.

Interrupt Enable Flag (IEF)

The interrupt enable flag is organized as an 8-bit binary register (IEF.0 to IEF.7). These bits are used to control the interrupt conditions. It is controlled by the MOV IEF, #I instruction. When one of these interrupts is accepted, the corresponding bit of the event flag will be reset, but the other bits are unaffected. In interrupt subroutine, these interrupts will be disabled till the instruction MOV IEF, #I or EN INT is executed again. Besides, these interrupts can be disabled by executing DIS INT instruction. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
IEF	w	–	–	–	–	w	–	w

Note: W means write only.

IEF.0 = 1 Interrupt 0 is accepted by overflow from Divider 0.

IEF.1 Reserved

IEF.2 = 1 Interrupt 2 is accepted by a signal change on port RC.

IEF.3, 4 Reserved

IEF.5, 6 Reserved

IEF.7 = 1 Interrupt 7 is accepted by underflow from Timer 1.

Port Enable Flag (PEF)

The port enable flag is organized as a 4-bit binary register (PEF.0 to PEF.3). Before port RC may be used to release the hold mode or perform an interrupt function, the content of the PEF must be set first. The PEF is controlled by the MOV PEF, #I instruction. The bit descriptions are as follows:

	3	2	1	0
PEF	w	w	w	w

Note: W means write only.

PEF.0: Enable/disable the signal change on pin RC.0 to release hold mode or perform interrupt.

PEF.1: Enable/disable the signal change on pin RC.1 to release hold mode or perform interrupt.

PEF.2: Enable/disable the signal change on pin RC.2 to release hold mode or perform interrupt.

PEF.3: Enable/disable the signal change on pin RC.3 to release hold mode or perform interrupt.

Stop Mode Wake-up Enable Flag for Port RC (SEF)

The stop mode wake-up flag for port RC is organized as a 4-bit binary register (SEF.0 to SEF.3). Before port RC may be used to make the device exit the stop mode, the content of the SEF must be set first. The SEF is controlled by the MOV SEF, #I instruction. The bit descriptions are as follows:

	3	2	1	0
SEF	w	w	w	w

Note: W means write only.

SEF 0 = 1 Device will exit stop mode when falling edge signal is applied to pin RC.0.

SEF 1 = 1 Device will exit stop mode when falling edge signal is applied to pin RC.1.

SEF 2 = 1 Device will exit stop mode when falling edge signal is applied to pin RC.2.

SEF 3 = 1 Device will exit stop mode when falling edge signal is applied to pin RC.3.

Hold Mode Release Condition Flag (HCF)

The hold mode release condition flag is organized as an 8-bit binary register (HCF0 to HCF7). It indicates by which interrupt source the hold mode has been released, and it is loaded by hardware. The HCF can be read out by the MOVA R, HCFL and MOVA R, HCFH instructions. When any of the HCF bits is "1," the hold mode will be released and the HOLD instruction is invalid. The HCF can be reset by the CLR EVF, #I (EVF.n = 0) or MOV HEF, #I (HEF.n = 0) instructions. When EVF or HEF has been reset, the corresponding bit of HCF is reset simultaneously. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
HCF	–	–	w	–	–	w	–	w

Note: R means read only.

HCF.0 = 1 Hold mode was released by overflow from Divider 0.

HCF.1 Reservsd

HCF.2 = 1 Hold mode was released by a signal change on port RC.

HCF.3, 4 Reserved.

HCF.5 = 1 Hold mode was released by underflow from Timer 1.

HCF.6, 7 Reserved.

Event Flag (EVF)

The event flag is organized as a 8-bit binary register (EVF0 to EVF7). It is set by hardware and reset by the CLR EVF, #I instruction or the occurrence of an interrupt. The bit descriptions are as follows:

	7	6	5	4	3	2	1	0
EVF	w	–	–	–	–	w	–	w

Note: R means read only.

EVF.0 = 1 Overflow from Divider 0 occurred.

EVF.1 Reserved

EVF.2 = 1 Signal change on port RC occurred.

EVF.3, 4 Reserved

EVF.5, 6 Reserved

EVF.7 = 1 Underflow from Timer 1 occurred.

Parameter Flag (PMF)

The parameter flag is organized as a 4-bit binary register (PMF.0 to PMF.3). The PMF is controlled by the SET PMF, #I or CLR PMF, #I instruction. The bit descriptions are as follows:

	3	2	1	0
PMF	W	–	–	–

Note: W means write only.

Bit 0, Bit1, Bit2 Reserved

Bit 3 = 0 The fundamental frequency of the watchdog timer is FOSC/1024.

= 1 The fundamental frequency of the watchdog timer is FOSC/16384.

Port Mode 0 Register (PM0)

The port mode 0 register is organized as a 4-bit binary register (PM0.0 to PM0.3). PM0 can be used to determine the structure of the input/output ports; it is controlled by the MOV PM0, #I instruction. The bit descriptions are as follows:

	3	2	1	0
PM0	—	w	w	w

Note: W means write only.

Bit 0 = 0 RA port is CMOS output type.
Bit 0 = 1 RA port is NMOS open drain output type.
Bit 1 = 0 RB port is CMOS output type.
Bit 1 = 1 RB port is NMOS open drain output type.
Bit 2 = 0 RC port pull-high resistor is disabled.
Bit 2 = 1 RC port pull-high resistor is enabled.
Bit 3 Reserved

Port Mode 1 Register (PM1)

The port mode 1 register is organized as a 4-bit binary register (PM1.0 to PM1.3). PM1 can be used to control the input/output mode of port RA. PM1 is controlled by the MOV PM1, #I instruction. The bit descriptions are as follows:

	3	2	1	0
PM1	w	w	w	w

Note: W means write only.

Bit 0 = 0 RA.0 works as output pin. Bit 0 = 1 RA.0 works as input pin.
Bit 1 = 0 RA.1 works as output pin. Bit 1 = 1 RA.1 works as input pin.
Bit 2 = 0 RA.2 works as output pin. Bit 2 = 1 RA.2 works as input pin.
Bit 3 = 0 RA.3 works as output pin. Bit 3 = 1 RA.3 works as input pin.

After initial reset, port RA is in input mode (PM1 = 1111B).

Port Mode 2 Register (PM2)

The port mode 2 register is organized as a 4-bit binary register (PM2.0 to PM2.3). PM2 can be used to control the input/output mode of port RB. PM2 is controlled by the MOV PM2, #I instruction. The bit descriptions are as follows:

	3	2	1	0
PM2	w	w	w	w

Note: W means write only.

Bit 0 = 0 RB.0 works as output pin. Bit 0 = 1 RB.0 works as input pin.

Bit 1 = 0 RB.1 works as output pin. Bit 1 = 1 RB.1 works as input pin.

Bit 2 = 0 RB.2 works as output pin. Bit 2 = 1 RB.2 works as input pin.

Bit 3 = 0 RB.3 works as output pin. Bit 3 = 1 RB.3 works as input pin.

After initial reset, port RB is in input mode (PM2 = 1111B).

Reset Function

The W741L240 is reset either by a power-on reset or by using the external $\overline{\text{RES}}$ pin. The initial state of the W741L240 after the reset function is executed is described below.

Program Counter (PC)	000H
TM1	Reset
MR1, PM0, PAGE, PMF registers	Reset
PM1, PM2 registers	Set (1111B)
PSR0 register	Reset
IEF, HEF, HCF, PEF, EVF, SEF flags	Reset
Timer 1 input clock	FOSC
MFP output	Low
Input/output ports RA,RB	Input mode
RA & RB ports output type	CMOS type
RC ports pull-high resistors	Disabled
Input clock of the watchdog timer	FOSC/1024
LCD display	OFF
Segment output mode	LCD drive output

Input/Output Ports RA, RB

Port RA consists of pins RA.0 to RA.3 and port RB consists of pins RB.0 to RB.3. After initial reset, input/output ports RA and RB are both in input mode. When RA and RB are used as output ports, CMOS or NMOS open drain output type can be selected by the PM0 register. Each pin of port RA or RB can be specified as input or output mode independently by the PM1 and PM2 registers. The MOVA R, RA or MOVA R, RB instructions operate the input functions and the MOV RA, R or MOV RB, R operate the output functions. For more details, refer to the instruction table and Figure 8.

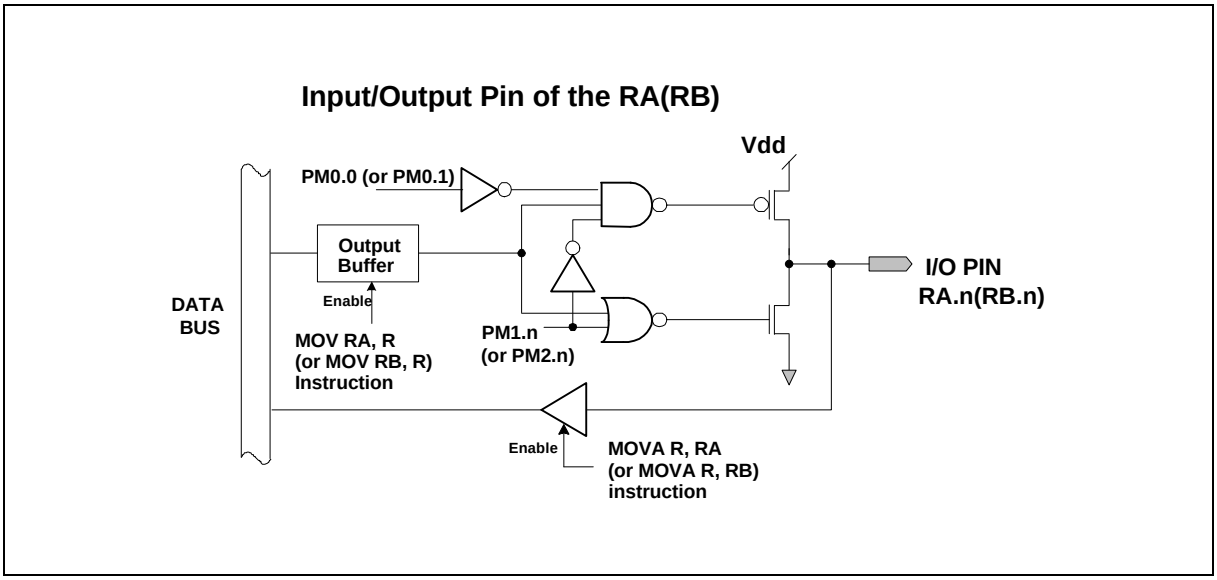


Figure 8. Architecture of Input/Output Pins

Input Ports RC

Port RC consists of pins RC.0 to RC.3. Each pin of port RC can be connected to a pull-up resistor, which is controlled by the port mode 0 register (PM0). When the PEF, HEF, and IEF corresponding to the RC port are set, a signal change on the specified pins of port RC will execute the hold mode release or interrupt subroutine. Port status register 0 (PSR0) records the status of ports RC, i.e., any signal changes on the pins that make up the port. PSR0 can be read out and cleared by the MOV R, PSR0, and CLR PSR0 instructions. In addition, the falling edge signal on the pin of port RC specified by the instruction MOV SEF, #I will cause the device to exit the stop mode. Refer to Figure 9 and the instruction table for more details. The RD port is used as input port only, it has no hold mode release, wake-up stop mode or interrupt functions.

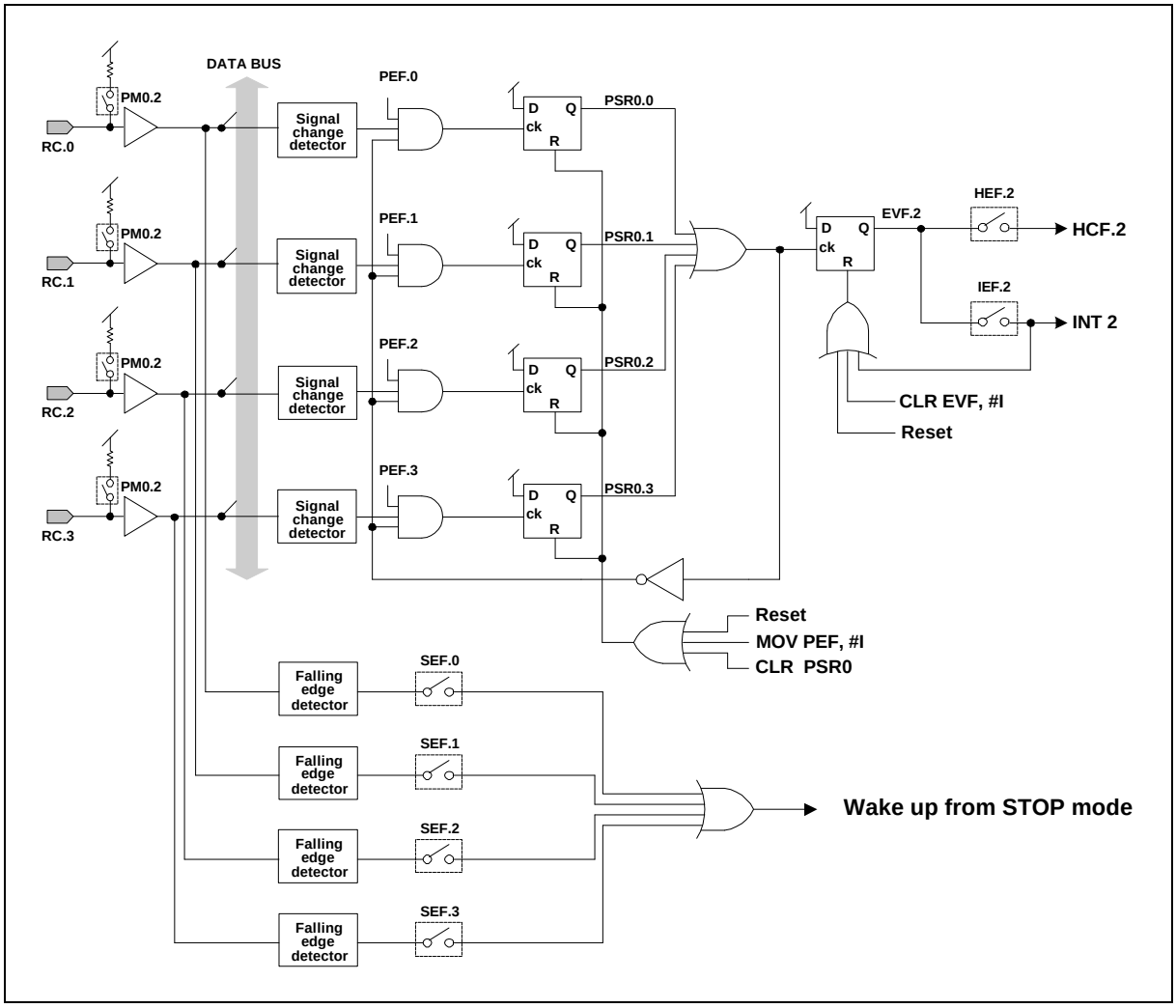


Figure 9. Architecture of Input Ports RC

Port Status Register 0 (PSR0)

Port status register 0 is organized as a 4-bit binary register (PSR0.0 to PSR0.3). PSR0 can be read or cleared by the MOVA R, PSR0, and CLR PSR0 instructions. The bit descriptions are as follows:

	3	2	1	0
PSR0	R	R	R	R

Note: R means read only.

Bit 0 = 1 Signal change on RC.0.
Bit 1 = 1 Signal change on RC.1.
Bit 2 = 1 Signal change on RC.2.
Bit 3 = 1 Signal change on RC.3.

MFP Output Pin (MFP)

The MFP output pin can output the Timer 1 clock or the modulation frequency; the output of the pin is determined by mode register 1 (MR1). The organization of MR1 is shown in Figure 6. When bit 2 of MR1 is reset to "0," the MFP output can deliver a modulation output in any combination of one signal from among DC, 4096 Hz, 2048 Hz, and one or more signals from among 128 Hz, 64 Hz, 8 Hz, 4 Hz, 2 Hz, or 1 Hz (when using a 32.768 KHz system clock). The MOV MFP, #I instruction is used to specify the modulation output combination. The data specified by the 8-bit operand and the MFP output pin are shown as below:

(FOSC = 32.768 KHz)

R7 R6	R5	R4	R3	R2	R1	R0	FUNCTION
0 0	0	0	0	0	0	0	Low level
	0	0	0	0	0	1	128 Hz
	0	0	0	0	1	0	64 Hz
	0	0	0	1	0	0	8 Hz
	0	0	1	0	0	0	4 Hz
	0	1	0	0	0	0	2 Hz
	1	0	0	0	0	0	1 Hz
0 1	0	0	0	0	0	0	High level
	0	0	0	0	0	1	128 Hz
	0	0	0	0	1	0	64 Hz
	0	0	0	1	0	0	8 Hz
	0	0	1	0	0	0	4 Hz
	0	1	0	0	0	0	2 Hz
	1	0	0	0	0	0	1 Hz
1 0	0	0	0	0	0	0	2048 Hz
	0	0	0	0	0	1	2048 Hz * 128 Hz
	0	0	0	0	1	0	2048 Hz * 64 Hz
	0	0	0	1	0	0	2048 Hz * 8 Hz
	0	0	1	0	0	0	2048 Hz * 4 Hz
	0	1	0	0	0	0	2048 Hz * 2 Hz
	1	0	0	0	0	0	2048 Hz * 1 Hz
1 1	0	0	0	0	0	0	4096 Hz
	0	0	0	0	0	1	4096 Hz * 128 Hz
	0	0	0	0	1	0	4096 Hz * 64 Hz
	0	0	0	1	0	0	4096 Hz * 8 Hz
	0	0	1	0	0	0	4096 Hz * 4 Hz
	0	1	0	0	0	0	4096 Hz * 2 Hz
	1	0	0	0	0	0	4096 Hz * 1 Hz

LCD Controller/Driver

The W741L240 can directly drive an LCD with 24 segment output pins and 4 common output pins for a total of 24 × 4 dots. Option codes can be used to select one of five options for the LCD driving mode: static, 1/2 bias 1/2 duty, 1/2 bias 1/3 duty, 1/3 bias 1/3 duty, or 1/3 bias 1/4 duty (see Figure 12). The alternating frequency of the LCD can be set as Fw/64, Fw/128, Fw/256, or Fw/512. The structure of the LCD alternating frequency (F_{LCD}) is shown in the figure below.

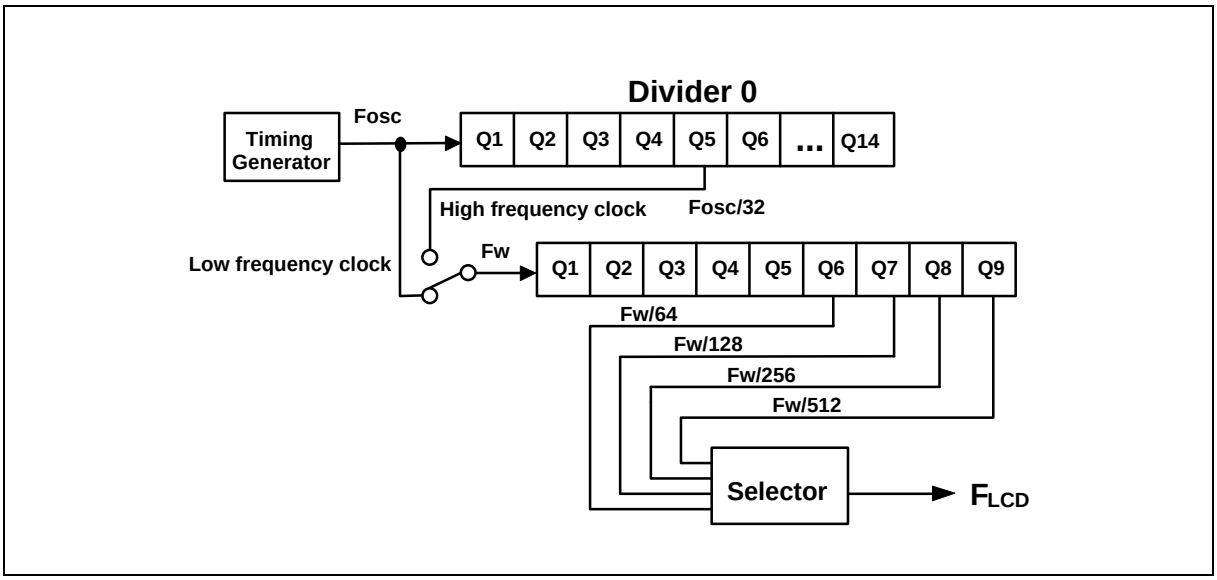


Figure 11. LCD Alternating Frequency (F_{LCD}) Circuit Diagram

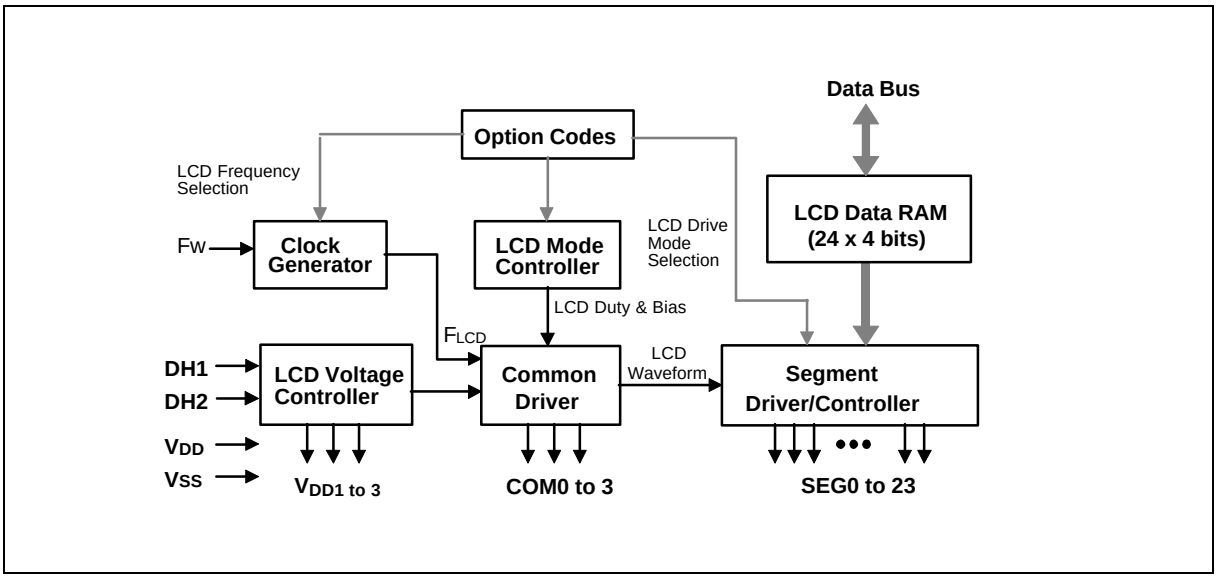


Figure 12. LCD Driver/Controller Circuit Diagram

When Fw = 32.768 KHz, the LCD frequency is as shown in the table below.

LCD FREQUENCY	STATIC	1/2 DUTY	1/3 DUTY	1/4 DUTY
Fw/512 (64 Hz)	64	32	21	16
Fw/256 (128 Hz)	128	64	43	32
Fw/128 (256 Hz)	256	128	85	64
Fw/64 (512 Hz)	512	256	171	128

Corresponding to the 24 LCD drive output pins, there are 24 LCD data RAM segments (LCDR00 to LCDR17). Instructions such as MOV LCDR, #I; MOV WR, LCDR; MOV LCDR, WR; and MOV LCDR, ACC are used to control the LCD data RAM. The data in the LCD data RAM are transferred to the segment output pins automatically without program control. When the bit value of the LCD data RAM is "1," the LCD is turned on. When the bit value of the LCD data RAM is "0," the LCD is turned off. The contents of the LCD data RAM (LCDR) are sent out through the segment 0 to segment 23 pins by a direct memory access. The relationship between the LCD data RAM and segment/common pins is shown below.

		COM3	COM2	COM1	COM0
LCD data RAM	Output pin	bit 3	bit 2	bit 1	bit 0
LCDR00	SEG0	0/1	0/1	0/1	0/1
LCDR01	SEG1	0/1	0/1	0/1	0/1
. . .	. . .	. . .	. . .	. . .	. . .
LCDR16	SEG22	0/1	0/1	0/1	0/1
LCDR17	SEG23	0/1	0/1	0/1	0/1

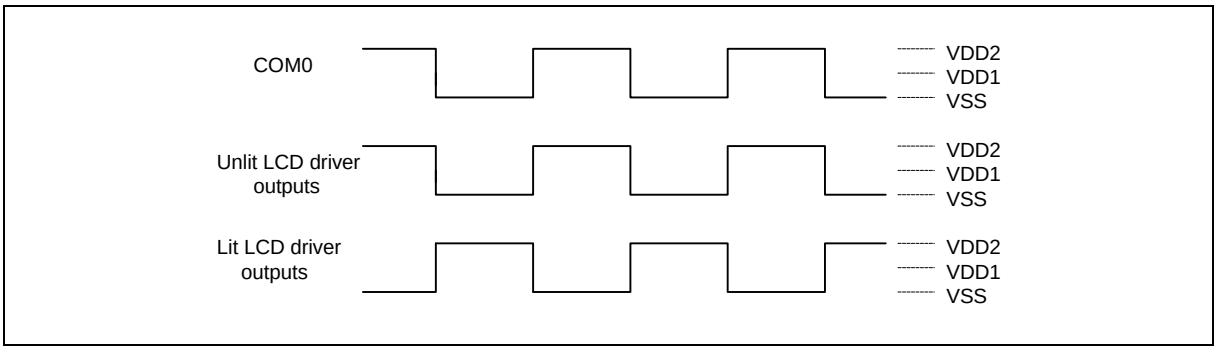
The LCDON instruction turns the LCD display on (even in HOLD mode), and the LCDOFF instruction turns the LCD display off. At initial reset, all the LCD segments are lit. When the initial reset state ends, the LCD display is turned off automatically. To turn on the LCD display, the instruction LCDON must be executed. The relationship between the LCD drive mode and the maximum number of drivable LCD segments is shown below.

LCD DRIVE MODE	MAX. NUMBER OF DRIVABLE LCD SEGMENTS	CONNECTION AT POWER INPUT
Static	24 (COM1)	Connect V_{DD3}, V_{DD2} to V_{DD1}
1/2 bias 1/2 duty	48 (COM1–COM2)	Connect V_{DD3} to V_{DD2}
1/2 bias 1/3 duty	72 (COM1–COM3)	Connect V_{DD3} to V_{DD2}
1/3 bias 1/3 duty	72 (COM1–COM3)	-
1/3 bias 1/4 duty	96 (COM1–COM4)	-

The output waveforms for the five LCD driving modes are shown below.

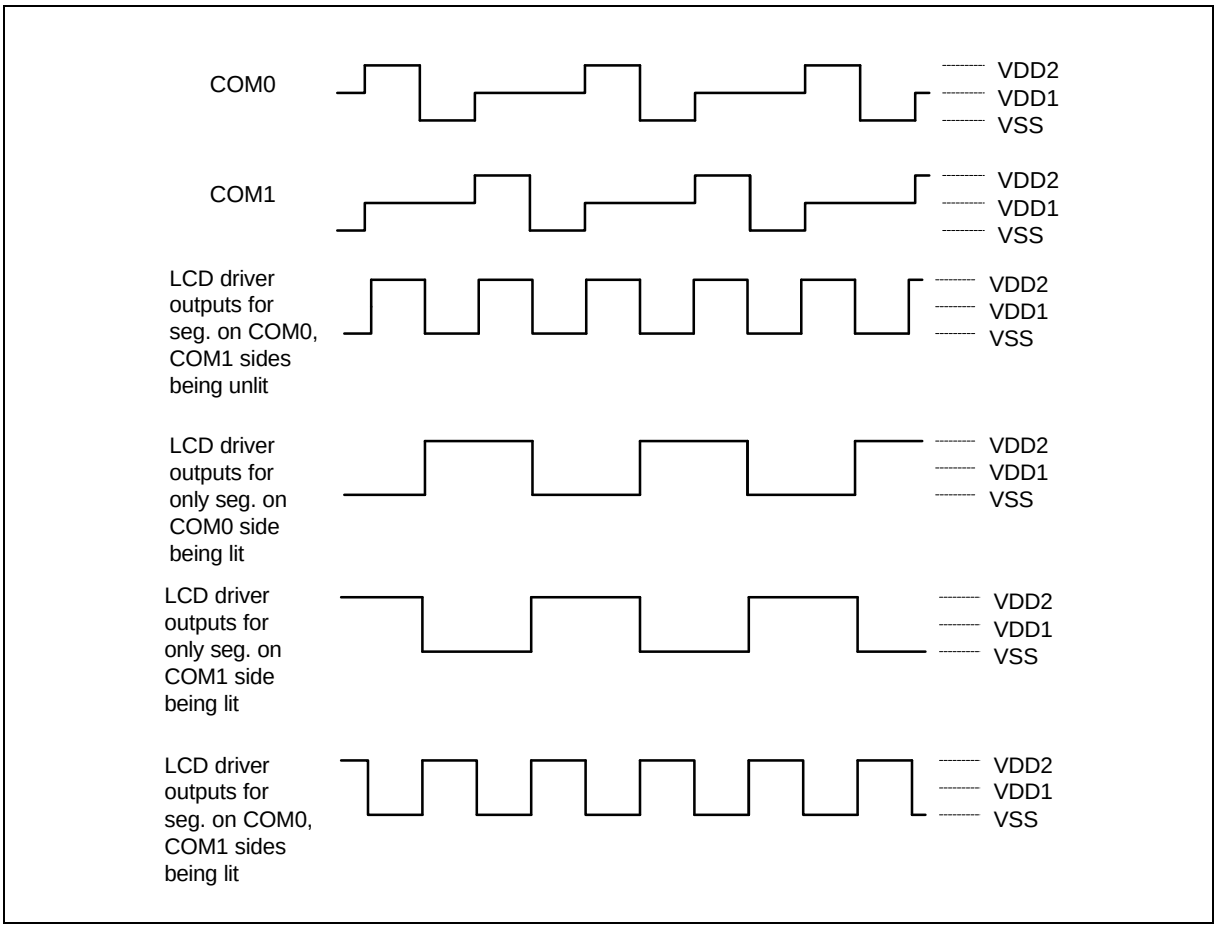
Static Lighting System (Example)

Normal Operating Mode



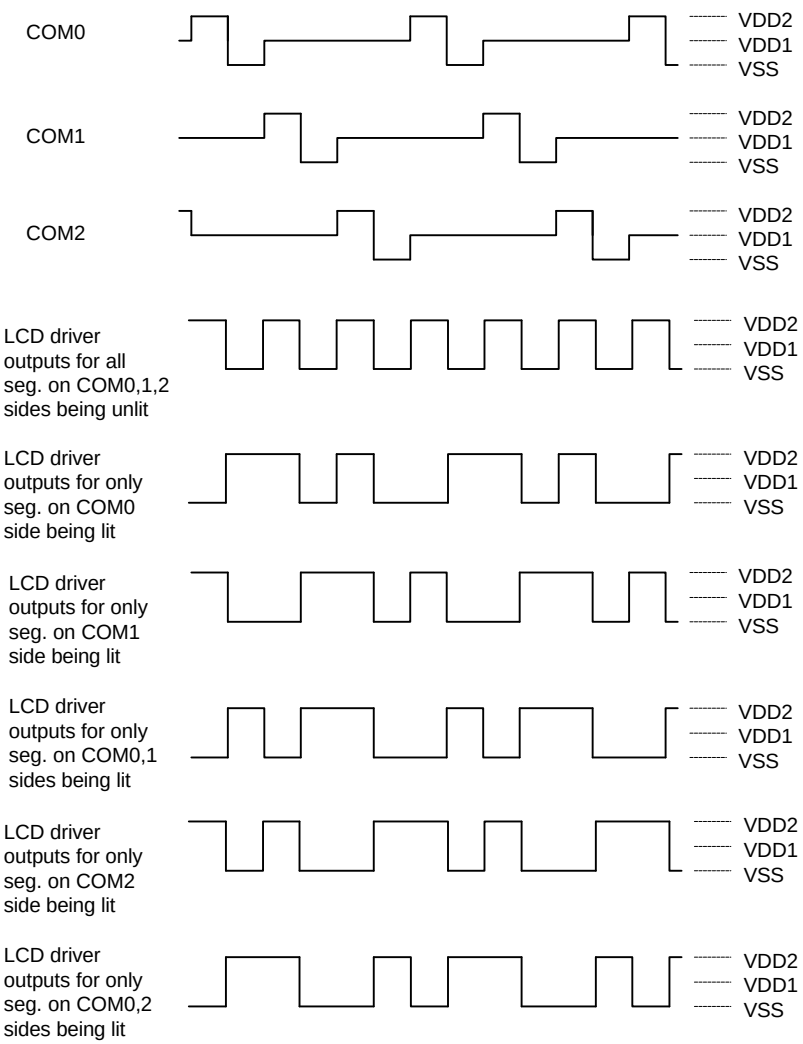
1/2 Bias 1/2 Duty Lighting System (Example)

Normal Operating Mode



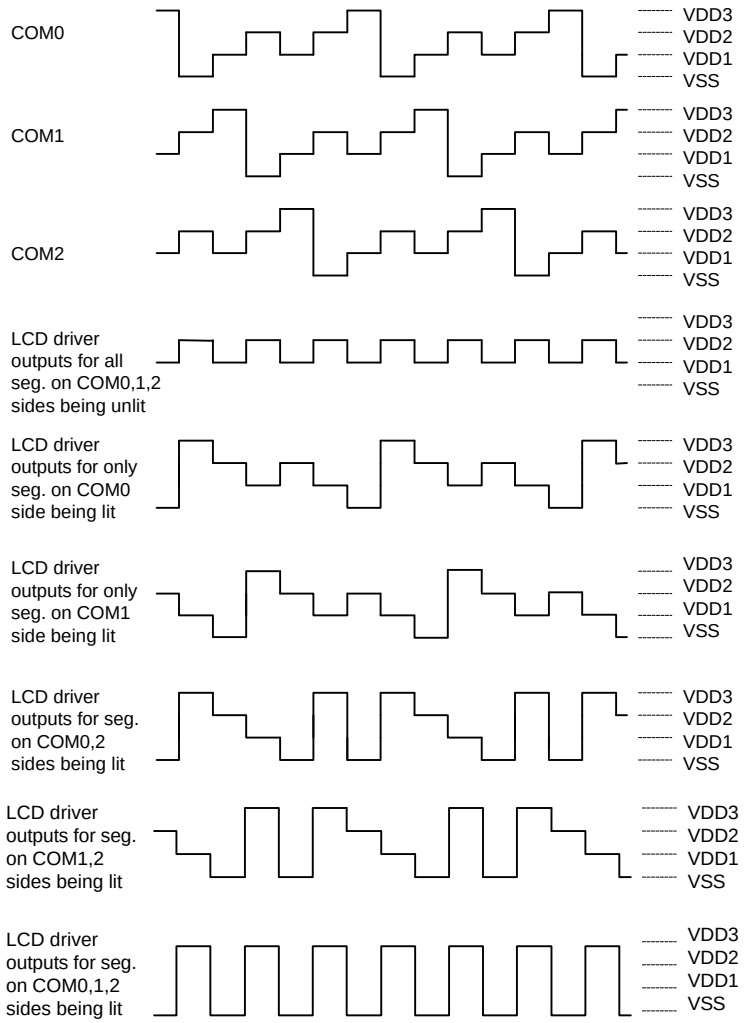
1/2 Bias 1/3 Duty Lighting System (Example)

Normal Operating Mode



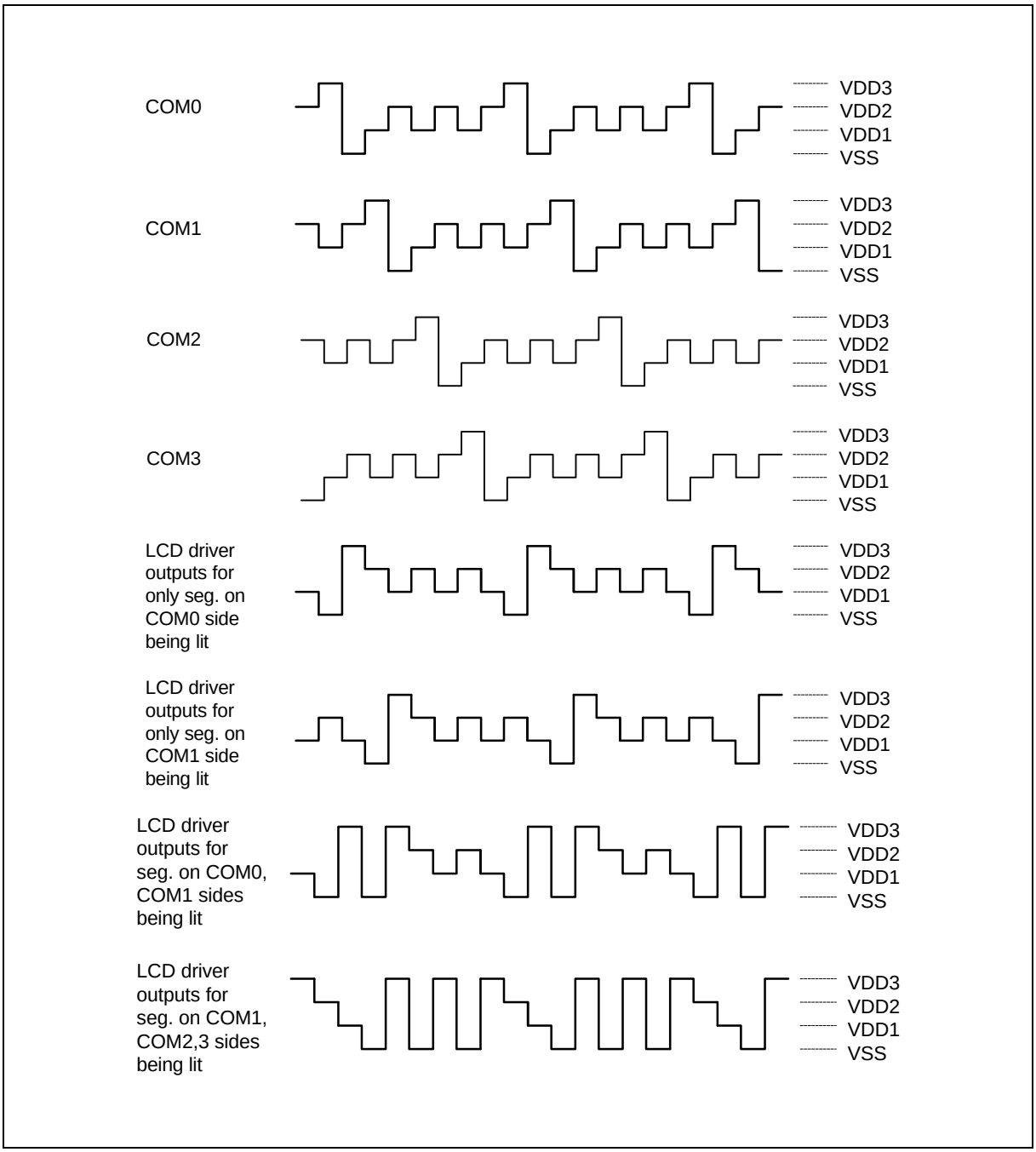
1/3 Bias 1/3 Duty Lighting System (Example)

Normal Operating Mode

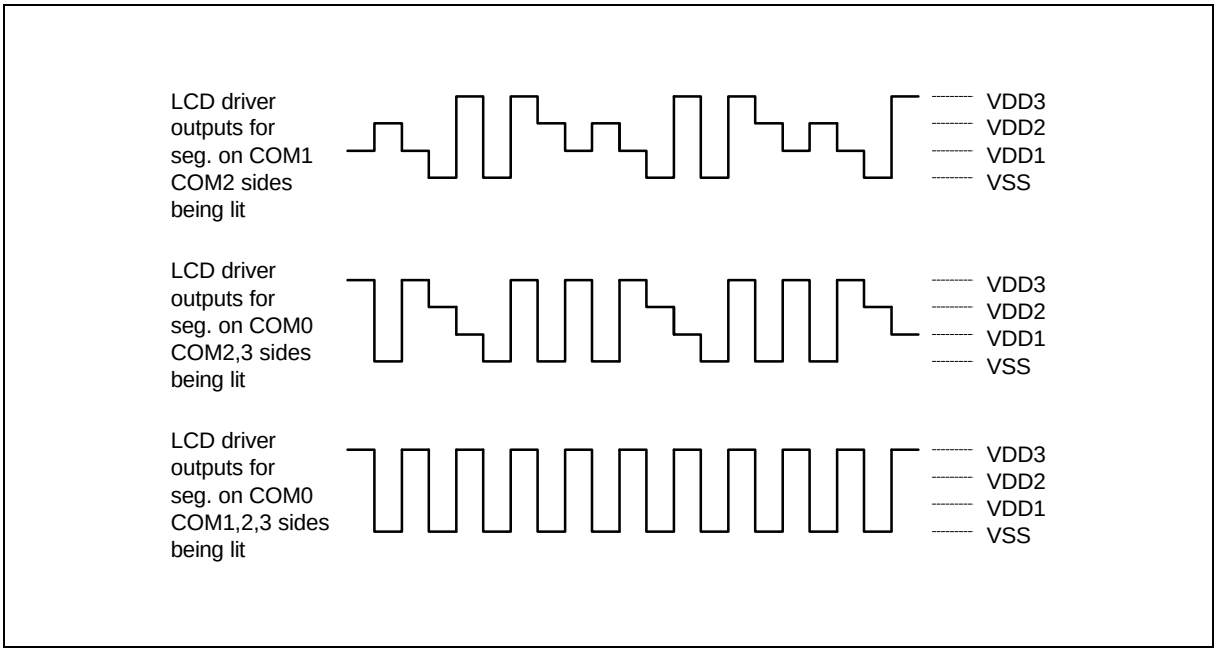


1/3 Bias 1/4 Duty Lighting System (Example)

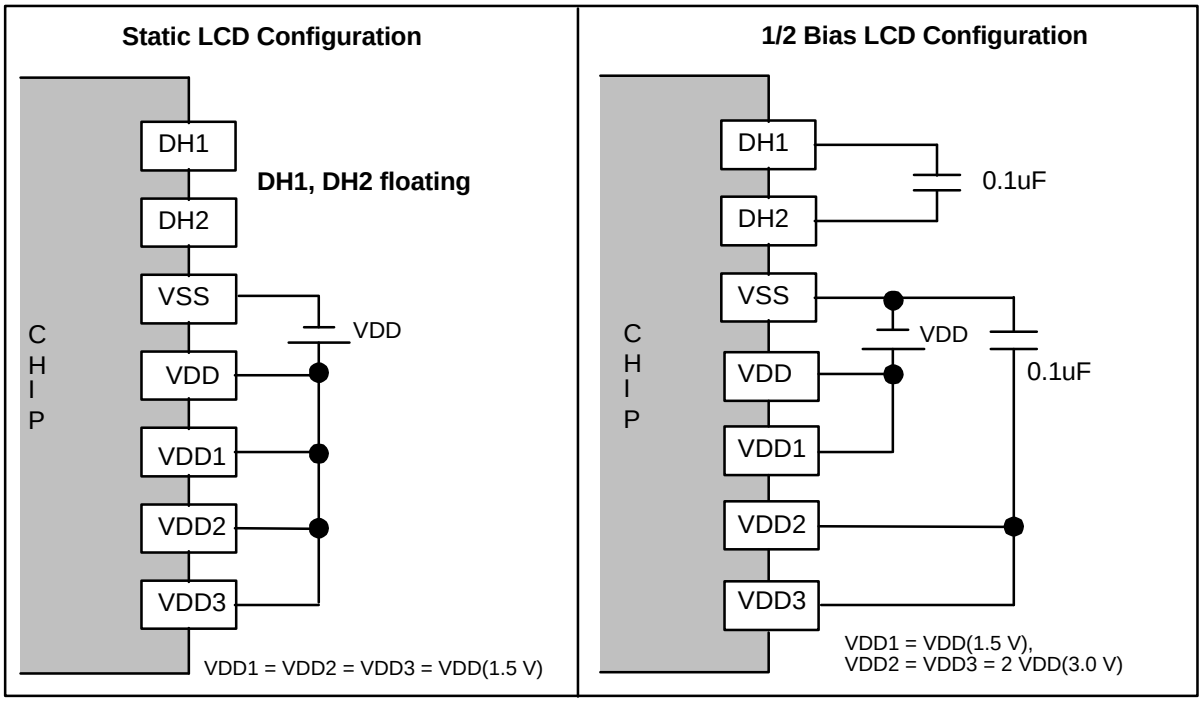
Normal Operating Mode



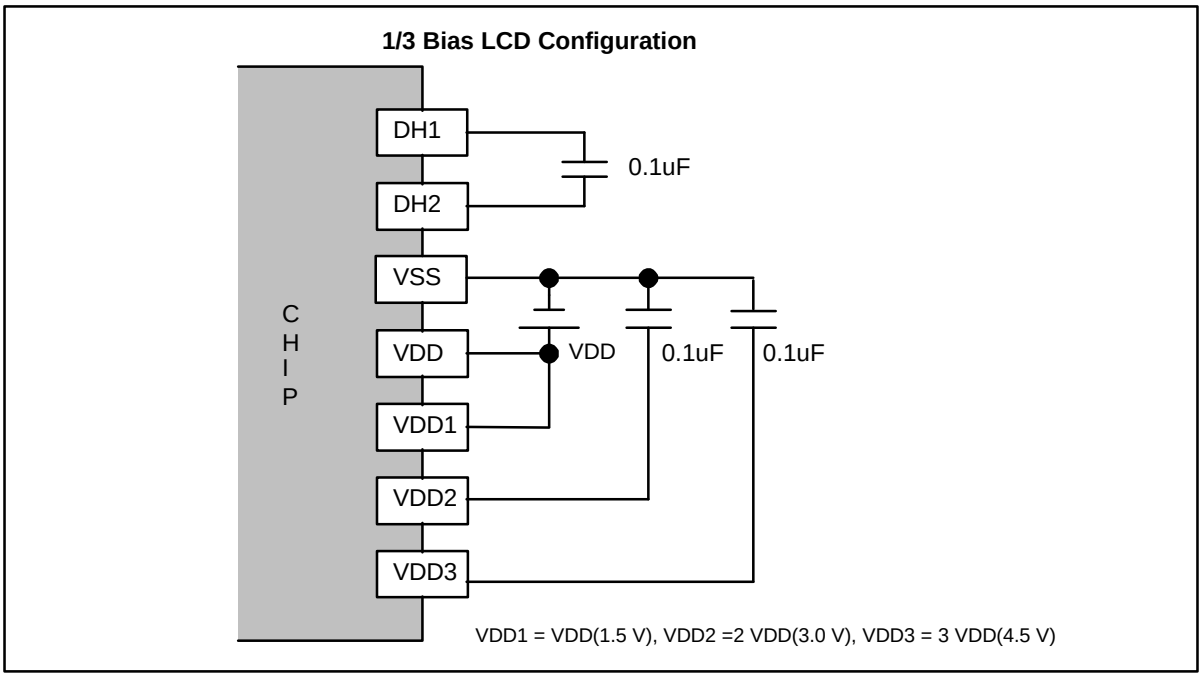
1/3 Bias 1/4 Duty Normal Lighting System, continued



The power connections for each LCD driving mode, which are determined by a mask option, are shown below.



LCD Configuration, continued



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +7.0	V
Applied Input/Output Voltage	-0.3 to +7.0	V
Power Dissipation	120	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0V, $F_{OSC.}$ = 32.768 KHz, T_A = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{DD}	-	1.2	-	1.8	V
Op. Current (Crystal type)	I_{OP1}	No load (Ext-V)	-	4	12	µA
Op. Current (RC type)	I_{OP2}	No load (Ext-V)	-	35	65	µA

DC Characteristics, continued

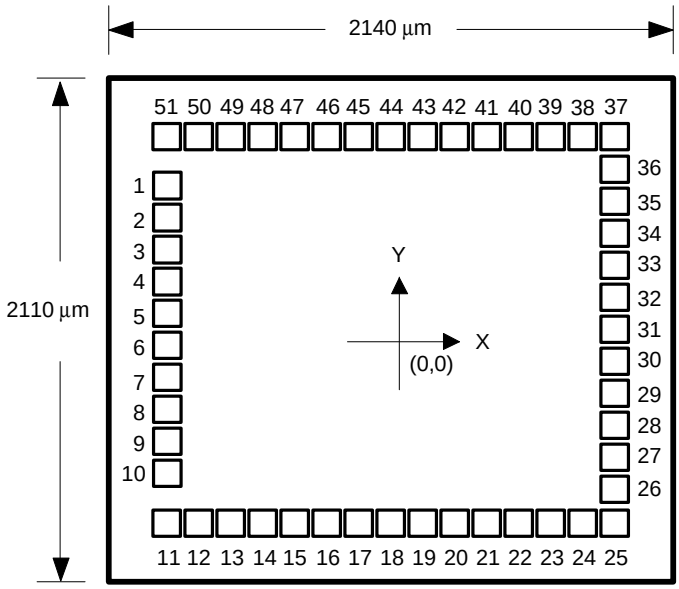
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Hold Current (Crystal type)	I_{HM1}	Hold mode No load (Ext-V)	-	4	6	µA
Hold Current (RC type)	I_{HM2}	Hold mode No load (Ext-V)	-	16	40	µA
Stop Current (Crystal type)	I_{SM1}	Stop mode No load (Ext-V)	-	0.1	2	µA
Stop Current (RC type)	I_{SM2}	Stop mode No load (Ext-V)	-	0.1	2	µA
Input Low Voltage	V_{IL}	-	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
MFP Output Low Voltage	V_{ML}	I_{OL} = 3.5 mA	-	-	0.3	V
MFP Output High Voltage	V_{MH}	I_{OH} = -3.5 mA	1.2	-	-	V
Port RA, RB Output Low Voltage	V_{ABL}	I_{OL} = 2.0 mA	-	-	0.3	V
Port RA, RB Output high Voltage	V_{ABH}	I_{OH} = -2.0 mA	1.2	-	-	V
LCD Supply Current	I_{LCD}	All Seg. On	-	-	3	µA
SEG0–SEG23 Sink Current (work as LCD output pins)	I_{OL}	V_{OL} = 0.4V V_{LCD} = 0.0V	4	-	-	µA
SEG0–SEG23 Drive Current (work as LCD output pins)	I_{OH}	V_{OH} = 2.4V V_{LCD} = 3.0V	15	-	-	µA
Input Port Pull-up Resistor	R_{CD}	Port RC, RD	100	300	1000	KΩ
$\overline{RES}$ Pull-up Resistor	R_{RES}	-	20	100	500	KΩ

AC CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0V, T_A = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Frequency	F_{OSC}	RC type	-	-	1000	KHz
		Crystal type (Option low-speed type)	-	32.768	-	
Frequency Deviation by Voltage Drop for RC Oscillator	$\frac{\Delta f}{f}$	$\frac{f(3V) - f(2.4V)}{f(3V)}$	-	-	10	%
Oscillator Start-up Time	T_S	V_{DD} = 1.2 V, F_{OSC} = 32.768 KHz	-	1	2	S
Instruction Cycle Time	T_I	One machine cycle	-	4/F_{OSC}	-	mS
Reset Active Width	T_{RAW}	F_{OSC} = 32.768 KHz	1	-	-	µS

PAD ASSIGNMENT & POSITIONS



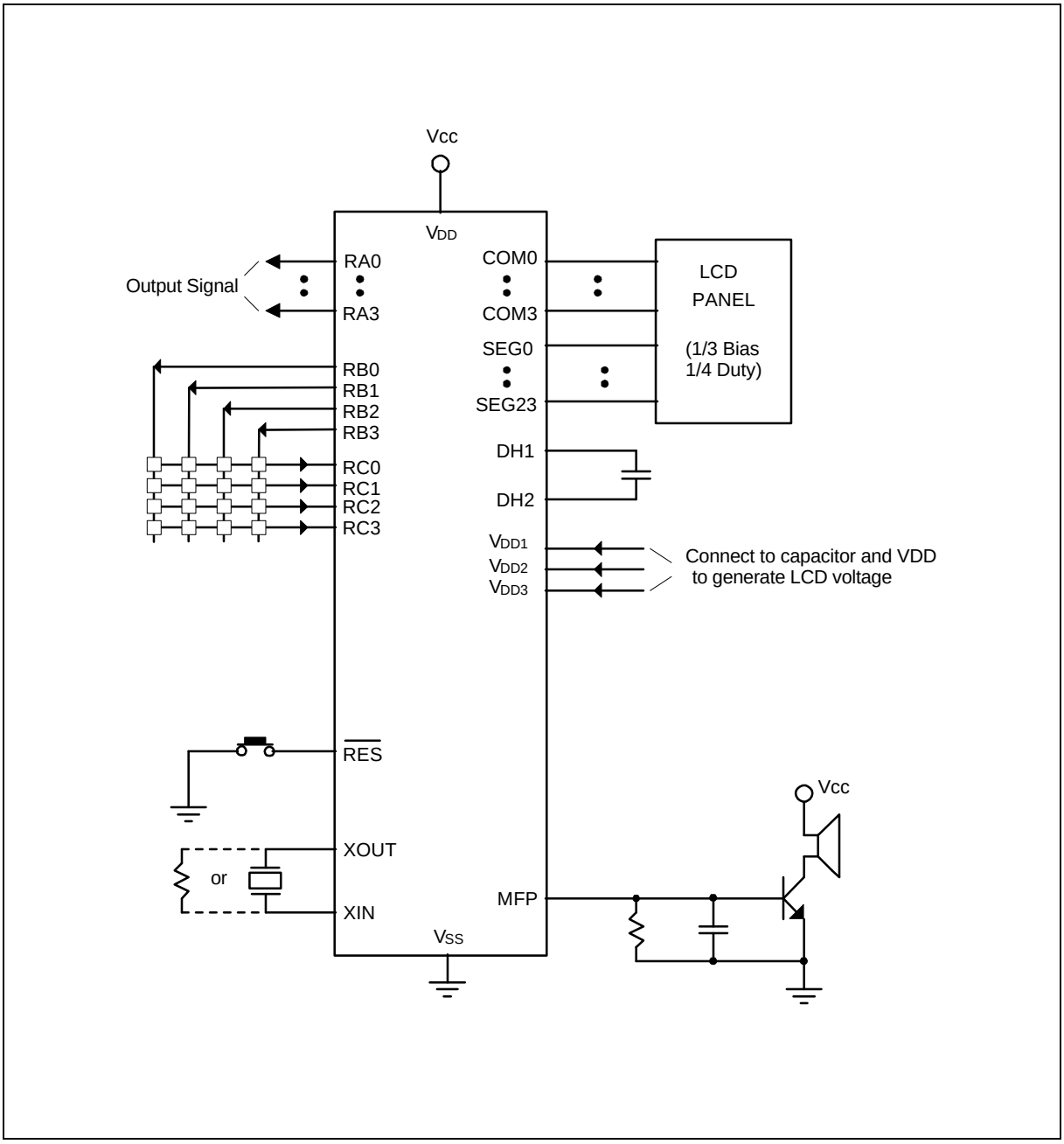
Note: The chip substrate must be connected to system ground (VSS).

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
1	VSS	-915.00	603.23	11	SEG5	-905.00	-900.00
2	COM3	-915.00	466.18	12	SEG6	-775.00	-900.00
3	COM2	-915.00	327.00	13	SEG7	-645.00	-900.00
4	COM1	-915.00	187.83	14	SEG8	-515.00	-900.00
5	COM0	-915.00	48.65	15	SEG9	-385.00	-900.00
6	SEG0	-915.00	-86.23	16	SEG10	-258.00	-900.00
7	SEG1	-915.00	-216.23	17	SEG11	-131.00	-900.00
8	SEG2	-915.00	-346.23	18	SEG12	-4.00	-900.00
9	SEG3	-915.00	-476.23	19	SEG13	123.00	-900.00
10	SEG4	-915.00	-606.23	20	SEG14	250.00	-900.00

Pad positions, continued

PAD NO.	PAD NAME	X	Y	PAD NO.	PAD NAME	X	Y
21	SEG15	377.00	-900.00	41	RA1	377.00	879.10
22	SEG16	507.00	-900.00	42	RA2	250.00	879.10
23	SEG17	637.00	-900.00	43	RA3	123.00	879.10
24	SEG18	767.00	-900.00	44	RB0	-4.00	879.10
25	SEG19	897.00	-900.00	45	RB1	-131.00	879.10
26	SEG20	907.00	-644.45	46	RB2	-258.00	879.10
27	SEG21	907.00	-514.45	47	RB3	-385.00	879.10
28	SEG22	907.00	-384.45	48	RC0	-515.00	879.10
29	SEG23	907.00	-254.45	49	RC1	-645.00	879.10
30	V_{DD3}	907.00	-124.45	50	RC2	-775.00	879.10
31	V_{DD2}	907.00	5.55	51	RC3	-905.00	879.10
32	V_{DD1}	907.00	135.55				
33	DH2	907.00	265.55				
34	DH1	907.00	395.55				
35	V_{DD}	907.00	525.55				
36	X_{OUT}	907.00	655.55				
37	X_{IN}	897.00	879.10				
38	$\overline{RES}$	767.00	879.10				
39	MFP	637.00	879.10				
40	RA0	507.00	879.10				

TYPICAL APPLICATION CIRCUIT



INSTRUCTION SET TABLE

Symbol Description

ACC:	Accumulator
ACC.n:	Accumulator bit n
WR:	Working Register
PAGE:	Page Register
MR1:	Mode Register 1
PM0:	Port Mode 0
PM1:	Port Mode 1
PM2:	Port Mode 2
PSR0:	Port Status Register 0
R:	Memory (RAM) of address R
LCDR:	LCD data RAM of address LDR
R.n:	Memory bit n of address R
I:	Constant parameter
L:	Branch or jump address
CF:	Carry Flag
ZF:	Zero Flag
PC:	Program Counter
TM1:	Timer 1
IEF.n:	Interrupt Enable Flag n
HCF.n:	HOLD mode release Condition Flag n
HEF.n:	HOLD mode release Enable Flag n
SEF.n:	STOP mode wake-up Enable Flag n
PEF.n:	Port Enable Flag n
EVFn:	Event Flag n
BF:	Backup Flag
! =:	Not equal
&:	AND
^:	OR

Symbol Description, continued

EX: Exclusive OR

←: Transfer direction, result

[PAGE*10H+()]: Contents of address PAGE(bit2, bit1, bit0)*10H+()

[P()]: Contents of port P()

INSTRUCTION SET TABLE 1

MNEMONIC		FUNCTION	FLAG AFFECTED	CYCLE
Arithmetic				
ADD	R, ACC	ACC←(R) + (ACC)	ZF, CF	1
ADD	WR, #I	ACC←(WR) + I	ZF, CF	1
ADDR	R, ACC	ACC, R←(R) + (ACC)	ZF, CF	1
ADDR	WR, #I	ACC, WR←(WR) + I	ZF, CF	1
ADC	R, ACC	ACC←(R) + (ACC) + (CF)	ZF, CF	1
ADC	WR, #I	ACC←(WR) + I + (CF)	ZF, CF	1
ADCR	R, ACC	ACC, R←(R) + (ACC) + (CF)	ZF, CF	1
ADCR	WR, #I	ACC, WR←(WR) + I + (CF)	ZF, CF	1
SUB	R, ACC	ACC←(R) - (ACC)	ZF, CF	1
SUB	WR, #I	ACC←(WR) - I	ZF, CF	1
SUBR	R, ACC	ACC, R←(R) - (ACC)	ZF, CF	1
SUBR	WR, #I	ACC, WR←(WR) - I	ZF, CF	1
SBC	R, ACC	ACC←(R) - (ACC) - (CF)	ZF, CF	1
SBC	WR, #I	ACC←(WR) - I - (CF)	ZF, CF	1
SBCR	R, ACC	ACC, R←(R) - (ACC) - (CF)	ZF, CF	1
SBCR	WR, #I	ACC, WR←(WR) - I - (CF)	ZF, CF	1
INC	R	ACC, R←(R) + 1	ZF, CF	1
DEC	R	ACC, R←(R) - 1	ZF, CF	1

Instruction Set Table 1, continued

MNEMONIC		FUNCTION	FLAG AFFECTED	CYCLE
Logic Operations				
ANL	R, ACC	ACC←(R) & (ACC)	ZF	1
ANL	WR, #I	ACC←(WR) & I	ZF	1
ANLR	R, ACC	ACC, R←(R) & (ACC)	ZF	1
ANLR	WR, R #I	ACC, WR←(WR) & I	ZF	1
ORL	R, ACC	ACC←(R) ∧ (ACC)	ZF	1
ORL	WR, #I	ACC←(WR) ∧ I	ZF	1
ORLR	R, ACC	ACC, R←(R) ∧ (ACC)	ZF	1
ORLR	WR, #I	ACC, WR←(WR) ∧ I	ZF	1
XRL	R, ACC	ACC←(R) EX (ACC)	ZF	1
XRL	WR, #I	ACC←(WR) EX I	ZF	1
XRLR	R, ACC	ACC, R←(R) EX (ACC)	ZF	1
XRLR	WR, #I	ACC, WR←(WR) EX I	ZF	1
Branch				
JMP	L	PC10–PC0←L10–L0		1
JB0	L	PC10–PC0←L10–L0; if ACC.0 = "1"		1
JB1	L	PC10–PC0←L10–L0; if ACC.1 = "1"		1
JB2	L	PC10–PC0←L10–L0; if ACC.2 = "1"		1
JB3	L	PC10–PC0←L10–L0; if ACC.3 = "1"		1
JZ	L	PC10–PC0←L10–L0; if ACC = 0		1
JNZ	L	PC10–PC0←L10–L0; if ACC ! = 0		1
JC	L	PC10–PC0←L10–L0; if CF = "1"		1
JNC	L	PC10–PC0←L10–L0; if CF ! = "1"		1

Instruction Set Table 1, continued

MNEMONIC		FUNCTION	FLAG AFFECTED	CYCLE
Data Move				
MOV	WR, R	WR←(R)		1
MOV	R, WR	R←(WR)		1
MOVA	WR, R	ACC, WR←(R)	ZF	1
MOVA	R, WR	ACC, R←(WR)	ZF	1
MOV	R, ACC	R←(ACC)		1
MOV	ACC, R	ACC←(R)	ZF	1
MOV	R, #I	R←I		1
MOV	WR, @R	WR←[PR (bit2, bit1, bit0) × 10H + (R)]		2
MOV	@R, WR	[PR (bit2, bit1, bit0) × 10H +(R)]←WR		2
MOV	TABH, R	TAB High addresss ← R		1
MOV	TABL, R	TAB Low addresss ← R		1
MOVC	R	R←[TAB × 10H + (ACC)]		2
Input & Output				
MOVA	R, RA	ACC, R←[RA]	ZF	1
MOVA	R, RB	ACC, R←[RB]	ZF	1
MOVA	R, RC	ACC, R←[RC]	ZF	1
MOV	RA, R	[RA]←(R)		1
MOV	RB, R	[RB]←(R)		1
MOV	MFP, #I	[MFP]← I		1
Flag & Register				
MOVA	R, PAGE	ACC, R←PAGE (Page Register)	ZF	1
MOV	PAGE, R	PAGE←(R)		1
MOV	PAGE, #I	PAGE←I		1
MOV	MR0, #I	MR0←I		1
MOV	MR1, #I	MR1←I		1
MOVA	R, CF	ACC.0, R.0←CF	ZF	1
MOV	CF, R	CF←(R.0)	CF	1

Instruction Set Table 1, continued

MNEMONIC		FUNCTION	FLAG AFFECTED	CYCLE
MOVA	R, HCFL	ACC, R←HCF0–HCF3	ZF	1
MOVA	R, HCFH	ACC, R←HCF4–HCF7	ZF	1
CLR	PMF, #I	Clear Parameter Flag if In = 1		1
SET	PMF, #I	Set Parameter Flag if In = 1		1
MOV	PM0, #I	Port Mode 0← I		1
MOV	PM1, #I	Port Mode 1← I		1
MOV	PM2, #I	Port Mode 2← I		1
CLR	EVF, #I	Clear Event Flag if In = 1		1
MOV	PEF, #I	Set/Reset Port Enable Flag		1
MOV	IEF, #I	Set/Reset Interrupt Enable Flag		1
MOV	HEF, #I	Set/Reset HOLD mode release Enable Flag		1
MOV	SEF, #I	Set/Reset STOP mode wake-up Enable Flag for RC port		1
MOVA	R, PSR0	ACC, R←Port Status Register 0	ZF	1
CLR	PSR0	Clear Port Status Register 0		1
SET	CF	Set Carry Flag	CF	1
CLR	CF	Clear Carry Flag	CF	1
CLR	DIVR0	Clear last 4 bits of Divider 0		1
CLR	WDT	Clear Watchdog Timer		1
Shift & Rotate				
SHRC	R	ACC.n, R.n←(R.n+1); ACC.3, R.3←0; CF←R.0	ZF, CF	1
RRC	R	ACC.n, R.n←(R.n+1); ACC.3, R.3←CF; CF←R.0	ZF, CF	1
SHLC	R	ACC.n, R.n←(R.n-1); ACC.0, R.0←0; CF←R.3	ZF, CF	1
RLC	R	ACC.n, R.n←(R.n-1); ACC.0, R.0←CF; CF←R.3	ZF, CF	1

Instruction Set Table 1, continued

MNEMONIC		FUNCTION	FLAG AFFECTED	CYCLE
LCD				
MOV	LCDR, #I	LCDR← I		1
MOV	WR, LCDR	WR←(LCDR)		1
MOV	LCDR, WR	LCDR←(WR)		1
MOV	LCDR, ACC	LCDR←(ACC)		1
LCDON		LCD ON		1
LCDOFF		LCD OFF		1
Timer				
MOV	TM1H, R	Timer 1 High register ← R		1
MOV	TM1L, R	Timer 1 Low register ← R		1
Subroutine				
CALL	L	STACK ← (PC)+1; PC10–PC0 ← L10–L0		1
RTN		(PC)←STACK		1
Other				
HOLD		Enter Hold mode		1
STOP		Enter Stop mode		1
NOP		No Operation		1
EN	INT	Enable Interrupt Function		1
DIS	INT	Disable Interrupt Function		1

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