

TC74AC00P, TC74AC00F, TC74AC00FN, TC74AC00FT

QUAD 2-INPUT NAND GATE

The TC74AC00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C²MOS technology.

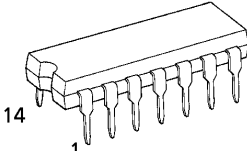
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

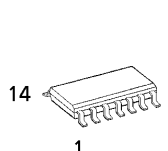
- High Speed..... $t_{pd} = 3.8\text{ns}(\text{typ.})$ at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 4\mu\text{A}(\text{Max.})$ at $T_a = 25^{\circ}\text{C}$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC} (\text{Min.})$
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 24\text{mA}(\text{Min.})$
Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays..... $t_{pLH} \approx t_{pHL}$
- Wide Operating Voltage Range.... $V_{CC} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Pin and Function Compatible with 74F00

(Note) The JEDEC SOP (FN) is not available in Japan.



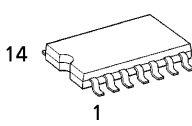
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P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)



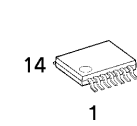
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FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)



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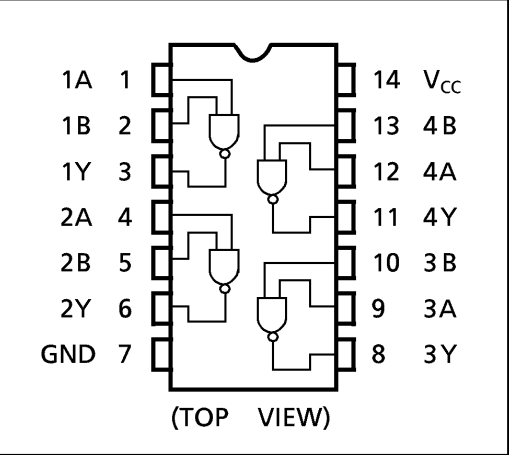
F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



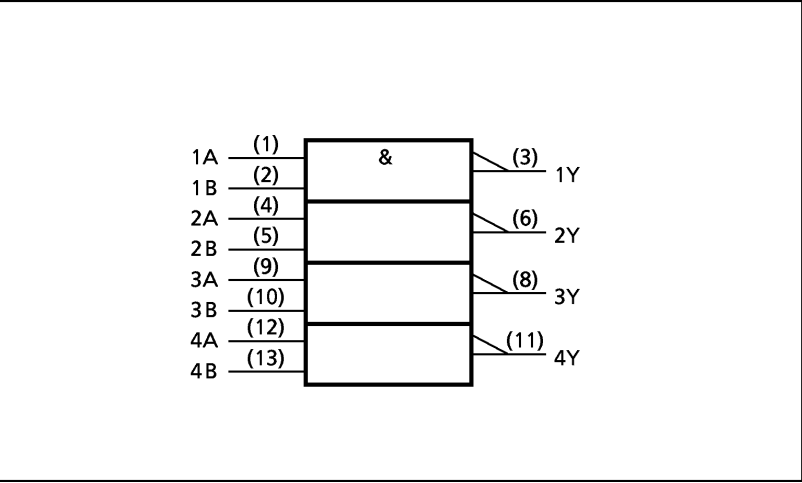
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FT (TSSOP14-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 50	mA
DC Output Current	I_{OUT}	± 50	mA
DC V_{CC} /Ground Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP/TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise and Fall Time	dt/dV	$0 \sim 100$ ($V_{CC} = 3.3 \pm 0.3\text{V}$) $0 \sim 20$ ($V_{CC} = 5 \pm 0.5\text{V}$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	V_{IH}		2.0 3.0 5.5	1.50 2.10 3.85	— — —	— — —	1.50 2.10 3.85	— — —	V
Low - Level Input Voltage	V_{IL}		2.0 3.0 5.5	— — —	— — —	0.50 0.90 1.65	— — —	0.50 0.90 1.65	V
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -50\mu\text{A}$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	V
			$I_{OH} = -4\text{mA}$	3.0	2.58	—	—	2.48	
			$I_{OH} = -24\text{mA}$	4.5	3.94	—	—	3.80	
			$I_{OH} = -75\text{mA}^*$	5.5	—	—	—	3.85	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$	$I_{OL} = 50\mu\text{A}$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	— — —	0.1 0.1 0.1	V
			$I_{OL} = 12\text{mA}$	3.0	—	—	—	0.36	
			$I_{OL} = 24\text{mA}$	4.5	—	—	—	0.36	
			$I_{OL} = 75\text{mA}^*$	5.5	—	—	—	—	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC} \text{ or } \text{GND}$	5.5	—	—	4.0	—	40.0	μA

* : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, $R_L = 500\Omega$, Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = − 40~85°C		UNIT
			V _{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH}		3.3 ± 0.3	—	6.6	11.2	1.0	12.9	ns
	t _{pHL}		5.0 ± 0.5	—	4.9	7.0	1.0	8.0	
Input Capacitance	C _{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C _{PD} (1)			—	68	—	—	—	

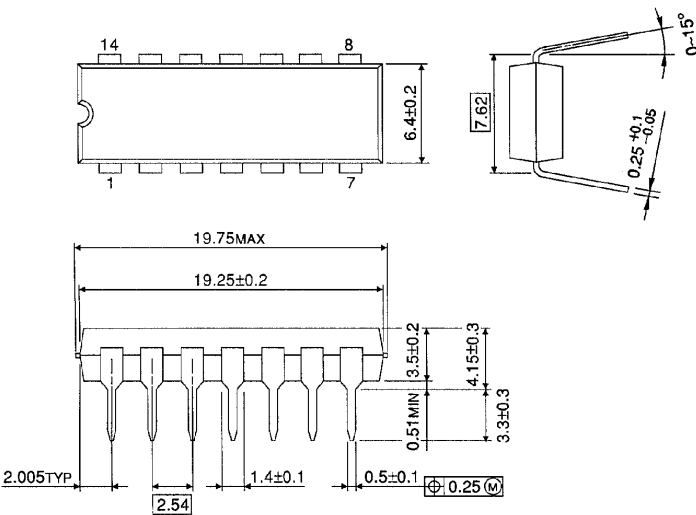
Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4 \text{ (per Gate)}$$

DIP 14PIN PACKAGE DIMENSIONS (DIP14-P-300-2.54)

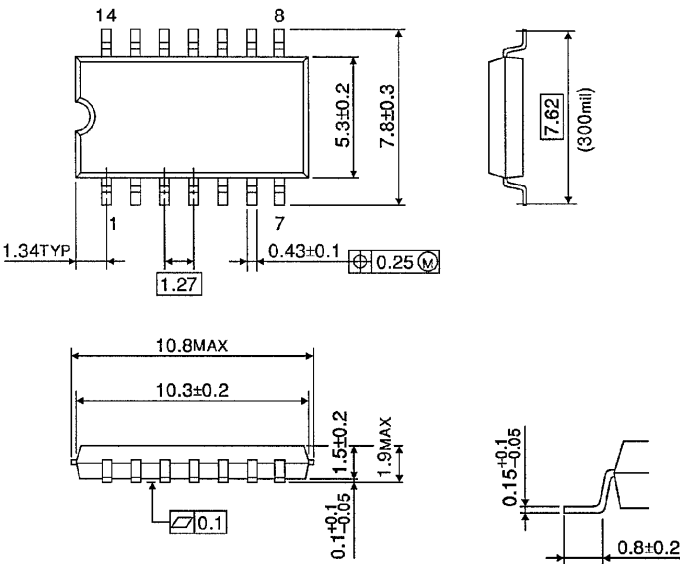
Unit in mm



Weight : 0.96g (Typ.)

SOP 14PIN (200mil BODY) PACKAGE DIMENSIONS (SOP14-P-300-1.27)

Unit in mm

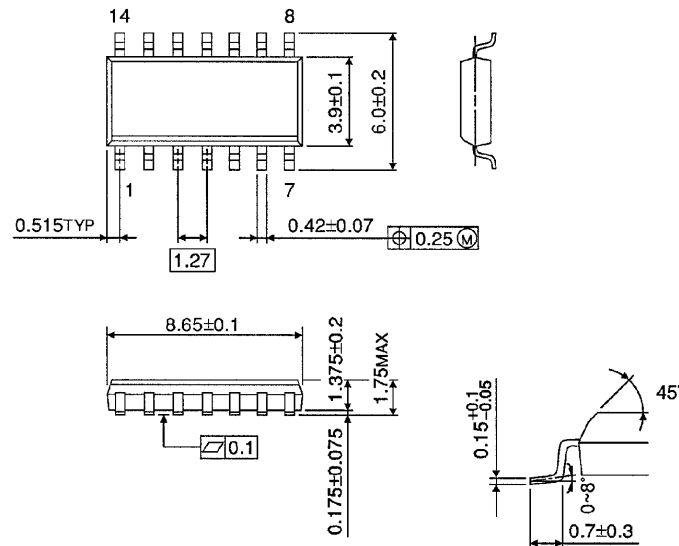


Weight : 0.18g (Typ.)

SOP 14PIN (150mil BODY) PACKAGE DIMENSIONS (SOL14-P-150 -1.27)

Unit in mm

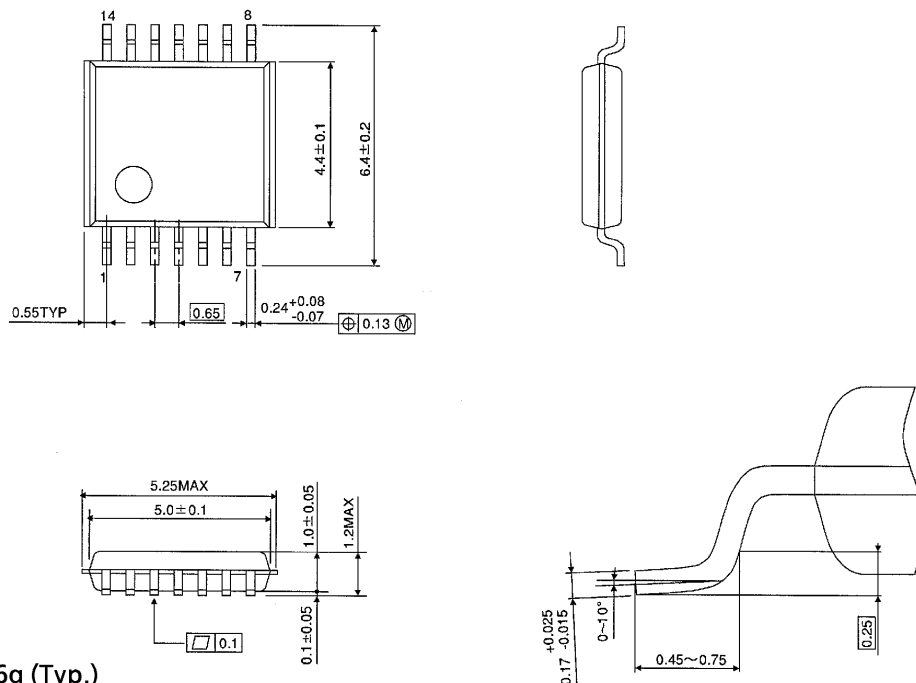
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

TSSOP 14PIN (170mil BODY) PACKAGE DIMENSIONS (TSSOP14-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)

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000707EBA

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