

# CMOS 8-Bit Microcontroller TMP88CS34N/F, TMP88CP34N/F

The TMP88CS34/CP34 is the high speed and high performance 8-bit single chip microcomputers. This MCU contain CPU core, ROM, RAM, input/output ports, four Multi-function timer/counters, serial bus interface, on-screen display, PWM output, 8-bit AD converter, and remote control signal preprocessor on chip.

| Product No.  | ROM          | RAM           | Package            | OTP MCU      |
|--------------|--------------|---------------|--------------------|--------------|
| TMP88CS34N/F | 64 K × 8-bit | 1.5 K × 8-bit | P-SDIP42-600-1.78  | TMP88PS34N/F |
| TMP88CP34N/F | 48 K × 8-bit | 1.5 K × 0-bit | P-QFP44-1414-0.80D | TWF00F334N/F |

#### **Features**

- ◆ 8-bit single chip microcomputer TLCS-870/X Series
- Instruction execution time: 0.25 μs (at 16 MHz)
- ◆ 842 basic instructions
  - Multiplication and Division (8 bits × 8 bits, 16 bits × 8 bits, 16 bits/8 bits)
  - Bit manipulations (Set/Clear/Complement/Move/Test/Exclusive or)
  - 16-bit data and 20-bit data operations
  - 1-byte jump/subroutine-call (Short relative jump/Vector call)
- ◆ I/O ports: Maximum 33 (High current output: 4)
- ◆ 15 interrupt sources: External 6, Internal 10
  - All sources have independent latches each, and nested interrupt control is available.
  - Edge-selectable external interrupts with noise reject
  - High-speed task switching by register bank changeover
- ◆ ROM corrective function
- ◆ Two 16-bit timer/counters: TC1, TC2
  - Timer, Event-counter, Pulse width measurement, External trigger timer, Window modes
- ◆ Two 8-bit timer/counters: TC3, TC4
  - Timer, Event counter, Capture (Pulse width/duty measurement) mode

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- For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.
  TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general
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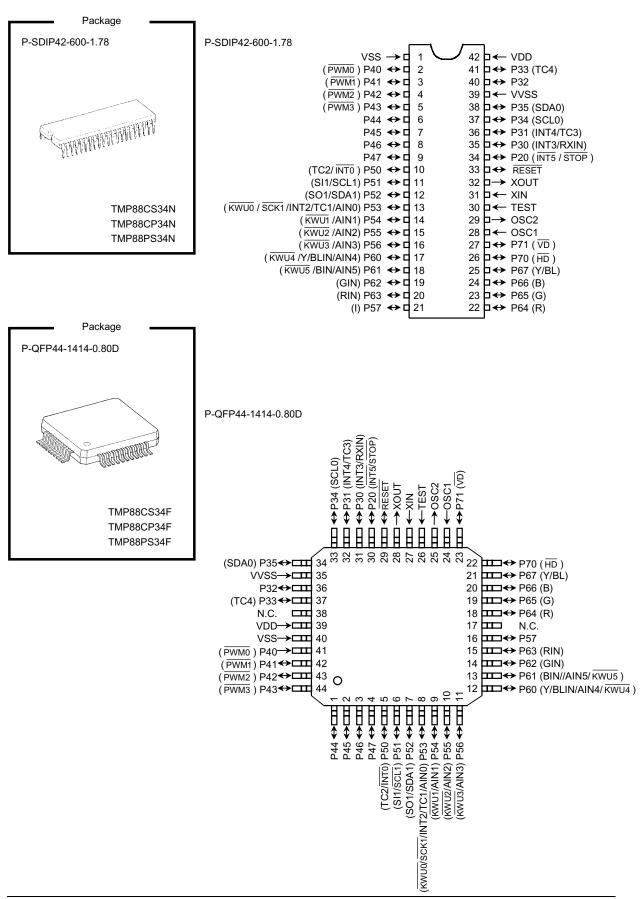


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- ◆ Time base timer (Interrupt frequency: 0.95 Hz to 31250 Hz)
- ◆ Watchdog timer
  - Interrupt source/reset output
- ◆ Serial bus interface
  - I<sup>2</sup>C bus, 8-bit SIO mode (Selectable two I/O channels)
- ♦ On-screen display circuit
  - Font ROM characters: Mono font 383 characters, color font 96 characters or mono font 447 characters, color font 64 characters
  - Characters display: 32 columns × 12 lines
  - Composition: 16 × 18 dots
  - Size of character: 4 kinds (line by line)
  - Color of character: 8 or 27 kinds (character by character)
  - Variable display position: Horizontal 256 steps, Vertical 625 steps
  - Fringing, Smoothing, Slant, Underline, Blinking function
- ♦ Jitter elimination
- ◆ DA conversion (Pulse Width Modulation) outputs
  - 14/12-bit resolution (2 channels)
  - 12-bit resolution (2 channels)
- ♦ 8-bit successive approximate type AD converter with sample and hold
- ♦ High current output: 1 pin (typ. 20 mA)
- ◆ Remote control signal preprocessor
- ◆ Two power saving operating modes
  - STOP mode: Oscillation stops. Battery/Capacitor back-up. Port output hold/high-impedance.
  - IDLE mode: CPU stops, and Peripherals operate using high-frequency clock. Release by interrupts.
- ♦ Operating voltage: 4.5 to 5.5 V at 16 MHz
- ◆ Emulation POD: BM88CS34N0A-M15

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# Pin Assignments



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# Pin Functions (1/2)

| Pin Name                               | I/O   | Fund  | ction   |  |
|--|---|---|---|--|
| P20 (INT5 / STOP)                      | I/O (Input)                                 | 1-bit input/output port with latch. When used as an input port, the latch must be set to "1".                       | External interrupt input 5 or STOP mode release signal input  |  |
| P35 (SDA0)                             | I/O (Input/Output)                          | 6-bit programmable input/output   | I <sup>2</sup> C bus serial data input/output 0   |  |
| P34 (SCL0)                             | I/O (Input/Output)                          | port. Each bit of these ports can be  | I <sup>2</sup> C bus serial clock input/output 0  |  |
| P33 (TC4)                              | I/O (Input)                                 | individually configured as an input or an output under software control.  |   |  |
| P32                                    | I/O   | During reset, all bits are configured as inputs. When used as a serial bus  | Video signal input 1 or Composite sync input  |  |
| P31 (INT4/TC3)                         | I/O (Input)                                 | interface input/output, the latch must be set to "1".   | External interrupt input 4 or<br>Timer/Counter input 3  |  |
| P30 (INT3/RXIN)                        | I/O (Input)                                 |   | External interrupt input 3 or Remote control signal preprocessor input  |  |
| P47                                    | I/O   | 8-bit programmable input/output   |   |  |
| P46                                    | I/O   | port. Each bit of these ports can be  |   |  |
| P45                                    | I/O   | individually configured as an input or an output under software control.  |   |  |
| P44                                    | I/O   | During reset, all bits are configured   |   |  |
| P43 ( PWM3 )                           | I/O (Output)                                | as inputs.  | 12 bit DA conversion (DM/M) outputs   |  |
| P42 ( PWM2 )                           | I/O (Output)                                |   | 12-bit DA conversion (PWM) outputs  |  |
| P41 (PWM1)                             | I/O (Output)                                |   | 14/12-bit DA conversion (PWM)   |  |
| P40 ( PWM0 )                           | I/O (Output)                                |   | outputs   |  |
| P57 (I)                                | I/O (Output)                                | 8-bit programmable input/output   | Translucent signal output   |  |
| P56 (KWU3 /AIN3)                       | I/O (Input)                                 | port. Each bit of these ports can be  |   |  |
| P55 (KWU2/AIN2)                        | I/O (Input)                                 | individually configured as an input or an output under software control.  | Key on wake-up inputs or AD converter analog inputs   |  |
| P54 (KWU1/AIN1)                        | I/O (Input)                                 | During reset, all bits are configured   | converter analog inputs   |  |
| P53<br>(KWU0 /AIN0/TC1<br>/INT2/ SCK1) | I/O<br>(Input/Input/Input<br>/Input/Output) | as inputs. When used as a serial bus interface input/output, the latch must be set to "1".                          | Key on wake-up input or AD converter analog input or Timer/counter input 1 or External interrupt input 2 or SIO serial clock input/output 1 |  |
| P52 (SDA1/SO1)                         | I/O<br>(Input/Output/Output)                |   | I <sup>2</sup> C bus serial data Input/Output 1 or<br>SIO serial data output 1  |  |
| P51 (SCL1/SI1)                         | I/O<br>(Input/Output/Input)                 |   | I <sup>2</sup> C bus serial data Input/Output 1 or SIO serial data input 1  |  |
| P50 (TC2/ INT0 )                       | I/O<br>(Input/Input)                        |   | Timer/Counter input 2 or External interrupt input 0   |  |
| P67 (Y/BL)                             | I/O (Output)                                | 8-bit programmable input/output   | Y or BL output  |  |
| P66 (B)                                | I/O (Output)                                | port. (P67 to 61: Tri-State, P60: High  |   |  |
| P65 (G)                                | I/O (Output)                                | current output) Each bit of these ports can be individually configured  | R/G/B outputs   |  |
| P64 (R)                                | I/O (Output)                                | as an input or an output under  |   |  |
| P63 (RIN)                              | I/O (Input)                                 | software control. During reset, all   | R input   |  |
| P62 (GIN)                              | I/O (Input)                                 | bits are configured as inputs. When used P64 to P67 as port, each bit of  | G input   |  |
| P61<br>( KWU5 /BIN/AIN5)               | I/O (Input)                                 | the P6 port data selection register (bit 7 to 4 in ORP6S) must be set to "1"  | Key on wake-up input 5 or B input or<br>AD converter analog input 5   |  |
| P60<br>( KWU4 /YBLIN/AIN4)             | I/O (Input)                                 | P63 to P61 output "0" after a reset. When these dual-function pins are used as ports, be sure to set ORP6S2 to "1". | Key on wake-up input 4 or Y/BL input or AD converter analog input 4   |  |

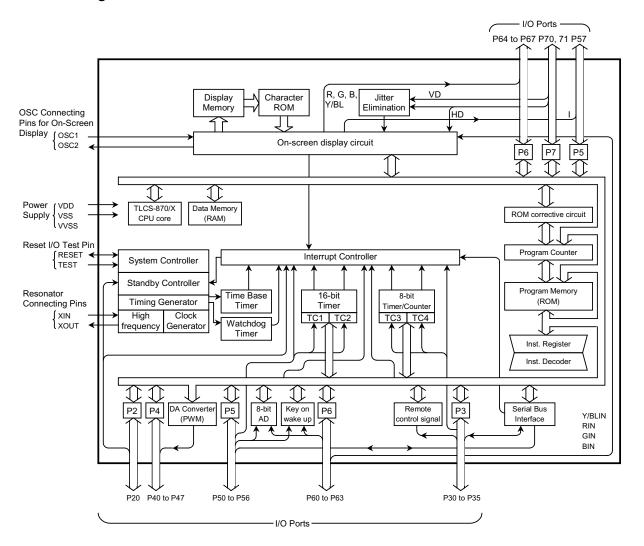
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# Pin Functions (2/2)

| Pin Name       | I/O           | Function  |                                     |  |  |  |
|----------------|---------------|---|-------------------------------------|--|--|--|
| P71 (√D)       | I/O (Input)   | 2-bit programmable input/output port. Each bit of these ports can be individually configured as an input or |                                     |  |  |  |
| P70 (HD)       | I/O (Input)   | an output under software control.  During reset, all bits are configured as inputs.                         | Horizontal synchronous signal input |  |  |  |
| XIN, XOUT      | Input, Output | Resonator connecting pins. For inputting external clock, XIN is used and XOUT is opened.                    |                                     |  |  |  |
| RESET          | I/O           | Reset signal input or watchdog timer output/address-trap-reset output/system-clock-rest output              |                                     |  |  |  |
| TEST           | Input         | Test pin for out-going test. Be tied to low.  |                                     |  |  |  |
| OSC1, OSC2     | Input, Output | Resonator connecting pins for on-screen display circuitry   |                                     |  |  |  |
| VDD, VSS, VVSS | Power Supply  | +5 V, 0 V (GND)   |                                     |  |  |  |

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# **Block Diagram**



# **Operational Description**

#### CPU Core Functions

The CPU core consists of a CPU, a system clock controller, and an interrupt controller.

This section provides a description of the CPU core, the program memory, the data memory, the external memory interface, and the reset circuit.

## 1.1 Memory Address Map

The TMP88CS34/CP34 memory consists of four blocks: ROM, RAM, SFR (Special Function Register), and DBR (Data Buffer Register). They are all mapped to a 1-Mbyte address space. Figure 1.1.1 shows the TMP88CS34/CP34 memory address map. There are 16 banks of the general-purpose register. The register banks are also assigned to the RAM address space.

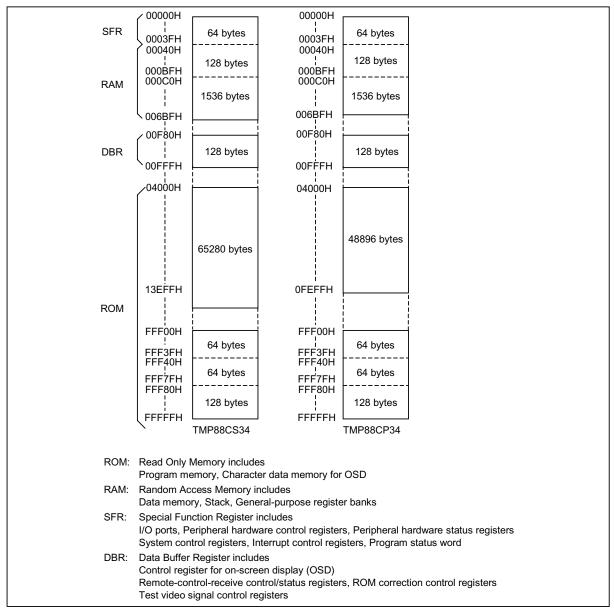


Figure 1.1.1 Memory Address Map

## **Electrical Characteristics**

Absolute maximum ratings (V<sub>SS</sub> = 0 V)

| Parameter                        | Symbol              | Pins                                 | Ratings                       | Unit |
|----------------------------------|---------------------|--------------------------------------|-------------------------------|------|
| Supply Voltage                   | $V_{DD}$            | -                                    | -0.3 to 6.5                   |      |
| Input Voltage                    | V <sub>IN</sub>     | -                                    | -0.3 to V <sub>DD</sub> + 0.3 | ٧    |
| Output Voltage                   | V <sub>OUT1</sub>   | =                                    | -0.3 to V <sub>DD</sub> + 0.3 |      |
| Output Current (Por 1 pin)       | I <sub>OUT1</sub>   | Ports P2, P3, P4, P5, P61 to P67, P7 | 3.2                           |      |
| Output Current (Per 1 pin)       | I <sub>OUT2</sub>   | Ports P60                            | 30                            | mA   |
| Output Current (Total)           | Σ l <sub>OUT1</sub> | Ports P2, P3, P4, P5, P64 to P67, P7 | 30                            | IIIA |
| Output Current (Total)           | Σ l <sub>OUT2</sub> | Ports P60                            | 30                            |      |
| Power Dissipation [Topr = 70 °C] | PD                  | -                                    | 400                           | mW   |
| Soldering Temperature (time)     | Tsld                | -                                    | 260 (10 s)                    |      |
| Storage Temperature              | Tstg                | =                                    | -55 to 125                    | °C   |
| Operating Temperature            | Topr                | -                                    | −30 to 70                     |      |

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

Recommended operating conditions

 $(V_{SS} = 0 \text{ V}, \text{Topr} = -30 \text{ to } 70 \,^{\circ}\text{C})$ 

| Parameter          | Symbol           | Pins                    | Conditions                    |               | Min                  | Max      | Unit                 |     |
|--------------------|------------------|-------------------------|-------------------------------|---------------|----------------------|----------|----------------------|-----|
|                    |                  |                         | fc = 16 MHz                   | NOR           | MAL mode             |          |                      |     |
| Supply Voltage     | $V_{DD}$         |                         | fc = 16 MHz                   | IDLE          | mode                 | 4.5      | 5.5                  |     |
|                    |                  |                         |                               | STO           | P mode               |          |                      |     |
|                    | V <sub>IH1</sub> | Except hysteresis input | V <sub>DD</sub> = 4.5 to 5.5V |               | $V_{DD} \times 0.70$ |          |                      |     |
| Input High Voltage | $V_{\text{IH2}}$ | Hysteresis input        |                               |               | $V_{DD}\times 0.75$  | $V_{DD}$ | V                    |     |
|                    | $V_{IH3}$        | Key-on Wake-up input    |                               |               | $V_{DD}\times 0.90$  |          |                      |     |
|                    | V <sub>IL1</sub> | Except hysteresis input | $V_{DD} = 4.5 \text{ to } 5$  | . <b>5</b> \/ |                      |          | $V_{DD}\times 0.30$  |     |
| Input Low Voltage  | $V_{IL2}$        | Hysteresis input        | VDD = 4.5 to 5                | 1.5 V         |                      | 0        | $V_{DD}\times 0.25$  |     |
|                    | $V_{IL3}$        | Key-on Wake-up input    | V <sub>DD</sub> = 4.5 to 5.5V |               |                      |          | $V_{DD} \times 0.65$ |     |
|                    | fc               | XIN, XOUT               | $V_{DD} = 4.5 \text{ to } 5$  | .5V           |                      | 8.0      | 16.0                 |     |
| Clock Frequency    | fooo             | Internal clock          | $V_{DD} = 4.5 \text{ to } 5$  | 51/           | fc = 8 MHz           | 8.0      | 12.0                 | MHz |
|                    | fosc             | Internal clock          | v DD = 4.5 to 5               | 5.5 V         | fc = 16 MHz          | 16.0     | 24.0                 |     |

- Note 1: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC/DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.
- Note 2: Clock frequency fc: Supply voltage range is specified in NORMAL mode and IDLE mode.
- Note 3: Smaller value is alternatively specified as the maximum value.

| DC Characteristics | (V <sub>SS</sub> = 0 V, Topr = $-30$ to 70 °C) |
|--------------------|--|
|--------------------|--|

| Parameter                     | Symbol           | Pins                      | Conditions   | Min | Тур. | Max | Unit |
|-------------------------------|------------------|---------------------------|--|-----|------|-----|------|
| Hysteresis voltage            | $V_{HS}$         | Hysteresis inputs         |  | -   | 0.9  | -   | V    |
|                               | I <sub>IN1</sub> | TEST                      | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V/0 V               | -   | _    | ± 2 |      |
| Input ourrent                 | I <sub>IN2</sub> | Open drain ports          | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V/0 V               | -   | _    | ± 2 | ^    |
| Input current                 | I <sub>IN3</sub> | Tri-state ports           | V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V/0 V               | -   | -    | ± 2 | μА   |
|                               | I <sub>IN4</sub> | RESET, STOP               | $V_{DD} = 5.5 \text{ V}, V_{IN} = 5.5 \text{ V/0 V}$               | -   | -    | ± 2 |      |
| Input resistance              | R <sub>IN2</sub> | RESET                     | $V_{DD} = 5.5 \text{ V}, V_{IN} = 0 \text{ V}$                     | 100 | 220  | 450 | kΩ   |
| Output leakage                | I <sub>LO1</sub> | Sink open drain ports     | V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = 5.5 V                  | -   | -    | 2   | ^    |
| current                       | I <sub>LO2</sub> | Tri-state ports           | $V_{DD} = 5.5 \text{ V}, V_{OUT} = 5.5 \text{ V/0 V}$              | -   | -    | ± 2 | μА   |
| Output high voltage           | V <sub>OH2</sub> | Tri-state ports           | $V_{DD} = 4.5 \text{ V}, I_{OH} = -0.7 \text{ mA}$                 | 4.1 | _    | -   |      |
| Output low voltage            | V <sub>OL</sub>  | Except XOUT and ports P60 | $V_{DD} = 4.5 \text{ V}, I_{OL} = 1.6 \text{ mA}$                  | -   | -    | 0.4 | V    |
| Output low current            | I <sub>OL3</sub> | Port P60                  | V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.0 V                   | -   | 20   | -   |      |
| Supply current in NORMAL mode |                  |                           | V <sub>DD</sub> = 5.5 V<br>fc = 16 MHz (Note3)                     | -   | 25   | 30  | mA   |
| Supply current in IDLE mode   | I <sub>DD</sub>  | -                         | fc = 16 MHz (Note3)<br>$V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$      | -   | 20   | 25  |      |
| Supply current in STOP mode   |                  |                           | $V_{DD} = 5.5 \text{ V}$<br>$V_{IN} = 5.3 \text{ V}/0.2 \text{ V}$ | -   | 0.5  | 10  | μА   |

Note 1: Typical values show those at Topr = 25  $^{\circ}\text{C},~\text{V}_{DD}$  = 5 V.

Note 2: Input Current  $I_{\mbox{\scriptsize IN}3}$ ; The current through resistor is not included.

Note 3: Supply Current  $I_{DD}$ ; The current (Typ. 0.5 mA) through ladder resistors of ADC is included in NORMAL mode and IDLE mode.

| AD Conversion Characteristics | $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}, \text{Topr} = -30 \text{ to } 70 ^{\circ}\text{C})$ |
|-------------------------------|---|

| Parameter                      | Symbol            | Conditions                         | Min             | Тур.     | Max      | Unit |
|--------------------------------|-------------------|------------------------------------|-----------------|----------|----------|------|
| Analog reference voltage       | V <sub>AREF</sub> | supplied from V <sub>DD</sub> pin. | _               | $V_{DD}$ | -        |      |
| Analog reference voltage       | V <sub>ASS</sub>  | supplied from V <sub>SS</sub> pin. | _               | 0        | ı        | V    |
| Analog reference voltage range | $\Delta V_{AREF}$ | $=V_{DD}-V_{SS}$                   | _               | $V_{DD}$ | ı        | V    |
| Analog input voltage           | V <sub>AIN</sub>  |                                    | V <sub>SS</sub> | _        | $V_{DD}$ |      |
| Nonlinearity error             |                   |                                    | _               | _        | ±1       |      |
| Zero point error               |                   | V50V                               | _               | _        | ±2       | LSB  |
| Full scale error               |                   | V <sub>DD</sub> = 5.0 V            | _               | _        | ±2       | LOD  |
| Total error                    |                   |                                    | _               | _        | ±3       |      |

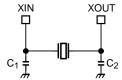
Note: The total error means all error except quanting error.

| AC characteristics           |                  | $(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}, \text{Topr} = -30 \text{ to } 70 ^{\circ}\text{C})$ |       |      |     |      |
|------------------------------|------------------|---|-------|------|-----|------|
| Parameter                    | Symbol           | Conditions  | Min   | Тур. | Max | Unit |
| Machine cycle time           |                  | In NORMAL mode  | 0.5   | -    | 1.0 | μS   |
| wachine cycle time           | t <sub>cy</sub>  | In IDLE mode  | 0.5   |      |     | μδ   |
| High level clock pulse width | t <sub>WCH</sub> | For external clock operation  | 31.25 |      |     | 200  |
| Low level clock pulse width  | t <sub>WCL</sub> | (XIN input), fc = 16 MHz  | 31.25 | _    | _   | ns   |

## Recommended oscillating conditions

(VSS = 0 V, VDD = 4.5 V to 5.5 V, Topr = –30 to 70 
$$^{\circ}\text{C}$$
)

| Parameter                  | Oscillator        | Oscillation | Recommended Oscillator  | Recommend      | ded Constant   |
|----------------------------|-------------------|-------------|-------------------------|----------------|----------------|
| raiametei                  | Oscillator        | Frequency   | Neconimended Oscillator | C <sub>1</sub> | C <sub>2</sub> |
| High-frequency oscillation | Ceramic resonator | 8 MHz       | Murata CSA 8.00MTZ      | 30 pF          | 30 pF          |
|                            |                   | 16 MHz      | Murata CSA 16.00MXZ040  | 5 pF           | 5 pF           |



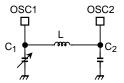
High-frequency Oscillation

- Note 1: To keep reliable operation, shield the device electrically with the metal plate on its package mold surface against the high electric field, for example, by CRT (Cathode Ray Tube) .
- Note 2: The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
  - http://www.murata.co.jp/search/index.html

Recommended oscillating conditions

$$(V_{SS} = 0 \text{ V}, V_{DD} = 4.5 \text{ V} \text{ to } 5.5 \text{ V}, \text{Topr} = -30 \text{ to } 70 \text{ }^{\circ}\text{C})$$

| ltem                | Resonator        | Oscillation | Recom  | mended paramete     | r value             |
|---------------------|------------------|-------------|--------|---------------------|---------------------|
|                     | Resortator       | Frequency   | L (μH) | C <sub>1</sub> (pF) | C <sub>2</sub> (pF) |
| Oscillation for OSD | DSD LC resonator | 8 MHz       | 33     | 5 to 30             | 10                  |
|                     |                  | 12 MHz      | 15     | 5 to 30             | 10                  |
|                     |                  | 16 MHz      | 10     | 5 to 30             | 10                  |
|                     |                  | 20 MHz      | 6.8    | 5 to 25             | 10                  |
|                     |                  | 24 MHz      | 4.7    | 5 to 25             | 10                  |



Oscillation for OSD

The frequency generated in LC oscillation can be obtained using the following equations.

$$f = \frac{1}{2\pi\sqrt{LC}}, C = \frac{C_1\boldsymbol{\cdot} C_2}{C_1 + C_2}$$

C1 is not fixed at a constant value. It can be changed to tune into the desired frequency.

Note 1: Toshiba's OSD circuit determines a horizontal display start position by counting clock pulses generated in LC oscillation. For this reason, the OSD circuit may fail to detect clock pulses normally, resulting in the horizontal start position becoming unstable, at the beginning of oscillation, if the oscillation amplitude is low.

Changing L and  $C_2$  from the values recommended for a specific frequency may hamper a stable OSD display.

If the LC oscillation frequency is the same as a high-frequency clock value, the oscillation of the high-frequency oscillator may cause the LC oscillation frequency to fluctuate, thus making OSD displays flicker.

When determining these parameters, please check the oscillation frequency and the stability of oscillation on your TV sets.

Also check the determined parameters on your final products, because the optimum parameter values may vary from one product to another.

Note 2: When using the LSI package in a strong electric field, such as near a CRT, electrically shield the package so that its normal operation can be maintained.