Low Input Voltage, Compact LCD Bias IC With VCOM Buffer

FEATURES

- 1.8-V to 6-V Input Voltage Range
- Integrated VCOM Buffer
- High Voltage Switch to Isolate VGH
- Gate Voltage Shaping of VGH
- 2-A Internal MOSFET Switch
- Main Output Vs up to 15 V With <1% Output Voltage Accuracy
- Virtual Synchronous Converter Technology
- Negative Regulated Charge Pump Driver VGL
- Positive Regulated Charge Pump Driver VGH
- Adjustable Power On Sequencing
- Adjustable Fault Detection Timing
- Gate Drive Signal for external isolation MOSFET
- Thermal Shutdown
- Available in TSSOP-24 Package
- Available in QFN-24 Package

APPLICATIONS

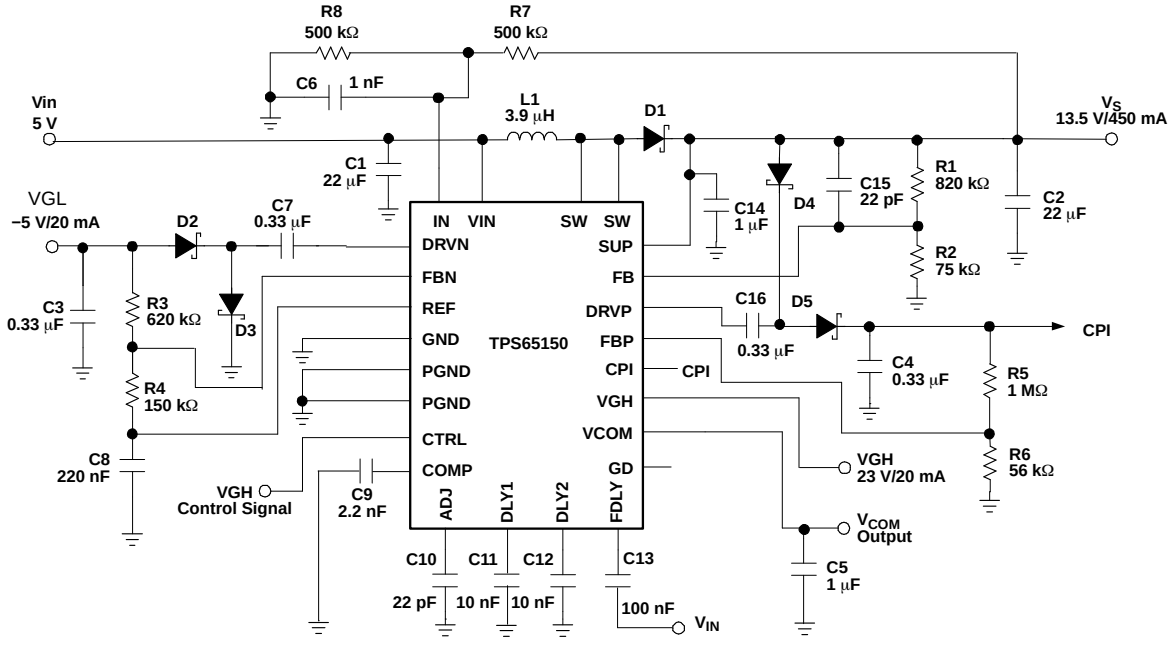
- TFT LCD Displays for Notebooks
- TFT LCD Display for Monitor
- Car Navigation Display

DESCRIPTION

The TPS65150 offers a very compact and small power supply solution that provides all three voltages required by thin film transistor (TFT) LCD displays. With an input voltage range of 1.8 V to 6.0 V the device is ideal for notebooks powered by a 2.5-V or 3.3-V input rail or monitor applications with a 5-V input voltage rail. Additionally the TPS65150 provides an integrated high current buffer to provide the VCOM voltage for the TFT backplane.

Two regulated adjustable charge pump driver provide the positive VGH and negative VGL bias voltages for the TFT. The device incorporates adjustable power on sequencing for VGL as well as for VGH. This avoids any additional external components to implement application specific sequencing. The device has an integrated high voltage switch to isolate VGH.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The same internal circuit can also be used to provide a gate shaping signal of VGH for the LCD panel controlled by the signal applied to the CTRL input. For highest safety the TPS65150 has an integrated adjustable shutdown latch feature to allow application specific flexibility. The device monitors the outputs (Vs, VGL, VGH); and, as soon as one of the outputs falls below its power good threshold, the device enters shutdown latch, after its adjustable delay time has passed by.

ORDERING INFORMATION(1)

T_A	ORDERING NUMBER	PACKAGE(2)	PACKAGE MARKING
–40°C to 85°C	TPS65150PWP	TSSOP24 (PWP)	TPS65150
	TPS65150RGE	QFN-24 (RGE)	TPS65150

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) The PWP package is available taped and reeled. Add R suffix to the device type (TPS65150PWPR) to order quantities of 2000 and (TPS65150RGER) to order quantities of 3000 devices per reel. Without suffix the device is shipped in tubes.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
Voltages on pin VIN(2)	–0.3 V to 7 V
Voltages on pin SUP	–0.3 V to 15.5 V
Voltage on pin SW	20 V
Voltage on CTRL	–0.3 V to 7 V
Voltage on GD	15.5 V
Voltage on CPI	32V
Continuous power dissipation	See Dissipation Rating Table
Operating junction temperature range	–40°C to 150°C
Storage temperature range	–65°C to 150°C
Lead temperature (soldering, 10 sec)	260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	θ_{JA}	$T_A \le 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
24 pin TSSOP	30.13 C°/W (PowerPad™ soldered)	3.3 W	1.83 W	1.32 W
24 pin QFN	30 C°/W (PowerPad™ soldered)	3.3 W	1.8 W	1.3 W

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
VIN	Input voltage range	1.8		6.0	V
V_S	Output voltage range of the main boost converter V_S			15	V
L	Inductor(1)		4.7		µH
T_A	Operating ambient temperature	–40		85	°C

(1) Refer to application section for further information.

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	TYP	MAX	UNIT
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

VIN = 3.3 V, Vs = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		1.8		6.0	V
I_{QVIN}	No load quiescent current into Vin	Device is not switching		14	25	µA
I_{QSUP}	No load quiescent current into SUP	Device is not switching		1.9	3	mA
I_{QVCOM}	VCOM quiescent current into SUP			750	1500	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.6	1.8	V
V_{hys}	Undervoltage lockout threshold	V_{IN} rising		1.7	1.9	V
	Thermal shutdown	Temperature rising		155		°C
	Thermal shutdown hysteresis			10		°C
LOGIC SIGNALS CTRL						
V_{IH}	High level input voltage		1.6			V
V_{IL}	Low level input voltage				0.4	V
I_I	Input leakage current	CTRL=GND or VIN		0.01	0.2	µA
MAIN BOOST CONVERTER						
V_S	Output voltage range				15	V
V_{FB}	Feedback regulation voltage		1.136	1.146	1.154	V
I_{FB}	Feedback input bias current			10	100	nA
$R_{DS(on)}$	N-MOSFET on-resistance (Q1)	Vs = 10 V; Isw = 500 mA		200	300	mΩ
		Vs = 5 V; Isw = 500 mA		305	450	
	P-MOSFET on-resistance (Q2)	Vs = 10 V; Isw = 500 mA		8	15	Ω
		Vs = 5 V; Isw = 500 mA		12	22	
I_{MAX}	Maximum P-MOSFET peak switch current				1	A
I_{LIM}	N-MOSFET switch current limit (Q1)		2.0	2.5	3.4	A
Ileak	Switch leakage current	V_{sw} = 15 V		1	10	µA
Vovp	Output overvoltage protection	V_{OUT} rising	16		20	V
f_{OSC}	Oscilator frequency		1.02	1.2	1.38	MHz
	Line regulation	Vin=1.8V to 5.0V, Iload=1mA		0.007		%/V
	Load regulation	Vin=5V, Iload=0A to 400mA		0.16		%/A
NEGATIVE CHARGE PUMP VGL						
VGL	Output voltage range				–2	V
V_{REF}	Reference Voltage on pin REF		1.205	1.213	1.219	V
V_{FB}	Feedback regulation voltage		–36	0	36	mV
I_{FB}	Feedback input bias current			10	100	nA
$R_{DS(on)}$	Q4 P-Channel switch RDSon	I_{OUT} = 20 mA		4.4		Ω
V_{DropN}	Current sink voltage drop (1)	I_{DRN} = 50 mA, $V_{FBN} = V_{FBNNominal}$ – 5%		130	300	mV
		I_{DRN} = 100 mA, $V_{FBN} = V_{FBNNominal}$ – 5%		280	450	
	Load regulation	VGL=-5V, Iload=0mA to 20mA		0.016		%/mA
POSITIVE CHARGE PUMP OUTPUT						
V_{CPO}	Output voltage range	CTRL = GND, VGH = open			30	V

(1) The maximum charge pump output current is half the drive current of the internal current source or sink.

ELECTRICAL CHARACTERISTICS (continued)

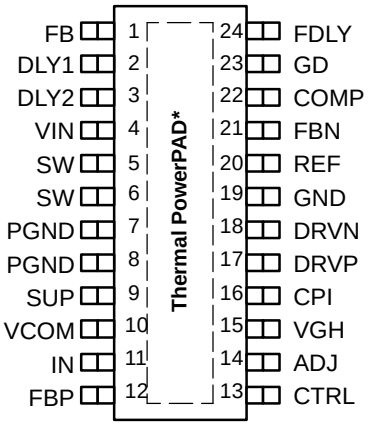
VIN = 3.3 V, Vs = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback regulation voltage	CTRL = GND, VGH = open	1.187	1.214	1.238	V
I_{FB}	Feedback input bias current	CTRL = GND, VGH = open		10	100	nA
$R_{DS(on)}$	Q3 P-Channel switch RDSon	I_{OUT} = 20 mA		1.1		Ω
V_{DropN}	Current sink voltage drop(1)	I_{DRP} = 50 mA, V_{FBP} = $V_{FBPNominal}$– 5%		420	650	mV
		I_{DRP}= 100 mA, V_{FBP} = $V_{FBPNominal}$– 5%		900	1400	
	Load regulation	VGH=24V, Iload=0mA to 20mA		0.07		%/mA
VGH ISOLATION SWITCH, GATE VOLTAGE FALL TIME CONTROL						
$R_{DS(on)}$	Q5 - Pass MOSFET R_{DSon}	I_{OUT} = 20 mA		12	30	Ω
Iadj	Capacitor charge current	Vadj = 20 V, CPI = 30 V	160	200	240	µA
	Minimum output voltage	Vadj = 0 V, I_{VGH} = 10 mA		2		V
I_{VGH}	Maximum output current		20			mA
TIMING CIRCUITS DLY1, DLY2, FDLY						
I_{DLY1}	Drive current into delay capacitor DLY1	V_{DLY1} = 1.213 V	3	5	7	µA
I_{DLY2}	Drive current into delay capacitor DLY1	V_{DLY2} = 1.213 V	3	5	7	µA
R_{FDLY}	Fault time delay resistror(2)		250	450	650	kΩ
GATE DRIVE (GD)						
$V_{(GD,\ Vs)}$	Gate drive threshold(3)	Vs rising	–12% of Vs		–4% of Vs	V
V_{OL}	Gate drive output low voltage	$I_{(sink)}$ = 500 µA			0.5	V
I_{LKG}	Gate drive output leakage current	V_{GD} = 15 V		0.001	1	µA
Vcom Buffer						
V_{CM}	Common mode input range		2.25		(Vs) –2V	V
V_{os}	Input offset voltage	I_{OUT} = 0 mA	–25		25	mV
	DC load regulation	Io = ±25 mA	–37		37	mV
		Io = ±50 mA	–77		55	
		Io = ±100 mA	–85		85	
		Io = ±150 mA	–110		110	
I_B	VCOMIN Input bias current		–300	–30	300	nA
I_{peak}	Peak output current	Vs = 15 V	1.2			A
		Vs = 10 V	0.65			
		Vs = 5 V	0.15			

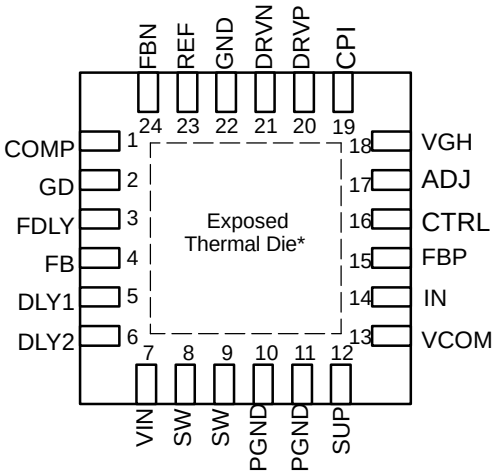
(2) The fault time is calculated as: t_F= C × R = C × 450 kΩ
(3) The GD signal is latched low when the main boost converter output Vs is within regulation. The GD signal is reset when the input voltage or enable of the boost converter is cycled low.

PIN ASSIGNMENT

TSSOP-24 Package
Top View



QFN-24 Package
Top View



* The thermal die (PowerPAD™) is connected to GND.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	QFN	TSSOP		
ADJ	17	14	I/O	Gate voltage shaping circuit. Connecting a capacitor to this pin sets the fall time of the positive gate voltage (VGH).
COMP	1	22	O	This is the compensation pin for the main boost converter. A small capacitor and if required a series resistor is connected to this pin.
CPI	19	16	I	Input of the VGH isolation switch and gate voltage shaping circuit.
CTRL	16	13	I	Control signal for the gate voltage shaping signal. Apply the control signal for the gate voltage control. Usually the timing controller of the LCD panel generates this signal. If this function is not required, this pin needs to be connected to VIN. By doing this, the internal switch between CPI and VGH provides isolation for the positive charge pump output VGH. DLY2 sets the delay time for VGH to come up.
DLY1	5	2	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to GND allows to set the delay time between the boost converter output Vs and the negative charge pump VGL during startup.
DLY2	6	3	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to GND allows to set the delay time between the negative charge pump VGL and the positive charge pump during startup. Note that Q5 in the Gate Voltage Shaping block only turns on when the positive charge pump (FBP) is within regulation. (This provides input to output isolation of VGH).
DRVN	21	18	I/O	Charge pump driver to generate the negative voltage VGL.
DRVP	20	17	I/O	Charge pump driver to generate the positive output voltage VGH.
FB	4	1	I	Feedback of the main boost converter generating Vsource (Vs).
FBN	24	21	I	Feedback pin of the negative charge pump VGL.
FBP	15	12	I	Feedback pin of the positive charge pump.
FDLY	3	24	I/O	Fault delay. Connecting a capacitor from this pin to Vin allows to set the delay time from the point when one of the outputs (VS, VGH, VGL) drops below its power good threshold until the devices enters the shutdown latch. To re-start the device the input voltage has to be cycled to GND. This feature can be disabled by connecting the FDLY pin to Vin.
GD	2	23	I	Active low open drain output. This output is latched low when the boost converter Vs is in regulation. This signal can be used to drive an external MOSFET to provide isolation for Vs.
GND	22	19		Analog ground

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	QFN	TSSOP		
IN	14	11	I	Input of the Vcom buffer. If this pin is connected to GND, the Vcom buffer is disabled.
PGND	10, 11	7, 8		Power ground
REF	23	20	O	Internal reference output typically 1.213 V
SUP	12	9	I/O	Supply pin of the positive, negative charge pump and Boost Converter Gate Drive Circuit. This pin needs to be connected to the output of the main boost converter and can't be connected to any other voltage rail.
SW	8, 9	5, 6	I	Switch pin of the boost converter
VGH	18	15	O	Positive output voltage to drive the TFT gates with an adjustable falltime. This pin is internally connected with a MOSFET switch to the positive charge pump input CPI.
VIN	7	4	I	This is the input voltage pin of the device.
VCOM	13	10	O	VCOM buffer output. Typically a 1-µF output capacitor is required on this pin.
PowerPAD™, exposed thermal die	NA	NA		The PowerPAD™ needs to be soldered to GND

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURES
Main Boost Converter			
η	Efficiency	vs Load current Vs=10 V	1
η	Efficiency	vs Load current Vs=13.5 V	2
η	Efficiency	vs Load current Vs=15 V	3
f_{SW}	Switching frequency	vs Input voltage and temperature	4
	PWM operation	at nominal load current	5
	PWM operation	at light load current	6
	Load transient response		7
	Softstart boost converter		8
	Power-on sequencing		9
	Power-on sequencing	External MOSFET in series to Vs	10
	Gate voltage shaping of V_{GH}		11
	Adjustable Fault detection		12
Negative Charge Pump Driver			
V_{GL}	V_{GL}	vs load current	13
Positive Charge Pump Driver			
V_{GH}	V_{GH}	vs load current; Charge pump doubler stage	14
V_{GH}	V_{GH}	vs load current; Charge pump tripler stage	15
VCOM Buffer			
	VCOM Buffer transconductance		16

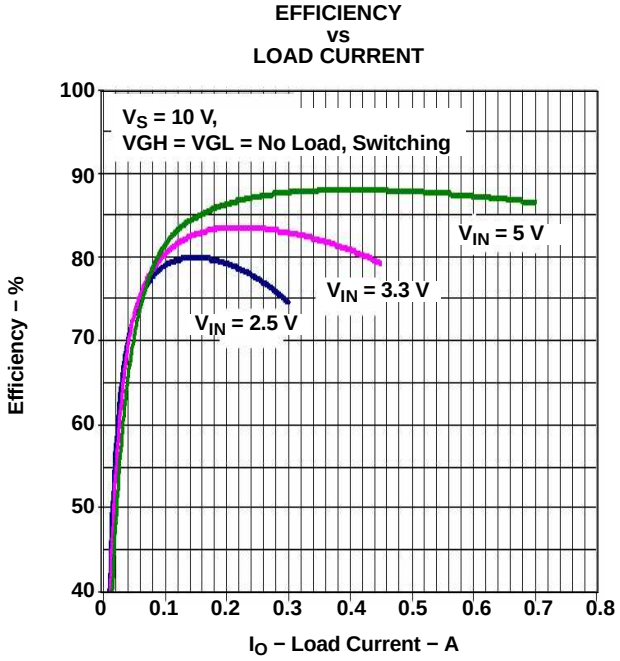


Figure 1.

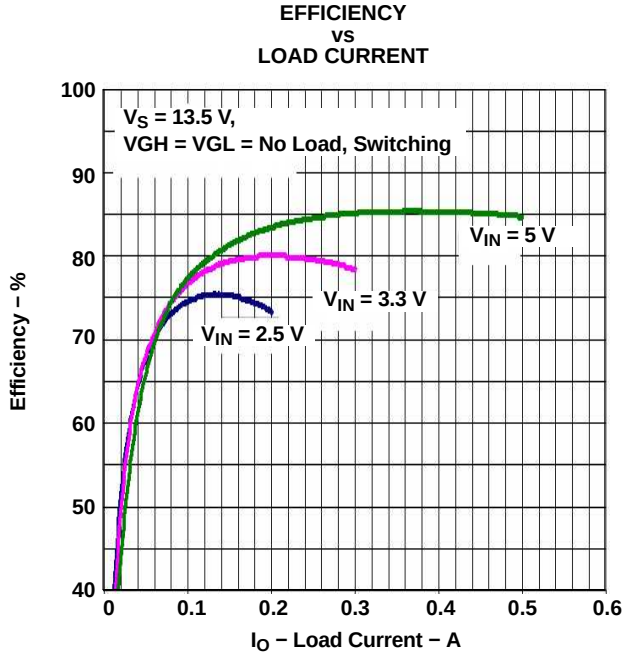


Figure 2.

EFFICIENCY
vs
LOAD CURRENT

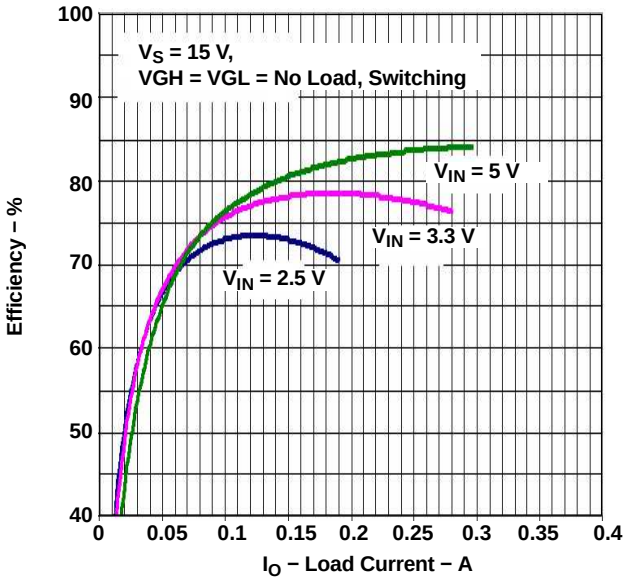


Figure 3.

SWITCHING FREQUENCY
vs
TEMPERATURE

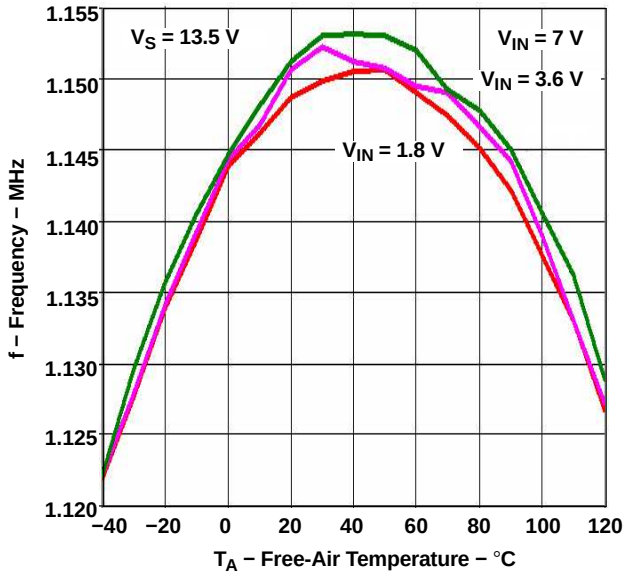


Figure 4.

PWM OPERATION
NOMINAL LOAD CURRENT

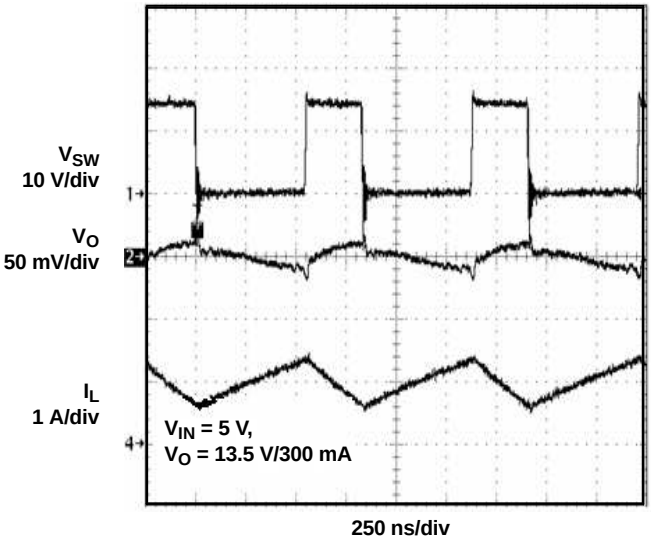


Figure 5.

PWM OPERATION
LIGHT LOAD CURRENT

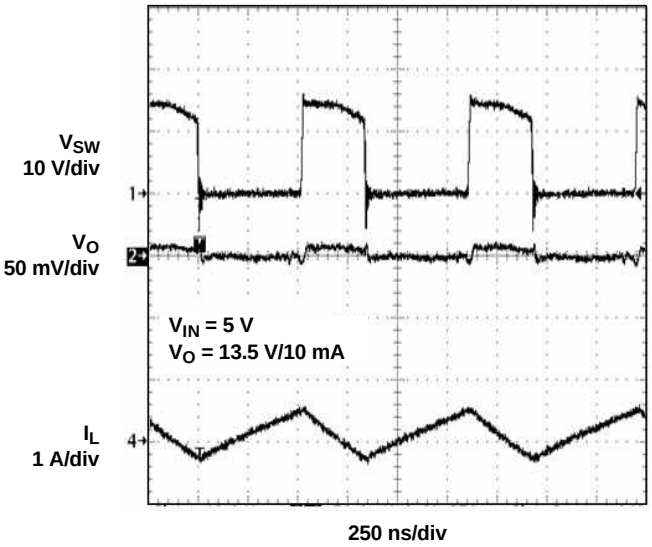


Figure 6.

LOAD TRANSIENT RESPONSE

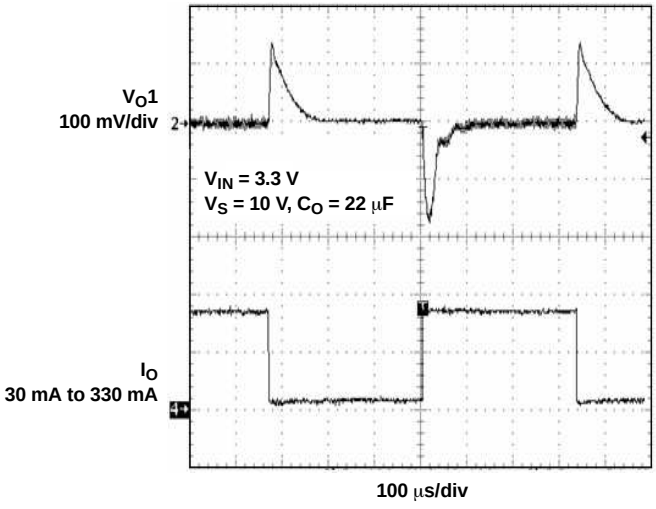


Figure 7.

SOFT START BOOST CONVERTER

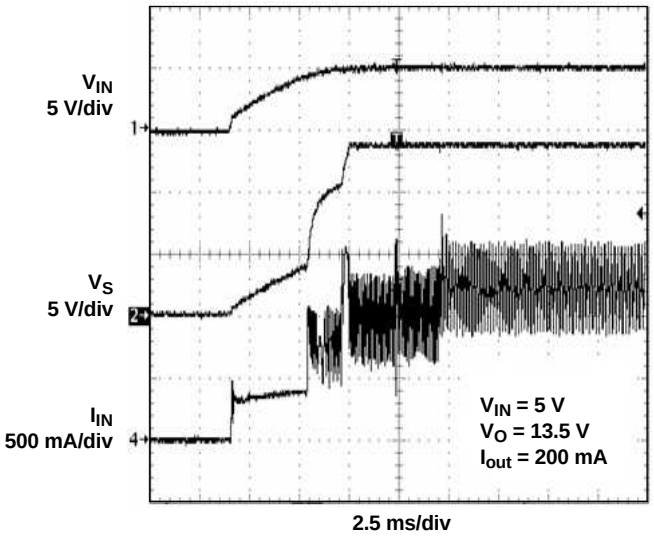


Figure 8.

POWER-ON SEQUENCING

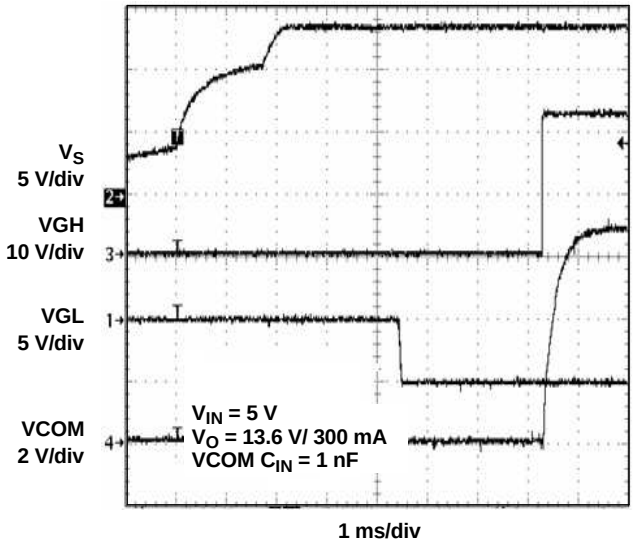


Figure 9.

POWER-ON SEQUENCING WITH EXTERNAL ISOLATION MOSFET AT V_S

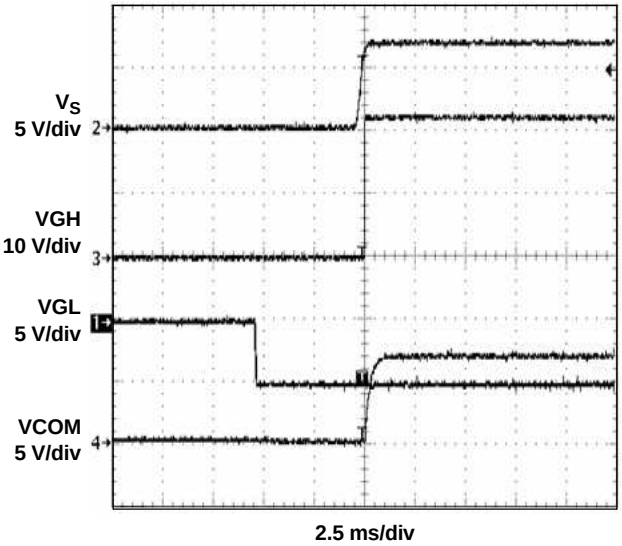


Figure 10.

GATE VOLTAGE SHAPING V_{GH}

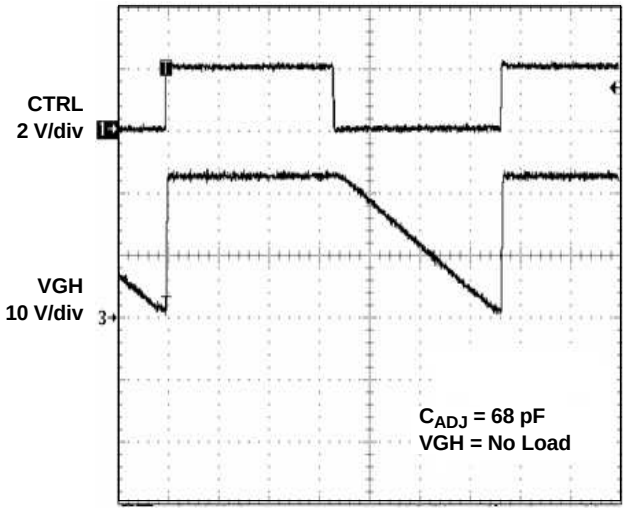


Figure 11.

ADJUSTABLE FAULT DETECTION

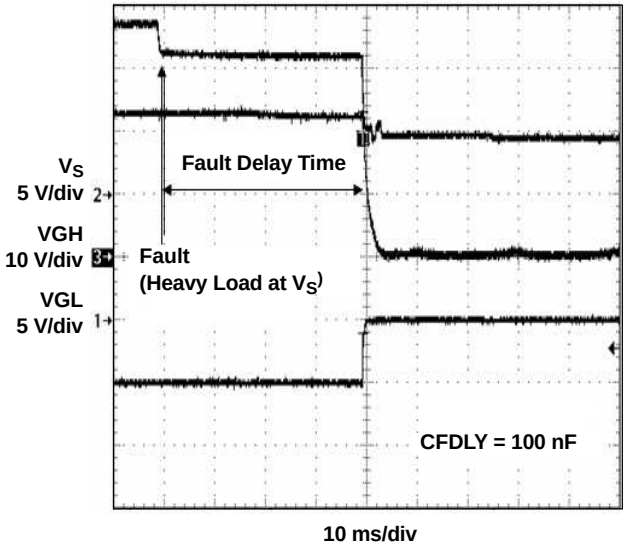


Figure 12.

V_{GL}– GATE VOLTAGE LOW
vs
LOAD CURRENT

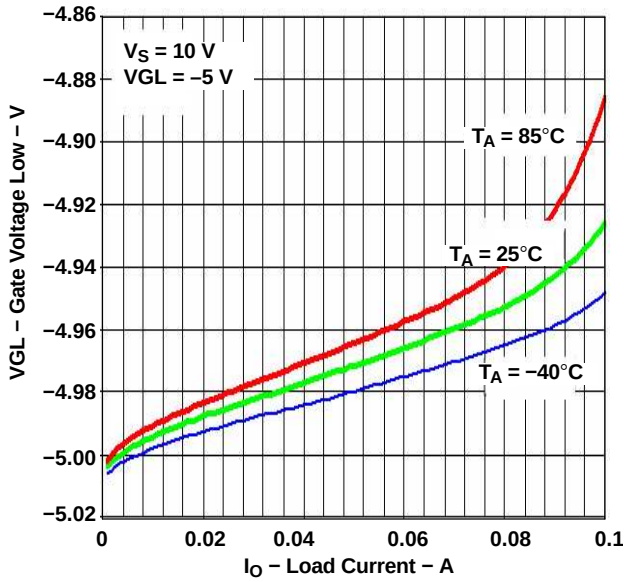


Figure 13.

V_{GH}– GATE VOLTAGE HIGH
vs
LOAD CURRENT –X2 STAGE

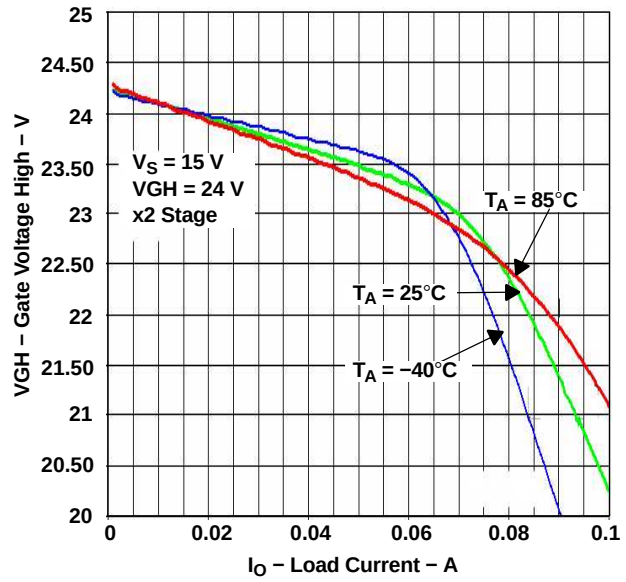
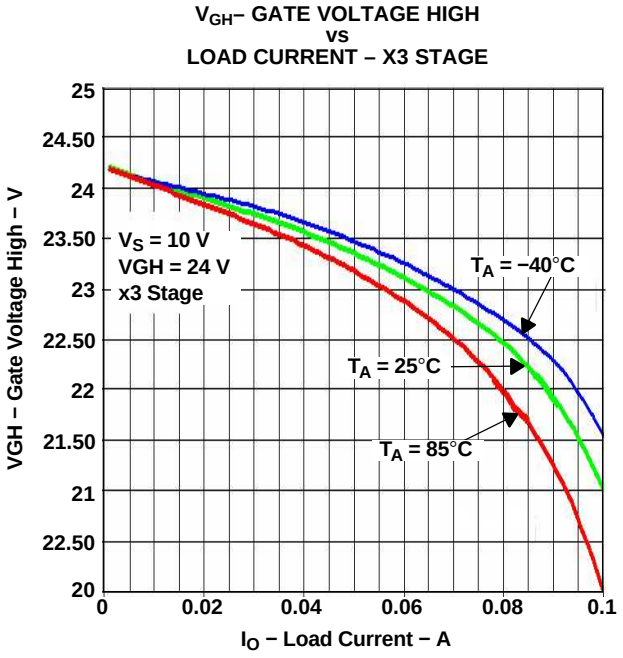
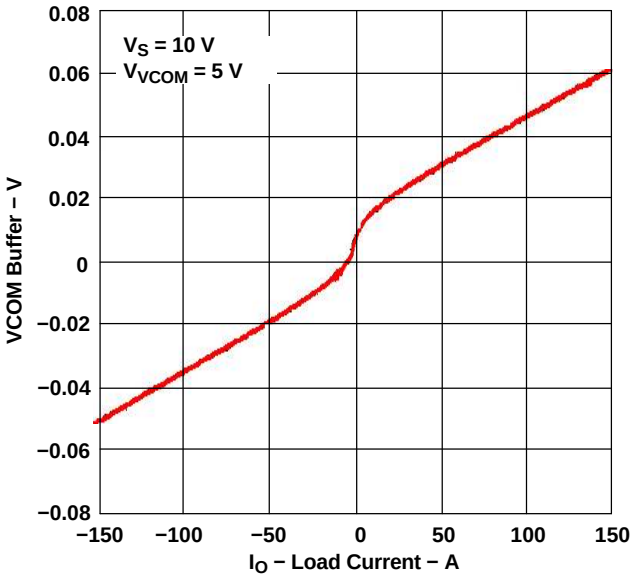


Figure 14.



V_{GH}– GATE VOLTAGE HIGH vs LOAD CURRENT – X3 STAGE

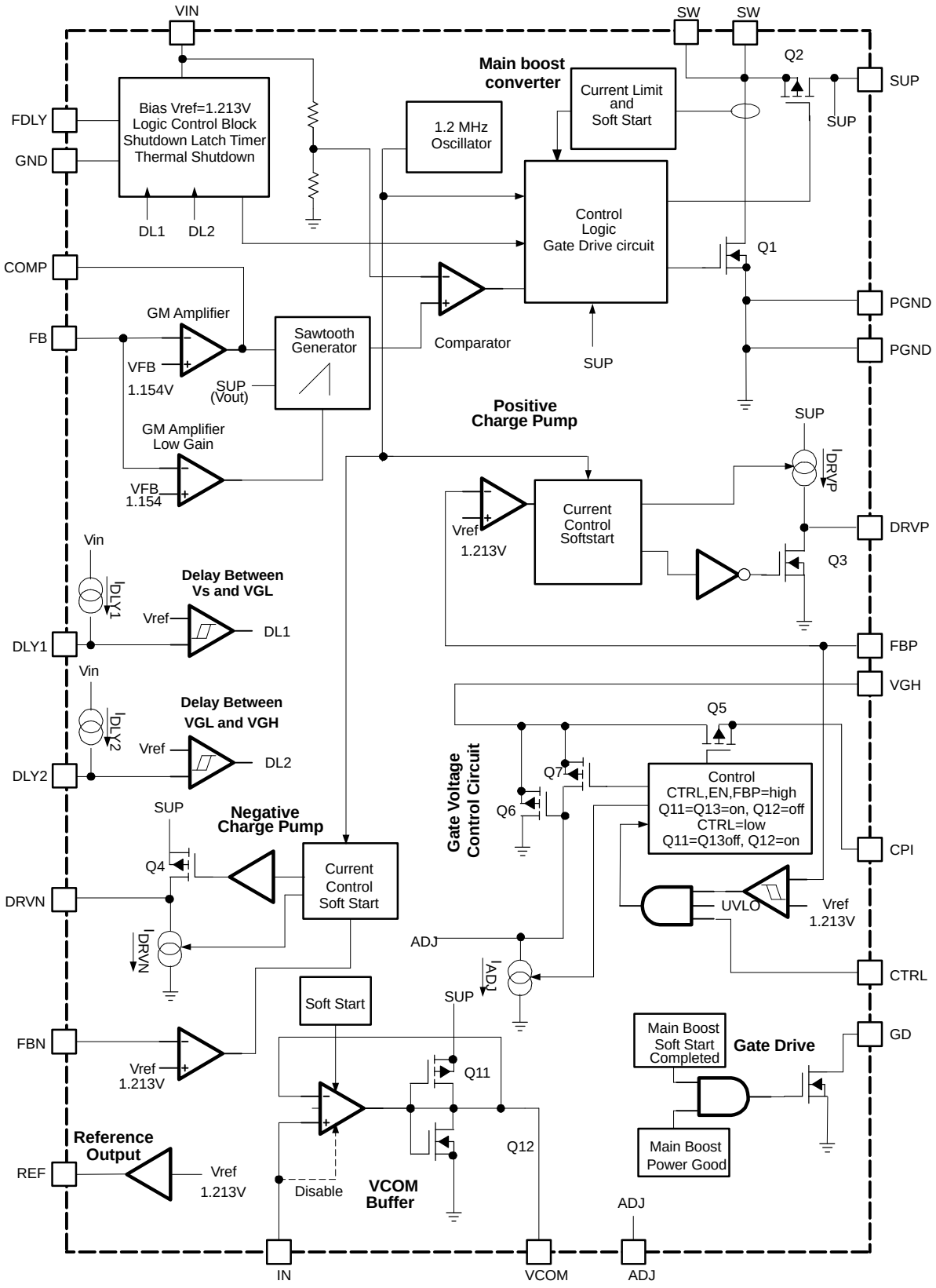
Figure 15.



VCOM BUFFER dV_{OUT} vs LOAD CURRENT

Figure 16.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Main Boost Converter

The main boost converter operates with pulse width modulation (PWM) and a fixed switching frequency of 1.2 MHz. The converter uses an unique fast response, voltage mode controller scheme with input voltage feedforward. This achieves excellent line and load regulation (0.16%/A load regulation typical) and allows the use of small external components. To add higher flexibility to the selection of external component values the device uses external loop compensation. Although the boost converter looks like a non-synchronous boost converter topology operating in discontinuous conduction mode at light load current the TPS65150 maintains continuous conduction even at light load currents. This is achieved by using the Virtual Synchronous Converter Technology having an external Schottky diode with an integrated MOSFET in parallel connected between SW pin and the SUP pin. See *Functional Block Diagram*. The intention of this MOSFET is to allow the current to go below ground which is the case at light load conditions. For this purpose a small integrated P-Channel MOSFET, with typically 10-Ω $R_{DS(on)}$, is sufficient. When the inductor current is positive the external Schottky diode with the lower forward voltage conducts the current. This causes the converter to operate with a fixed frequency in continuous conduction mode over the entire load current range. This avoids the ringing on the switch pin as seen with standard non-synchronous boost converter and allows a simpler compensation for the boost converter.

Soft Start

The main boost converter as well as the charge pump driver have an internal soft-start circuit. This avoids heavy voltage drops at the input voltage rail or at the output of the main boost converter Vs during startup caused by high inrush currents. As the main boost converter starts up the internal current limit threshold is increased in three steps. The device starts with the first step where the current limit is set to 2/5 of the typical current limit (2/5 of 2.3 A) for 2048 clock cycles then increased to 3/5 of the current limit for 2048 clock cycles and the 3rd step is the full current limit. This gives a typical start-up time around 5 ms.

Adjustable Fault Delay

The TPS65150 has an adjustable delay timer integrated shutting down the entire device in case of a fault at the outputs. The fault timer is also active during startup. Connecting a capacitor from the FDLY pin to Vin sets the delay time, from the point where one of the outputs (VS, VGH, VGL) drops below its power good threshold, until the device enters the shutdown latch. Since the fault delay timer is also active during startup, the device enters shutdown when the output voltage of the main boost converter, Vs, does not reach its power-good threshold after the fault delay time has passed. When an external isolation switch is used, shown in Figure 24, then the device provides short circuit protection even during start-up. To restart the device, the input voltage has to be cycled to GND. The shutdown function can be disabled by connecting FDLY to VIN. The fault delay time is calculated as: $t_F = C \times R = C \times 450\ k\Omega = 100\ nF \times 450\ k\Omega \approx 40\ ms$

Positive Charge Pump

The positive charge pump provides a regulated output voltage, set by the external resistor divider. Figure 17 shows an extract of the positive charge pump driver circuit out of the block diagram. The operation of the charge pump driver can be understood best by looking at Figure 17. During the first cycle Q3 is turned on and the flying capacitor, Cfly, is charged to the source voltage, Vs. During the next clock cycle Q3 is turned off, and the current source charges the drive pin, DRVP, up to the supply voltage, VSUP. Since the flying capacitor voltage sits on top of the drive pin voltage the maximum output voltage is VGH=Vsup + Vs - Vdrop. Vdrop is the voltage drop across the external diodes and internal charge pump MOSFETs.

DETAILED DESCRIPTION (continued)

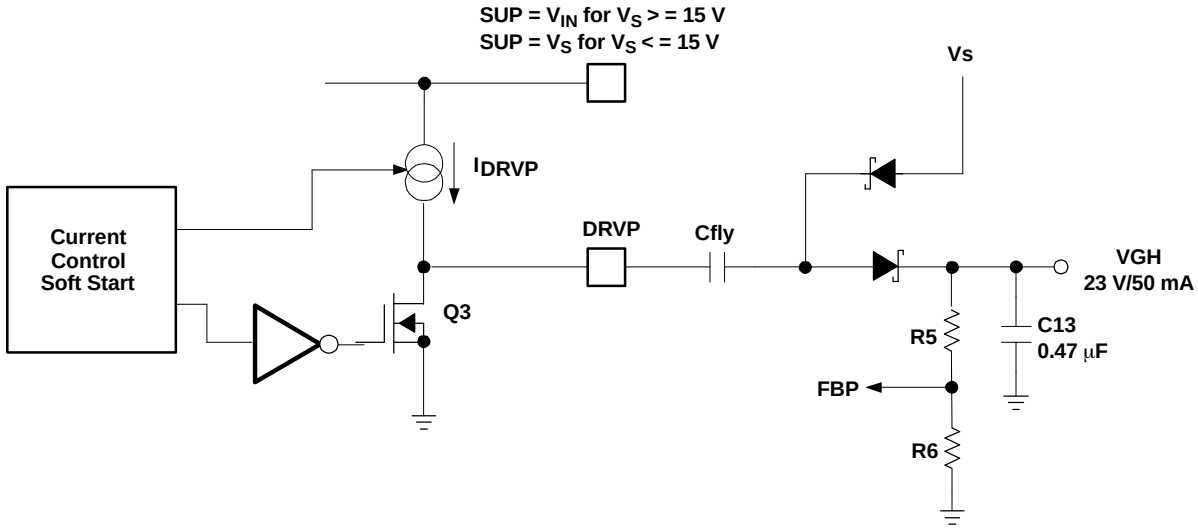


Figure 17. Extract of the Positive Charge Pump Driver

If higher output voltages are required another charge pump stage can be added to the output, as shown in Figure 21 at the end of the data sheet. To minimize quiescent current a high impedance feedback divider should be used. The top feedback resistor should not be selected larger than 1MΩ.

Setting the output voltage:

$$V_{out} = 1.213 \times \left(1 + \frac{R5}{R6}\right)$$

$$R5 = R6 \times \left(\frac{V_{out}}{V_{FB}} - 1\right) = R6 \times \left(\frac{V_{out}}{1.213} - 1\right) \quad (1)$$

Negative Charge Pump

The negative charge pump provides a regulated output voltage set by the external resistor divider. The negative charge pump operates very similar to the positive charge pump with the difference that the voltage on the supply pin SUP is inverted. The maximum output voltage for a single stage charge pump inverter is VGL = (–VSUP) + Vdrop. Vdrop is the voltage drop across the external diodes and internal charge pump MOSFETs.

Setting the output voltage:

$$V_{out} = -V_{REF} \times \frac{R3}{R4} = -1.213\,V \times \frac{R3}{R4}$$

$$R3 = R4 \times \frac{|V_{out}|}{V_{REF}} = R4 \times \frac{|V_{out}|}{1.213} \quad (2)$$

The lower feedback resistor value, R4, should range between 40 kΩ to 120 kΩ; or, the overall feedback resistance should be within 500 kΩ to 1 MΩ. Smaller values load the reference too heavily; and larger values may cause stability problems. The negative charge pump requires two external Schottky diodes. The peak current rating of the Schottky diode has to be twice the load current of the output. For a 20-mA output current, the BAT54 dual Schottky diode is a good choice.

DETAILED DESCRIPTION (continued)

Power-on Sequencing, DLY1, DLY2

As soon as the input voltage is applied, and rises above the undervoltage lockout (UVLO), the device starts with the main boost converter, Vs, coming up first. Then the negative voltage, VGL, comes up, set by the delay time DLY1; and then the positive charge pump, VGH, set by the delay time DLY2. Finally, the VCOM buffer starts up. The delay times, DLY1 and DLY2, are set by the capacitor value connected to these pins. An internal current source charges the capacitor with a constant current of typically 5 µA until the voltage reaches the internal comparator trip point of Vref = 1.213 V.

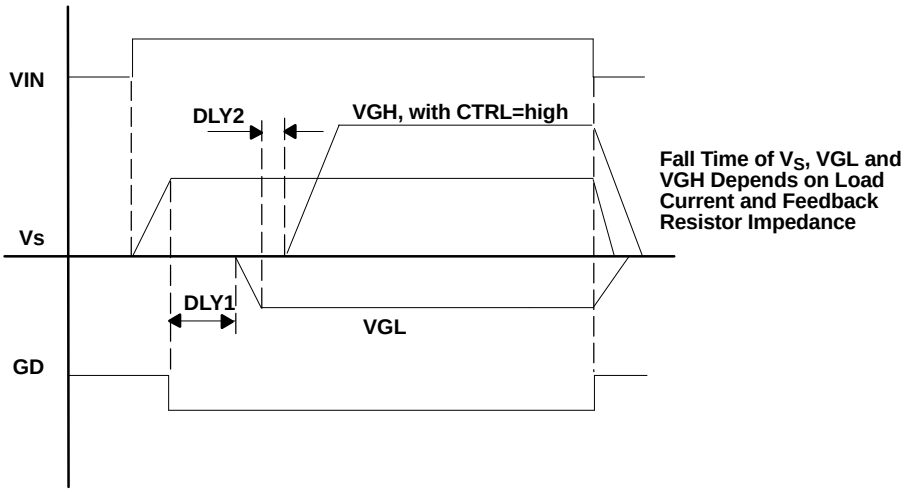


Figure 18. Power on Sequencing With CTRL = High

Setting the Delay Times DLY1, DLY2

Connecting an external capacitor to the DLY1 and DLY2 pins sets the delay time. If no delay time is required, these pins can be left open. To set the delay time, the external capacitor connected to DLY1 and DLY2 is charged with a constant current source of typically 5 µA . The delay time is terminated when the capacitor voltage has reached the internal reference voltage of Vref = 1.213 V. The external delay capacitor is calculated:

$$C_{dly} = \frac{5\ \mu A \times td}{V_{REF}} = \frac{5\ \mu A \times td}{1.213\ V} \quad \text{with td} = \text{Desired delay time} \tag{3}$$

Gate Drive, GD

The gate drive pin can be used to drive an external MOSFET, providing isolation for the main boost converter Vs. The gate drive is an open drain output capable of sinking typically 500 µA. The gate drive is latched low as soon as the main boost converter, Vs, reaches its power-good threshold. The gate drive signal goes high impedance when the input voltage falls below the undervoltage lockout (UVLO) or the device enters shutdown latch triggered by the fault delay.

VGH Switch / Gate Voltage Shaping, CPI – VGH

The gate voltage shaping circuit is used to reduce crosstalk between the LCD pixels by adjusting the fall time of the positive gate voltage, VGH. The CTRL pin needs to be connected to Vin if the gate voltage shaping function is not used. This function is implemented by adjusting the fall time of the gate voltage signal, VGH, generated by the positive charge pump. The fall time can be adjusted with the external capacitor, Cadj connected to the ADJ pin. The corresponding timing diagram is shown in Figure 20.

DETAILED DESCRIPTION (continued)

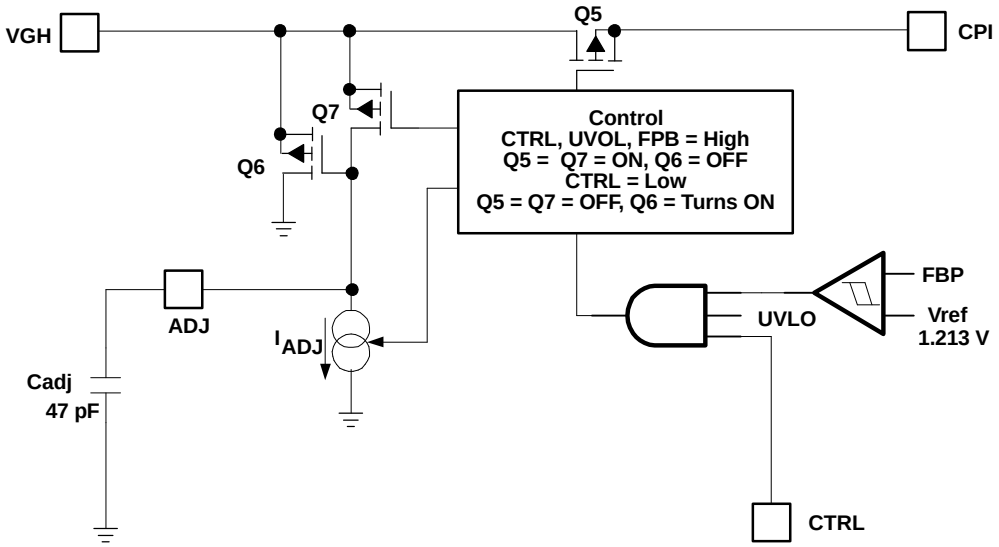


Figure 19. Implementation of the Gate voltage shaping

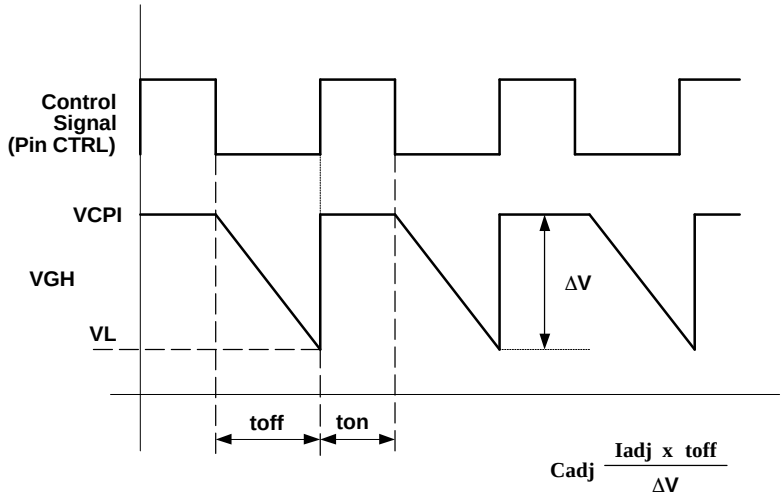


Figure 20. Timing Diagram of the Gate voltage shaping

The control signal applied to CTRL sets the timing of VGH. When CTRL is high, Q5 is turned on and the positive charge pump voltage applied on CPI is present on VGH. At the same time, the capacitor connected to ADJ is charged up by Q7 to VGH, while Q6 is turned off. When CTRL is taken low, Q5 and Q7 turn off, and Q6 is slowly turned on as the capacitor on ADJ is discharged by the discharge current I_{ADJ}, typically 200 µA. The capacitor value on C_{ADJ} determines the fall time of VGH. For a given off time (toff), external capacitor Cadj determines the desired voltage drop, ΔV.

$$Cadj = \frac{Iadj \times toff}{\Delta V} \quad \text{with } Iadj = 200\ \mu A \tag{4}$$

When the input voltage falls below the undervoltage threshold (UVLO) or the device enters shutdown latch triggered by the fault delay timer, then VGH is disconnected from CPI by Q5 and is high impedance.

DETAILED DESCRIPTION (continued)

Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Typically, the thermal shutdown threshold is 155°C . When this threshold is reached, the device enters shutdown. The device can be enabled again by cycling the input voltage to GND.

Vcom Buffer

The VCOM Buffer is a transconductance amplifier designed to drive capacitive loads. The IN pin is the input of the VCOM buffer. If the VCOM buffer is not required for certain applications, it is possible to shut down the VCOM buffer by connecting IN to ground, reducing the overall quiescent current. The VCOM buffer features a soft start, avoiding a large voltage drop at Vs during startup. The VCOM buffer input, IN, cannot be pulled dynamically to ground during operation.

Boost Converter Design Procedure

The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves, or use a worst case assumption for the expected efficiency, e.g. 75%.

1. Duty Cycle : $$D = 1 - \frac{Vin \times \eta}{Vout} \quad (5)$$

2. Maximum output current : $$I_{out} = \left(Isw - \frac{Vin \times D}{2 \times fs \times L} \right) \times (1 - D) \quad (6)$$

3. Peak switch current : $$I_{swpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{out}}{1 - D} \quad (7)$$

With

Isw = Converter switch current (minimum switch current limit = 2.0 A)

fs = Converter switching frequency (typical 1.2 MHz)

L = Selected inductor value

η = Estimated converter efficiency (use the number from the efficiency plots, or 0.75 as an estimation)

The peak switch current is the steady-state peak switch current that the integrated switch, inductor, and external Schottky diode has to be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest. For the calculation of the maximum current delivered by the boost converter it needs to be considered that the positive and negative charge pumps as well as the VCOM buffer run from the output of the boost converter as well.

Inductor Selection

Several inductors work with the TPS65150. Especially with external compensation, the performance can be adjusted to the specific application requirements. The main parameter for the inductor selection is the inductor saturation current, which should be higher than the peak switch current as calculated previously with additional margin to cover for heavy load transients. The alternative, more conservative approach, is to choose the inductor with a saturation current at least as high as the typical switch current limit of 2.5 A. The second important parameter is the inductor DC resistance. Usually the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. For a boost converter, where the inductor is the energy storage element, the type and material of the inductor influences the efficiency as well. Especially at high switching frequencies of 1.2 MHz, inductor core losses, proximity effects, and skin effects become more important. Usually an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary between 2% to 10%. For the TPS65150, inductor values between 3.3 µH and 6.8 µH are a good choice, but other values can be used as well. Possible inductors are shown in Table 1.

DETAILED DESCRIPTION (continued)

Table 1. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS IN mm	Isat – DC Resistance
4.7 µH	Coilcraft DO1813P-472HC	8,89 × 6,1 × 5,0	2.6 A – 54 mΩ
4.2 µH	Sumida CDRH5D28 4R2	5,7 × 5,7 × 3	2.2 A – 23 mΩ
4.7 µH	Sumida CDC5D23 4R7	6 × 6 × 2,5	1.6 A – 48 mΩ
4.2 µH	Sumida CDRH6D12 4R2	6,5 × 6,5 × 1,5	1.8 A – 60 mΩ
3.9 µH	Sumida CDRH6D28 3R9	7,0 × 7,0 × 3,0	2.6A – 20 mΩ
3.3 µH	Sumida CDRH6D12 4R2	6,5 × 6,5 × 1,5	1.9 A – 50 mΩ

Output Capacitor Selection

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value, but tantalum capacitors can be used as well, depending on the application. A 22-µF ceramic output capacitor works for most applications. Higher capacitor values can be used to improve the load transient regulation. See Table 2 for the selection of the output capacitor.

Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 22-µF ceramic input capacitor is sufficient for most applications. For better input voltage filtering, this value can be increased. See Table 2, and *Typical Applications* for input capacitor recommendations.

Table 2. Input and Output Capacitor Selection

CAPACITOR	VOLTAGE RATING	COMPONENT SUPPLIER	COMMENTS
22 µF/1206	16 V	Taiyo Yuden EMK325BY226MM	Cout
22 µF/1206	6.3 V	Taiyo Yuden JMK316BJ226	Cin

Rectifier Diode Selection

To achieve high efficiency, a Schottky diode should be used. The reverse voltage rating should be higher than the maximum output voltage of the converter. The required average rectified forward current rating of the Schottky diode is calculated as the off time of the converter times the maximum switch current of the TPS65150:

$$D = 1 - \frac{Vin}{Vout} \quad (8)$$

$$I_{avg} = (1 - D) \times Isw = \frac{Vin}{Vout} \times 2.0\ A \quad \text{with Isw} = \text{minimum switch current of the TPS65150 (2.0 A)} \quad (9)$$

Usually, a Schottky diode with 1-A maximum average rectified forward current rating is sufficient for most of the applications. Secondly, the Schottky rectifier has to be able to dissipate the power. The dissipated power is the average rectified forward current times the diode forward voltage.

PD = Iavg × VF = Isw × (1 – D) × VF with Isw = minimum switch current of the TPS65150 (2.0 A).

Typically, the diode should be able to dissipate 270 mW maximum depending on the load current and forward voltage. In terms of efficiency, the main parameters of the diode are the forward voltage and the reverse leakage current of the diode; both should be as low as possible.

Table 3. Rectifier Diode Selection

CURRENT RATING Iavg	Vr	$V_{forward}$	COMPONENT SUPPLIER
2 A	20 V	0.44 V at 2 A	SL22, Vishay Semiconductor
2 A	20 V	0.5 V at 2 A	SS22, Fairchild Semiconductor
1 A	30 V	0.44 V at 2 A	MBRS130L, Fairchild Semiconductor
1 A	20 V	0.45 V at 1 A	UPS120, Microsemi
1 A	20 V	0.45 V at 1 A	MBRM120, ON Semiconductor

Setting the Output Voltage

The output voltage is set by the external resistor divider and is calculated as:

$$V_{out} = 1.146\ V \times \left(1 + \frac{R1}{R2}\right) \quad (10)$$

To minimize quiescent current high impedance feedback resistors should be used. The upper feedback resistor R1 should not be larger than 1MΩ. Across the upper resistor, a bypass capacitor is required to speed up the circuit during load transients. The capacitor value is selected according to Table 4 and the formula (12) as shown in the next section.

Compensation (COMP) and feedforward capacitor

The regulator loop can be compensated by adjusting the external components connected to the COMP pin. The COMP pin is the output of the internal transconductance error amplifier. The compensation capacitor adjusts the low-frequency gain. Adding a resistor in series to it will increase the high frequency gain. Since the converter gain changes with the input voltage different compensation capacitors are required. Lower input voltages require a higher gain, and therefore a smaller compensation capacitor value.

Table 4. Compensation Components for different V_{IN} Voltages

V_{IN}	C_{COMP}	R_{COMP}	f_Z
2.5 V	470 pF	68 kΩ	8.8 kHz
3.3 V	470 pF	33 kΩ	7.8 kHz
5.0 V	2.2 nF	0 kΩ	11.2 kHz

The feedforward capacitor across the feedback resistor devider of the boost converter sets an additional zero at the frequency fz to compensate the loop. Typical values for fz are shown in Table 4 giving a feedforward capacitor value as calculated below.

$$C_{FF} = \frac{1}{2 \times \pi \times f_Z \times R1} = \frac{1}{2 \times \pi \times 8.8\ kHz \times R1} \quad (11)$$

Please refer to the typical application circuits at the end of the datasheet for detailed circuit configurations and values.

Layout Consideration

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching dc-dc converter at high load currents, too-thin PCB traces can cause significant voltage spikes. Good grounding becomes important as well. If possible, a common ground plane to minimize ground shifts between analog (GND) and power ground (PGND) is recommended. Additionally, the following PCB design layout guidelines are recommended for the TPS65150:

1. Boost converter output capacitor, input capacitor and Power ground (PGND) should form a star ground or should be directly connected together on a common power ground plane.
2. Place the input capacitor directly from the input pin (VIN) to ground.
3. Use a bold PCB trace to connect SUP to the output Vs.
4. Place a small baypass capacitor from the SUP pin to ground.
5. Use short traces for the charge-pump drive pins (DRVN, DRVP) of VGH and VGL because these traces carry switching currents.
6. Place the charge pump flying capacitors as close as possible to the DRVP and DRVN pin, avoiding a high voltage spikes at these pins.
7. Place the Schottky diodes as close as possible to the IC, respectively to the flying capacitors connected to DRVP and DRVN.
8. Carfully route the chare pump traces to avoid interference with other circuits since they carry high voltage switching currents .
9. Place the output capacitor of the VCOM buffer as close as possible to the output pin (VCOM).

10. The power pad of the TSSOP package needs to be soldered to the PCB for imroved thermal performance.
11. The thermal pad of the QFN package needs to be soldered to the PCB for reliability and thermal performance reasons.

APPLICATION INFORMATION

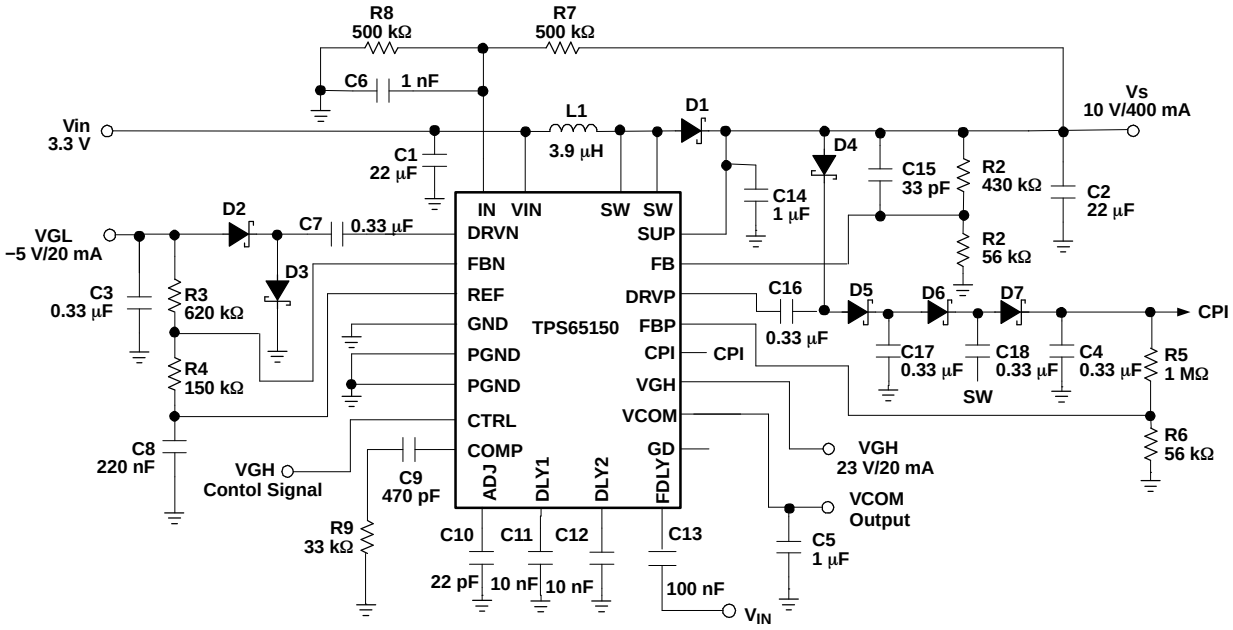


Figure 21. Notebook LCD Supply powered from a 3.3V rail

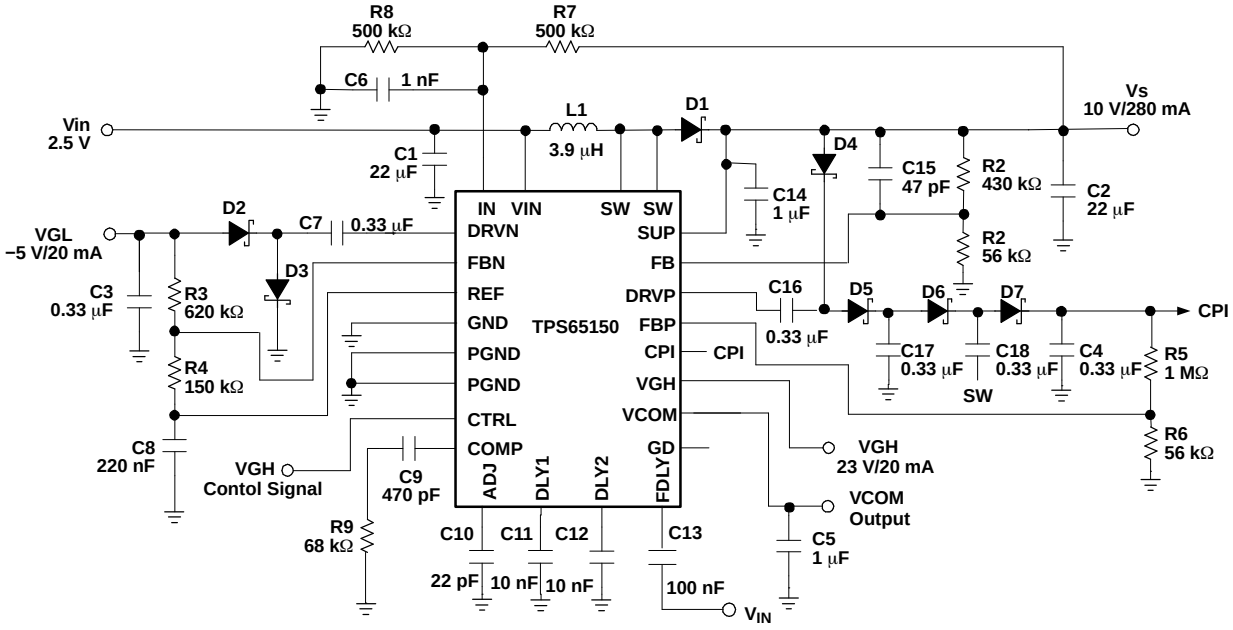


Figure 22. Notebook LCD Supply powered from a 2.5V rail

APPLICATION INFORMATION (continued)

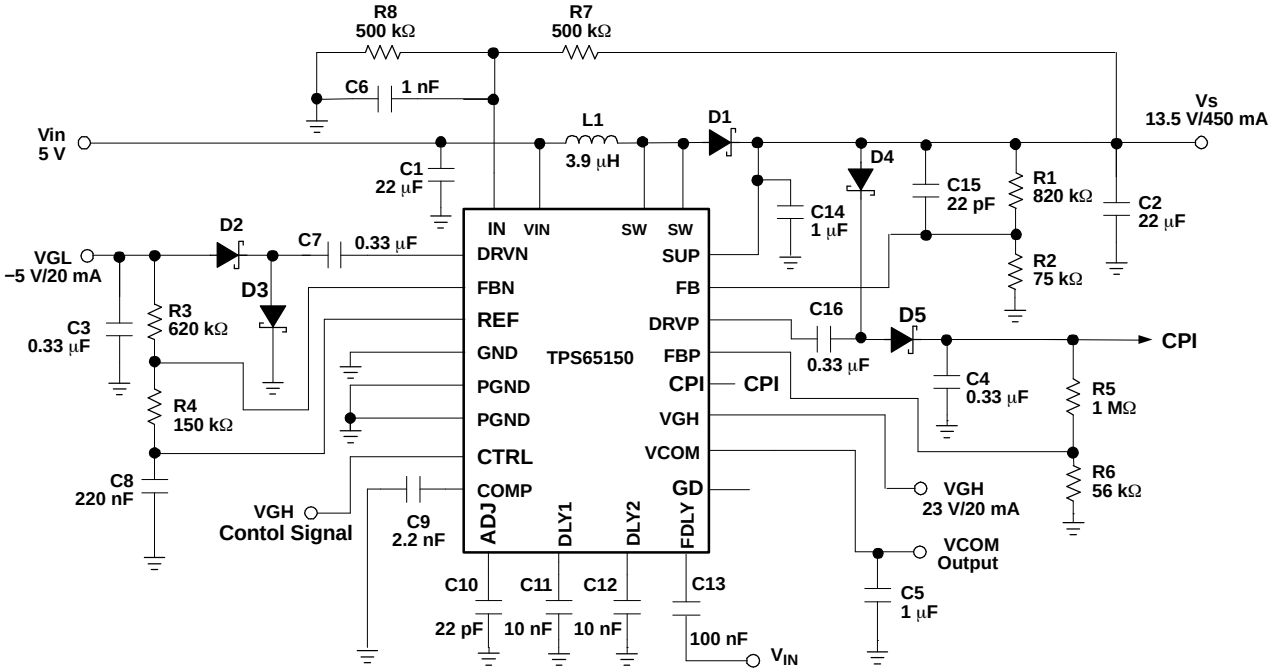


Figure 23. Monitor LCD Supply powered from a 5V rail

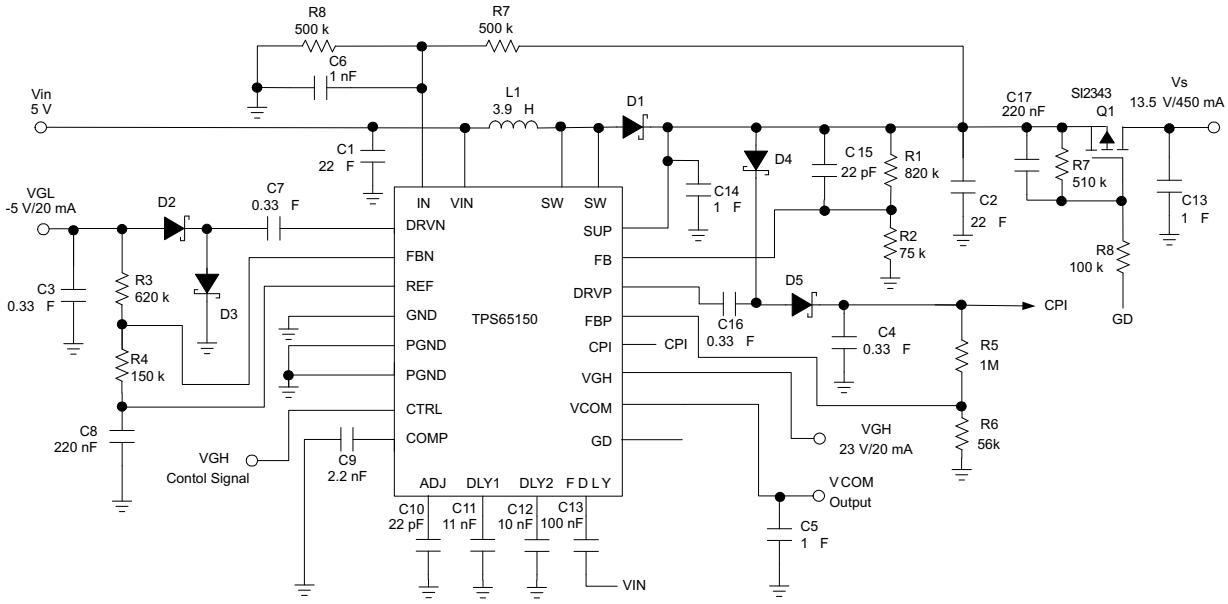


Figure 24. Typical Isolation and Short-Circuit Protection Switch for Vs using Q1 and Gate Drive Signal (GD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65150PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65150PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65150PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65150PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65150RGER	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65150RGERG4	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

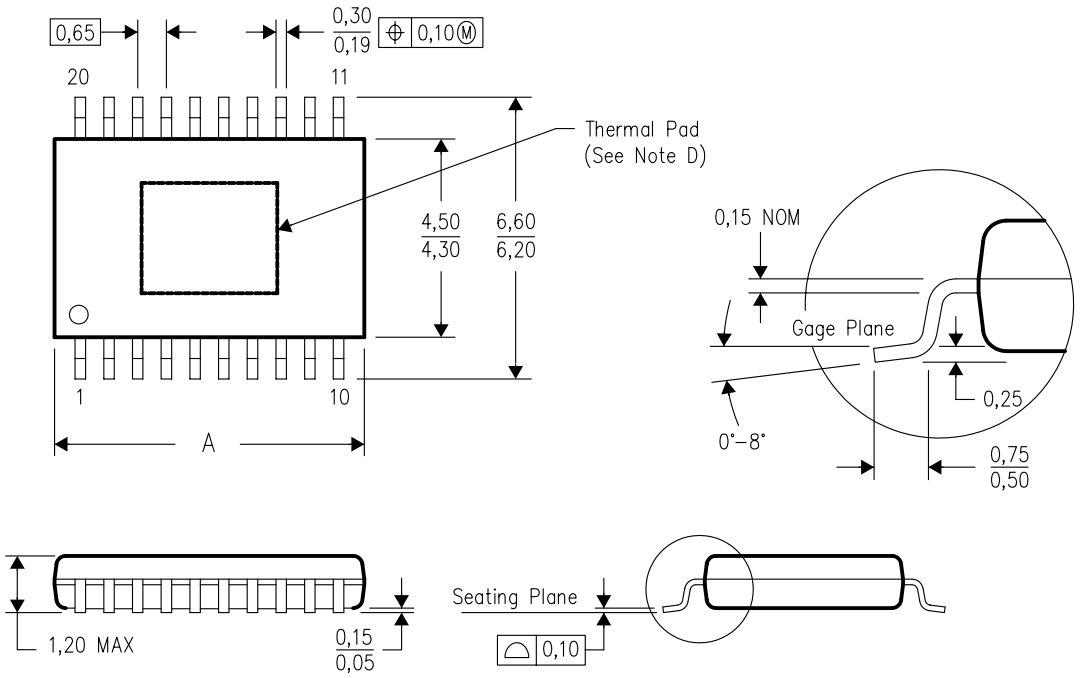
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

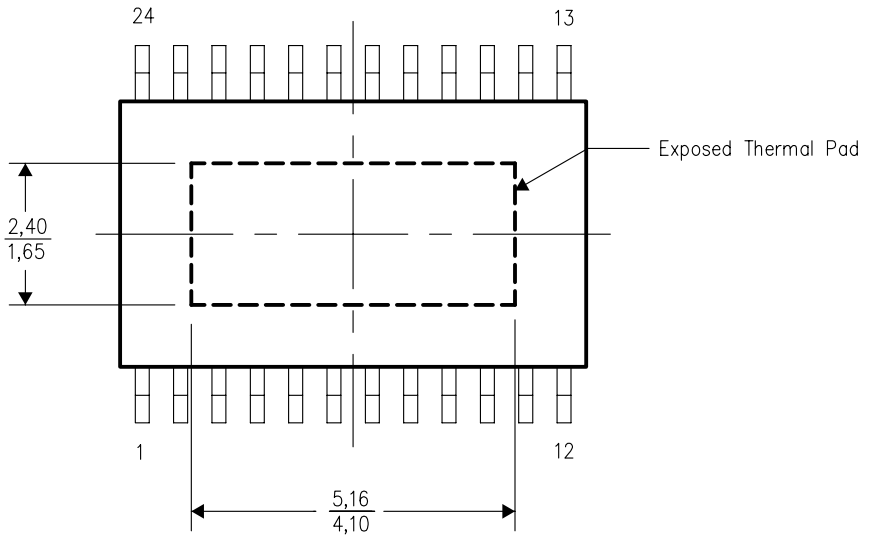
PWP (R–PDSO–G24)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

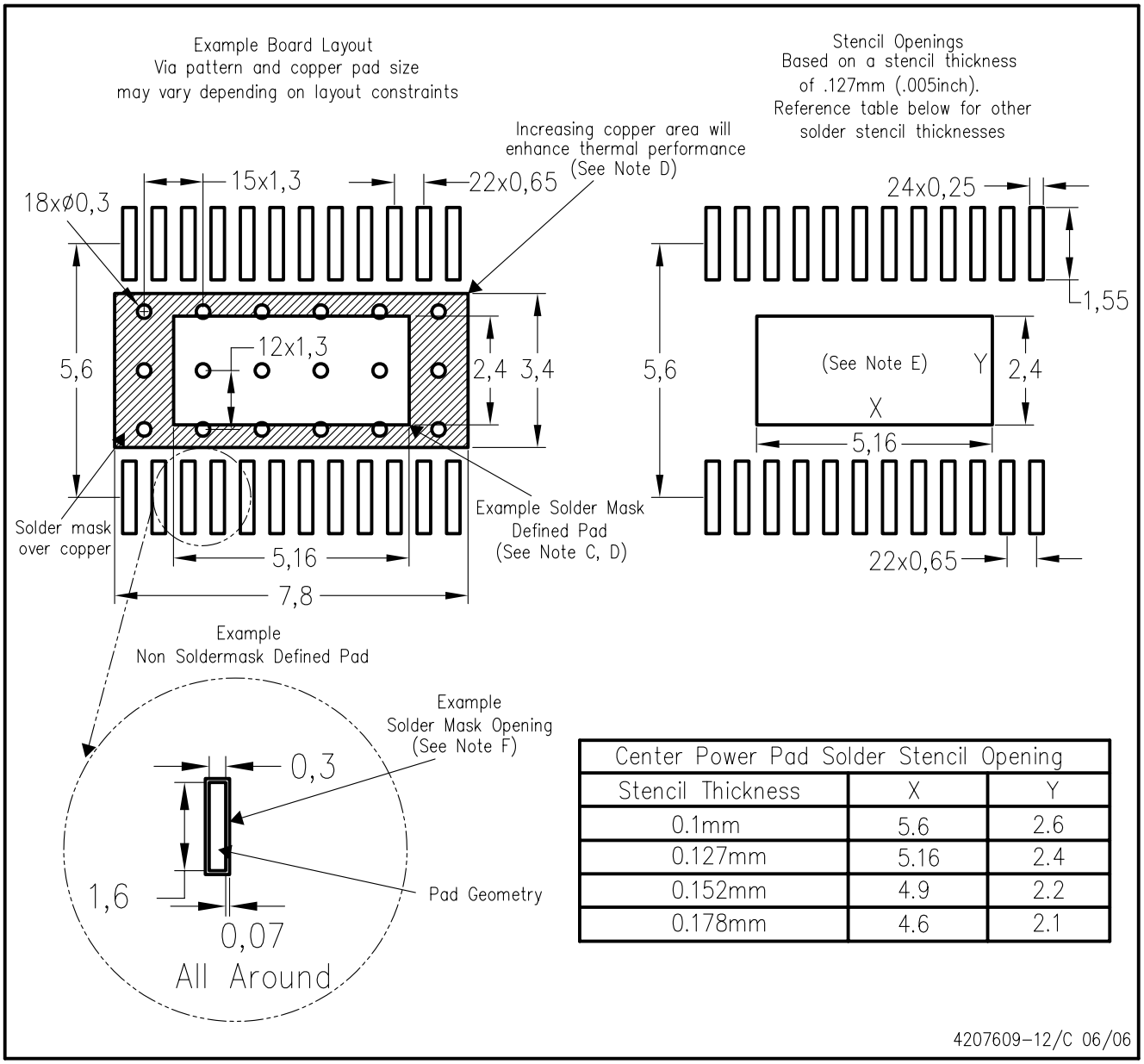


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G24) PowerPAD™

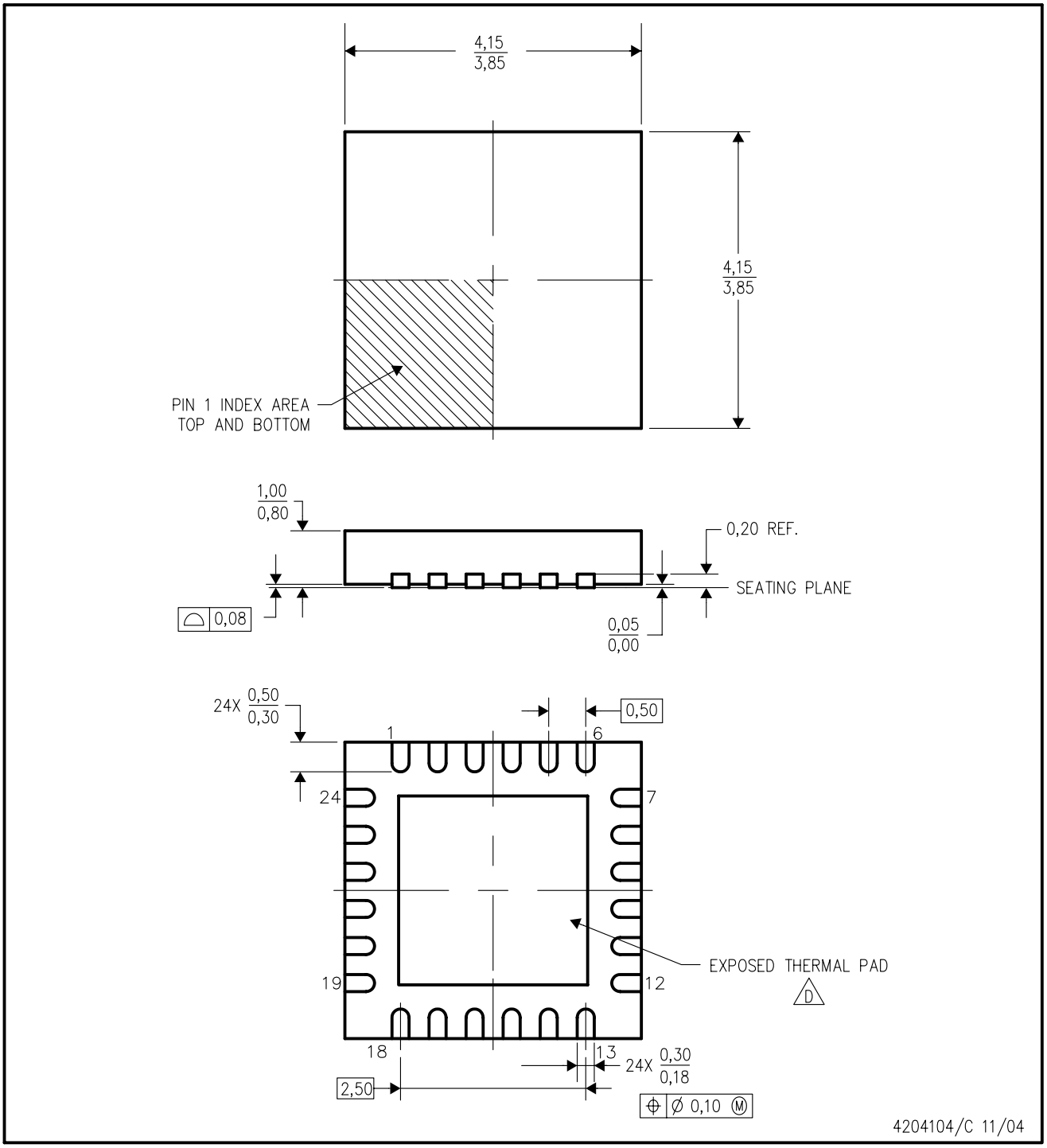


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	2.6
0.127mm	5.16	2.4
0.152mm	4.9	2.2
0.178mm	4.6	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

RGE (S–PQFP–N24) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

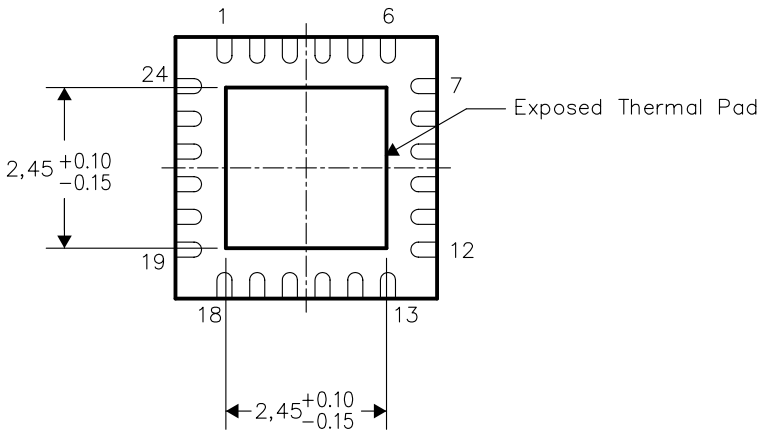
RGE (S–PQFP–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

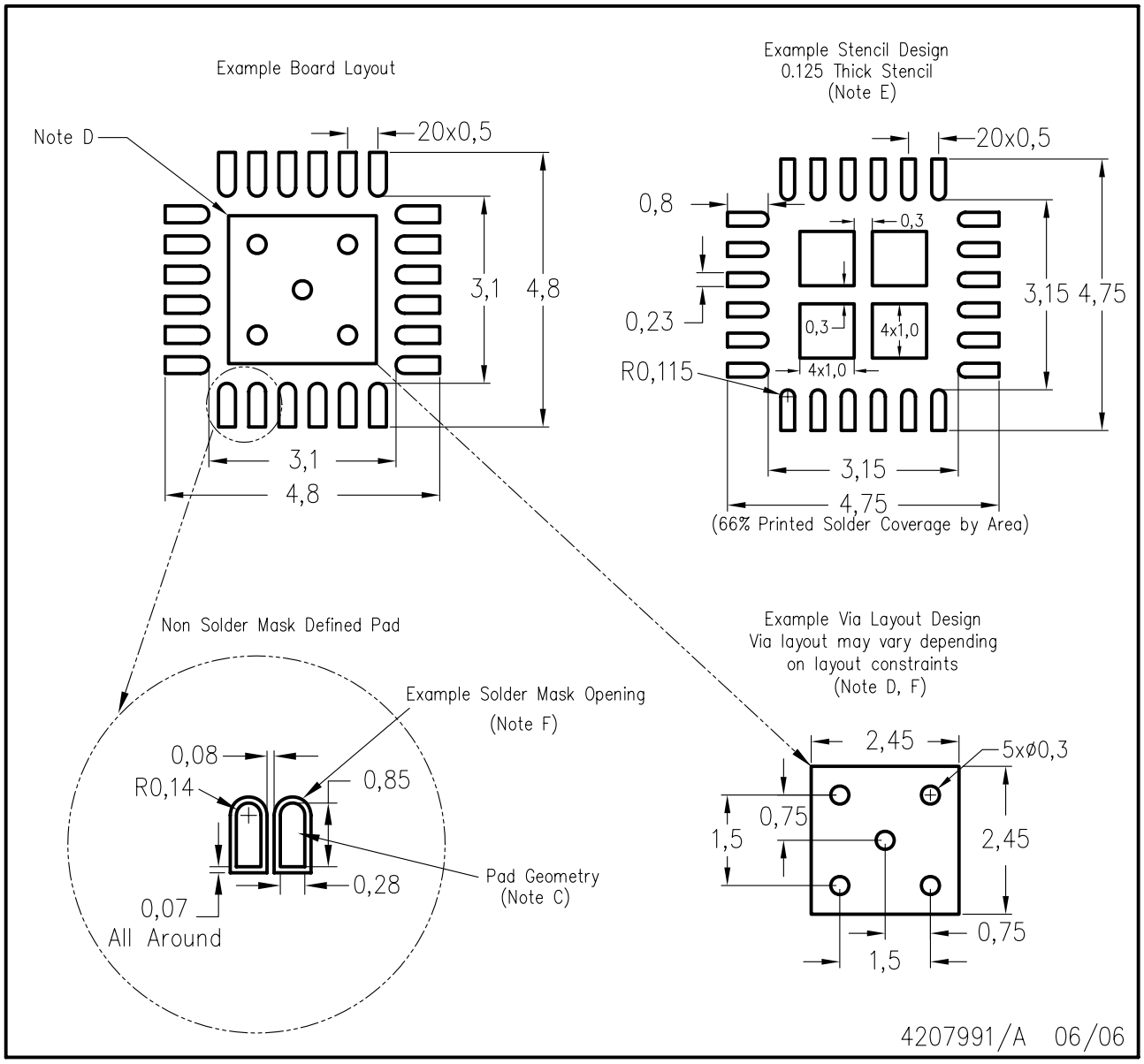


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGE (S–PQFP–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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