2.7-V TO 5.5-V LOW-POWER DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

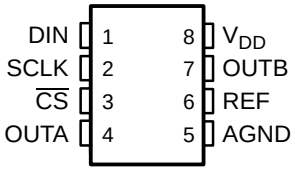
FEATURES

- **Dual 12-Bit Voltage Output DAC**
- **Programmable Internal Reference**
- **Programmable Settling Time:**
  - **1 µs in Fast Mode,**
  - **3.5 µs in Slow Mode**
- **Compatible With TMS320 and SPI™ Serial Ports**
- **Differential Nonlinearity <0.5 LSB Typ**
- **Monotonic Over Temperature**

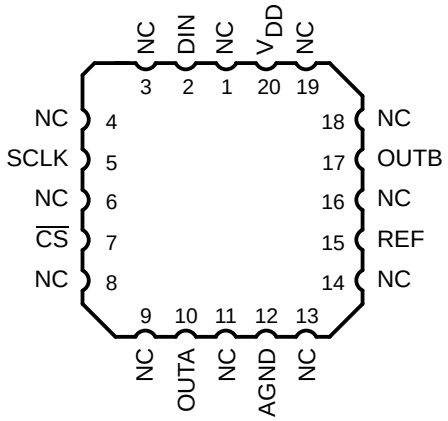
APPLICATIONS

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

D, JG PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



DESCRIPTION

The TLV5638 is a dual 12-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface allows glueless interface to TMS320, SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed vs power dissipation. With its on-chip programmable precision voltage reference, the TLV5638 simplifies overall system design.

Because of its ability to source up to 1 mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in an 8-pin SOIC package to reduce board space in standard commercial, industrial, and automotive temperature ranges. It is also available in JG and FK packages in the military temperature range.

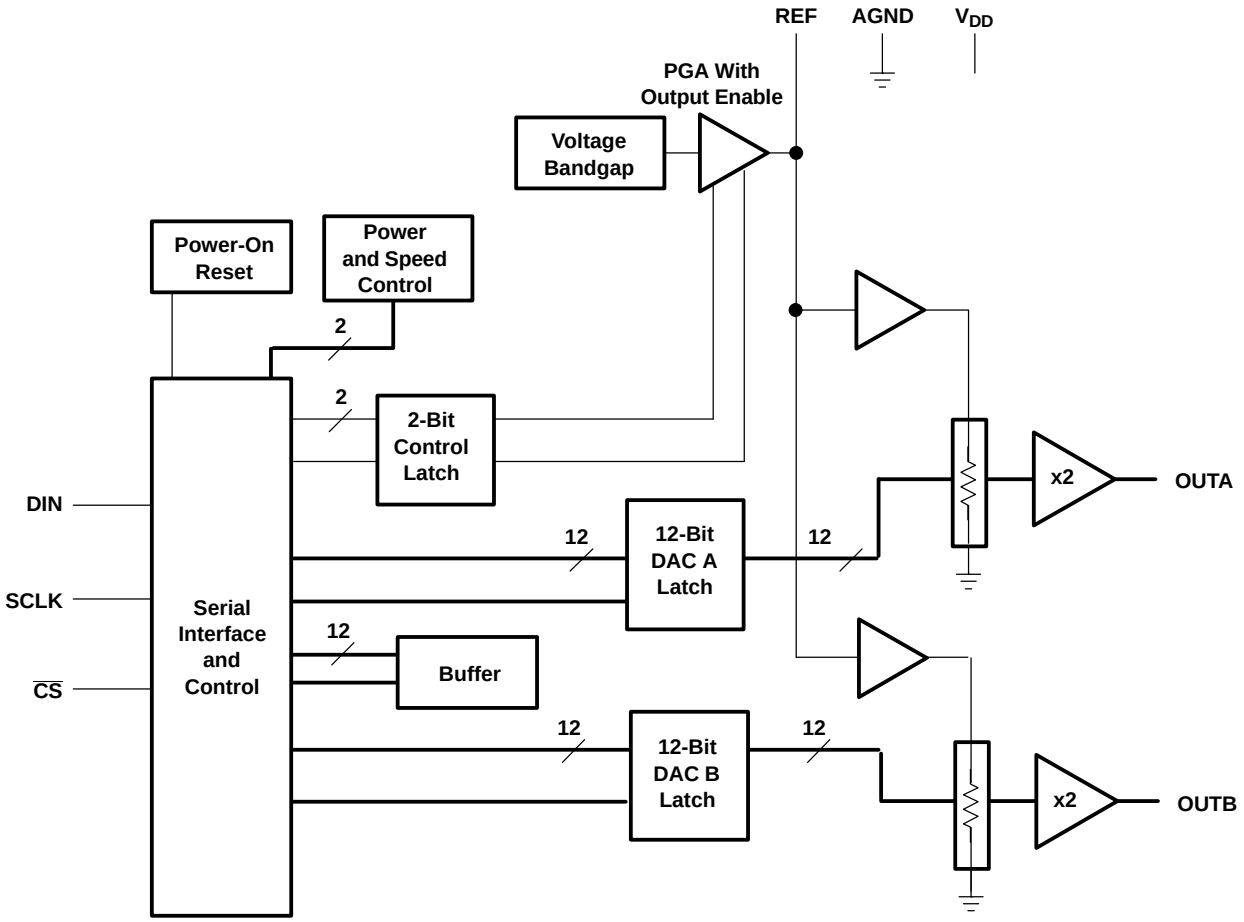
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

T_A	PACKAGE		
	SOIC (D)	CERAMIC DIP (JG)	20 PAD LCCC (FK)
0°C to 70°C	TLV5638CD	—	—
40°C to 85°C	TLV5638ID	—	—
40°C to 125°C	TLV5638QD TLV5638QDR	—	—
55°C to 125°C	—	TLV5638MJG	TLV5638MFK

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{CS}$	3	I	Chip select. Digital input active low, used to enable/disable inputs
DIN	1	I	Digital serial data input
OUT A	4	O	DAC A analog voltage output
OUT B	7	O	DAC B analog voltage output
REF	6	I/O	Analog reference voltage input/output
SCLK	2	I	Digital serial clock input
V_{DD}	8	P	Positive power supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage (V_{DD} to AGND)		7 V
Reference input voltage range		-0.3 V to V_{DD} + 0.3 V
Digital input voltage range		-0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A	TLV5638C	0°C to 70°C
	TLV5638I	-40°C to 85°C
	TLV5638Q	-40°C to 125°C
	TLV5638M	-55°C to 125°C
Storage temperature range, T_{stg}		-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listedunder„ absolute maximum ratings" may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the deviceat these or any other conditions beyond those indicated under„recommended operating conditions" is not implied. Exposure toabsolute-maximum-rated conditions for extended periods may affect devicereliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	635 mW	5.08 mW/°C	407 mW	330 mW	127 mW
FK	1375 mW	11.00 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.40 mW/°C	672 mW	546 mW	210 mW

(1) This is the inverse of thetraditional Junction-to-Ambient thermal Resistance ($R\theta_{JA}$). Thermal Resistances are not production testedand are for informational purposes only.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V		4.5	5	5.5	V
	V_{DD} = 3 V		2.7	3	3.3	V
Power on reset, POR			0.55(1)		2(1)	V
High-level digital input voltage, V_{IH}	V_{DD} = 2.7 V		2			V
	V_{DD} = 5.5 V		2.4			
Low-level digital input voltage, V_{IL}	V_{DD} = 2.7 V				0.6	V
	V_{DD} = 5.5 V	TLV5638C and TLV5638I			1	V
		TLV5638Q and TLV5638M			0.8	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (2)		AGND	2.048	V_{DD}-1.5	V
Reference voltage, V_{ref} to REF terminal	V_{DD} = 3 V (2)		AGND	1.024	V_{DD}-1.5	V
Load resistance, R_L			2			kΩ
Load capacitance, C_L					100	pF
Clock frequency, f_{CLK}					20	MHz
Operating free-air temperature, T_A	TLV5638C		0		70	°C
	TLV5638I		40		85	
	TLV5638Q		40		125	
	TLV5638M		55		125	

(1) This parameter is not testedfor Q and M suffix devices.
(2) Due to the x2 output buffer,a reference input voltage ≥ (V_{DD}-0.4 V)/2 causes clipping of the transfer function.The output buffer of the internal reference must be disabled, if an externalreference is used.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions, V_{ref} = 2.048 V, V_{ref}= 1.024 V (unless otherwise noted)

POWER SUPPLY							
PARAMETER		TEST CONDITIONS			TLV5638C, I TLV5638M		UNIT
					MIN	TYP	MAX	
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	V_{DD}= 5 V, Int. ref.	Fast		4.3	7	mA
				Slow		2.2	3.6	
			V_{DD} = 3 V, Int. ref.	Fast		3.8	6.3	mA
				Slow		1.8	3.0	
			V_{DD} = 5 V, Ext. ref.	Fast		3.9	6.3	mA
				Slow		1.8	3.0	
			V_{DD} = 3 V, Ext. ref.	Fast		3.5	5.7	mA
				Slow		1.5	2.6	
	Power-down supply current					0.01	10	µA
PSRR	Power supply rejection ratio	Zero scale, (1)				65		dB
		Full scale, (2)				65		

(1) Power supply rejection ratioat zero scale is measured by varying $V_{DD}$and is given by: PSRR = 20 log [(E_{ZS}(V_{DD}max) -E_{ZS}(V_{DD}min))/V_{DD}max]
(2) Power supply rejection ratioat full scale is measured by varying $V_{DD}$and is given by: PSRR = 20 log [(E_G(V_{DD}max) -E_G(V_{DD}min))/V_{DD}max]

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating conditions, V_{ref} = 2.048 V, V_{ref}= 1.024 V (unless otherwise noted)

STATIC DAC SPECIFICATIONS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution			12			bits
INL	Integral nonlinearity, end point adjusted	See (1)	C and I suffixes		±1.7	±4	LSB
			Q and M suffixes		±1.7	±6	LSB
DNL	Differential nonlinearity	See (2)			±0.4	±1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See (3)				±24	mV
$E_{ZS}TC$	Zero-scale-error temperature coefficient	See (4)			10		ppm/°C
E_G	Gain error	See(5)				±0.6	% full scale V
E_GT_C	Gain error temperature coefficient	See (6)			10		ppm/°C
OUTPUT SPECIFICATIONS							
V_O	Output voltage	R_L= 10 kΩ		0		V_{DD}-0.4	V
	Output load regulation accuracy	V_O = 4.096 V, 2.048 V, R_L= 2 kΩ				±0.25	% full scale V
REFERENCE PIN CONFIGURED AS OUTPUT (REF)							
Vref(OUTL)	Low reference voltage			1.003	1.024	1.045	V
Vref(OUTH)	High reference voltage	V_{DD} > 4.75 V		2.027	2.048	2.069	V
Iref(source)	Output source current					1	mA
Iref(sink)	Output sink current			-1			mA
	Load capacitance					100	pF
PSRR	Power supply rejection ratio				-65		dB
REFERENCE PIN CONFIGURED AS INPUT (REF)							
V_I	Input voltage			0		V_{DD}-1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc	Fast		1.3		MHz
			Slow		525		kHz
	Reference feedthrough	REF = 1 V_{pp} at 1.024 V dc(7)			-80		dB
DIGITAL INPUTS							
I_{IH}	HIgh-level digital input current	$V_I = V_{DD}$				1	µA
I_{IL}	Low-level digital input current	V_I = 0 V		-1			µA
C_i	Input capacitance				8		pF

(1) The relative accuracy orintegral nonlinearity (INL) sometimes referred to as linearity error, is themaximum deviation of the output from the line between zero and full scaleexcluding the effects of zero code and full-scale errors. Tested from code 32to 4095.
(2) The differential nonlinearity(DNL) sometimes referred to as differential error, is the difference betweenthe measured and ideal 1 LSB amplitude change of any two adjacent codes.Monotonic means the output voltage changes in the same direction (or remainsconstant) as a change in the digital input code.
(3) Zero-scale error is thedeviation from zero voltage output when the digital input code iszero.
(4) Zero-scale-error temperaturecoefficient is given by: E_{ZS} TC =[E_{ZS} (T_{max}) - E_{ZS}(T_{min})]/V_{ref}× 10^6/(T_{max} -T_{min}).
(5) Gain error is the deviationfrom the ideal output (2V_{ref} - 1 LSB) withan output load of 10 kΩ excluding the effects of thezero-error.
(6) Gain temperature coefficientis given by: E_G TC = [E_G(T_{max}) -E_G (T_{min})]/V_{ref}×10^6/(T_{max} - T_{min}).
(7) Reference feedthrough ismeasured at the DAC output with an input code = 0x000.

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating conditions, V_{ref} = 2.048 V, V_{ref}= 1.024 V (unless otherwise noted)

ANALOG OUTPUT DYNAMIC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF, See (1)	Fast		1	3	µs
			Slow		3.5	7	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ, C_L = 100 pF, See (2)	Fast		0.5	1.5	µs
			Slow		1	2	
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See (3)	Fast		12		V/µs
			Slow		1.8		
	Glitch energy	DIN = 0 to 1, FCLK = 100 kHz, $\overline{CS}$ = V_{DD}			5		nV-s
SNR	Signal-to-noise ratio	f_s = 480 kSPS, f_{out} = 1 kHz, R_L = 10 kΩ, C_L = 100 pF		69	74		dB
S/(N+D)	Signal-to-noise + distortion			58	67		
THD	Total harmonic distortion				69	57	
	Spurious free dynamic range			57	72		

(1) Settling time is the timefor the output signal to remain within ±0.5 LSB of the final measured value fora digital input code change of 0x020 to 0xFDF and 0xFDF to 0x020 respectively.Not tested, assured by design.
(2) Settling time is the timefor the output signal to remain within ± 0.5 LSB of the final measured valuefor a digital input code change of one count. Not tested, assured bydesign.
(3) Slew rate determines thetime it takes for a change of the DAC output from 10% to 90% full-scalevoltage.

DIGITAL INPUT TIMING REQUIREMENTS

		MIN	NOM	MAX	UNIT
$t_{su(CS-CK)}$	Setup time, $\overline{CS}$ low before first negative SCLK edge	10			ns
$t_{su(C16-CS)}$	Setup time, 16th negative SCLK edge (when D0 is sampled) before $\overline{CS}$ rising edge	10			ns
t_{wH}	SCLK pulse width high	25			ns
t_{wL}	SCLK pulse width low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	10			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns

PARAMETER MEASURMENT INFORMATION

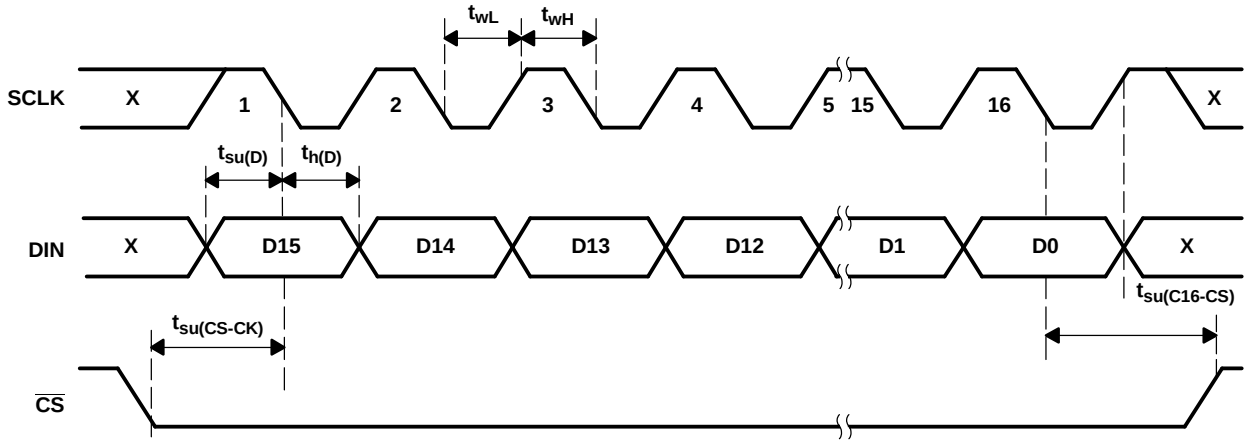


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

POWER DOWN SUPPLY CURRENT vs TIME

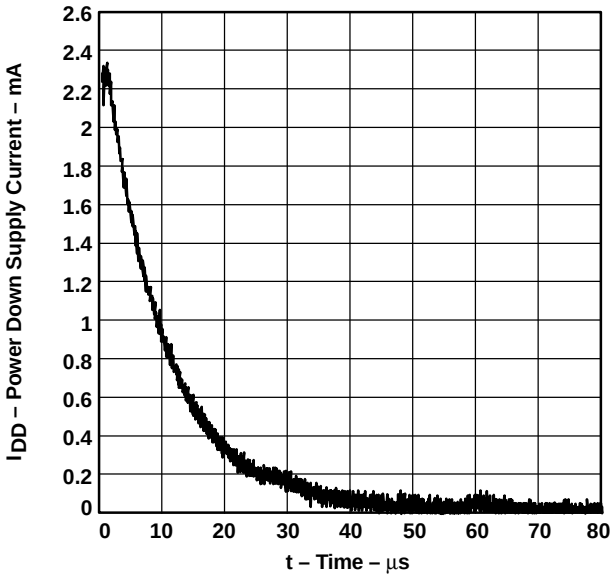


Figure 2.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

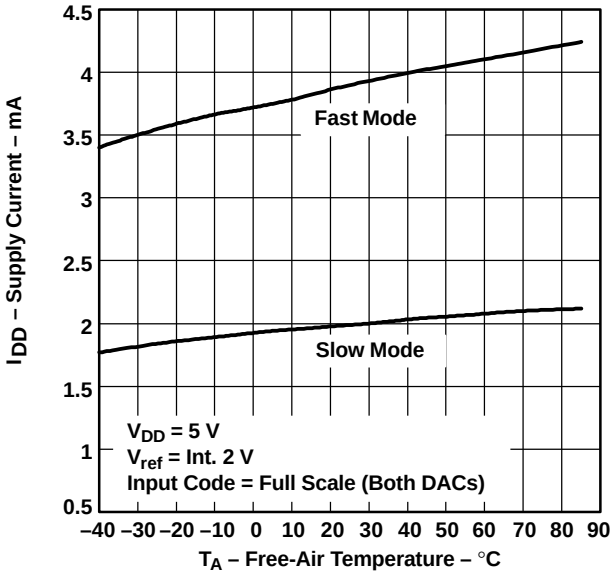


Figure 3.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

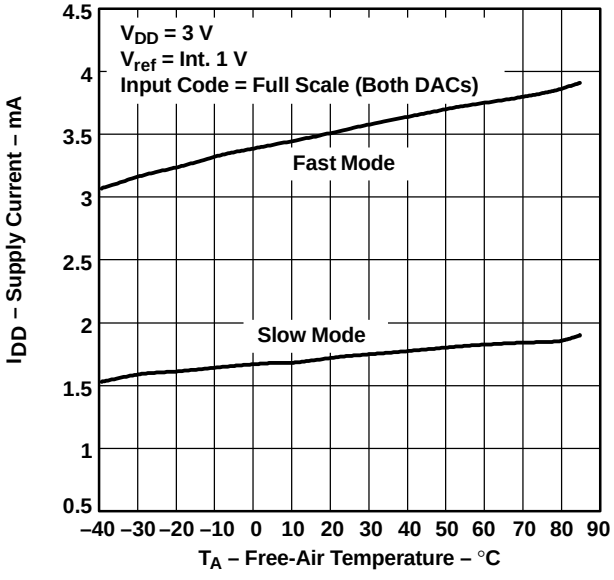


Figure 4.

OUTPUT VOLTAGE vs LOAD CURRENT

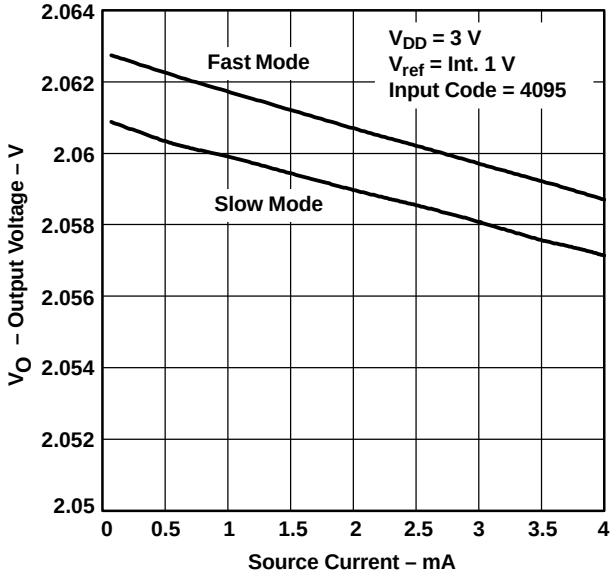


Figure 5.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE vs LOAD CURRENT

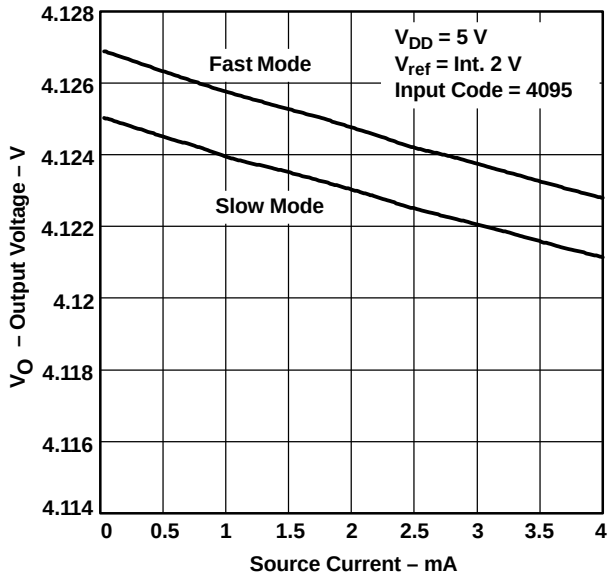


Figure 6.

OUTPUT VOLTAGE vs LOAD CURRENT

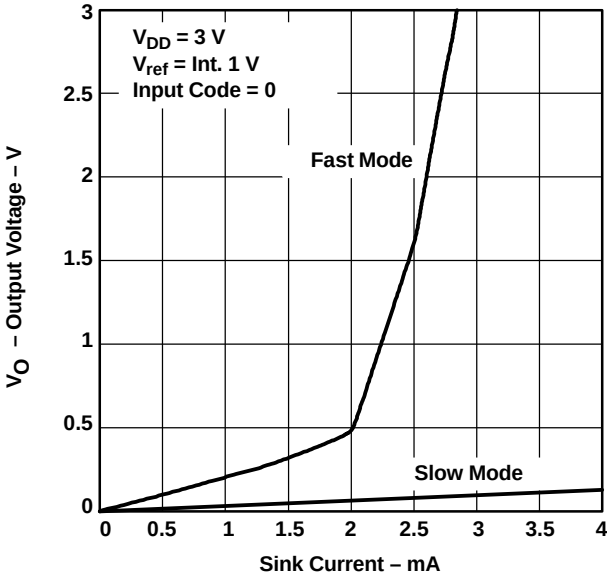


Figure 7.

OUTPUT VOLTAGE vs LOAD CURRENT

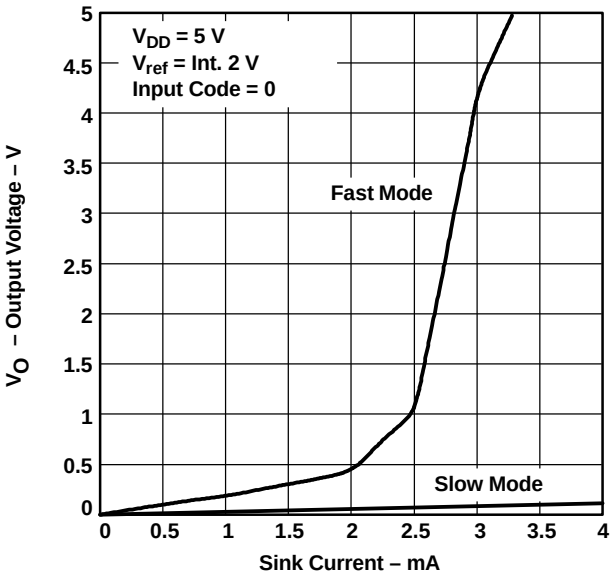


Figure 8.

TOTAL HARMONIC DISTORTION AND NOISE vs FREQUENCY

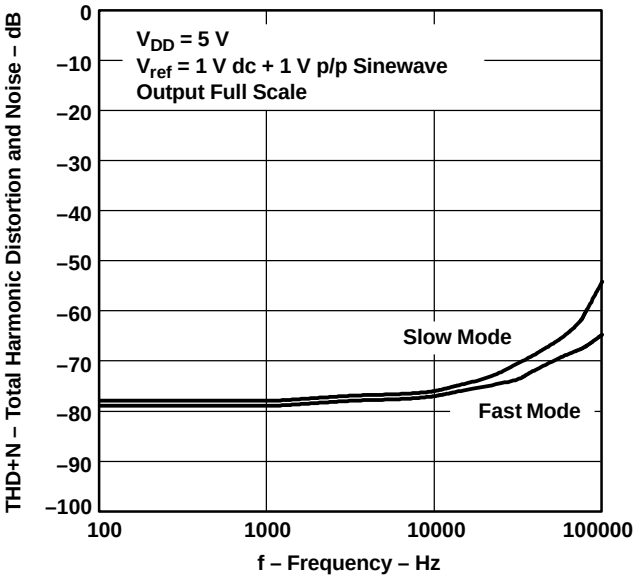


Figure 9.

TYPICAL CHARACTERISTICS (continued)

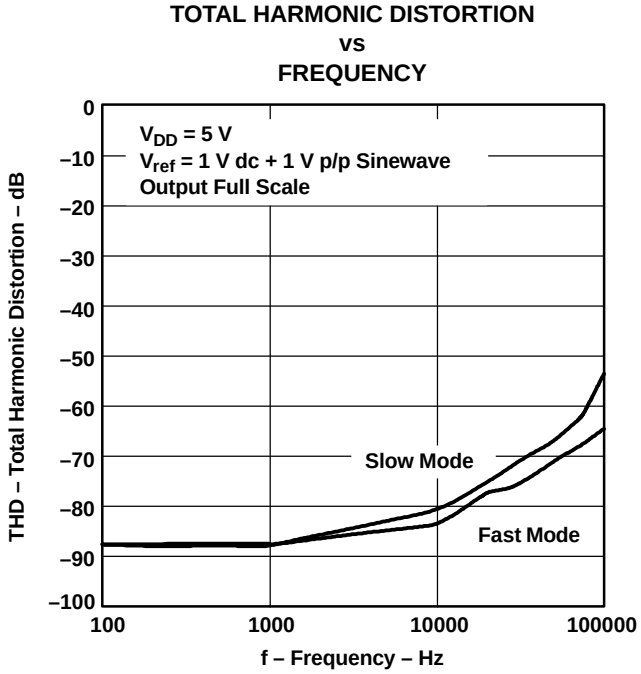


Figure 10.

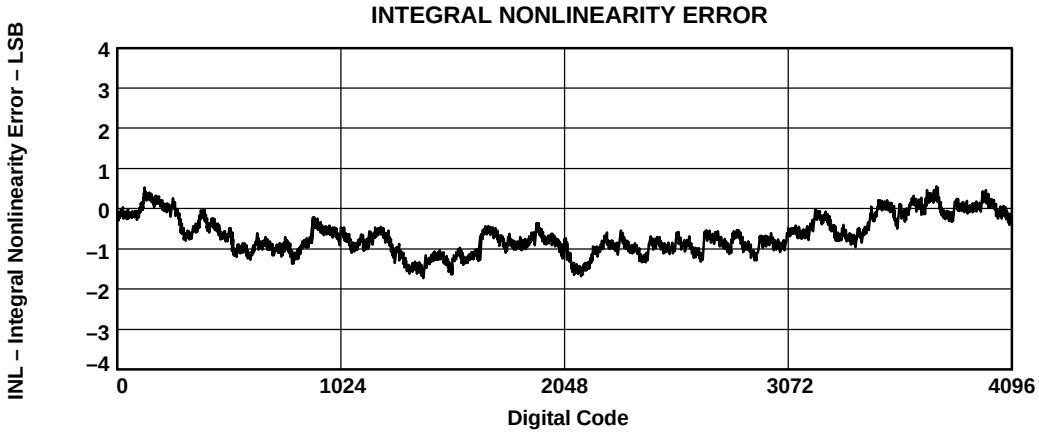


Figure 11.

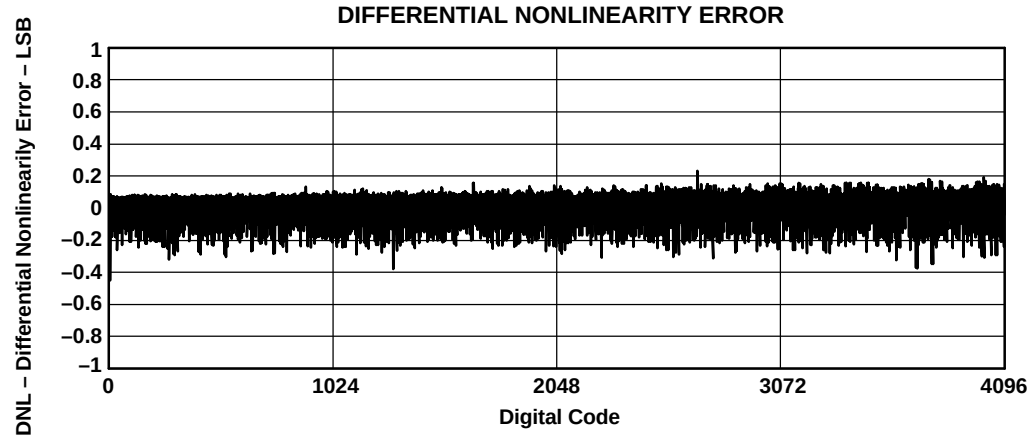


Figure 12.

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5638 is a dual 12-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{0\mathrm{x}1000}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

SERIAL INTERFACE

A falling edge of $\overline{CS}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{CS}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 13 shows examples of how to connect the TLV5638 to TMS320, SPI™, and Microwire™.

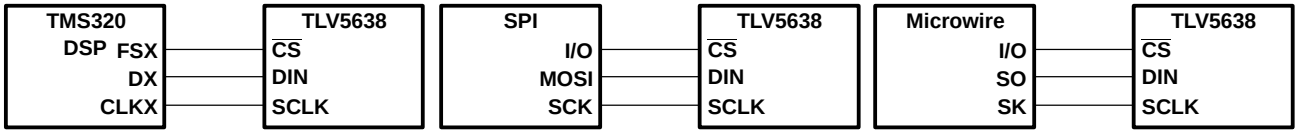


Figure 13. Three-Wire Interface

Notes on SPI™ and Microwire™: Before the controller starts the data transfer, the software has to generate a falling edge on the pin connected to FS. If the word width is 8 bits (SPI™ and Microwire™), two write operations must be performed to program the TLV5638. After the write operation(s), the holding registers or the control register are updated automatically on the 16th positive clock edge.

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 20\ \mathrm{MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.25\ \mathrm{MHz}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5638 has to be considered, too.

APPLICATION INFORMATION (continued)

DATA FORMAT

The 16-bit data word for the TLV5638 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	12 Data bits											

SPD: Speed control bit 1 → fast mode 0 → slow mode

PWR: Power control bit 1 → power down 0 → normal operation

The following table lists the possible combination of the register select bits:

REGISTERED SELECT BITS

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Write data to control register

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

DATA BITS: DAC A, DAC B and BUFFER

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
New DAC Value											

If control is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

DATA BITS: CONTROL

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	REF1	REF0

REF1 and REF0 determine the reference source and, if internal reference is selected, the reference voltage.

REFERENCE BITS

REF1	REF0	REFERENCE
0	0	External
0	1	1.024 V
1	0	2.048 V
1	1	External

CAUTION:

If external reference voltage is applied to the REF pin, external reference MUST be selected.

EXAMPLES OF OPERATION:

1. Set DAC A output, select fast mode, select internal reference at 2.048 V:
   a. Set reference voltage to 2.048 V (CONTROL register)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

   b. Write new DAC A value and update DAC A output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A output value											

   The DAC A output is updated on the rising clock edge after D0 is sampled.

   To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

2. Set DAC B output, select fast mode, select external reference:
   a. Select external reference (CONTROL register):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

   b. Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New BUFFER content and DAC B output value											

   The DAC A output is updated on the rising clock edge after D0 is sampled.

   To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

3. Set DAC A value, set DAC B value, update both simultaneously, select slow mode, select internal reference at 1.024 V:
   a. Set reference voltage to 1.024 V (CONTROL register)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

   b. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value											

   c. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value											

   Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

   To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

1. Set power-down mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X

#IMPLIED. X = Don't care

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

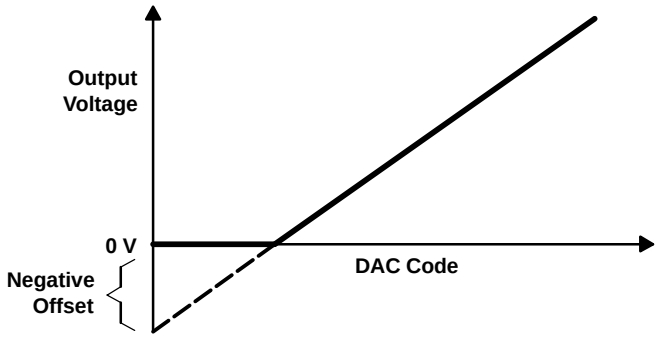


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY

Integral Nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

Differential Nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

Zero-Scale Error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

Gain Error (E_G)

Gain error is the error in slope of the DAC transfer function.

Total Harmonic Distortion (THD)

THD is the ratio of the rms value of the first six harmonic components to the value of the fundamental signal. The value for THD is expressed in decibels.

Signal-to-Noise Ratio + Distortion (S/N+D)

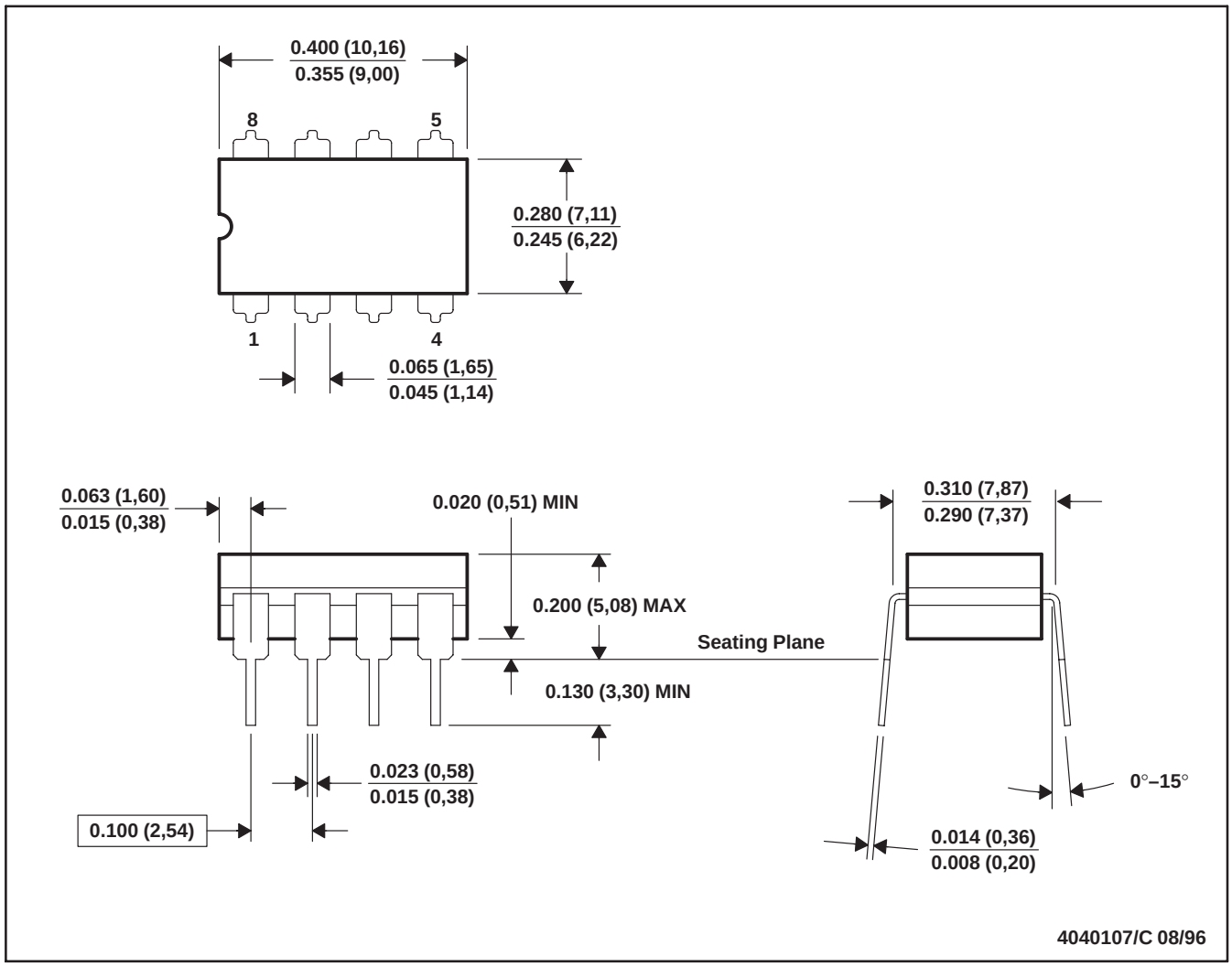
S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

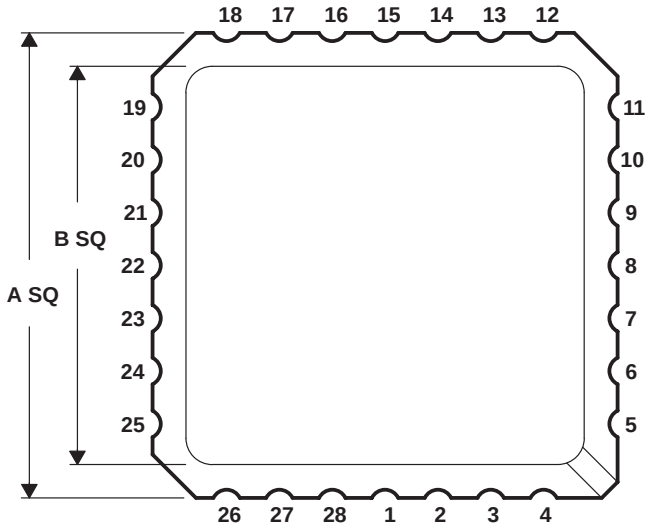
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



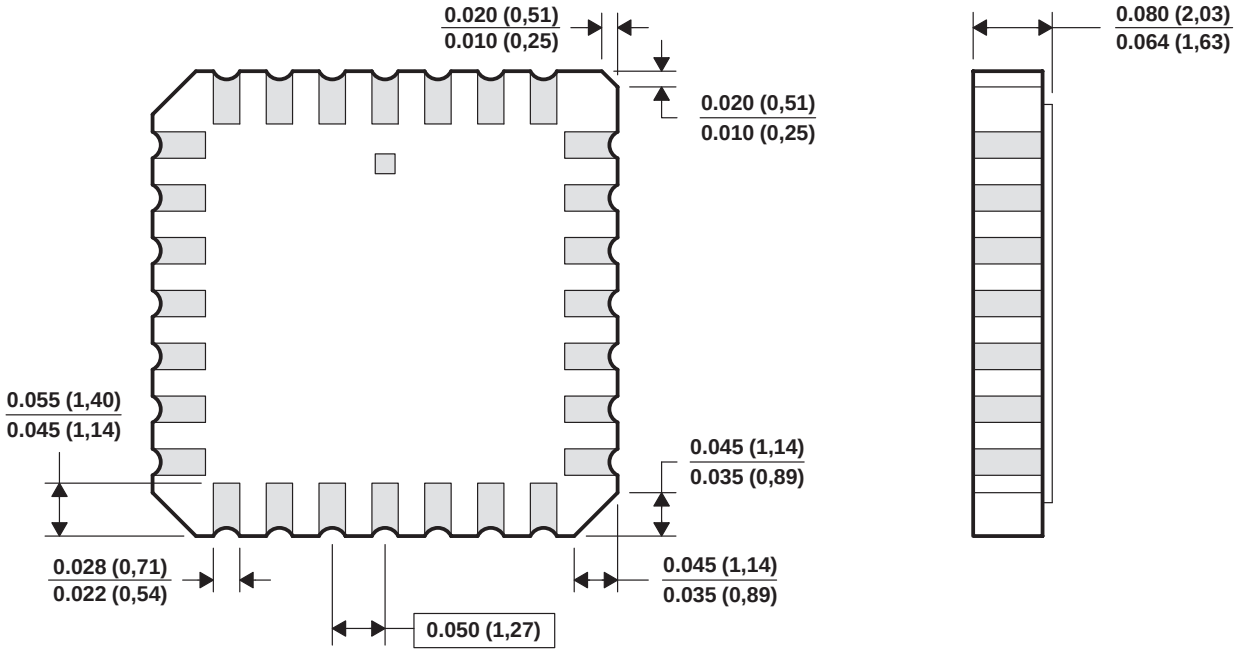
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



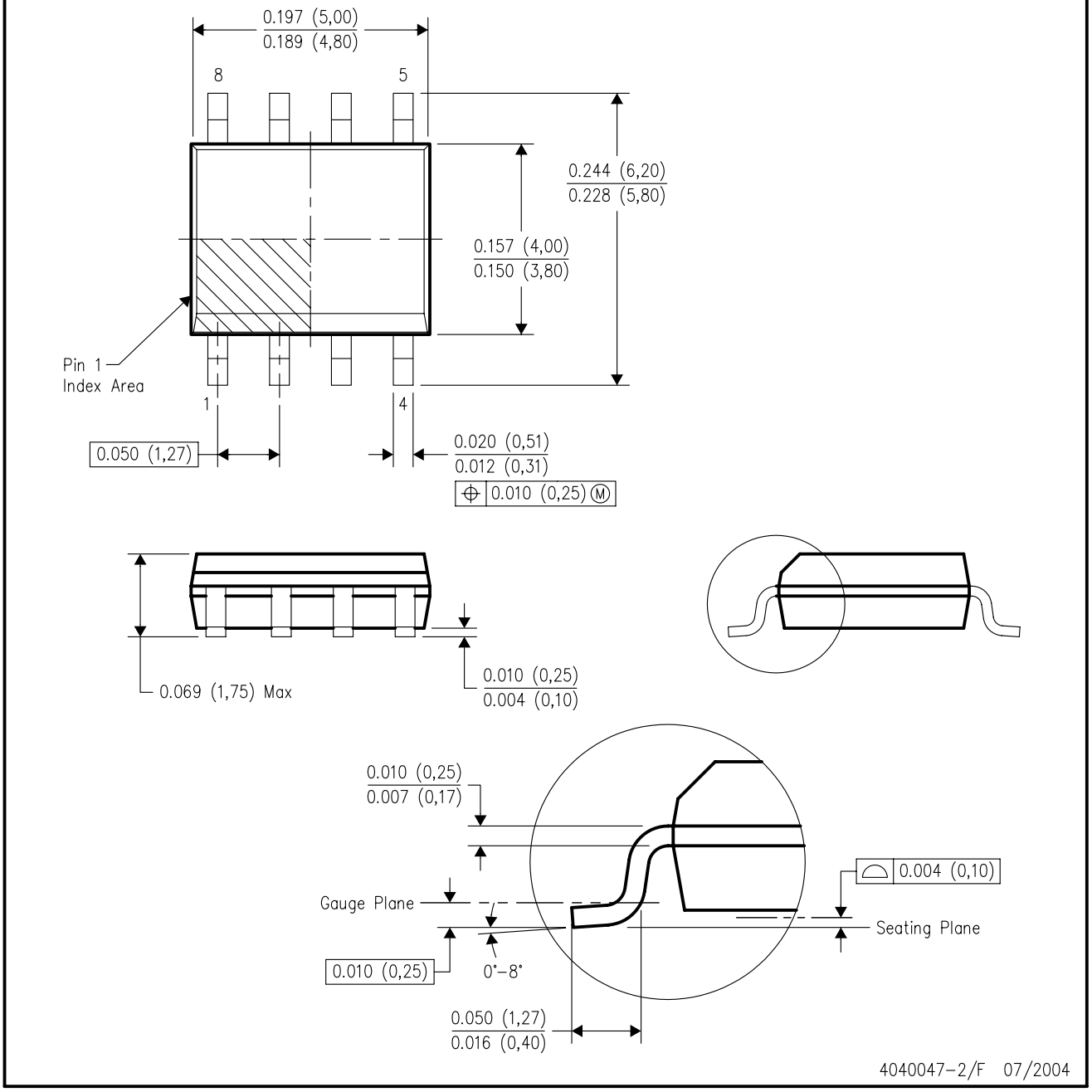
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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