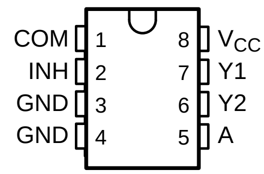
SINGLE-POLE DOUBLE-THROW (SPDT) ANALOG SWITCH OR 2:1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCES484A–AUGUST 2003–REVISED MARCH 2005

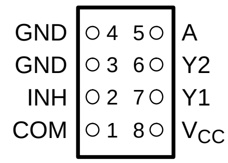
FEATURES

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Operates at 0.8 V to 2.7 V**
- **Sub-1-V Operable**
- **Low Power Consumption, 10 μA at 2.7 V**
- **High On-Off Output Voltage Ratio**
- **High Degree of Linearity**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE (TOP VIEW)



YEP OR YZP PACKAGE (BOTTOM VIEW)



DESCRIPTION/ORDERING INFORMATION

This analog switch is operational at 0.8-V to 2.7-V V_{CC}, but is designed specifically for 1.1-V to 2.7-V V_{CC} operation.

The SN74AUC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION

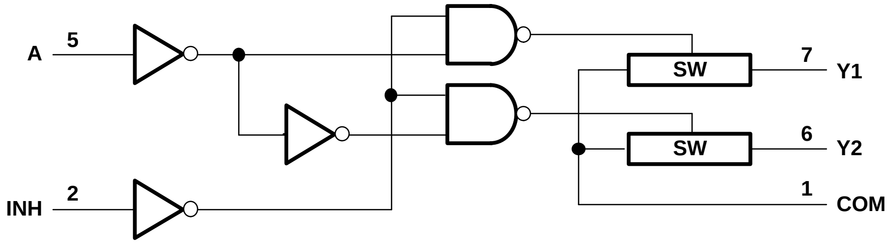
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AUC2G53YEPR	_ _ _U4_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUC2G53YZPR	
	SSOP – DCT	Tape and reel	SN74AUC2G53DCTR	U53_ _ _
	VSSOP – DCU	Tape and reel	SN74AUC2G53DCUR	U53_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, · = Pb-free).

FUNCTION TABLE

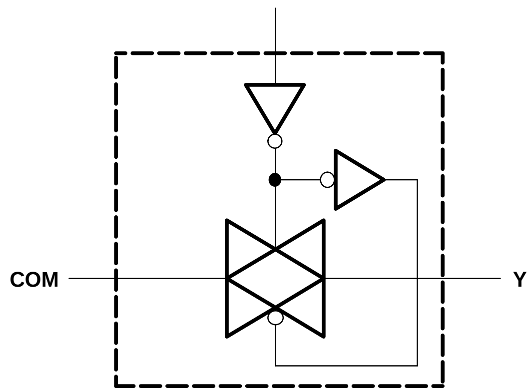
CONTROL INPUTS		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

LOGIC DIAGRAM (POSITIVE LOGIC)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

SIMPLIFIED SCHEMATIC, EACH SWITCH (SW)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		–0.5	3.6	V
V_I	Input voltage range(2)(3)		–0.5	3.6	V
$V_{I/O}$	Switch I/O voltage range(2)(3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	$V_I < 0$		–50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O} < 0$ or $V_{I/O} > V_{CC}$		±50	mA
I_T	On-state switch current current	$V_{I/O} = 0$ to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(4)	DCT package		220	°C/W
		DCU package		227	
		YEP/YZP package		102	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground unless otherwise specified.
(3) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_I	Control input voltage		0	3.6	V
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.6 V		20	ns/V
		V_{CC} = 1.65 V to 1.95 V		10	
		V_{CC} = 2.3 V to 2.7 V		3.5	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	On-state switch resistance		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V			40	Ω
					1.65 V		12.5	20	
				I_S = 8 mA	2.3 V		6	15	
$r_{on(p)}$	Peak on resistance		$V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V		131	180	Ω
					1.65 V		32	80	
				I_S = 8 mA	2.3 V		15	20	
Δr_{on}	Difference of on-state resistance between switches		$V_I = V_{CC}$ to GND, $V_C = V_{IH}$ (see Figure 1 and Figure 2)	I_S = 4 mA	1.1 V			4	Ω
					1.65 V			1	
				I_S = 8 mA	2.3 V			1	
$I_{S(off)}$	Off-state switch leakage current		$V_I = V_{CC}$ and V_O = GND, or V_I = GND and $V_O = V_{CC}$, $V_{INH} = V_{IH}$ (see Figure 3)		2.7 V			±1	µA
								±0.1(1)	
$I_{S(on)}$	On-state switch leakage current		$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$, V_O = Open (see Figure 4)		2.7 V			±1	µA
								±0.1(1)	
I_I	Control input current		$V_C = V_{CC}$ or GND		2.7 V			±5	µA
I_{CC}	Supply current		$V_C = V_{CC}$ or GND		2.7 V			10	µA
C_{ic}	Control input capacitance				2.5 V		2		pF
$C_{io(off)}$	Switch input/output capacitance	Y			2.5 V		3		pF
		COM					4.5		
$C_{io(on)}$	Switch input/output capacitance				2.5 V		9		pF

(1) T_A = 25°C

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd} (1)	COM or Y	Y or COM	0.3		0.3		0.3			0.2		0.1	ns
t_{en}	INH	COM or Y	9.2	0.5	3.5	0.5	2.2	0.5	1	1.9	0.5	1.8	ns
t_{dis}			8.1	0.5	4.2	0.5	3.2	0.5	1.9	3.4	0.5	2.6	
t_{en}	A	COM or Y	9.2	0.5	3.6	0.5	2.3	0.5	1.1	1.9	0.5	1.6	ns
t_{dis}			10	0.5	3.6	0.5	2.3	0.5	1.1	2	0.5	1.6	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd} (1)	COM or Y	Y or COM			0.4		0.2	ns
t_{en}	INH	COM or Y	0.5	1.6	3.1	0.5	2.2	ns
t_{dis}			0.5	2.2	3.4	0.5	2.2	
t_{en}	A	COM or Y	0.5	1.6	3	0.5	2.2	ns
t_{dis}			0.5	1.6	3	0.5	2.3	

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (1) (switch ON)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	90	MHz
				1.1 V	101	
				1.4 V	110	
				1.65 V	122	
				2.3 V	198	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see Figure 6)	0.8 V	>500	
				1.1 V	>500	
				1.4 V	>500	
				1.65 V	>500	
				2.3 V	>500	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.

Analog Switch Characteristics (continued)

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Crosstalk(2) (between switches)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–59	dB
				1.1 V	–59	
				1.4 V	–59	
				1.65 V	–59	
				2.3 V	–60	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see Figure 7)	0.8 V	–55	
				1.1 V	–55	
				1.4 V	–55	
				1.65 V	–55	
				2.3 V	–55	
Crosstalk (control input to signal output)	INH	COM or Y	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see Figure 8)	0.8 V	0.56	mV
				1.1 V	0.68	
				1.4 V	0.81	
				1.65 V	0.93	
				2.3 V	1.5	
Feed-through attenuation(2) (switch OFF)	COM or Y	Y or COM	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	–60	dB
				1.1 V	–60	
				1.4 V	–60	
				1.65 V	–60	
				2.3 V	–60	
			C_L = 5 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see Figure 9)	0.8 V	–59	
				1.1 V	–59	
				1.4 V	–59	
				1.65 V	–59	
				2.3 V	–59	
Sine-wave distortion	COM or Y	Y or COM	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see Figure 10)	0.8 V	6.19	%
				1.1 V	0.39	
				1.4 V	0.06	
				1.65 V	0.02	
				2.3 V	0.01	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see Figure 10)	0.8 V	3.55	
				1.1 V	0.38	
				1.4 V	0.04	
				1.65 V	0.02	
				2.3 V	0.02	

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

for INH input, T_A = 25°C

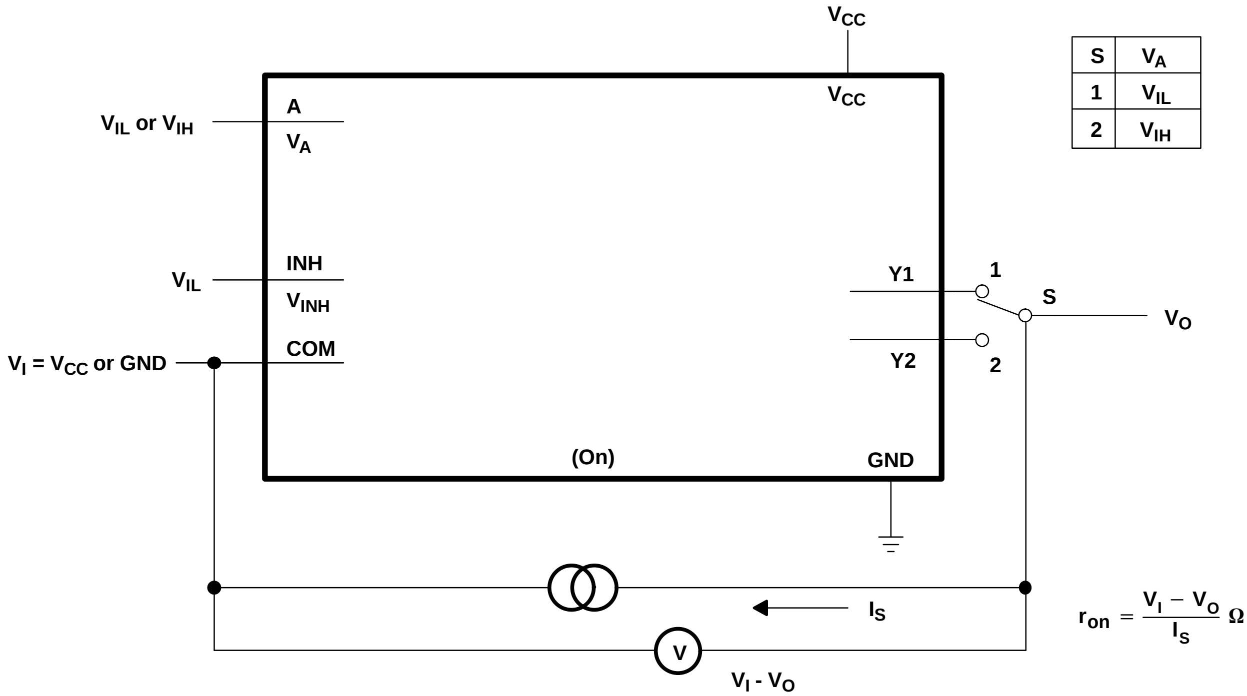
PARAMETER		TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	f = 10 MHz	3	3	3	3	3	pF

Operating Characteristics

for A input, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	5.5	5.5	5.5	5.5	5.5	pF
		Outputs disabled		0.5	0.5	0.5	0.5	0.5	

PARAMETER MEASUREMENT INFORMATION



S	V_A
1	V_{IL}
2	V_{IH}

Figure 1. On-State Resistance Test Circuit

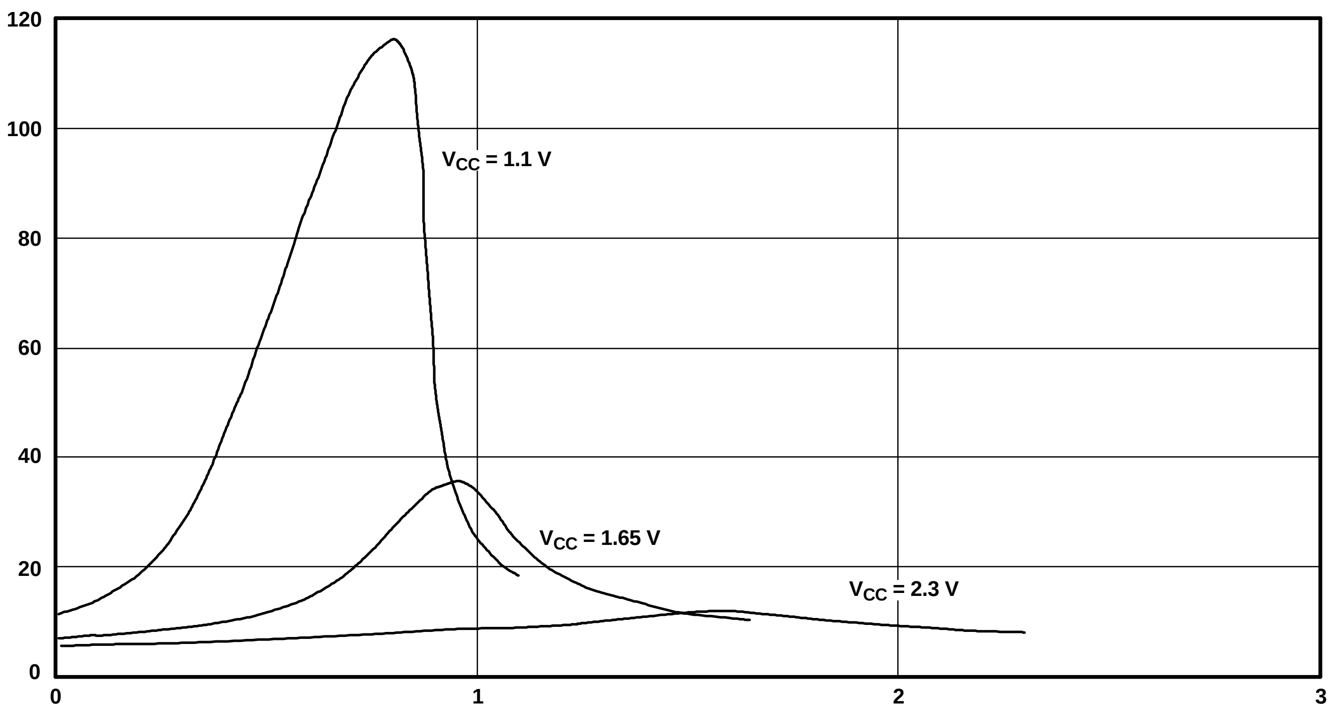
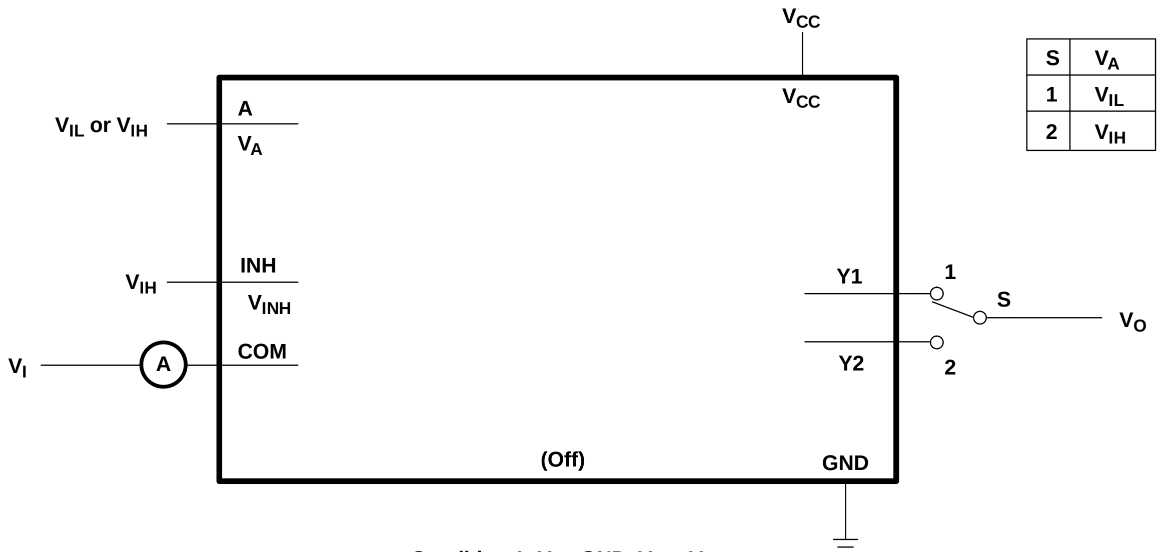


Figure 2. Typical r_{on} as a Function of Voltage (V_I) for V_I = 0 to V_{CC}

PARAMETER MEASUREMENT INFORMATION



Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

Figure 3. Off-State Switch Leakage-Current Test Circuit

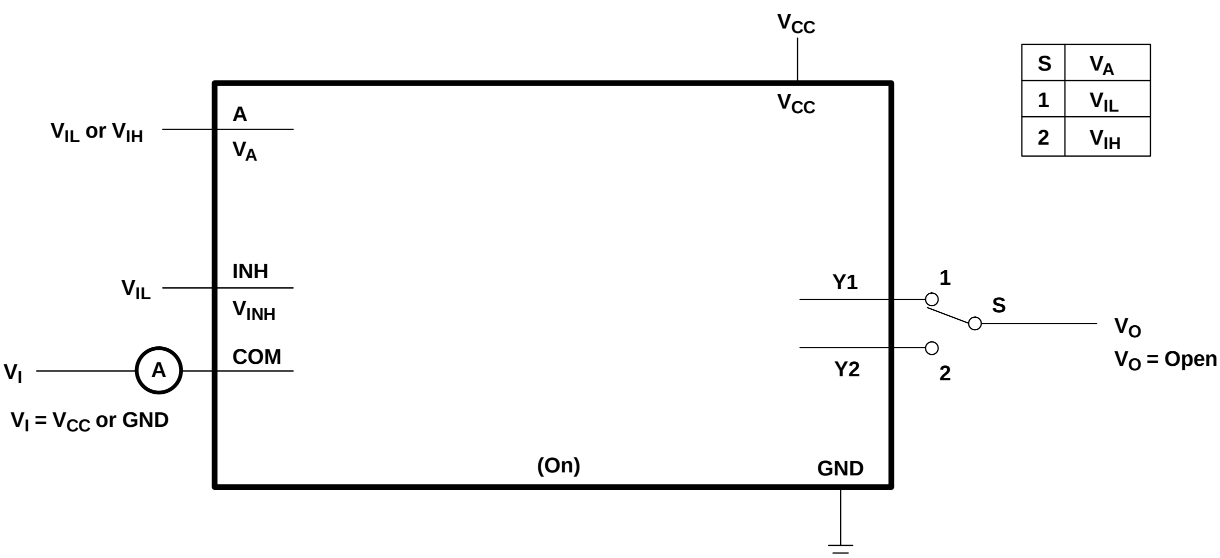
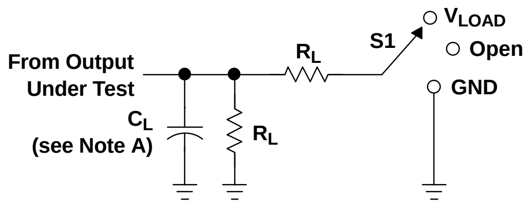


Figure 4. On-State Switch Leakage-Current Test Circuit

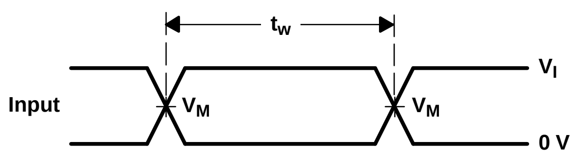
PARAMETER MEASUREMENT INFORMATION



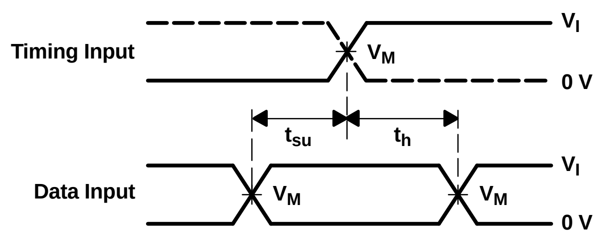
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

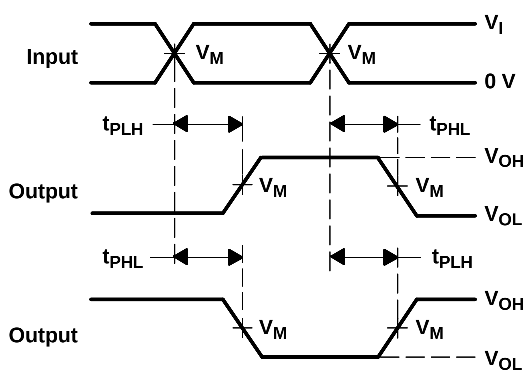
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
0.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V



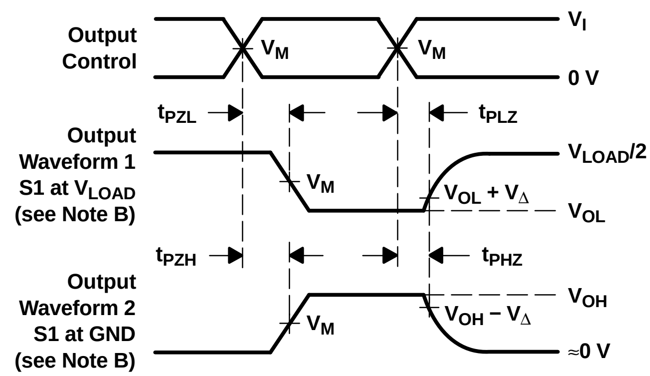
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

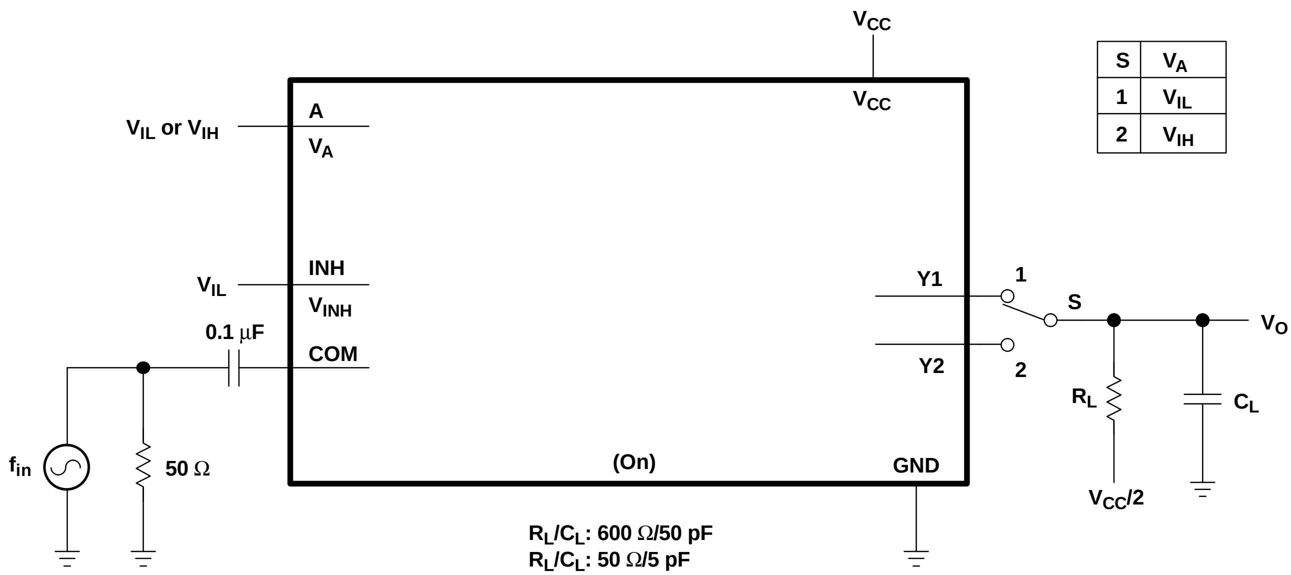


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

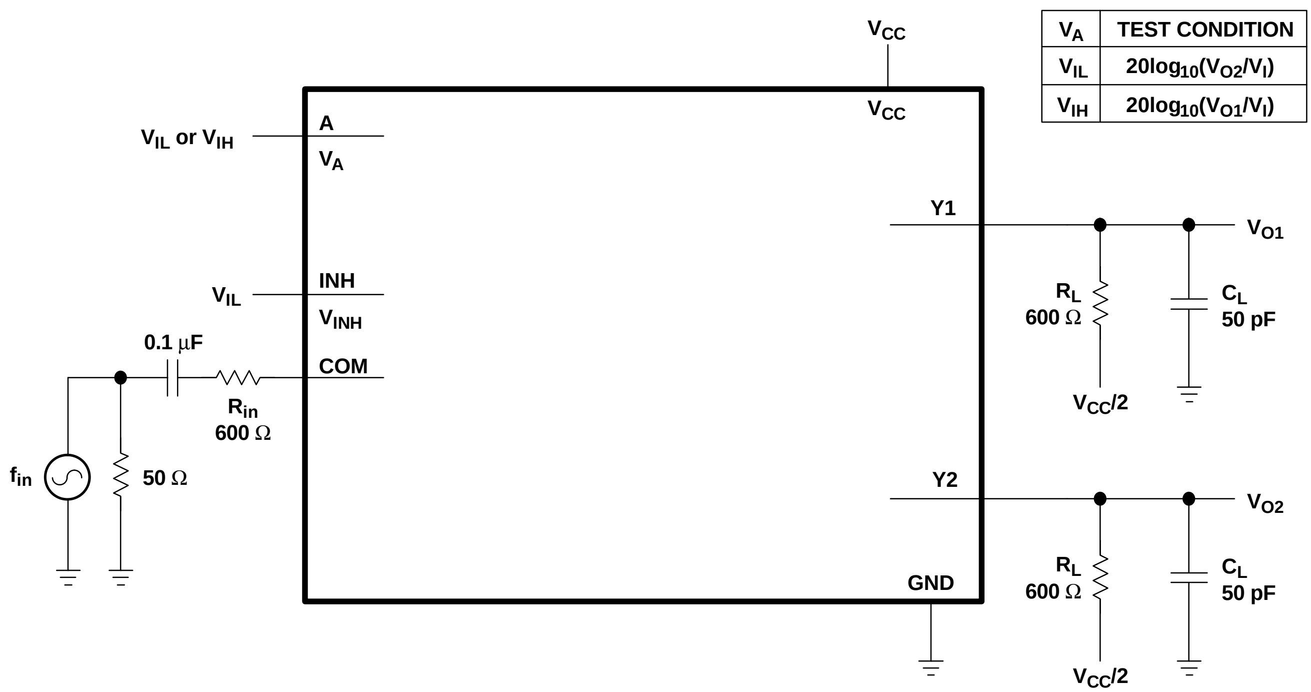
Figure 5. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



S	V_A
1	V_{IL}
2	V_{IH}

Figure 6. Frequency Response (Switch On)



V_A	TEST CONDITION
V_{IL}	$20\log_{10}(V_{O2}/V_I)$
V_{IH}	$20\log_{10}(V_{O1}/V_I)$

Figure 7. Crosstalk (Between Switches)

PARAMETER MEASUREMENT INFORMATION

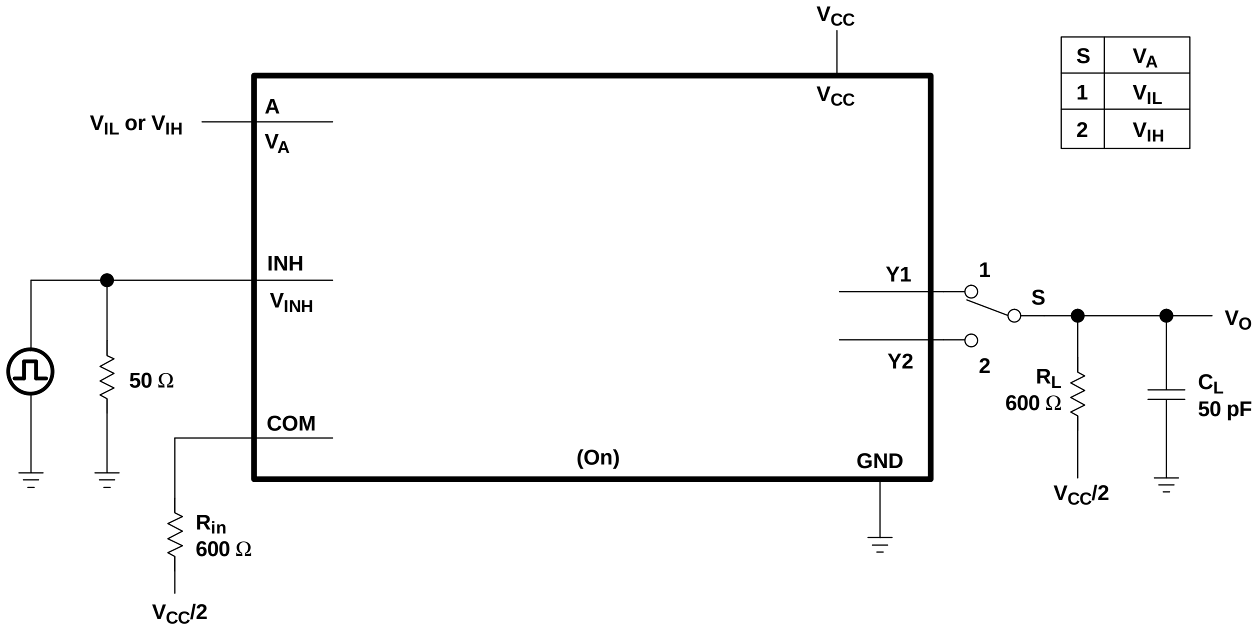


Figure 8. Crosstalk (Control Input, Switch Output)

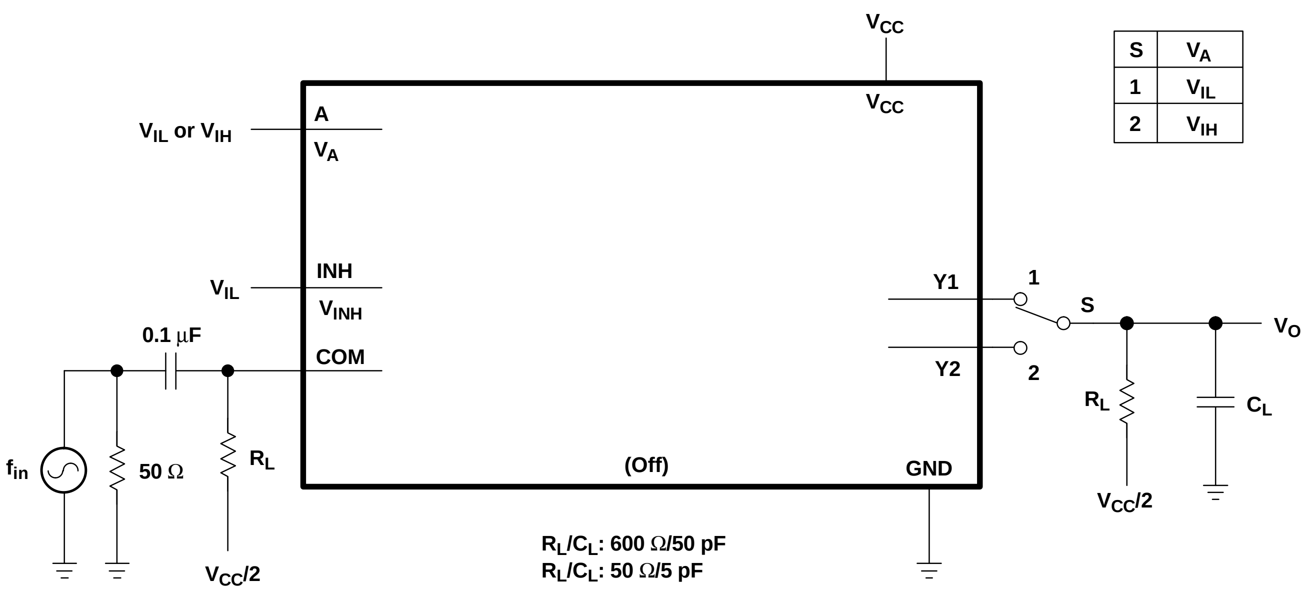
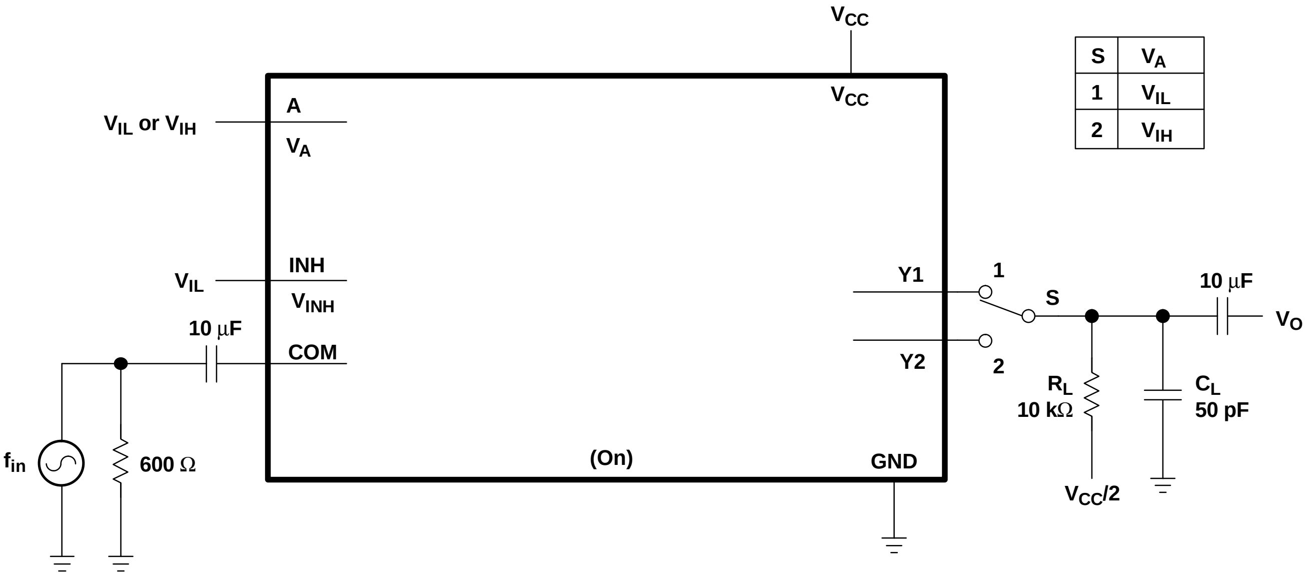


Figure 9. Feedthrough (Switch Off)

PARAMETER MEASUREMENT INFORMATION



V_{CC} = 0.8 V, V_I = 0.7 V_{P-P}
V_{CC} = 1.1 V, V_I = 1 V_{P-P}
V_{CC} = 1.4 V, V_I = 1.2 V_{P-P}
V_{CC} = 1.65 V, V_I = 1.4 V_{P-P}
V_{CC} = 2.3 V, V_I = 2 V_{P-P}

Figure 10. Sine-Wave Distortion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AUC2G53DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G53DCUR	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G53DCURE4	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUC2G53YEPR	ACTIVE	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74AUC2G53YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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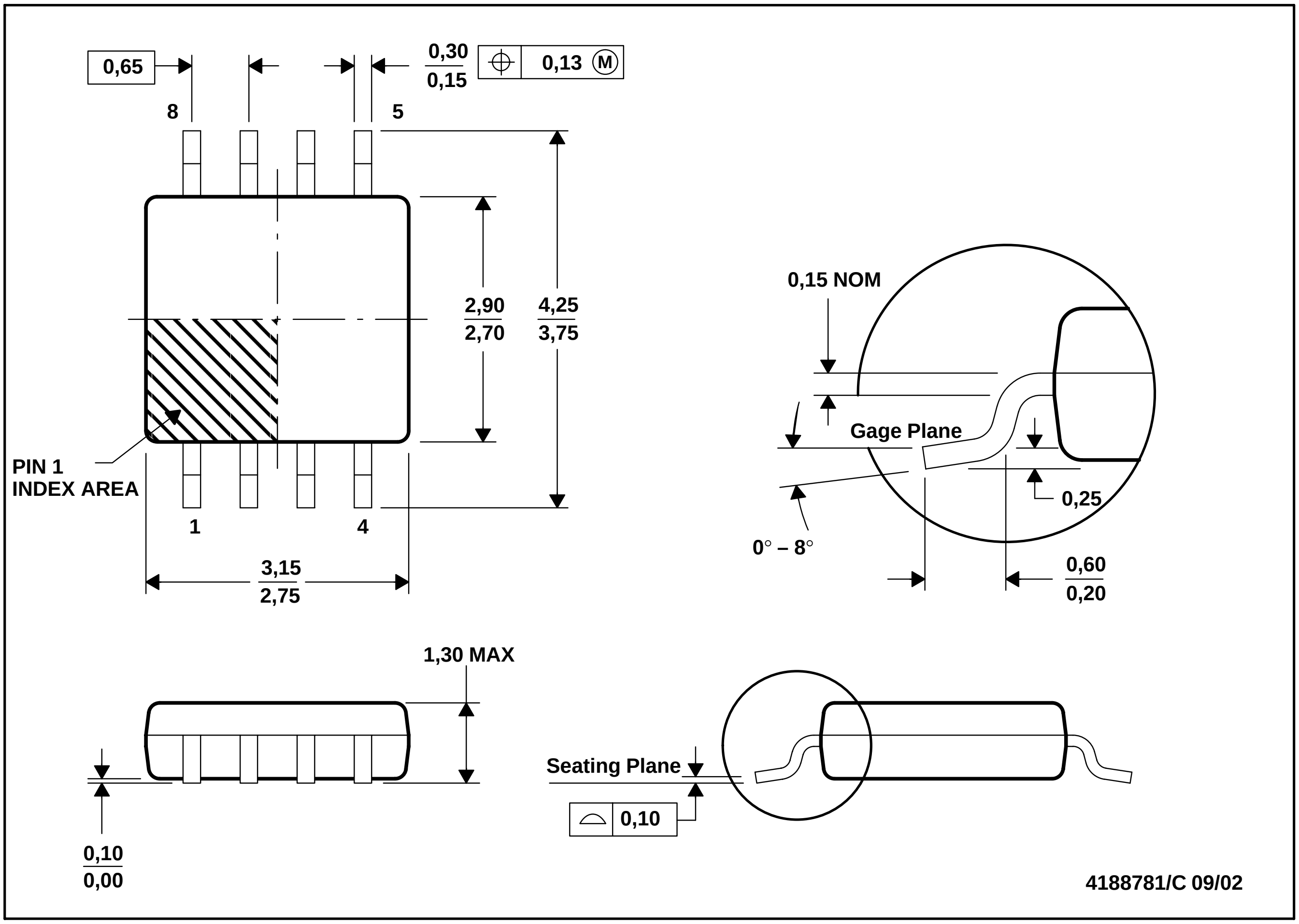
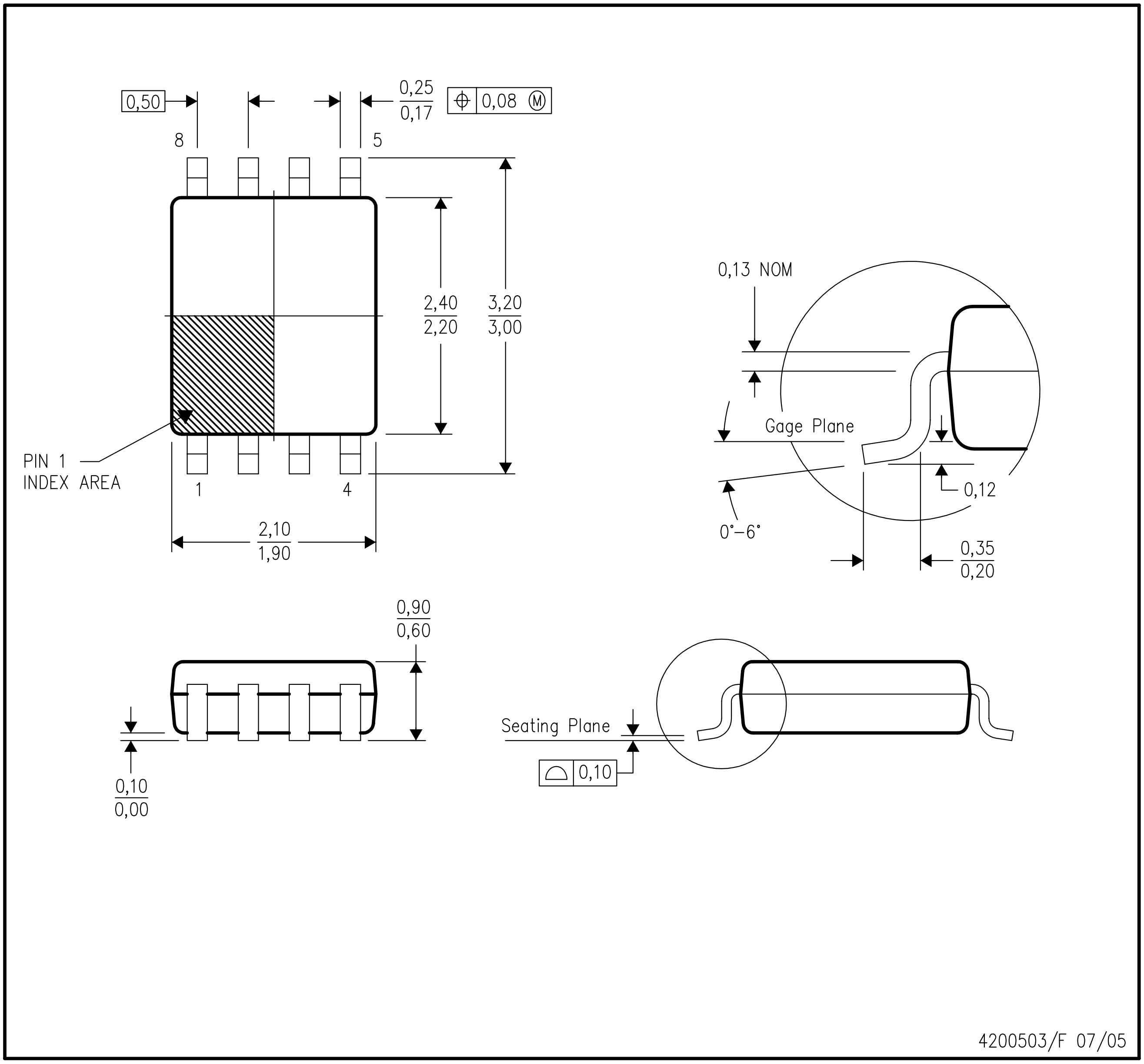
DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



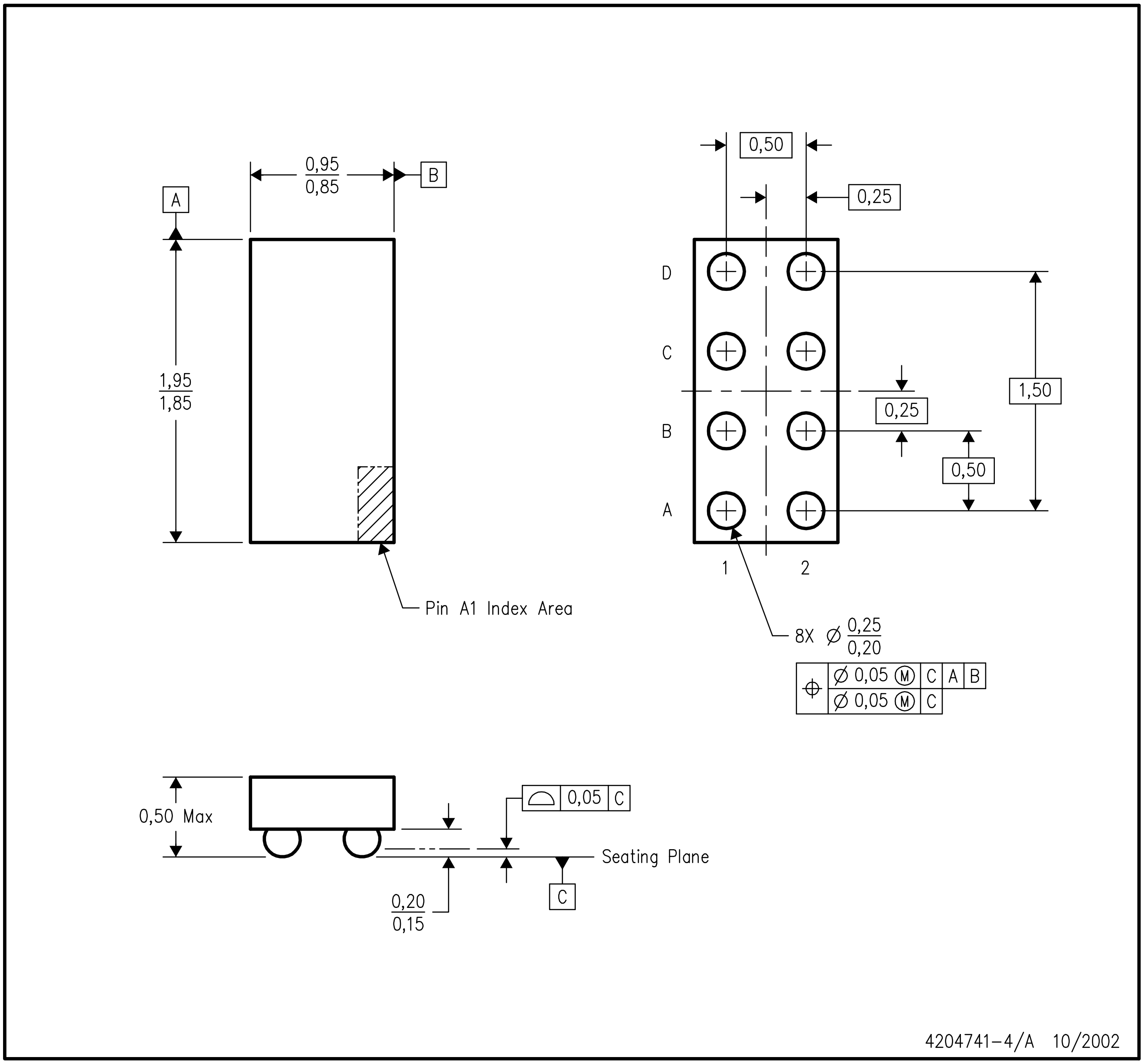
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-187 variation CA.

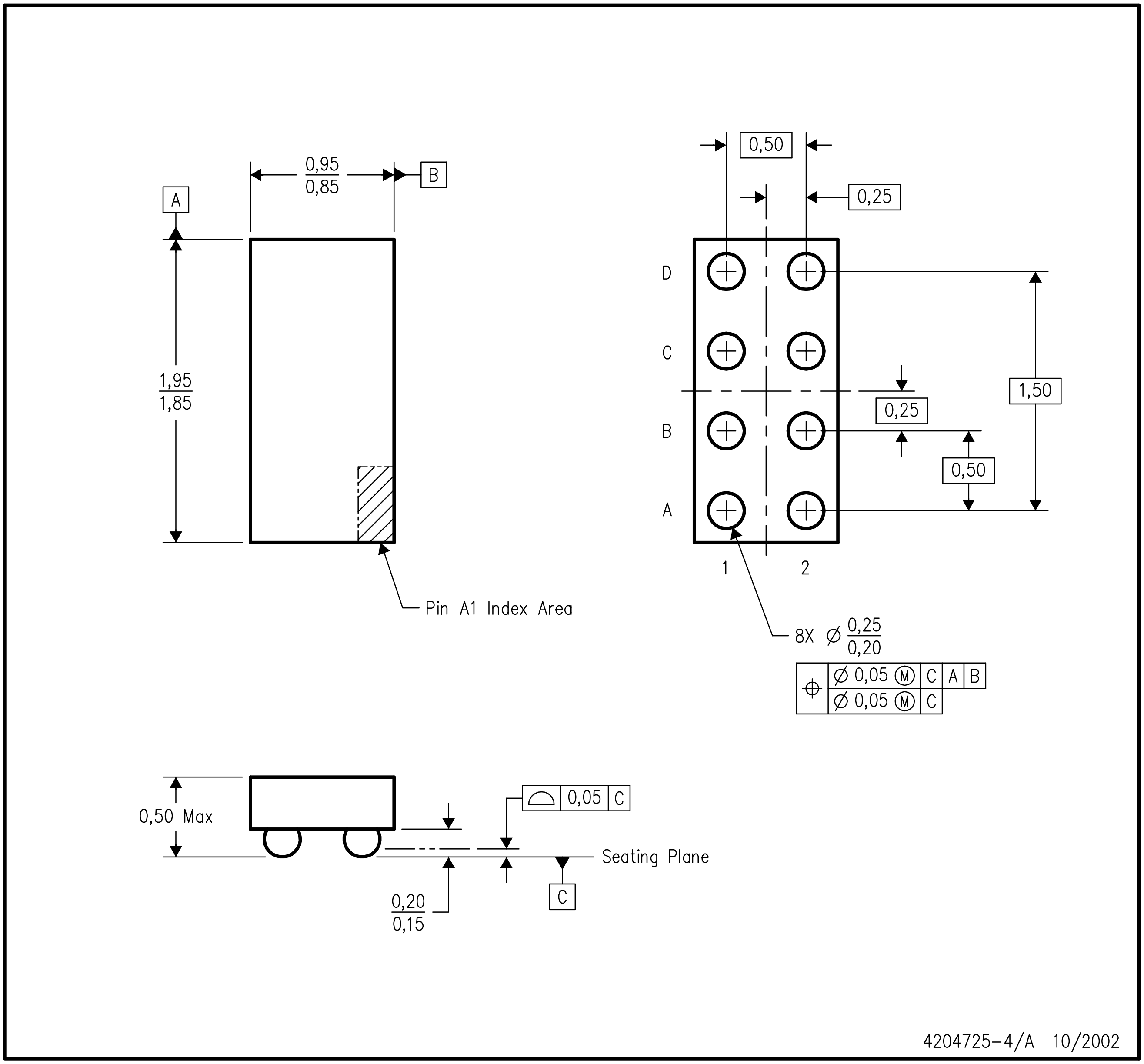
YZP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 8 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead–free.

NanoStar is a trademark of Texas Instruments.

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