

- **EPIC™ (Enhanced-Performance Implanted CMOS) Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)**  
 $<0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)**  
 $>2.3\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$
- **2-V to 5.5-V  $V_{CC}$  Operation**
- **Support Mixed-Mode Voltage Operation on All Ports**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds 200 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200\text{ pF}$ ,  $R = 0$ )**
- **Package Options Include Plastic Small-Outline (DW, NS), Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), and Thin Shrink Small-Outline (PW) Packages, Ceramic Flat (W) Package, Chip Carriers (FK), and DIPs (J)**

## description

The 'LV541A devices are octal buffers/drivers designed for 2-V to 5.5-V  $V_{CC}$  operation.

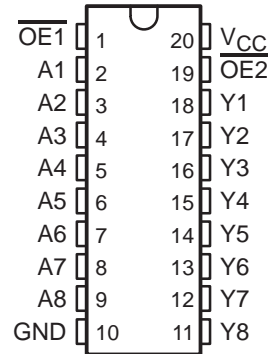
These devices are ideal for driving bus lines or buffer memory address registers. They feature inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

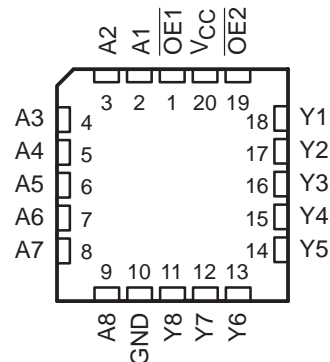
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LV541A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV541A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**SN54LV541A . . . J OR W PACKAGE**  
**SN74LV541A . . . DB, DGV, DW, NS, OR PW PACKAGE**  
**(TOP VIEW)**



**SN54LV541A . . . FK PACKAGE**  
**(TOP VIEW)**



**FUNCTION TABLE**  
**(each buffer/driver)**

INPUTS			OUTPUT Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



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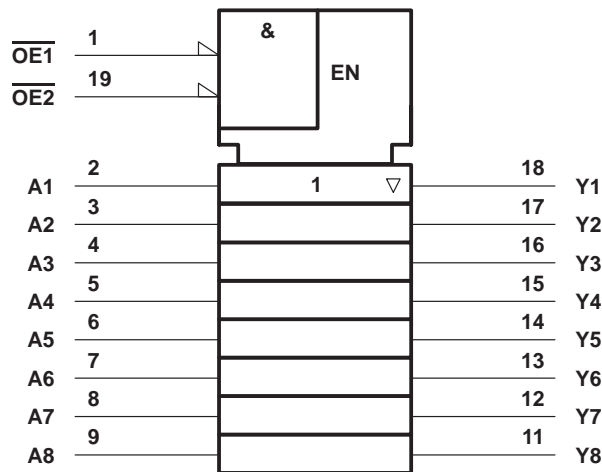
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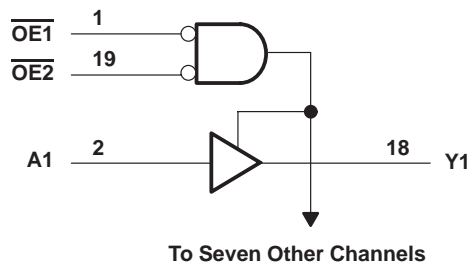
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Output voltage range applied in the high or low state, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±35 mA
Continuous current through $V_{CC}$ or GND	±70 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	70°C/W
DGV package	92°C/W
DW package	58°C/W
NS package	60°C/W
PW package	83°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. This value is limited to 5.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51.

**recommended operating conditions (see Note 4)**

			SN54LV541A		SN74LV541A		UNIT
			MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage		2	5.5	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		1.5		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		V <sub>CC</sub> × 0.7		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V		0.5		0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V		V <sub>CC</sub> × 0.3		V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage		0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
		3-state	0	5.5	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		–50		–50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		–2		–2	
		V <sub>CC</sub> = 3 V to 3.6 V		–8		–8	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		–16		–16	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50		50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V		2		2	
		V <sub>CC</sub> = 3 V to 3.6 V		8		8	mA
		V <sub>CC</sub> = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	0	200	0	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	0	100	0	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0	20	0	20	
T <sub>A</sub>	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV541A			SN74LV541A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 V to 5.5 V	V <sub>CC</sub> –0.1			V <sub>CC</sub> –0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			2			
	I <sub>OH</sub> = –8 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = –16 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 8 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 16 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V	±1			±1			μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±5			±5			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2			2			pF

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# SN54LV541A, SN74LV541A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCLS410D – APRIL 1998 – REVISED MAY 2000

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	6.7*	11.3*		1*	13.5*	1	13.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		8.5*	16.6*		1*	19.5*	1	19.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		8.4*	13.1*		1*	15*	1	15	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	8.7	15.9		1	18.5	1	18.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		10.5	20.7		1	24	1	24	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		12.3	17.9		1	20	1	20	
t <sub>sk(o)</sub>					2					2	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	4.8*	7*		1*	8.5*	1	8.5	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		6.1*	10.5*		1*	12.5*	1	12.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		5.8*	11*		1*	12*	1	12	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	6.1	10.5		1	12	1	12	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		7.4	14		1	16	1	16	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		8.8	15.4		1	17.5	1	17.5	
t <sub>sk(o)</sub>					1.5					1.5	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**switching characteristics over recommended operating free-air temperature range,  
V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN54LV541A		SN74LV541A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	3.5*	5*		1*	6*	1	6	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		4.3*	7.2*		1*	8.5*	1	8.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		3.9*	7.5*		1*	8*	1	8	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 50 pF	4.3	7		1	8	1	8	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y		5.3	9.2		1	10.5	1	10.5	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y		5.6	8.8		1	10	1	10	
t <sub>sk(o)</sub>					1					1	

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics,  $V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see Note 5)

PARAMETER		SN74LV541A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		–0.4	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 5: Characteristics are for surface-mount packages only.

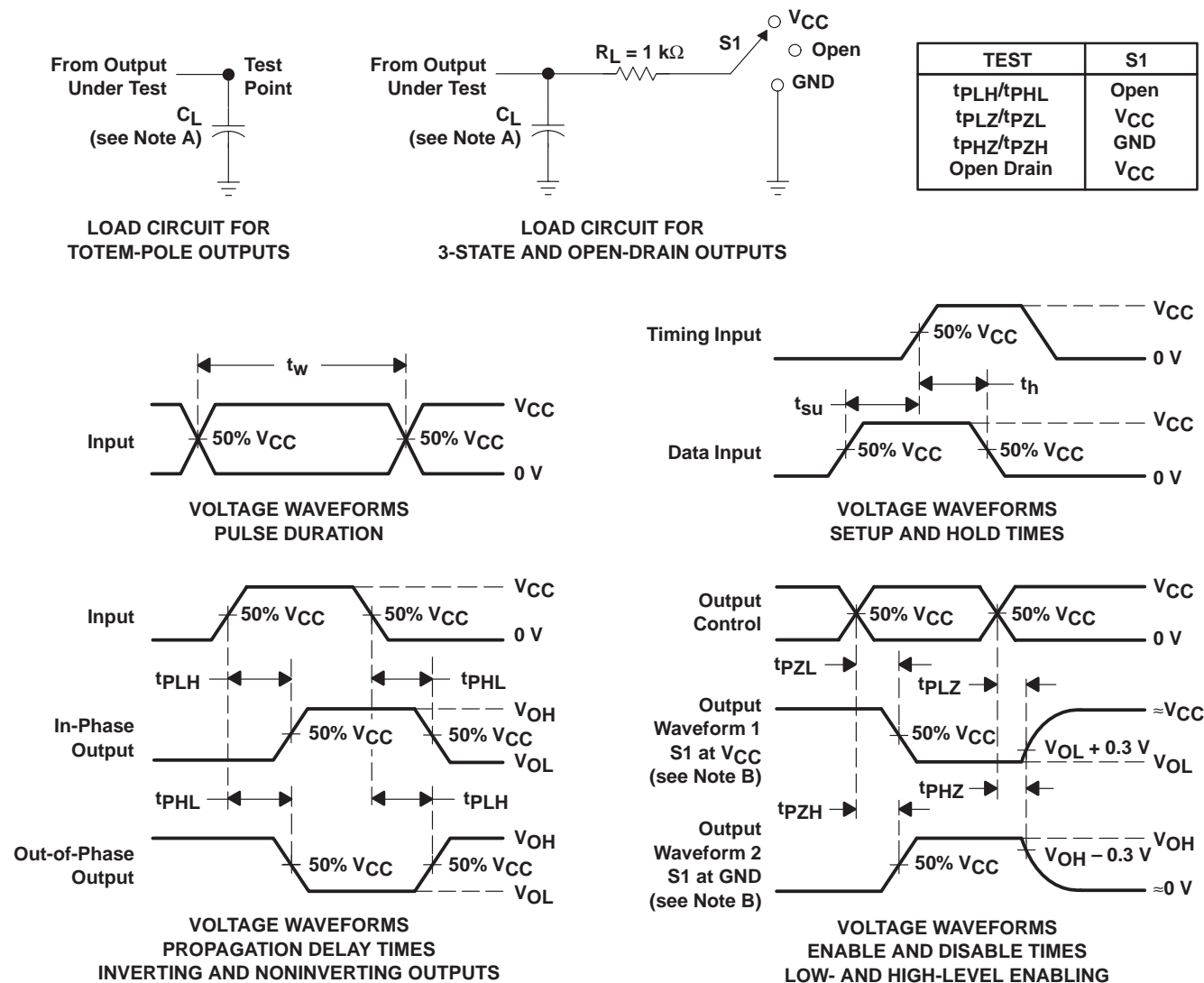
operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled $C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	16.3	pF
			5 V	17.8	

# SN54LV541A, SN74LV541A OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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