

SN54LV07A, SN74LV07A HEX BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

SCES337G – MAY 2000 – REVISED DECEMBER 2004

- 2-V to 5.5-V V_{CC} Operation
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Outputs Are Disabled During Power Up and Power Down With Inputs Tied to V_{CC}
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

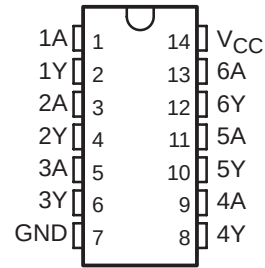
These hex buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The 'LV07A devices perform the Boolean function $Y = A$ in positive logic.

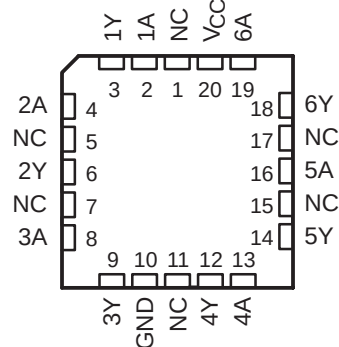
The open-drain outputs require pullup resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

SN54LV07A ... J OR W PACKAGE
SN74LV07A ... D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV07A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tube of 50	SN74LV07AD	LV07A
		Reel of 2500	SN74LV07ADR	
	SOP – NS	Reel of 2000	SN74LV07ANSR	74LV07A
	SSOP – DB	Reel of 2000	SN74LV07ADBR	LV07A
	TSSOP – PW	Tube of 90	SN74LV07APW	LV07A
		Reel of 2000	SN74LV07APWR	
		Reel of 250	SN74LV07APWT	
–55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LV07ADGVR	LV07A
	CDIP – J	Tube of 25	SNJ54LV07AJ	SNJ54LV07AJ
	CFP – W	Tube of 150	SNJ54LV07AW	SNJ54LV07AW
	LCCC – FK	Tube of 55	SNJ54LV07AFK	SNJ54LV07AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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FUNCTION TABLE
(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

logic diagram, each buffer/driver (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	–35 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2):	
D package	86°C/W
DB package	96°C/W
DGV package	127°C/W
NS package	76°C/W
PW package	113°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

			SN54LV07A		SN74LV07A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	5.5	0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 2 V		50		50	μA
		V _{CC} = 2.3 V to 2.7 V		2		2	
		V _{CC} = 3 V to 3.6 V		8		8	
		V _{CC} = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V _{CC} = 3 V to 3.6 V		100		100	
		V _{CC} = 4.5 V to 5.5 V		20		20	
T _A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LV07A			SN74LV07A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V			0.1			0.1	V
	I _{OL} = 2 mA	2.3 V			0.4			0.4	
	I _{OL} = 8 mA	3 V			0.44			0.44	
	I _{OL} = 16 mA	4.5 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1			±1	μA
I _{OH}	V _I = V _{IH} , V _{OH} = V _{CC}	5.5 V			±2.5			±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20			20	μA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5			5	μA
C _i	V _I = V _{CC} or GND	3.3 V		1.6			1.6		pF

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV07A		SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	6.6*	10.4*		1*	13*	1	13	ns
t_{PHL}	A	Y		7.5*	10.4*		1*	13*	1	13	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	11.1	15.2		1	18	1	18	ns
t_{PHL}	A	Y		9.6	15.2		1	18	1	18	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV07A		SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5*	7.1*		1*	8.5*	1	8.5	ns
t_{PHL}	A	Y		5*	7.1*		1*	8.5*	1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	8.2	10.6		1	12	1	12	ns
t_{PHL}	A	Y		6.6	10.6		1	12	1	12	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV07A		SN74LV07A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8*	5.5*		1*	6.5*	1	6.5	ns
t_{PHL}	A	Y		3.4*	5.5*		1*	6.5*	1	6.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.7	7.5		1	8.5	1	8.5	ns
t_{PHL}	A	Y		4.5	7.5		1	8.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER		SN74LV07A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.4	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.1	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage		0.99		V

NOTE 4: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ\text{C}$

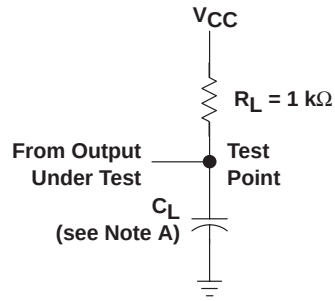
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$C_L = 50\text{ pF}$, $f = 10\text{ MHz}$	3.3 V	2.9	pF
			5 V	5.3	

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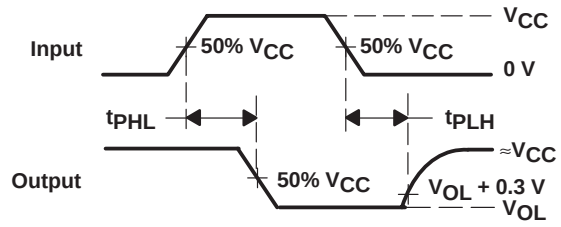


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PARAMETER MEASUREMENT INFORMATION



**LOAD CIRCUIT FOR
OPEN-DRAIN OUTPUTS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

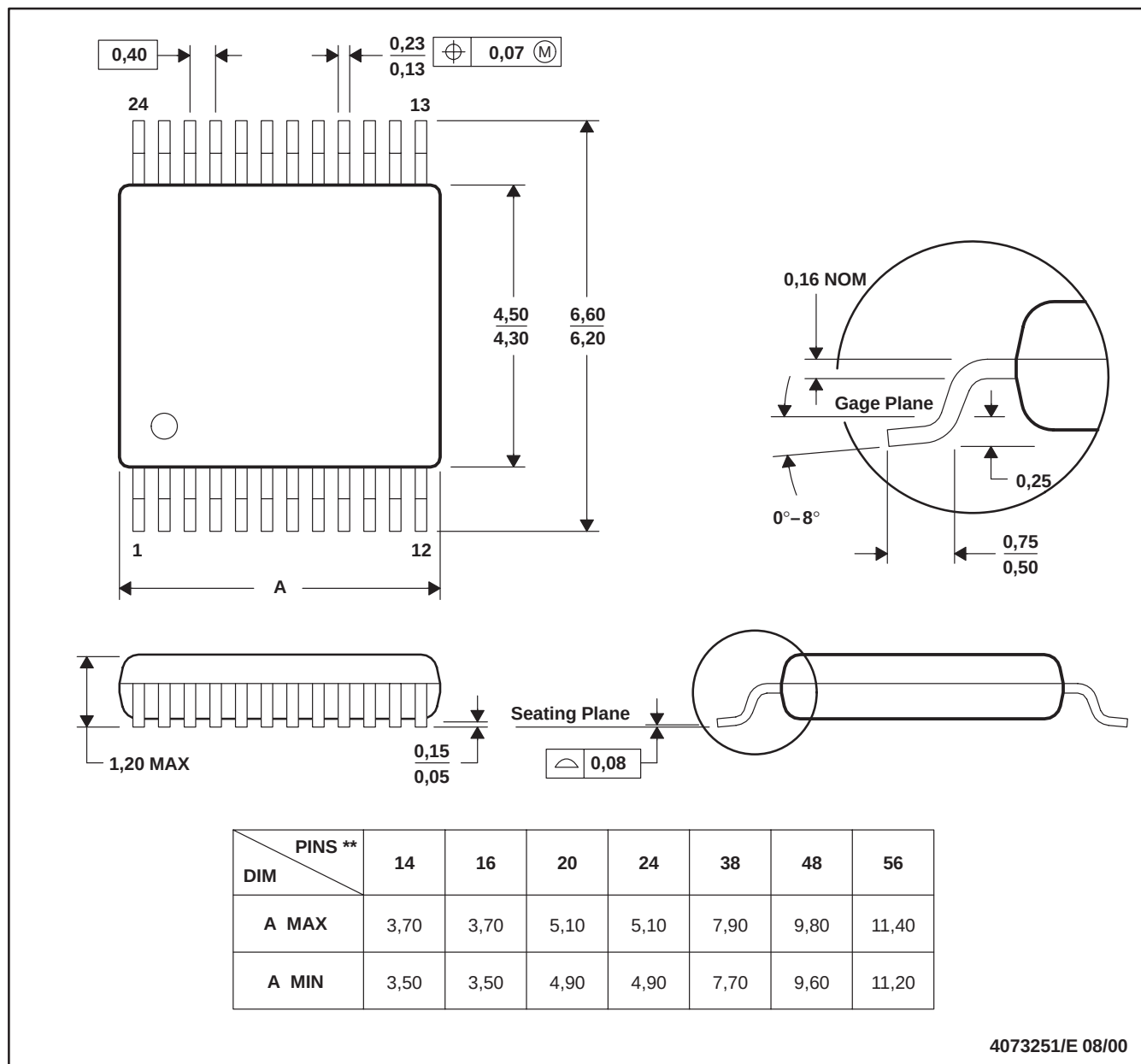
- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

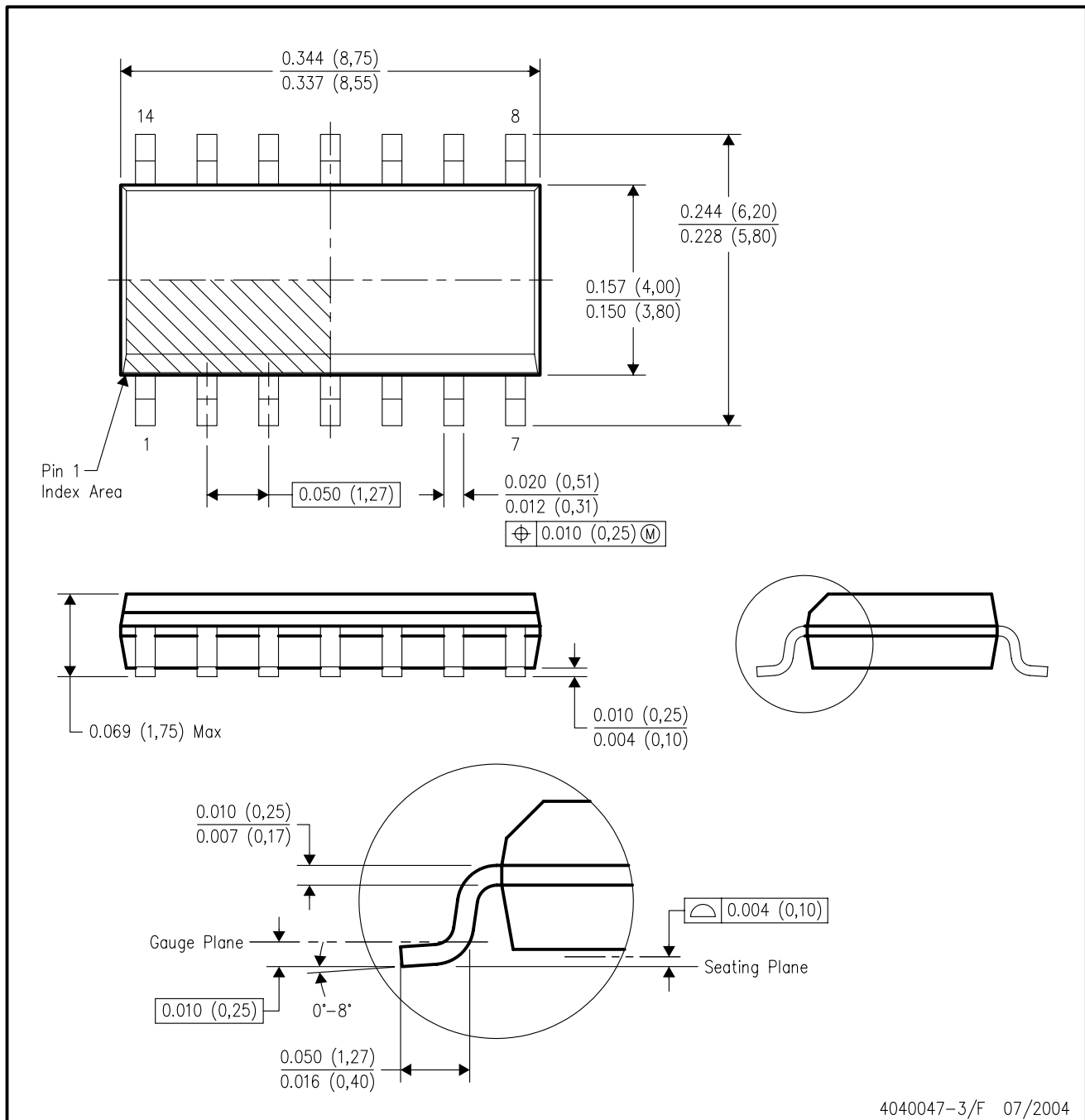
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



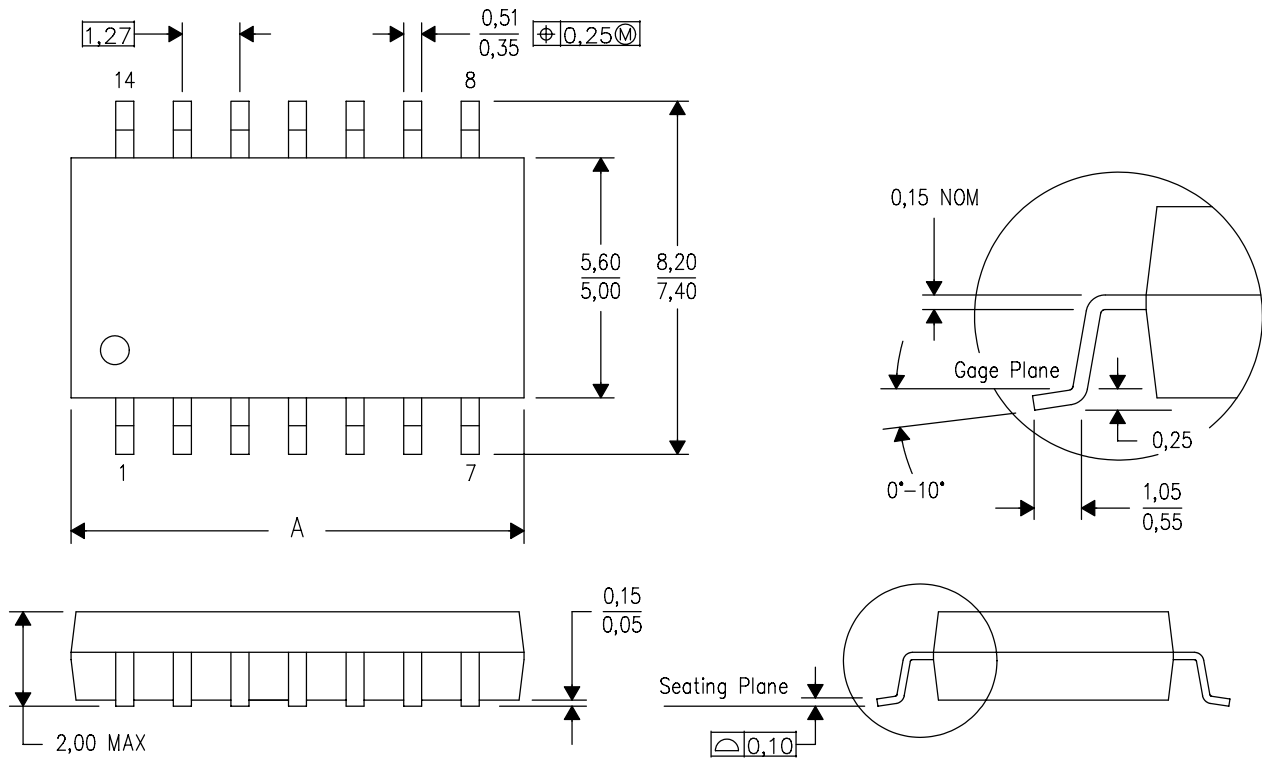
4040047-3/F 07/2004

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

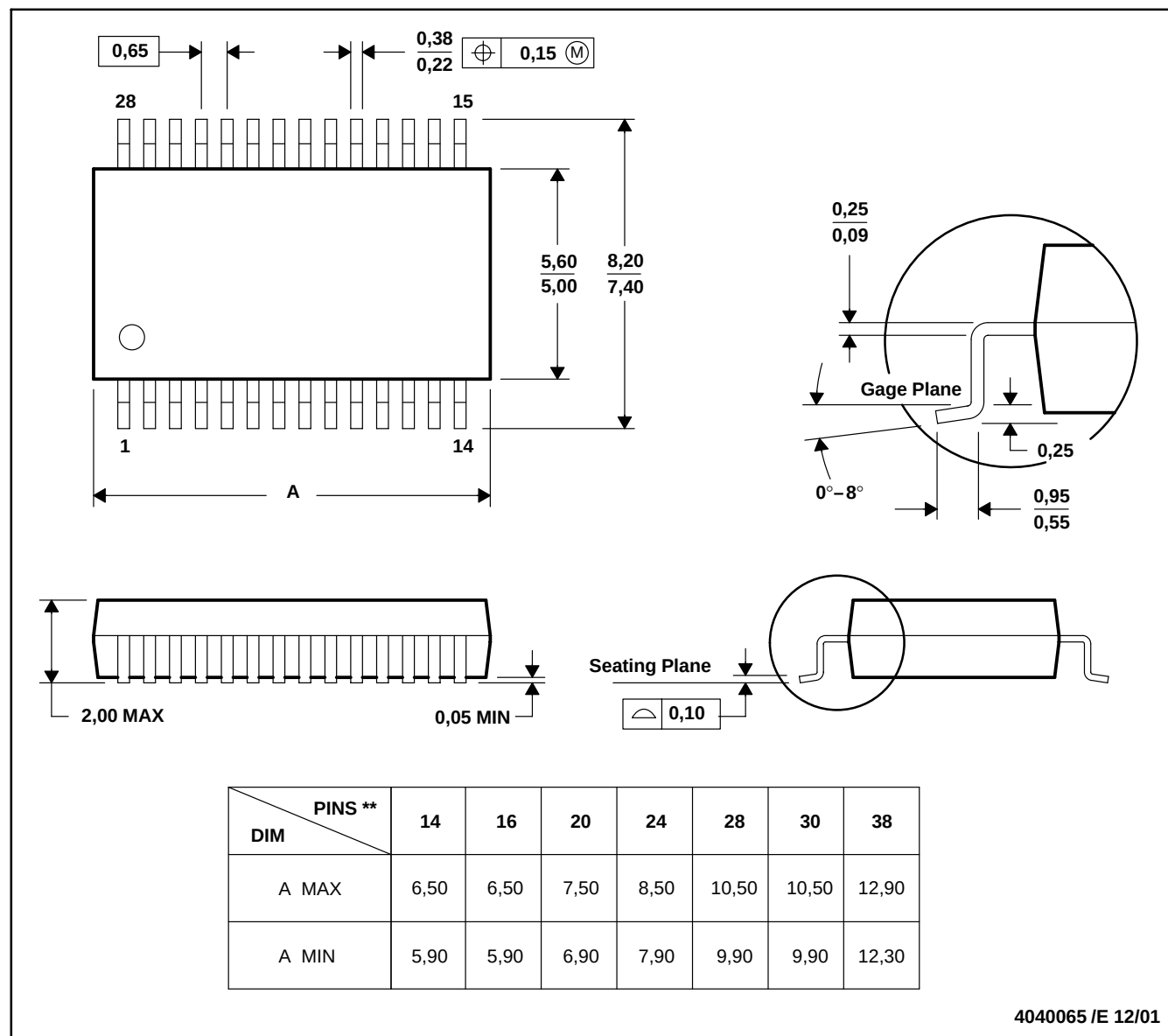
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

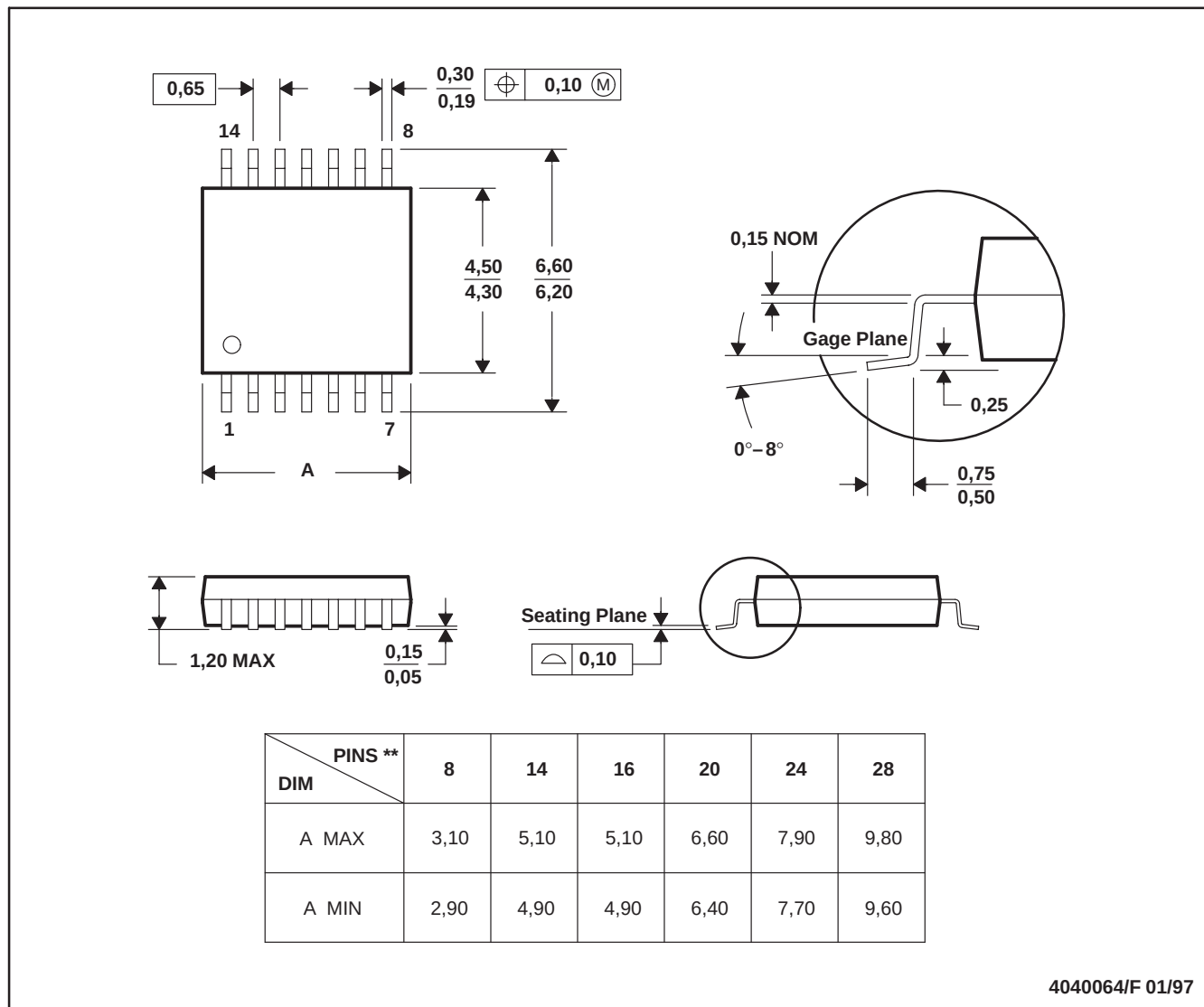


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
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 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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