



16-Bit, Dual Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **LOW POWER:** 4mW
- **UNIPOLAR OR BIPOLAR OPERATION**
- **SETTLING TIME:** 10 μ s to $\pm 0.003\%$ FSR
- **15-BIT LINEARITY AND MONOTONICITY:** -40°C to $+85^{\circ}\text{C}$
- **PROGRAMMABLE RESET TO MID-SCALE OR ZERO-SCALE**
- **DOUBLE-BUFFERED DATA INPUTS**

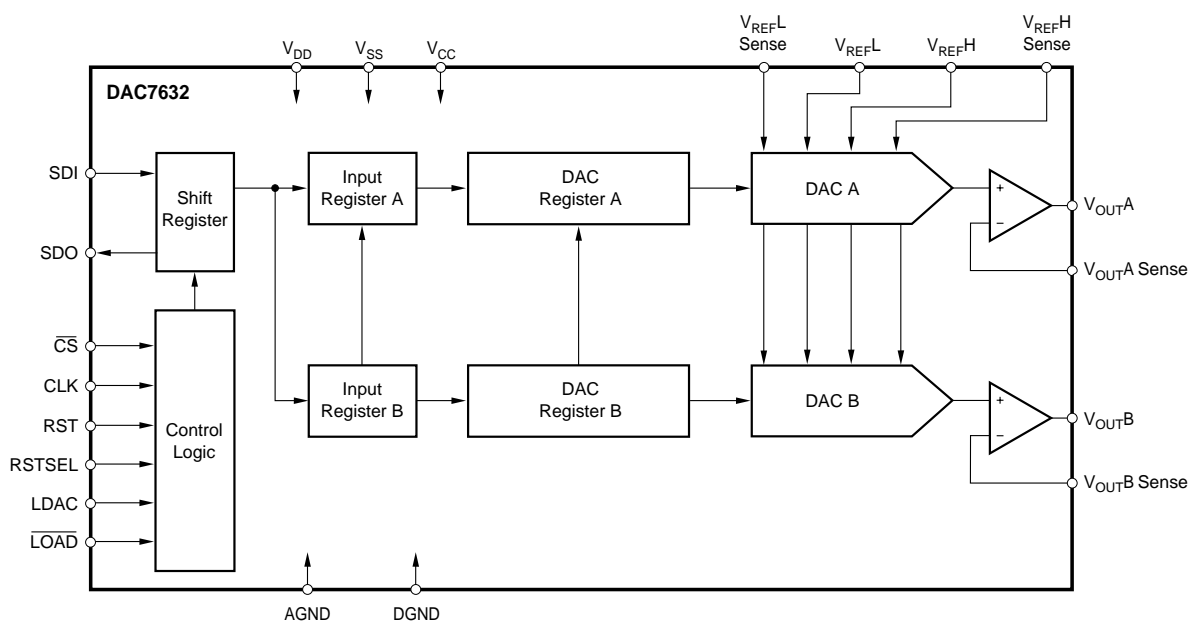
APPLICATIONS

- **PROCESS CONTROL**
- **CLOSED-LOOP SERVO-CONTROL**
- **MOTOR CONTROL**
- **DATA ACQUISITION SYSTEMS**
- **DAC-PER-PIN PROGRAMMERS**

DESCRIPTION

The DAC7632 is a 16-bit, dual channel, voltage output, Digital-to-Analog Converter (DAC) which provides 15-bit monotonic performance over the specified temperature range. The device accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of both DACs), and provides a serial data output for daisy-chaining multiple devices. A programmable asynchronous reset clears all registers to a mid-scale code of 8000_H or to a zero-scale code of 0000_H. The DAC7632 can operate from a single +5V supply or from +5V and -5V supplies, providing an output range of 0V to +2.5V or -2.5V to +2.5V, respectively.

Low power and small size per DAC make the DAC7632 ideal for industrial process control, data acquisition systems, and closed-loop servo-control. The DAC7632 is available in an LQFP-32 package and specified over a -40°C to $+85^{\circ}\text{C}$ temperature range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

V_{CC} and V_{DD} to V_{SS}	–0.3V to 11V
V_{CC} and V_{DD} to GND	–0.3V to 5.5V
V_{REFL} to V_{SS}	–0.3V to ($V_{CC} - V_{SS}$)
V_{CC} to V_{REFH}	–0.3V to ($V_{CC} - V_{SS}$)
V_{REFH} to V_{REFL}	–0.3V to ($V_{CC} - V_{SS}$)
Digital Input Voltage to GND	–0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to GND	–0.3V to $V_{DD} + 0.3V$
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MONOTONICITY	PACKAGE-LEAD	PACKAGE DESIGNATOR ⁽¹⁾	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7632VF	14 Bits	LQFP-32	VF	–40°C to +85°C	DAC7632	DAC7632VFT	Tape and Reel, 250
"	"	"	"	"	"	DAC7632VFR	Tape and Reel, 1000
DAC7632VFB	15 Bits	LQFP-32	VF	–40°C to +85°C	DAC7632B	DAC7632VFBT	Tape and Reel, 250
"	"	"	"	"	"	DAC7632VFB R	Tape and Reel, 1000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS (Dual Supply)

At $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, and $V_{REFL} = -2.5V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7632VF			DAC7632VFB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY								
Linearity Error			± 3	± 4		± 2	± 3	LSB
Linearity Match			± 4			± 2		LSB
Differential Linearity Error			± 2	± 3		± 1	± 2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			Bits
Bipolar Zero Error			± 1	± 3		*	*	mV
Bipolar Zero Error Drift			5	10		*	*	ppm/°C
Full-Scale Error			± 1	± 3		*	*	mV
Full-Scale Error Drift			5	10		*	*	ppm/°C
Bipolar Zero Matching	Channel-to-Channel Matching		± 1	± 3		*	*	mV
Full-Scale Matching	Channel-to-Channel Matching		± 1	± 3		*	*	mV
Power-Supply Rejection Ratio (PSRR)	At Full Scale		10	100		*	*	ppm/V
ANALOG OUTPUT								
Voltage Output	$R_L = 10k\Omega$	V_{REFL}		V_{REFH}	*		*	V
Output Current		-1.25		+1.25	*		*	mA
Maximum Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			-10, +30			*		mA
Short-Circuit Duration	GND or V_{CC} or V_{SS}		Indefinite			*		
REFERENCE INPUT								
Ref High Input Voltage Range		$V_{REFL} + 1.25$		+2.5	*		*	V
Ref Low Input Voltage Range		-2.5		$V_{REFH} - 1.25$	*		*	V
Ref High Input Current			500			*		μA
Ref Low Input Current			-500			*		μA
DYNAMIC PERFORMANCE								
Settling Time	To $\pm 0.003\%$, 5V Output Step		8	10		*	*	μs
Channel-to-Channel Crosstalk			0.5			*		LSB
Digital Feedthrough			2			*		nV-s
Output Noise Voltage	$f = 10kHz$		60			*		nV/√Hz
DAC Glitch	7FFF _H to 8000 _H or 8000 _H to 7FFF _H		40			*		nV-s
DIGITAL INPUT								
V_{IH}		$0.7 \cdot V_{DD}$			*			V
V_{IL}				$0.3 \cdot V_{DD}$			*	V
I_{IH}				± 10			*	μA
I_{IL}				± 10			*	μA
DIGITAL OUTPUT								
V_{OH}	$I_{OH} = -0.8mA$	3.6	4.5		*	*		V
V_{OL}	$I_{OL} = 1.6mA$		0.3	0.4		*	*	V
POWER SUPPLY								
V_{DD}		+4.75	+5.0	+5.25	*	*	*	V
V_{CC}		+4.75	+5.0	+5.25	*	*	*	V
V_{SS}		-5.25	-5.0	-4.75	*	*	*	V
I_{CC}			0.7	1.1		*	*	mA
I_{DD}			50			*	*	μA
I_{SS}		-1.2	-0.8		*	*	*	mA
Power			7.5	11.5		*	*	mW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	°C

* Specifications same as DAC7632VF.

SPECIFICATIONS (Dual Supply)

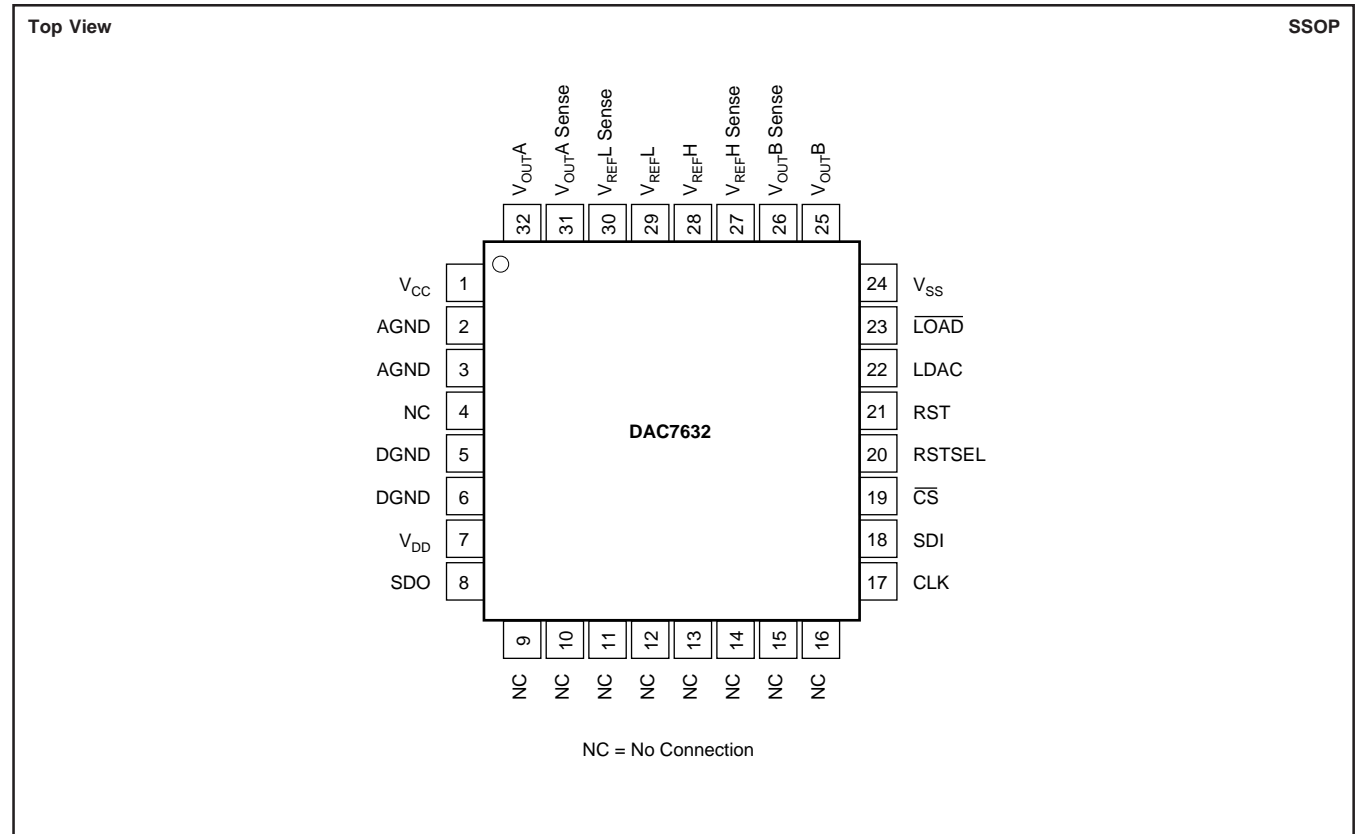
At $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, and $V_{REFL} = 0V$, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7632VF			DAC7632VFB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY Linearity Error ⁽¹⁾ Linearity Match Differential Linearity Error Monotonicity, T_{MIN} to T_{MAX} Zero Scale Error Zero Scale Error Drift Full-Scale Error Full-Scale Error Drift Zero Scale Matching Full-Scale Matching Power Supply Rejection Ratio (PSRR)	Channel-to-Channel Matching Channel-to-Channel Matching At Full Scale	14	± 3	± 4	15	± 2	± 3	LSB LSB LSB Bits mV ppm/°C mV ppm/°C mV mV ppm/V
			± 4			± 2		
			± 2	± 3		± 1	± 2	
			± 1	± 3		*	*	
			5	10		*	*	
			± 1	± 3		*	*	
			5	10		*	*	
			± 1	± 3		*	*	
			± 1	± 3		*	*	
			10	100		*	*	
						*	*	
ANALOG OUTPUT Voltage Output Output Current Maximum Load Capacitance Short-Circuit Current Short-Circuit Duration	$R_L = 10k\Omega$ No Oscillation GND or V_{CC}	0 -1.25		V_{REFH} +1.25	*		*	V mA pF mA
REFERENCE INPUT Ref High Input Voltage Range Ref Low Input Voltage Range Ref High Input Current Ref Low Input Current		$V_{REFL} + 1.25$ -2.5		+2.5 $V_{REFH} - 1.25$	*		*	V V μA μA
DYNAMIC PERFORMANCE Settling Time Channel-to-Channel Crosstalk Digital Feedthrough Output Noise Voltage, $f = 10kHz$ DAC Glitch	To $\pm 0.003\%$, 5V Output Step 7FFF _H to 8000 _H or 8000 _H to 7FFF _H		8 0.5 2 60 40	10		*	*	μs LSB nV-s nV/√Hz nV-s
DIGITAL INPUT V_{IH} V_{IL} I_{IH} I_{IL}		$0.7 \cdot V_{DD}$		$0.3 \cdot V_{DD}$ ± 10 ± 10	*		*	V V μA μA
DIGITAL OUTPUT V_{OH} V_{OL}	$I_{OH} = -0.8mA$ $I_{OL} = 1.6mA$	3.6	4.5 0.3	0.4	*	*	*	V V
POWER SUPPLY V_{DD} V_{CC} V_{SS} I_{CC} I_{DD} Power		+4.75 +4.75 0	+5.0 +5.0 0 0.5 50 2.5	+5.25 +5.25 0 0.9 4.5	*	*	*	V V V mA μA mW
TEMPERATURE RANGE Specified Performance		-40		+85	*		*	°C

* Specifications same as DAC7632VF.

NOTE: (1) If $V_{SS} = 0V$, the specification applies to Code 0040_H and above due to possible negative zero-scale error.

PIN CONFIGURATION



PIN DESCRIPTIONS

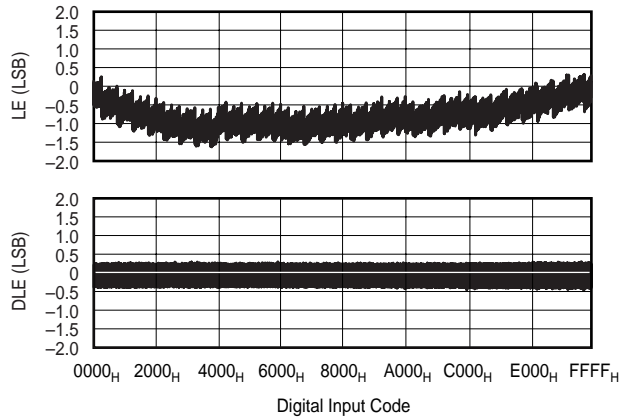
PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	V _{CC}	Analog +5V Power Supply	22	LDAC	DAC Register Load Control, Rising Edge Triggered
2, 3	AGND	Analog Ground	23	$\overline{\text{LOAD}}$	DAC Input Register Load Control, Active LOW
4	NC	No Connection	24	V _{SS}	Analog -5V Power Supply (or 0V for Single Supply)
5, 6	DGND	Digital Ground	25	V _{OUTB}	DAC B Output Voltage
7	V _{DD}	Digital +5V Power Supply	26	V _{OUTB} Sense	DAC B Output Amplifier Inverting Input. Used to close the feedback loop at the load.
8	SDO	Serial Data Output	27	V _{REFH} Sense	DAC A and B Reference High Sense Input
9-16	NC	No Connection	28	V _{REFH}	DAC A and B Reference High Input
17	CLK	Data Clock Input	29	V _{REFL}	DAC A and B Reference Low Input
18	SDI	Serial Data Input	30	V _{REFL} Sense	DAC A and B Reference Low Sense Input
19	$\overline{\text{CS}}$	Chip Select, Active LOW	31	V _{REFA} Sense	DAC A Output Amplifier Inverting Input. Used to close the feedback loop at the load.
20	RSTSEL	Reset Select. Determines the action of RST. If HIGH, a RST common will set the DAC registers to mid-scale code (8000 _H). If LOW, a RST command will set the DAC registers to zero-scale code (0000 _H).	32	V _{OUTA}	DAC A Output Voltage
21	RST	Reset, Rising Edge Triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale code or zero-scale code.			

TYPICAL CHARACTERISTICS: $V_{SS} = 0V$

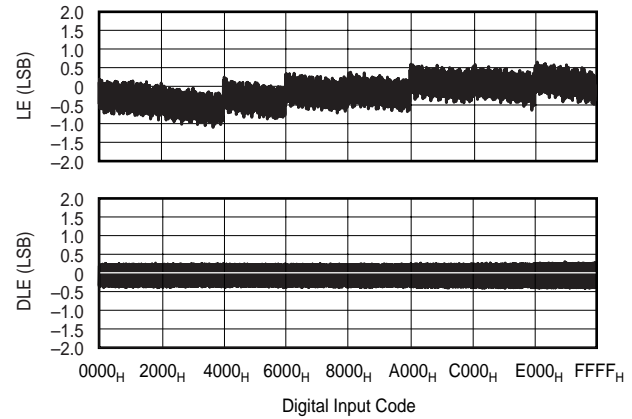
At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.

+25°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +25°C)

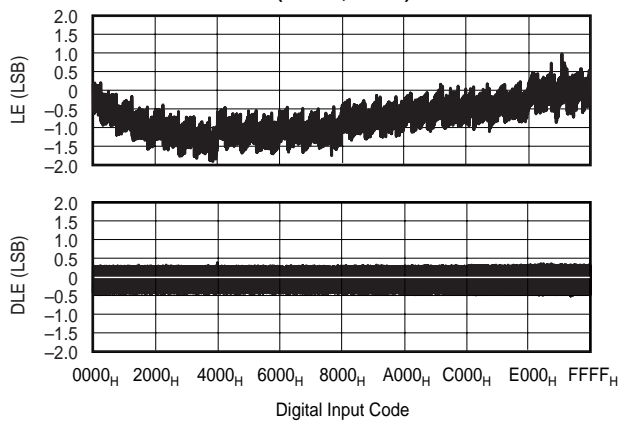


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +25°C)

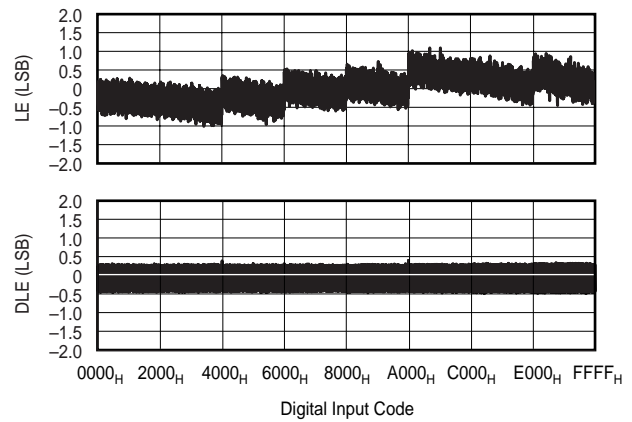


+85°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, +85°C)

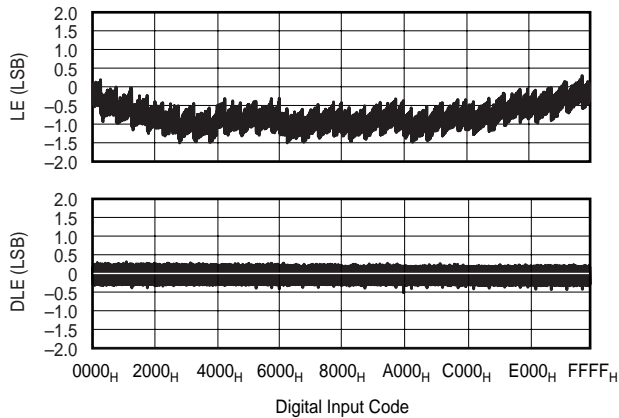


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, +85°C)

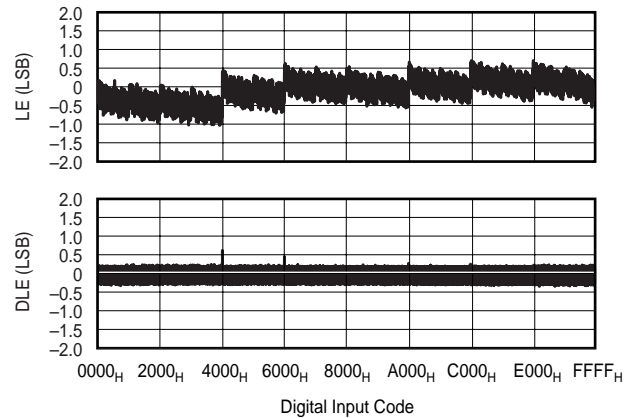


-40°C

LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, -40°C)

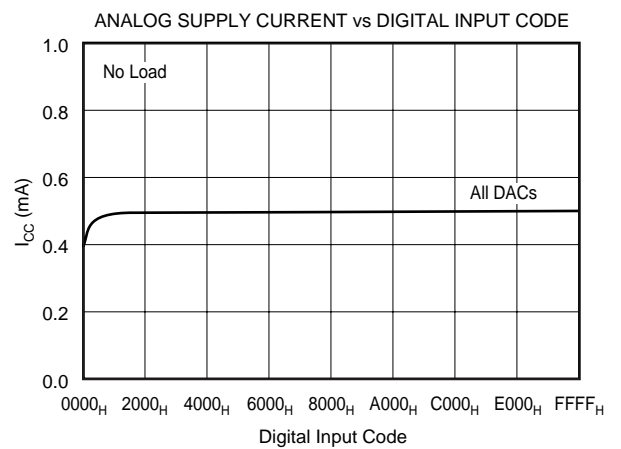
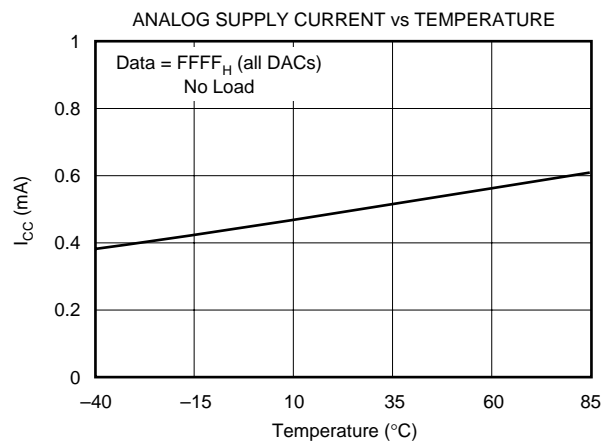
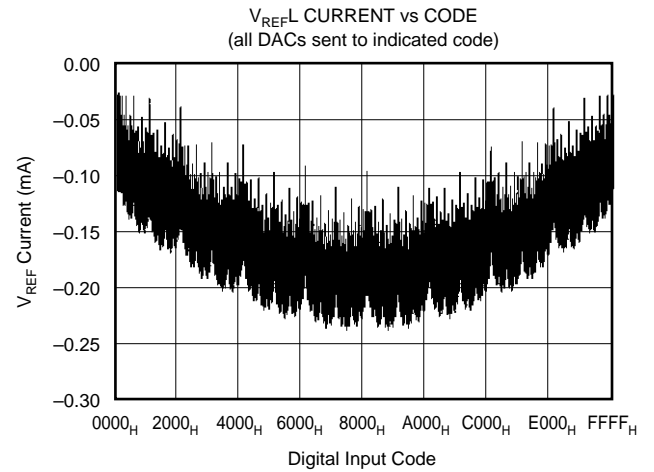
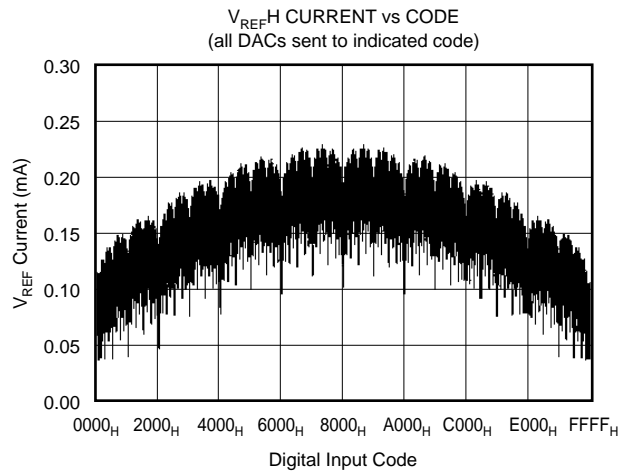
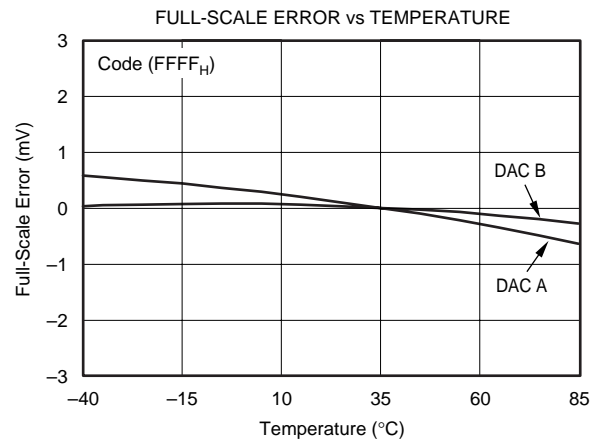
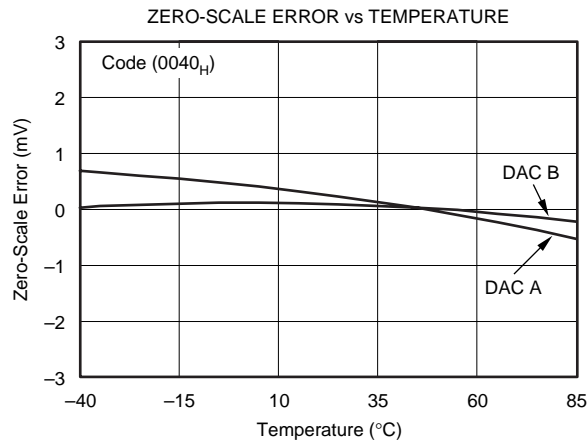


LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, -40°C)



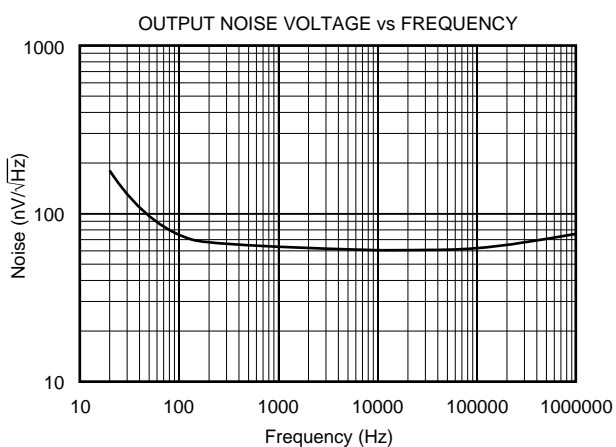
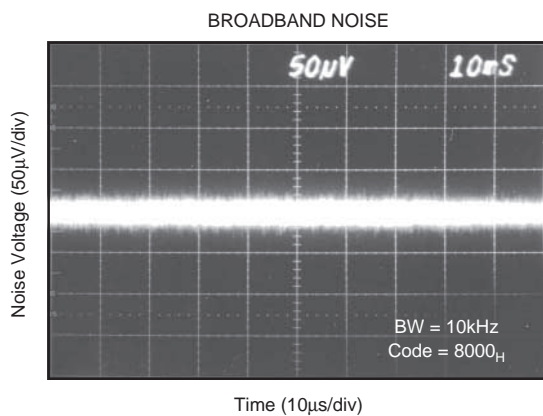
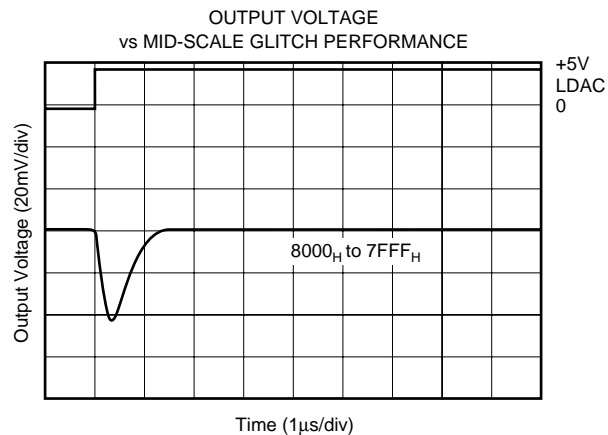
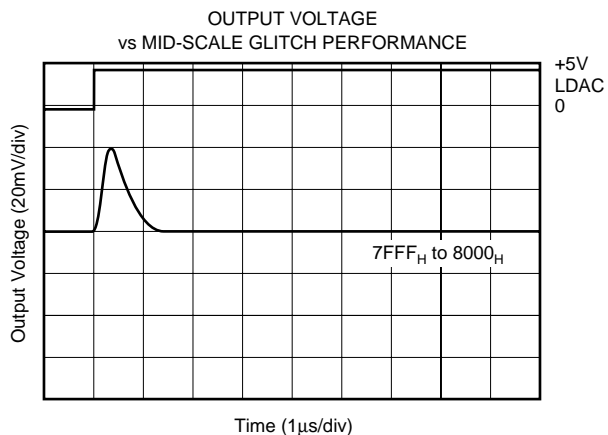
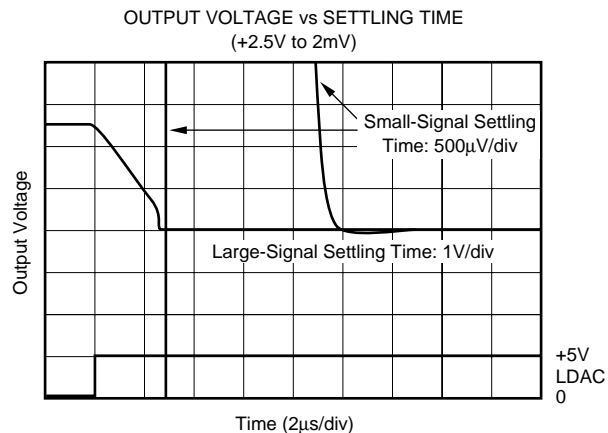
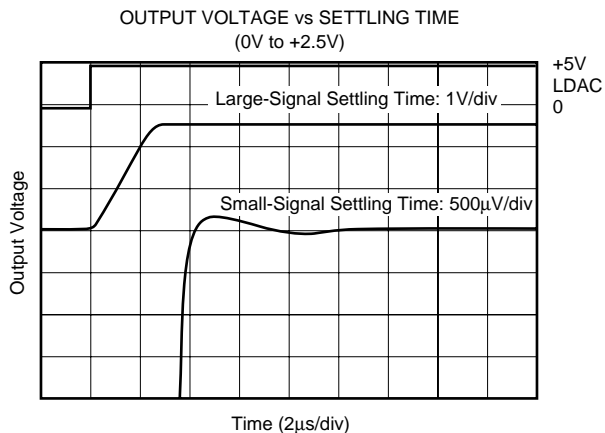
TYPICAL CHARACTERISTICS: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



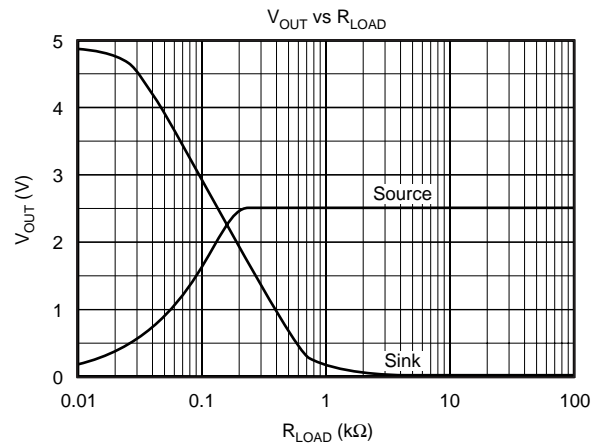
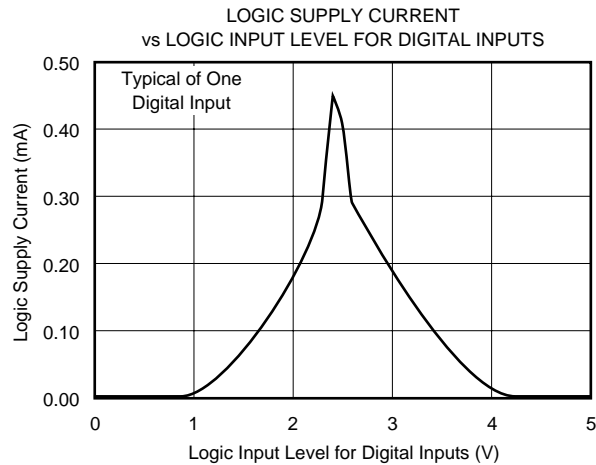
TYPICAL CHARACTERISTICS: $V_{SS} = 0V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



TYPICAL CHARACTERISTICS: $V_{SS} = 0V$ (Cont.)

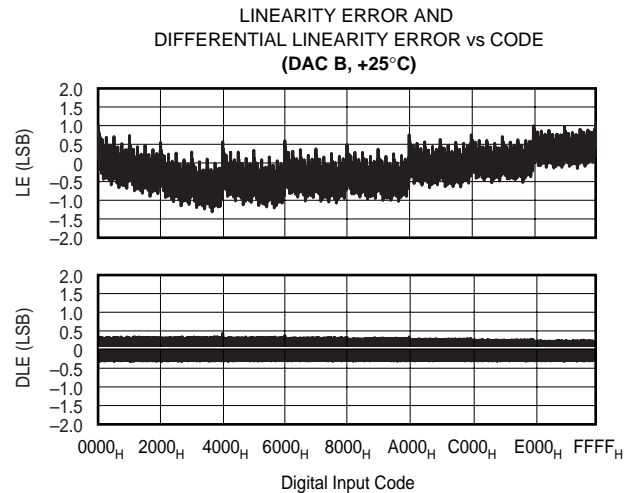
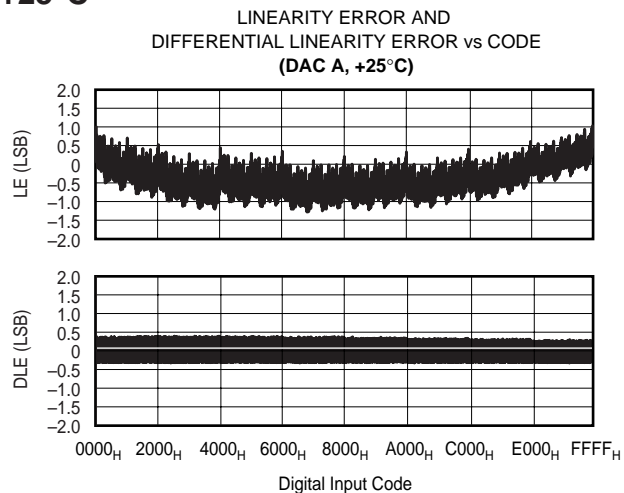
At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = 0V$, $V_{REFH} = +2.5V$, $V_{REFL} = 0V$, representative unit, unless otherwise specified.



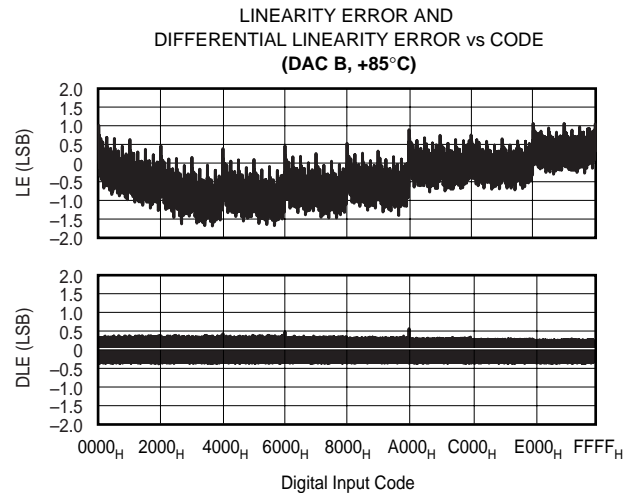
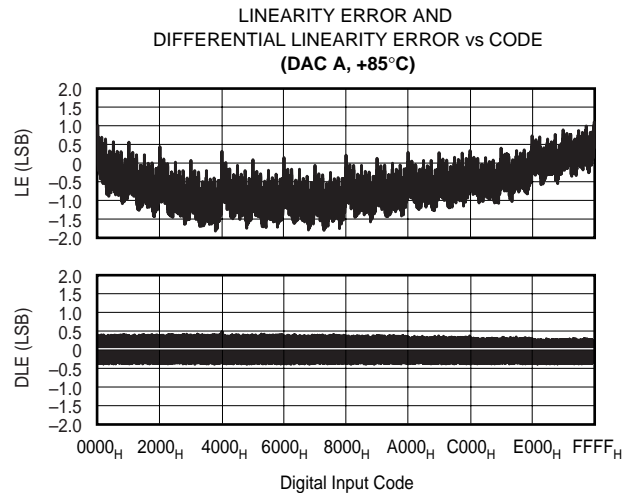
$V_{SS} = -5V$

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, $V_{REFL} = -2.5V$, representative unit, unless otherwise specified.

$+25^\circ C$



$+85^\circ C$

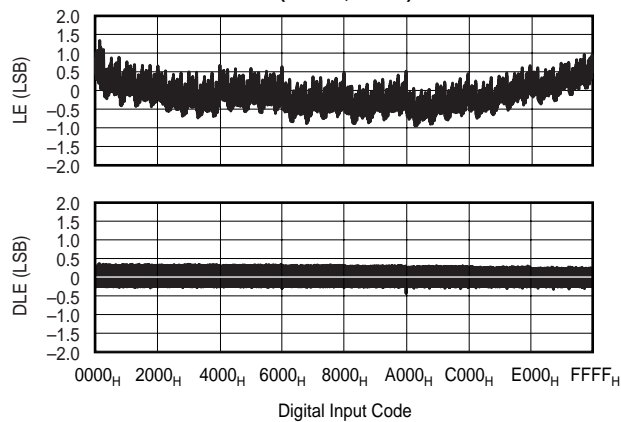


TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (Cont.)

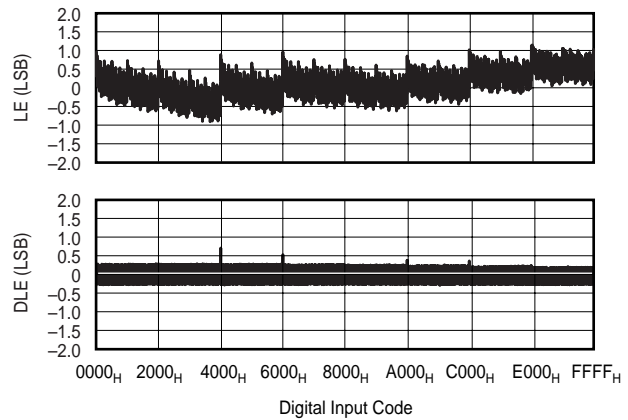
At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, $V_{REFL} = -2.5V$, representative unit, unless otherwise specified.

$-40^\circ C$

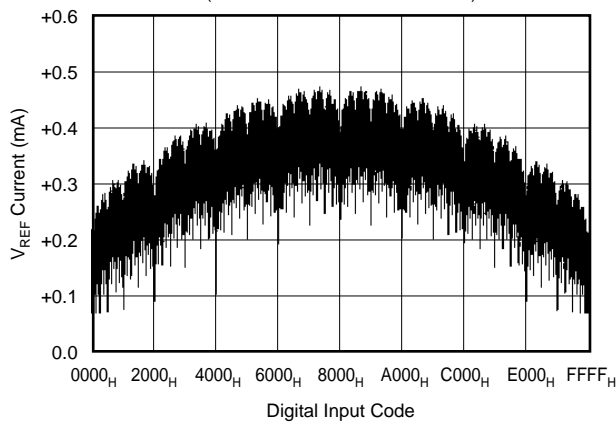
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC A, $-40^\circ C$)



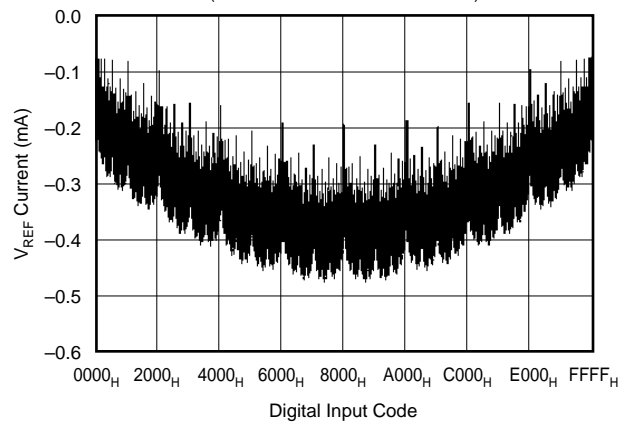
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
(DAC B, $-40^\circ C$)



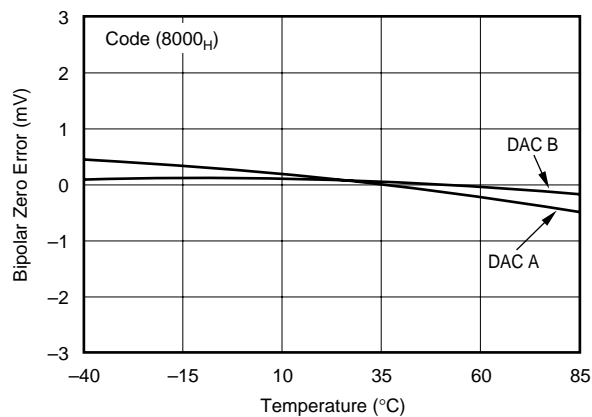
V_{REFH} CURRENT vs CODE
(all DACs sent to indicated code)



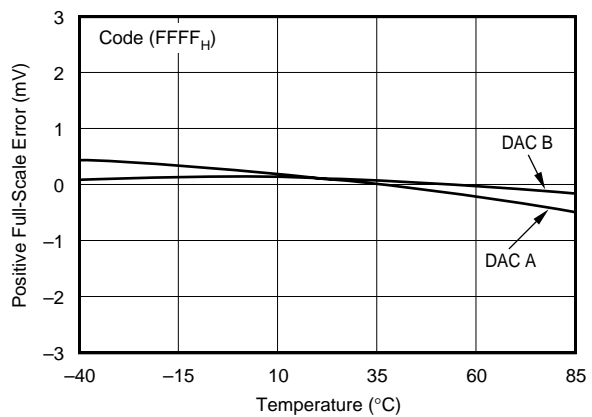
V_{REFL} CURRENT vs CODE
(all DACs sent to indicated code)



BIPOLAR ZERO ERROR vs TEMPERATURE

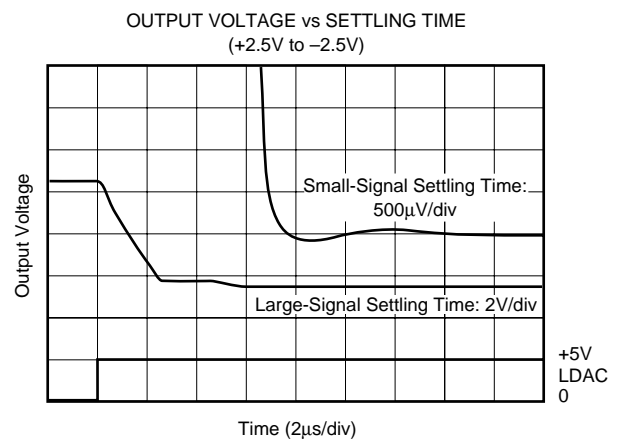
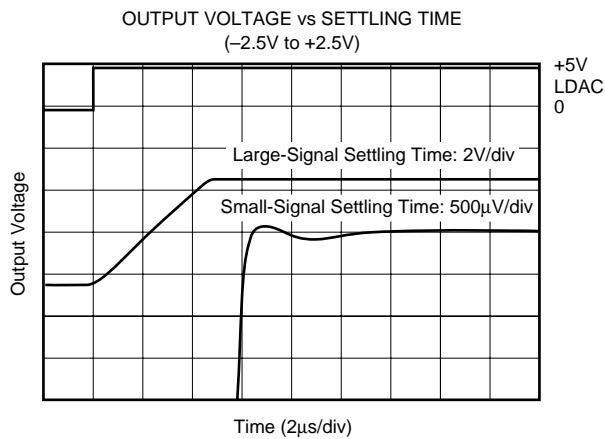
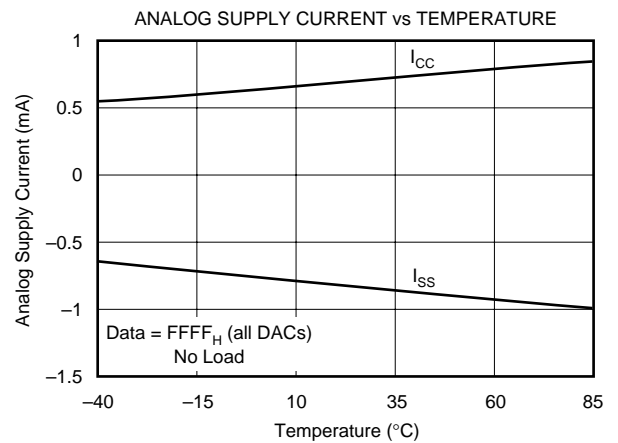
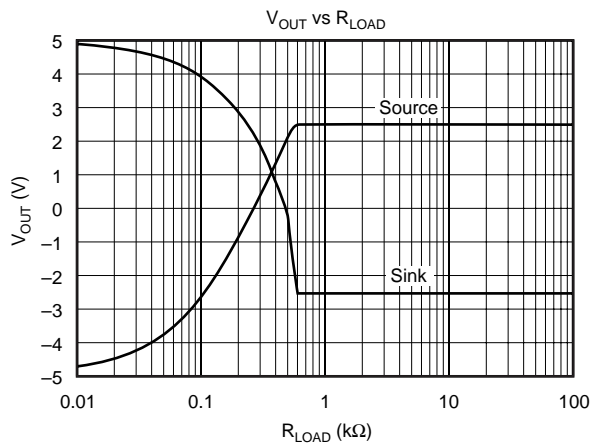
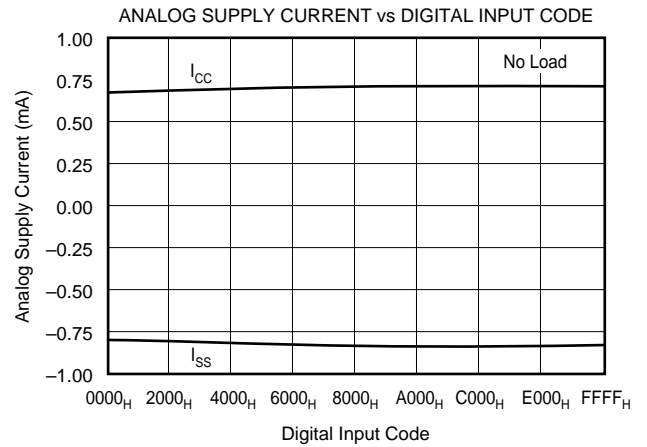
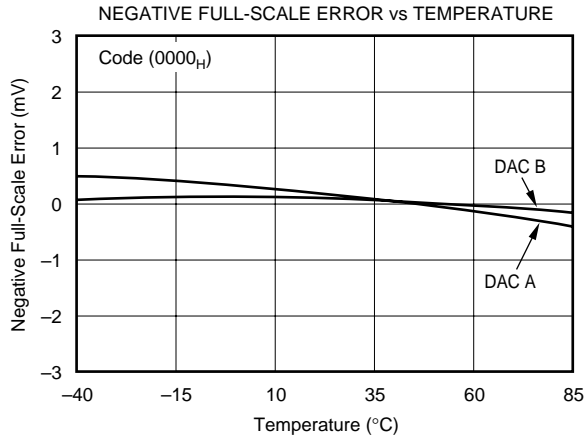


POSITIVE FULL-SCALE ERROR vs TEMPERATURE

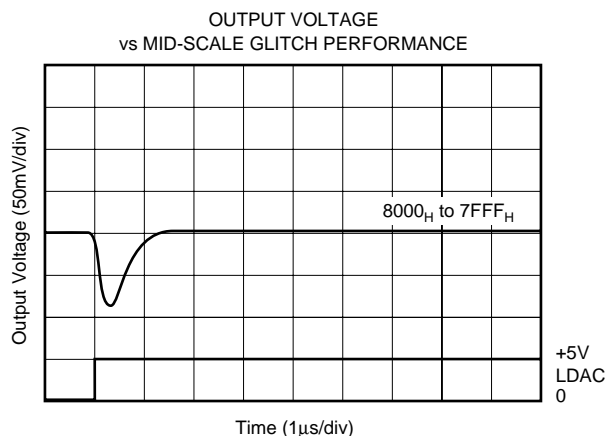


TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (Cont.)

At $T_A = +25^\circ C$, $V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, $V_{REFH} = +2.5V$, $V_{REFL} = -2.5V$, representative unit, unless otherwise specified.



At $T_A = +25^\circ\text{C}$, $V_{DD} = V_{CC} = +5\text{V}$, $V_{SS} = -5\text{V}$, $V_{REFH} = +2.5\text{V}$, $V_{REFL} = -2.5\text{V}$, representative unit, unless otherwise specified.



The DAC7632 is a dual channel, voltage output, 16-bit DAC. The architecture is an R-2R ladder configuration with the three MSB's segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R-2R ladder network, segmented MSBs, and output op amp, as shown in Figure 1. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the external voltage references V_{REFL} and V_{REFH} , respectively.

The diagram shows a 1-bit DAC circuit. It consists of a resistor ladder with a total resistance of $2R$ connected to a reference voltage V_{REFH} . The ladder is composed of a series of $2R$ resistors. A feedback resistor R_F is connected from the output V_{OUT} to the inverting input of the op-amp. The non-inverting input is connected to V_{REFL} . The output V_{OUT} is also labeled as $V_{OUT\ Sense}$.

FIGURE 1. DAC7632 Architecture.

ANALOG OUTPUTS

When $V_{SS} = -5V$ (dual-supply operation), the output amplifier can swing to within 2.25V of the supply rails over the $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. When $V_{SS} = 0V$ (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to ground. Care must also be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output cannot swing below ground, the output voltage may not change for the first few digital input codes (0000_H, 0001_H, 0002_H, etc.) if the output amplifier has a negative offset. At the negative limit of $-2mV$, the first specified output starts at code 0040_H.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of $38\mu V$. With a load current of 1mA, series wiring and connector resistance of only $40m\Omega$ (R_{W2}) will cause a voltage drop of $40\mu V$, as shown in Figure 4. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is $1/2m\Omega$ per square. For a 1mA load, a 10 milli-inch wide printed circuit conductor 600 milli-inches long will result in a voltage drop of $30\mu V$.

The DAC7632 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load, as shown in Figure 4, thus ensuring an accurate output voltage.

REFERENCE INPUTS

The reference inputs, V_{REFL} and V_{REFH} , can be any voltage between $V_{SS} + 2.5V$ and $V_{CC} - 2.5V$, provided that V_{REFH} is at least 1.25V greater than V_{REFL} . The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note

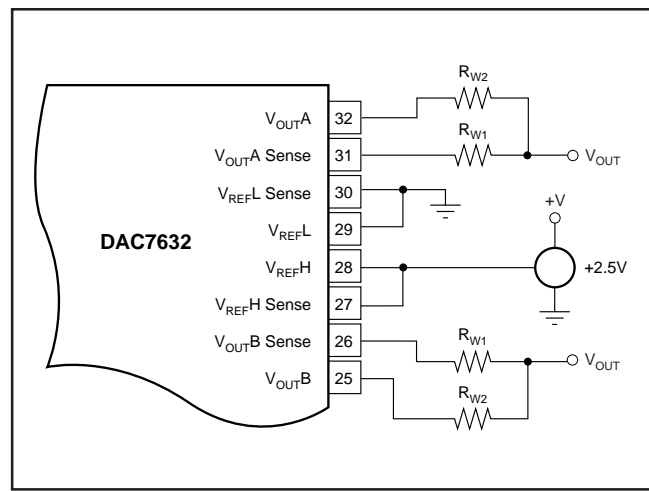


FIGURE 4. Analog Output Closed-Loop Configuration
 R_W represents wiring resistances.

that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of $-4.75V$ to $-5.25V$. The voltage on V_{SS} sets several bias points within the converter. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device may be affected.

The current into the V_{REFH} input and out of V_{REFL} depends on the DAC output voltages, and can vary from a few microamps to approximately 0.5mA. The reference input appears as a varying load to the reference supply. If the reference applied can sink or source the required current, a reference buffer is not required. The DAC7632 features reference drive and sense connections such that the internal errors caused by the changing reference current and the circuit impedances can be minimized. Figures 5 through 13 show different reference configurations and the effect on the integral linearity and differential linearity, for each case.

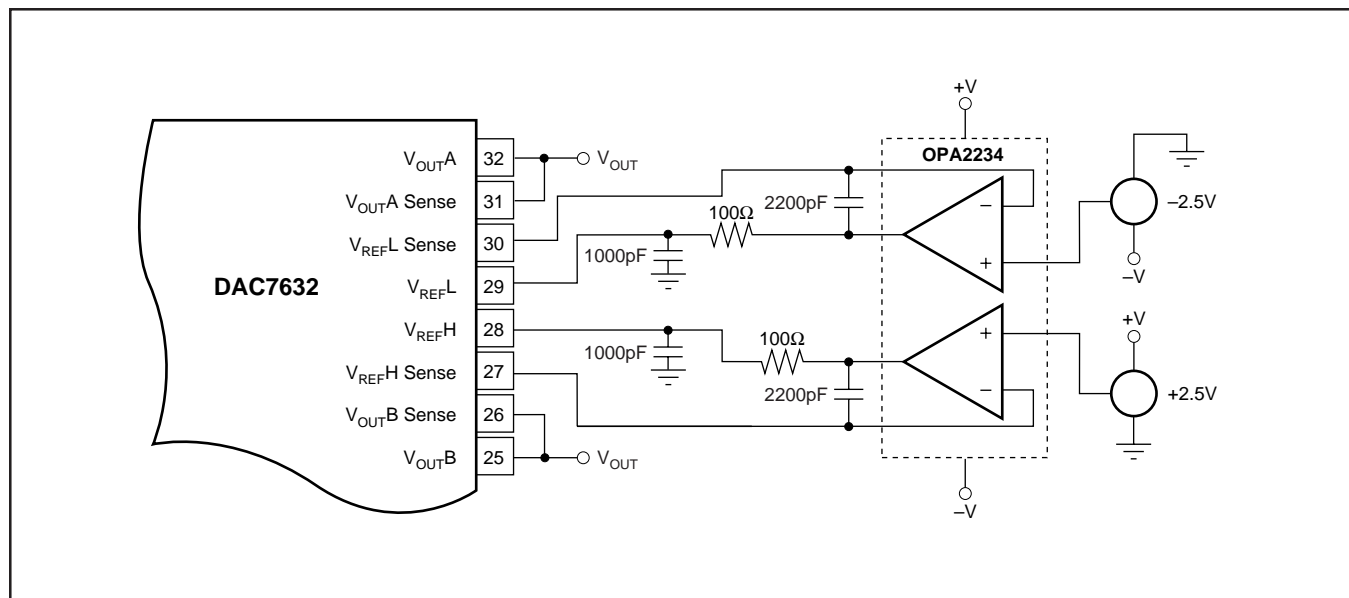


FIGURE 5. Dual Supply Configuration-Buffered References, used for Dual-Supply Performance.

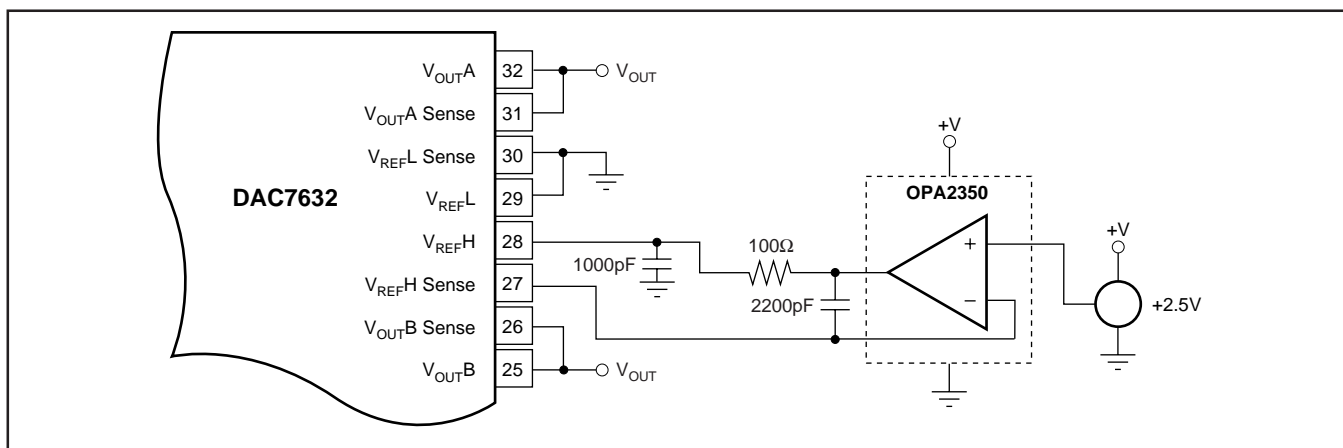


FIGURE 10. Single-Supply Buffered V_{REFH} .

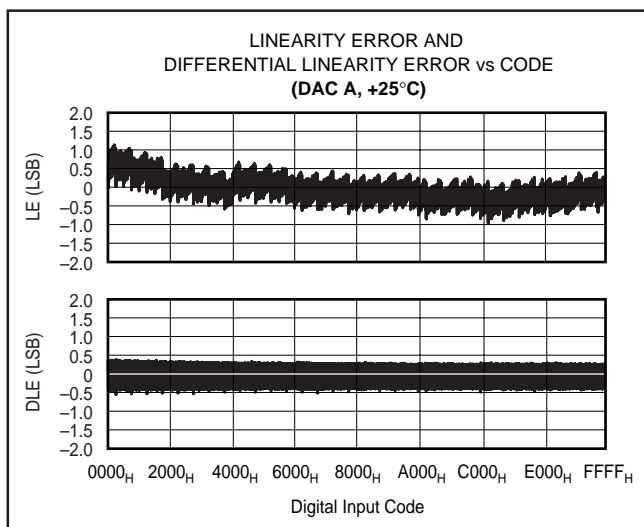


FIGURE 11. Linearity and Differential Linearity Error Characteristic Curves for Figure 10.

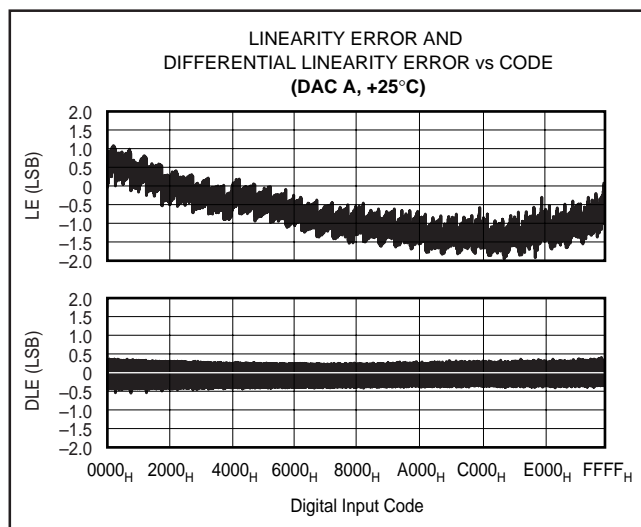


FIGURE 13. Linearity and Differential Linearity Error Characteristic Curves for Figure 12.

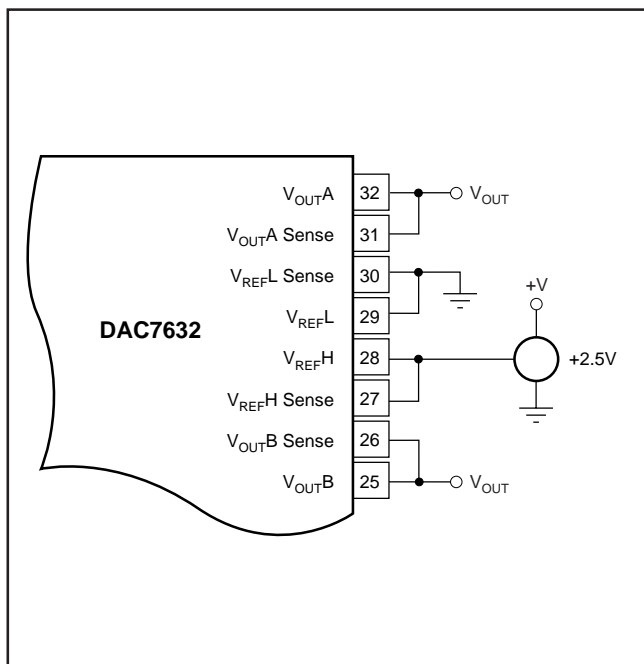


FIGURE 12. Low-Cost Single-Supply Configuration.

DIGITAL INTERFACE

See Table I for the basic control logic for the DAC7632. The interface consists of a Serial Data Clock (CLK) input, Serial Data Input (SDI), Input Register Load Control Signal (\overline{LOAD}), and DAC Register Load Control Signal (\overline{LDAC}). In addition, a Chip Select (\overline{CS}) input is available to enable serial communication when there are multiple serial devices attached to a single serial bus. An asynchronous Reset (RST) input (rising edge triggered) is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the Reset Select (RSTSEL) signal.

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Figure 15). The first bit (DACSEL) selects the input register that will be updated when \overline{LOAD} goes LOW. The third bit is a “Quick Load” bit such that if HIGH, the code in the shift register is loaded into both input registers when the \overline{LOAD} signal goes LOW. If the “Quick Load” bit is LOW when an active \overline{LOAD} signal is issued, the content of the shift register is loaded only to the input register that is addressed by DACSEL. The “Quick Load” bit is followed by five unused bits. The last 16 bits (MSB first) make up the DAC code.

SERIAL DATA INPUT

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
DACSEL	X	QUICK LOAD	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

DACSEL	$\overline{\text{CS}}$	RST	RSTSEL	LDAC	$\overline{\text{LOAD}}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
0	L	H	X	X	L	Write	Hold	Write Input	A
1	L	H	X	X	L	Write	Hold	Write Input	B
X	H	H	X	\uparrow	H	Hold	Write	Update	All
X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	\uparrow	L	X	X	Reset to 0000 _H	Reset to 0000 _H	Reset to Zero-Scale	All
X	X	\uparrow	H	X	X	Reset to 8000 _H	Reset to 8000 _H	Reset to Mid-scale	All

TABLE I. DAC7632 Logic Truth Table.

Data presented to SDI is clocked into the shift register on each rising CLK edge. This data is latched into the input register(s) via a logic-low level on $\overline{\text{LOAD}}$. The data is directed from the shift register to the desired input register(s) specified by data bits 21 and 23. The internal DAC registers are edge triggered and not level triggered. When the LDAC signal is transitioned from LOW to HIGH, the digital word currently in the input registers are latched. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, both DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows the input registers to be written to at any point, then the DAC output voltages can be synchronously changed via a trigger signal (LDAC).

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. In addition, care must be taken with the state of CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is LOW when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data one additional bit. The result will be incorrect data and possible selection of the wrong input register(s). If both $\overline{\text{CS}}$ and CLK are used, $\overline{\text{CS}}$ should rise only when CLK is HIGH. If not, then either $\overline{\text{CS}}$ or CLK can be used to operate the shift register (the remaining pin should be tied to DGND). Please refer to Table II for more information.

$\overline{\text{CS}}^{(1)}$	CLK ⁽¹⁾	$\overline{\text{LOAD}}$	RST	SERIAL SHIFT REGISTER
H ⁽²⁾	X ⁽³⁾	H	H	No Change
L ⁽⁴⁾	L	H	H	No Change
L	$\uparrow^{(5)}$	H	H	Advanced One Bit
\uparrow	L	H	H	Advanced One Bit
H ⁽⁶⁾	X	L ⁽⁷⁾	H	No Change
H ⁽⁶⁾	X	H	$\uparrow^{(8)}$	No Change

NOTES: (1) $\overline{\text{CS}}$ and CLK are interchangeable. (2) H = Logic HIGH. (3) X = Don't Care. (4) L = Logic LOW. (5) = Positive Logic Transition. (6) A HIGH value is suggested in order to avoid a "false clock" from advancing the shift register and changing the shift register. (7) If data is clocked into the serial register while $\overline{\text{LOAD}}$ is LOW, the input registers will change as data flows through the shift register. This will corrupt the data in each DAC register that has been erroneously selected. (8) Rising edge of RST causes no change in the contents of the serial shift register.

TABLE II. Serial Shift Register Truth Table.

SERIAL-DATA OUTPUT

The Serial-Data Output pin (SDO) is the internal shift register's output. For the DAC7632, SDO is a driven output and does not require an external pull-up. Any number of DAC7632s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 14.

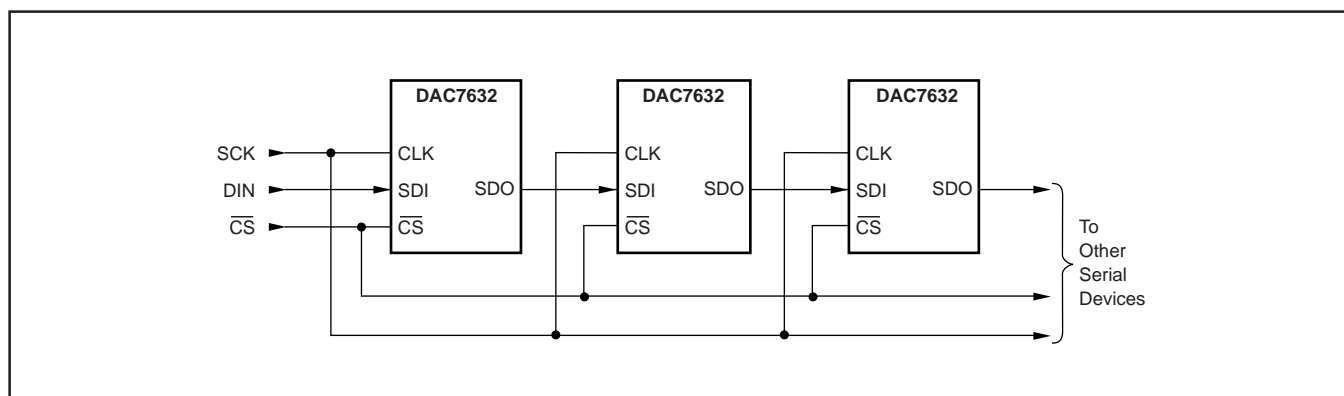


FIGURE 14. Daisy-Chaining Multiple DAC7632s.

DIGITAL TIMING

Figure 15 and Table III provide detailed timing for the digital interface of the DAC7632.

DIGITAL INPUT CODING

The DAC7632 input data is in Straight Binary format. The output voltage is given by Equation 1.

$$V_{OUT} = V_{REFL} + \frac{(V_{REFH} - V_{REFL}) \cdot N}{65,536}$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

DIGITALLY-PROGRAMMABLE CURRENT SOURCE

The DAC7632 offers a unique set of features that allows a wide range of flexibility in designing application circuits such as programmable current sources. The DAC7632 offers both a differential reference input, as well as an open-loop configuration around the output amplifier. The open-loop configuration around the output amplifier allows a transistor to be placed within the loop to implement a digitally-programmable, unidirectional current source. The availability of a differential reference allows programmability for both the full-scale and zero-scale currents. The output current is calculated as:

$$I_{OUT} = \left(\left(\frac{V_{REFH} - V_{REFL}}{R_{SENSE}} \right) \cdot \left(\frac{N}{65,536} \right) \right) + (V_{REFL} / R_{SENSE})$$

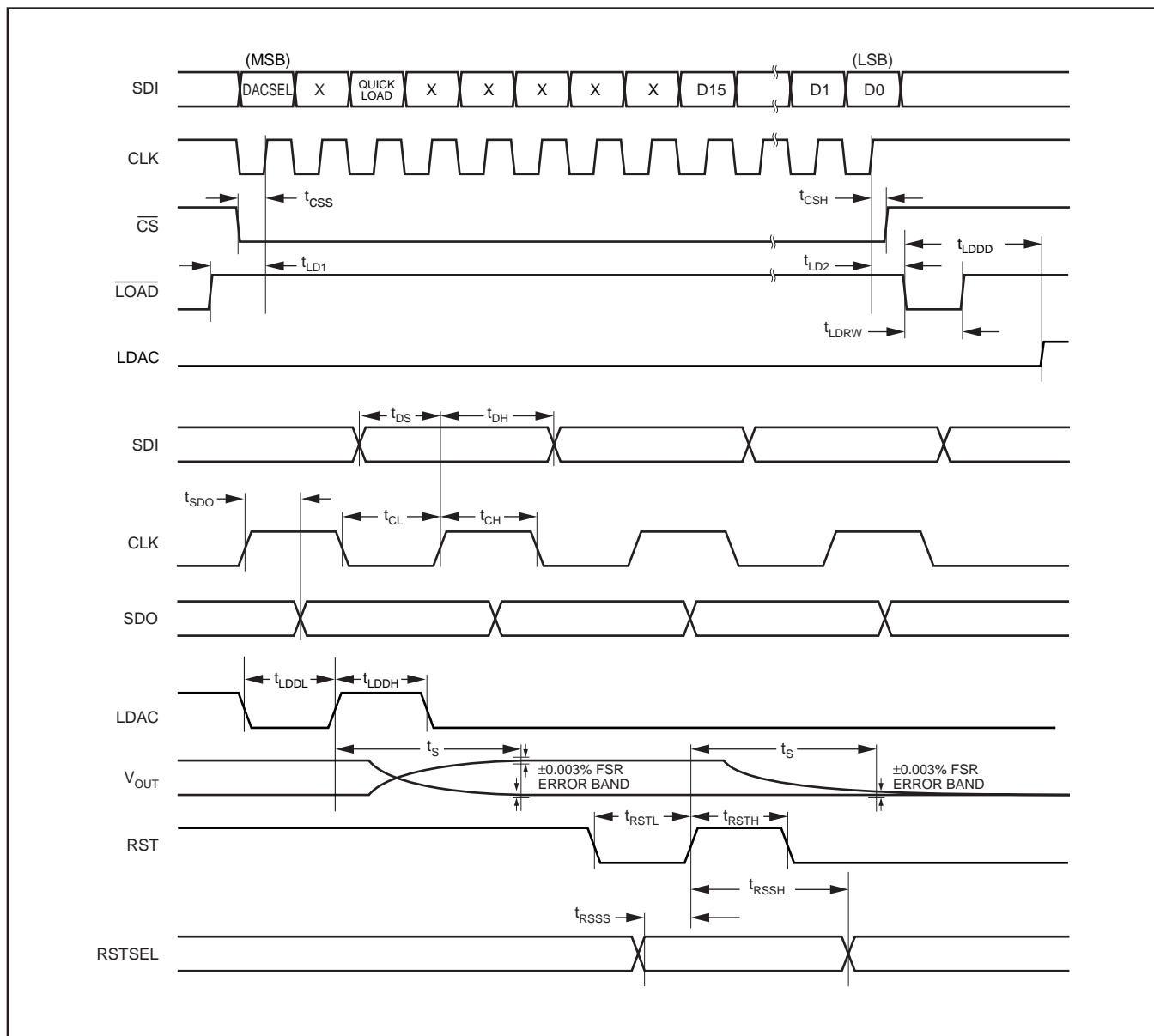


FIGURE 15. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{DS}	Data Valid to CLK Rising	10		ns
t_{DH}	Data Held Valid after CLK Rises	20		ns
t_{CH}	CLK HIGH	25		ns
t_{CL}	CLK LOW	25		ns
t_{CSS}	\overline{CS} LOW to CLK Rising	15		ns
t_{CSH}	CLK HIGH to \overline{CS} Rising	0		ns
t_{LD1}	\overline{LOAD} HIGH to CLK Rising	10		ns
t_{LD2}	CLK Rising to \overline{LOAD} LOW	30		ns
t_{LDRW}	\overline{LOAD} LOW Time	30		ns
t_{LDDL}	LDAC LOW Time	100		ns
t_{LDDH}	LDAC HIGH Time	100		ns
t_{LDD}	\overline{LOAD} LOW to LDAC Rising	40		ns
t_{RSS}	RESETSEL Valid to RESET HIGH	0		ns
t_{RSSH}	RESET HIGH to RESETSEL Not Valid	100		ns
t_{RSTL}	RESET LOW Time	10		ns
t_{RSTH}	RESET HIGH Time	10		ns
t_{SDO}	SDO Propagation Delay	10	30	ns
t_S	Settling Time		10	μ s

TABLE III. Timing Specifications ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$).

Figure 16 shows a DAC7632 in a 4-20mA current output configuration. The output current can be determined by Equation 3:

$$I_{OUT} = \left(\left(\frac{2.5V - 0.5V}{125\Omega} \right) \cdot \left(\frac{N}{65,536} \right) \right) + \left(\frac{0.5V}{125\Omega} \right)$$

At full-scale, the output current is 16mA, plus the 4mA, for the zero current. At zero scale the output current is the offset current of 4mA ($0.5V/125\Omega$).

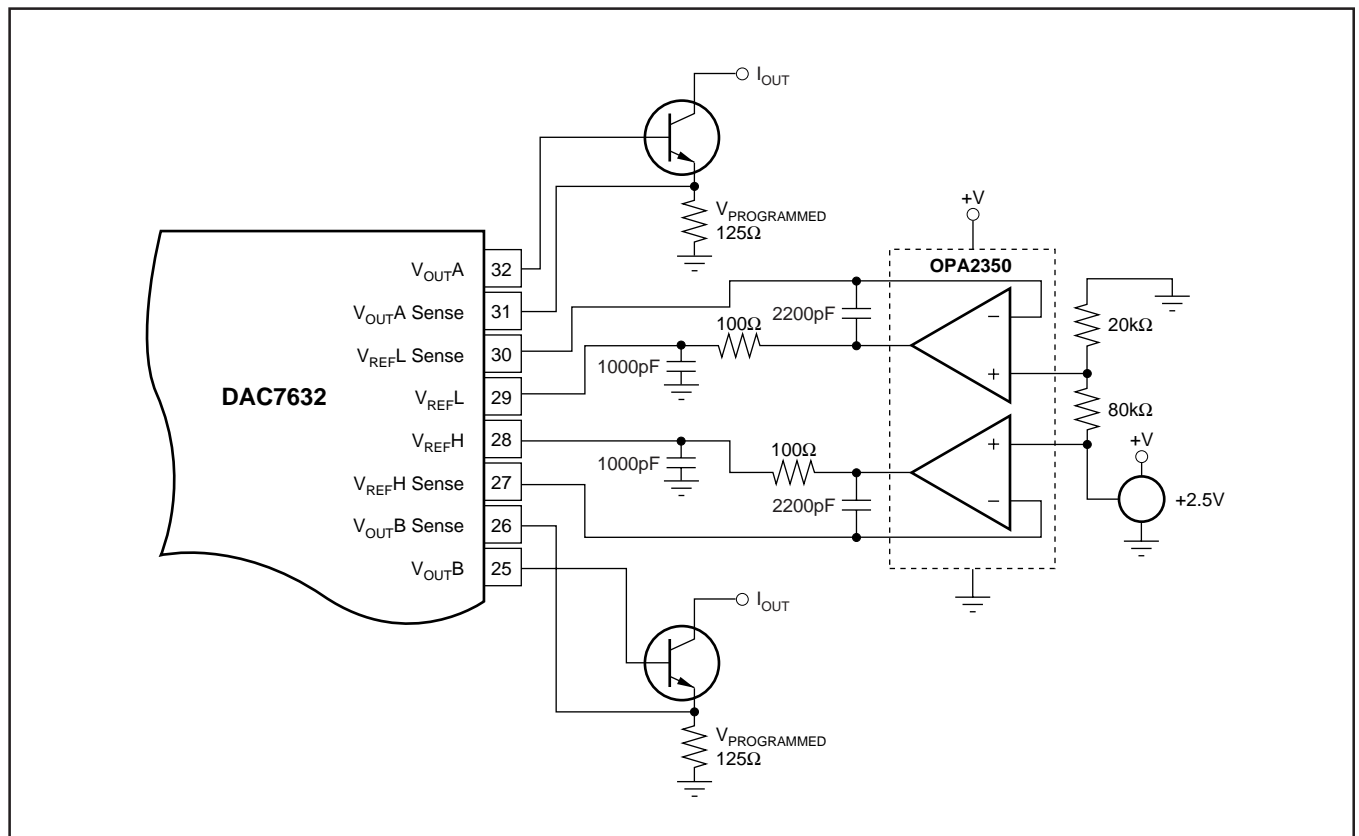
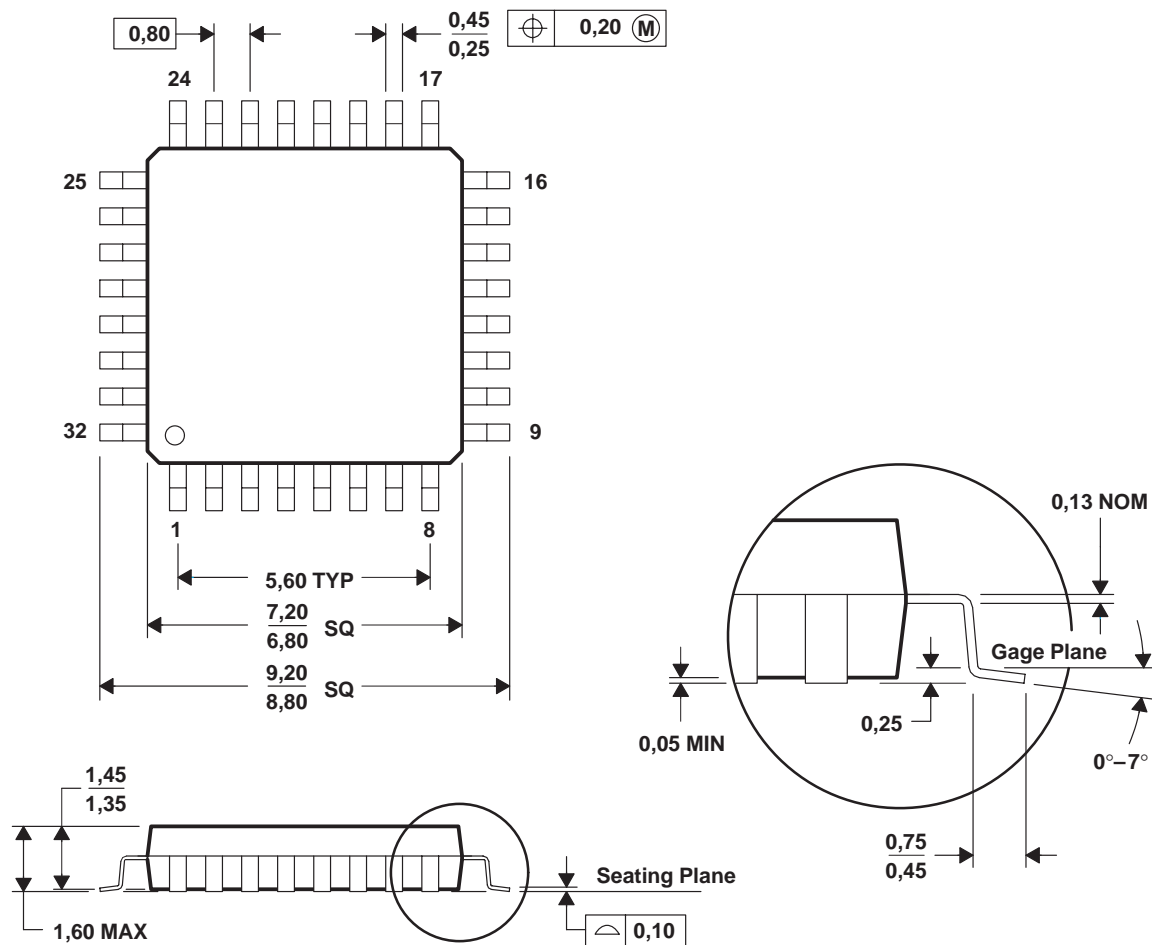


FIGURE 16. 4-20mA Digitally-Controlled Current Source.

VF (S-PQFP-G32)

PLASTIC QUAD FLATPACK



4040172/D 04/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC7632VFBR	ACTIVE	LQFP	VF	32	1000	TBD	CU NIPDAU	Level-3-235C-168 HR
DAC7632VFBT	ACTIVE	LQFP	VF	32	250	TBD	CU NIPDAU	Level-3-235C-168 HR
DAC7632VFR	ACTIVE	LQFP	VF	32	1000	TBD	CU NIPDAU	Level-3-235C-168 HR
DAC7632VFT	ACTIVE	LQFP	VF	32	250	TBD	CU NIPDAU	Level-3-235C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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