

## CMOS Dual J-K Master-Slave Flip-Flop

### High-Voltage Types (20-Volt Rating)

■ CD4027B is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and  $\bar{Q}$  signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013B dual D-type flip-flop.

The CD4027B is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.

The CD4027B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

#### MAXIMUM RATINGS, Absolute-Maximum Values:

##### DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )

Voltages referenced to  $V_{SS}$  Terminal) ..... -0.5V to +20V

##### INPUT VOLTAGE RANGE, ALL INPUTS

..... -0.5V to  $V_{DD}$  + 0.5V

##### DC INPUT CURRENT, ANY ONE INPUT

.....  $\pm 10$ mA

##### POWER DISSIPATION PER PACKAGE ( $P_D$ ):

For  $T_A = -55^\circ\text{C}$  to  $+100^\circ\text{C}$  ..... 500mW

For  $T_A = +100^\circ\text{C}$  to  $+125^\circ\text{C}$  ..... Derate Linearly at 12mW/ $^\circ\text{C}$  to 200mW

##### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR  $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$  ..... 100mW

##### OPERATING-TEMPERATURE RANGE ( $T_A$ )

.....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$

##### STORAGE TEMPERATURE RANGE ( $T_{stg}$ )

.....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

##### LEAD TEMPERATURE (DURING SOLDERING):

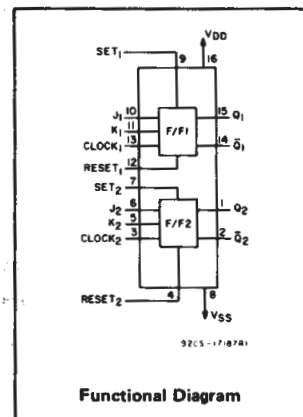
At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$ mm) from case for 10s max .....  $+265^\circ\text{C}$

#### Features:

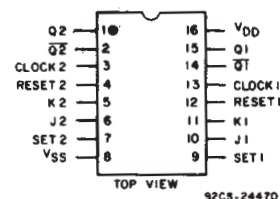
- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium speed operation — 16 MHz (typ.) clock toggle rate at 10 V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package-temperature range):
  - 1 V at  $V_{DD} = 5 \text{ V}$
  - 2 V at  $V_{DD} = 10 \text{ V}$
  - 2.5 V at  $V_{DD} = 15 \text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

#### Applications:

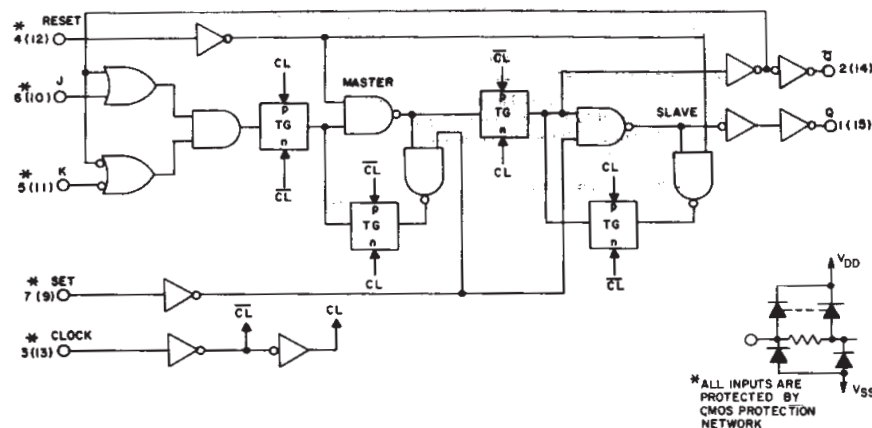
- Registers, counters, control circuits



Functional Diagram



TERMINAL ASSIGNMENT



PRESENT STATE					NEXT STATE	
J	K	S	R	Q	Q	$\bar{Q}$
1	x	0	0	0	1	0
x	0	0	0	1	1	0
0	x	0	0	0	0	1
x	1	0	0	1	0	1
x	x	0	0	x	← NO CHANGE	
x	x	1	0	x	1	0
x	x	0	1	x	0	1
x	x	1	1	x	1	1

LOGIC 1 = HIGH LEVEL  
LOGIC 0 = LOW LEVEL  
x = DON'T CARE

92CM-27551R1

Fig. 1 — Logic diagram and truth table for CD4027B (one of two identical J-K flip flops).

## CD4027B Types

**RECOMMENDED OPERATING CONDITIONS** at  $T_A = 25^\circ\text{C}$ , Except as Noted.  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS		UNITS
		All Packages		
		Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range)	—	3	18	V
Data Setup Time t <sub>S</sub>	5 10 15	200 75 50	— — —	ns
Clock Pulse Width t <sub>W</sub>	5 10 15	140 60 40	— — —	ns
Clock Input Frequency (Toggle Mode) f <sub>CL</sub>	5 10 15	dc	3.5 8 12	MHz
Clock Rise or Fall Time t <sub>rCL</sub> *, t <sub>fCL</sub>	5 10 15	— — —	45 5 2	μs
Set or Reset Pulse Width t <sub>W</sub>	5 10 15	180 80 50	— — —	ns

\* If more than one unit is cascaded in a parallel clocked operation,  $t_{rCL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

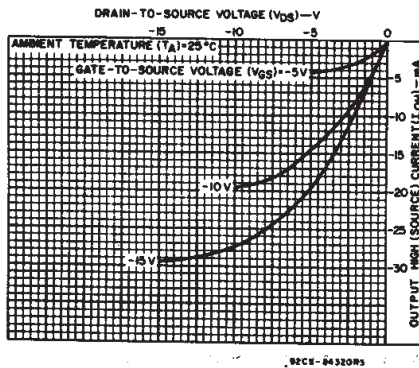


Fig. 4 - Typical output high (source) current characteristics.

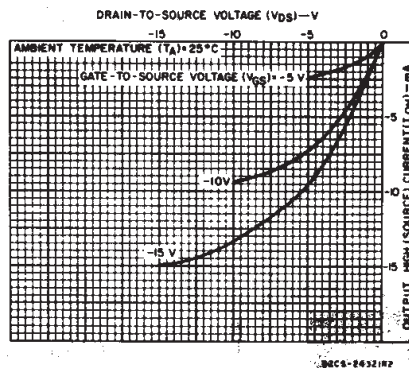


Fig. 5 - Minimum output high (source) current characteristics.

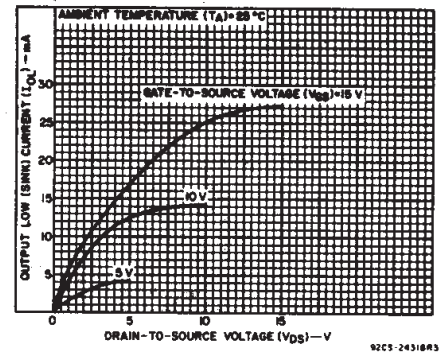


Fig. 2 - Typical output low (sink) current characteristics.

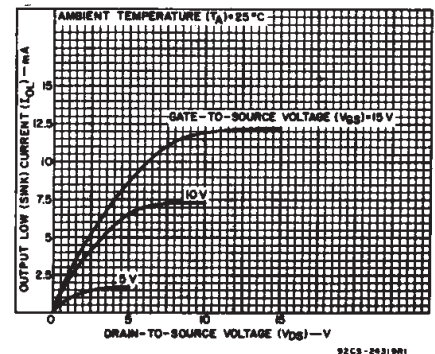


Fig. 3 - Minimum output low (sink) current characteristics.

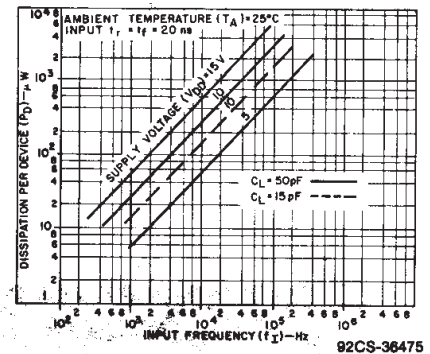


Fig. 6 - Typical power dissipation vs. frequency.

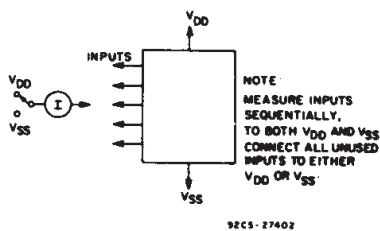


Fig. 7 - Input current test circuit.

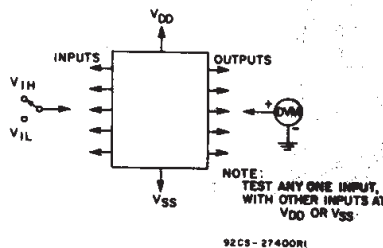


Fig. 8 - Input-voltage test circuit.

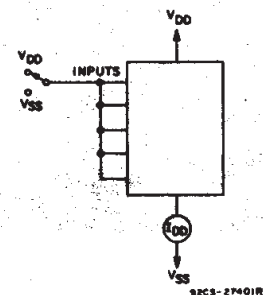
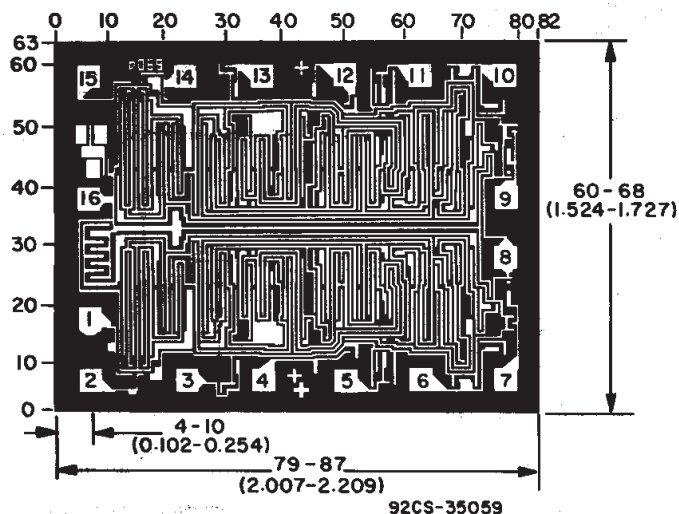


Fig. 9 - Quiescent device current test circuit.

## CD4027B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	—	0,5	5	1	1	30	30	—	0.02	1	μA	
	—	0,10	10	2	2	60	60	—	0.02	2		
	—	0,15	15	4	4	120	120	—	0.02	4		
	—	0,20	20	20	20	600	600	—	0.04	20		
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—		
	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—		
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
Output High (Source) Current, I <sub>OH</sub> Min.	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
	Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0,5	5	0.05				—	0	0.05	V
		—	0,10	10	0.05				—	0	0.05	
—		0,15	15	0.05				—	0	0.05		
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0,5	5	4.95				4.95	5	—	V	
	—	0,10	10	9.95				9.95	10	—		
	—	0,15	15	14.95				14.95	15	—		
Input Low Voltage, V <sub>IL</sub> Max.	0.5,4.5	—	5	1.5				—	—	1.5	V	
	1,9	—	10	3				—	—	3		
	1.5,13.5	—	15	4				—	—	4		
Input High Voltage, V <sub>IH</sub> Min.	0.5,4.5	—	5	3.5				3.5	—	—	V	
	1,9	—	10	7				7	—	—		
	1.5,13.5	—	15	11				11	—	—		
Input Current, I <sub>IN</sub> Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA	



Dimensions in millimeters are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$ ).

Dimensions and Pad Layout for CD4027BH

## CD4027B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS			UNITS
		All Packages			
		Min.	Typ.	Max.	
Propagation Delay Time: Clock to Q or $\bar{Q}$ Outputs $t_{PHL}, t_{PLH}$	5 10 15	— — —	150 65 45	300 130 90	ns
Set to Q or Reset to $\bar{Q}$ $t_{PLH}$	5 10 15	— — —	150 65 45	300 130 90	ns
Set to $\bar{Q}$ or Reset to Q $t_{PHL}$	5 10 15	— — —	200 85 60	400 170 120	ns
Transition Time $t_{THL}, t_{TLH}$	5 10 15	— — —	100 50 40	200 100 80	ns
Maximum Clock Input Frequency# (Toggle Mode) $f_{CL}$	5 10 15	3.5 8 12	7 16 24	— — —	MHz
Minimum Clock Pulse Width $t_W$	5 10 15	— — —	70 30 20	140 60 40	ns
Minimum Set or Reset Pulse Width $t_W$	5 10 15	— — —	90 40 25	180 80 50	ns
Minimum Data Setup Time $t_S$	5 10 15	— — —	100 35 25	200 75 50	ns
Clock Input Rise or Fall Time $t_{rCL}, t_{fCL}$	5 10 15	— — —	— — —	45 5 2	$\mu$ s
Input Capacitance $C_i$		—	5	7.5	pF

# Input  $t_r, t_f = 5\text{ ns}$ .

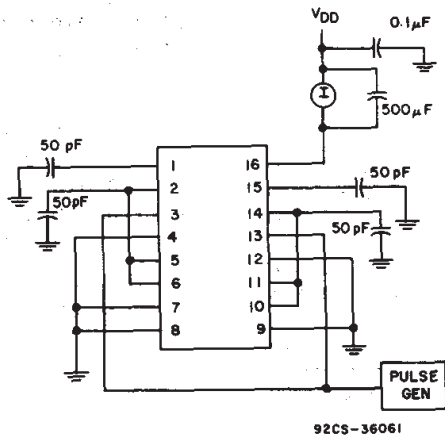


Fig. 13—Dynamic power dissipation test circuit.

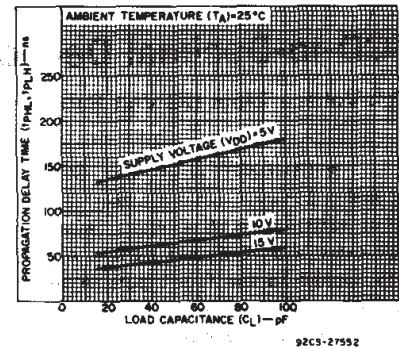


Fig. 10—Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to  $\bar{Q}$ ).

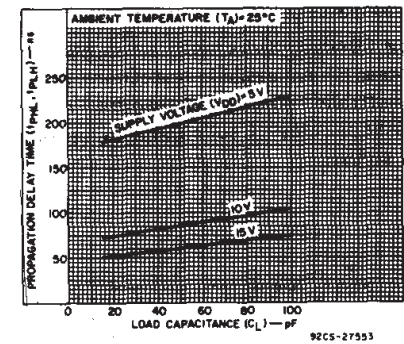


Fig. 11—Typical propagation delay time vs. load capacitance (SET to Q or RESET to Q).

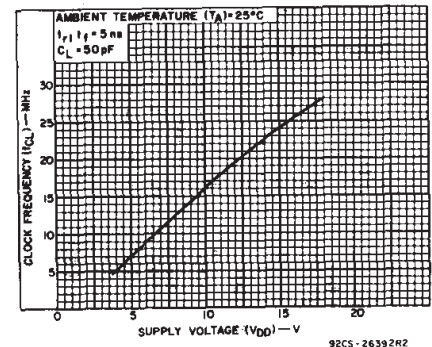


Fig. 12—Typical maximum clock frequency vs. supply voltage (toggle mode).

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4027BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4027BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4027BF	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4027BF3A	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
CD4027BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4027BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
JM38510/05152BEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

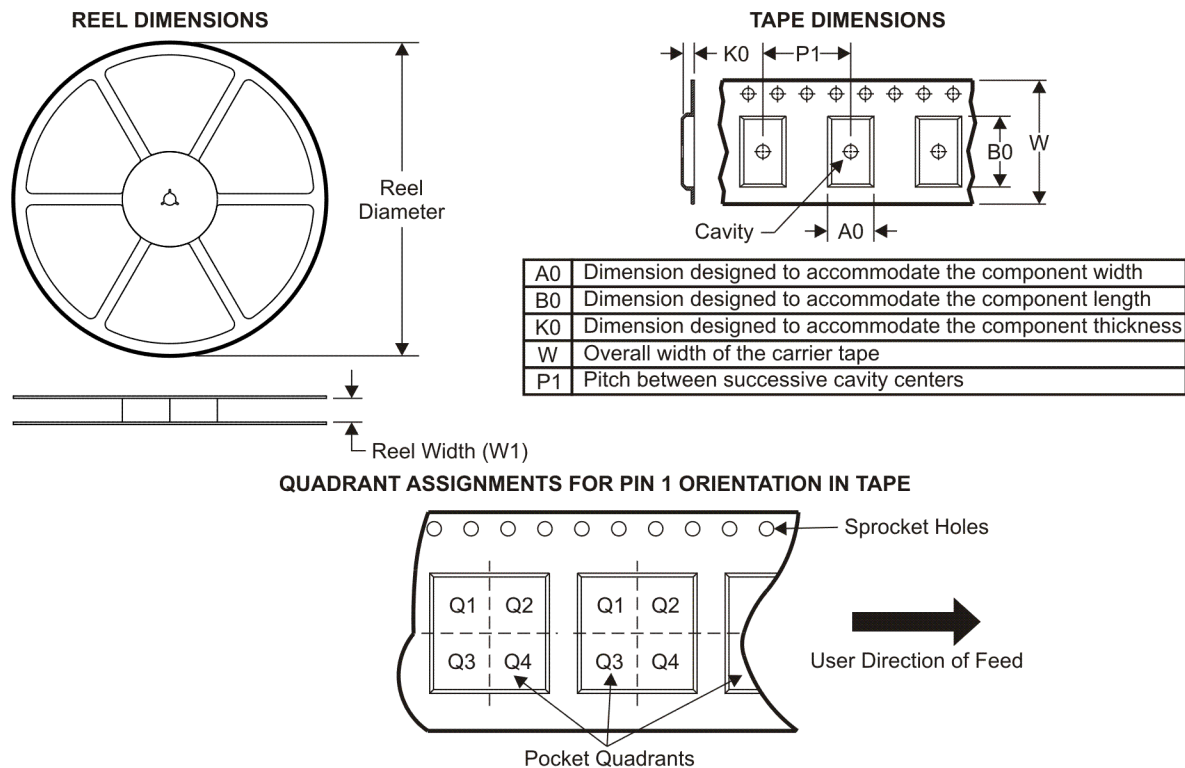
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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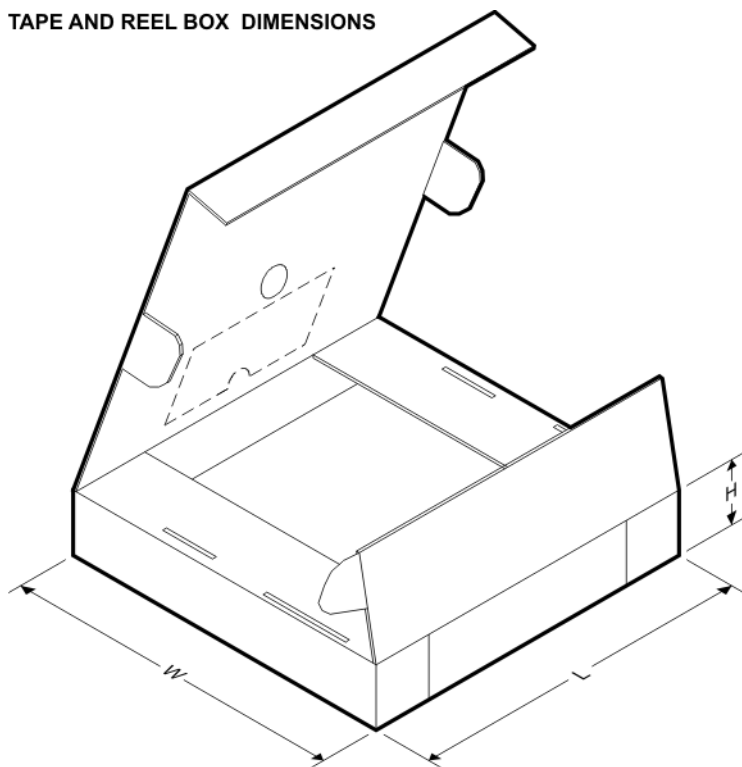
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4027BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4027BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4027BPWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

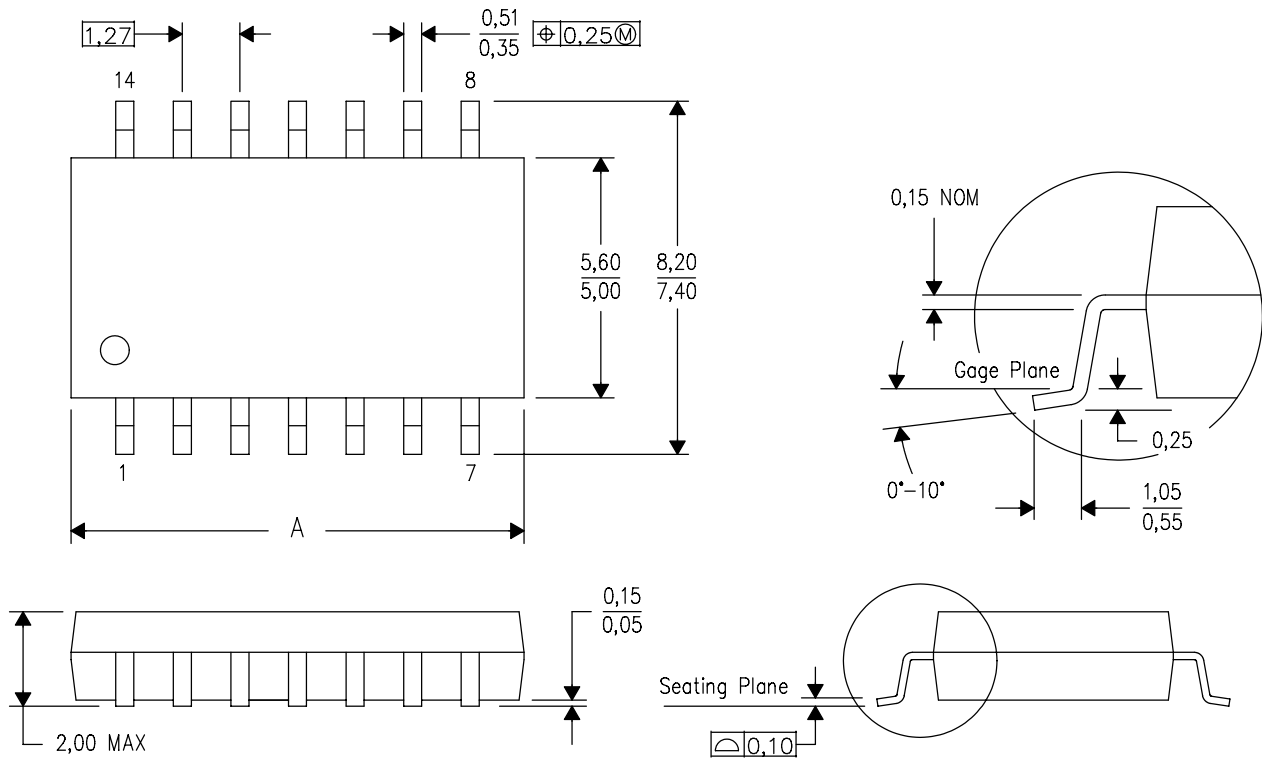
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4027BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4027BNSR	SO	NS	16	2000	346.0	346.0	33.0
CD4027BPWR	TSSOP	PW	16	2000	346.0	346.0	29.0

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



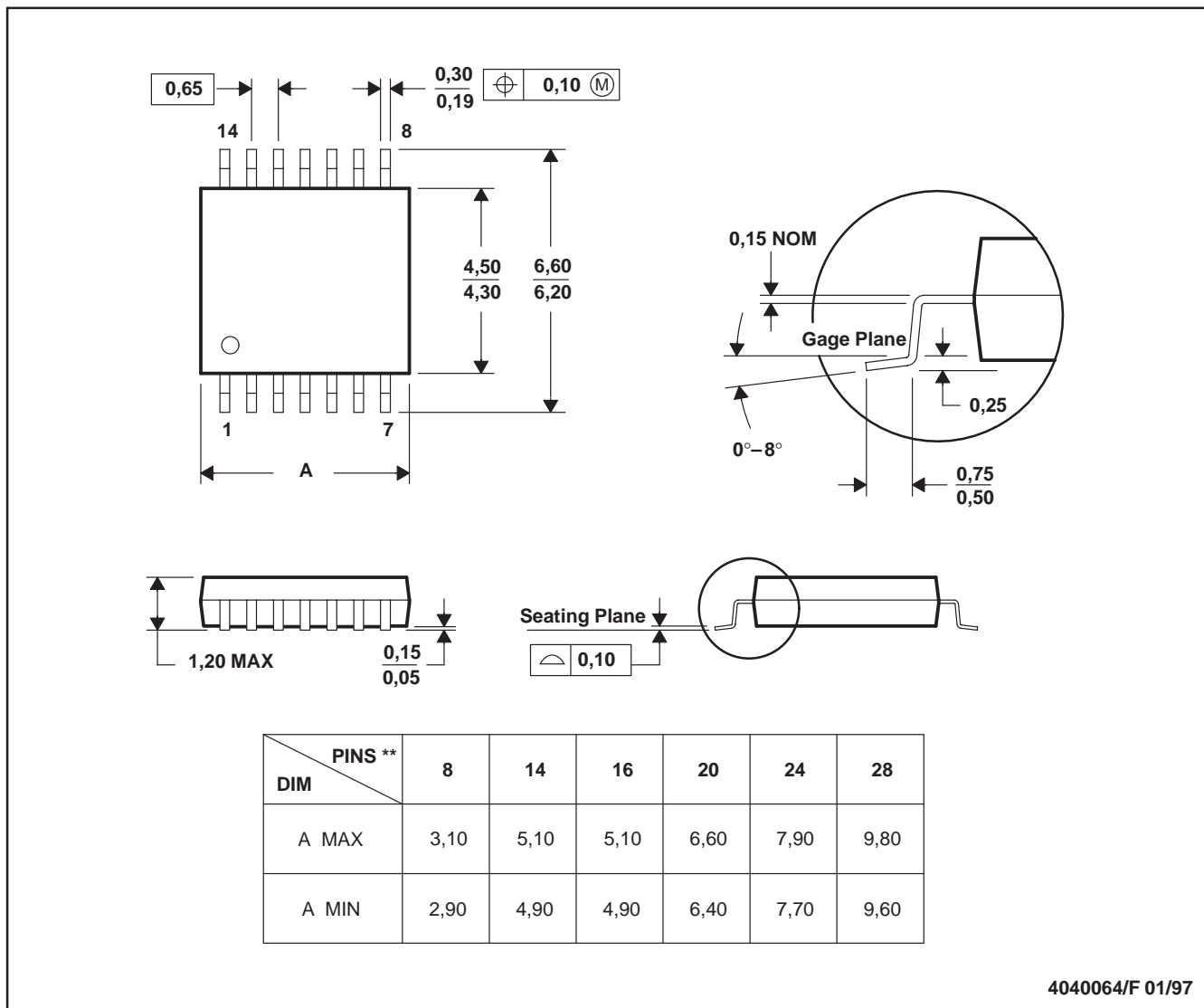
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

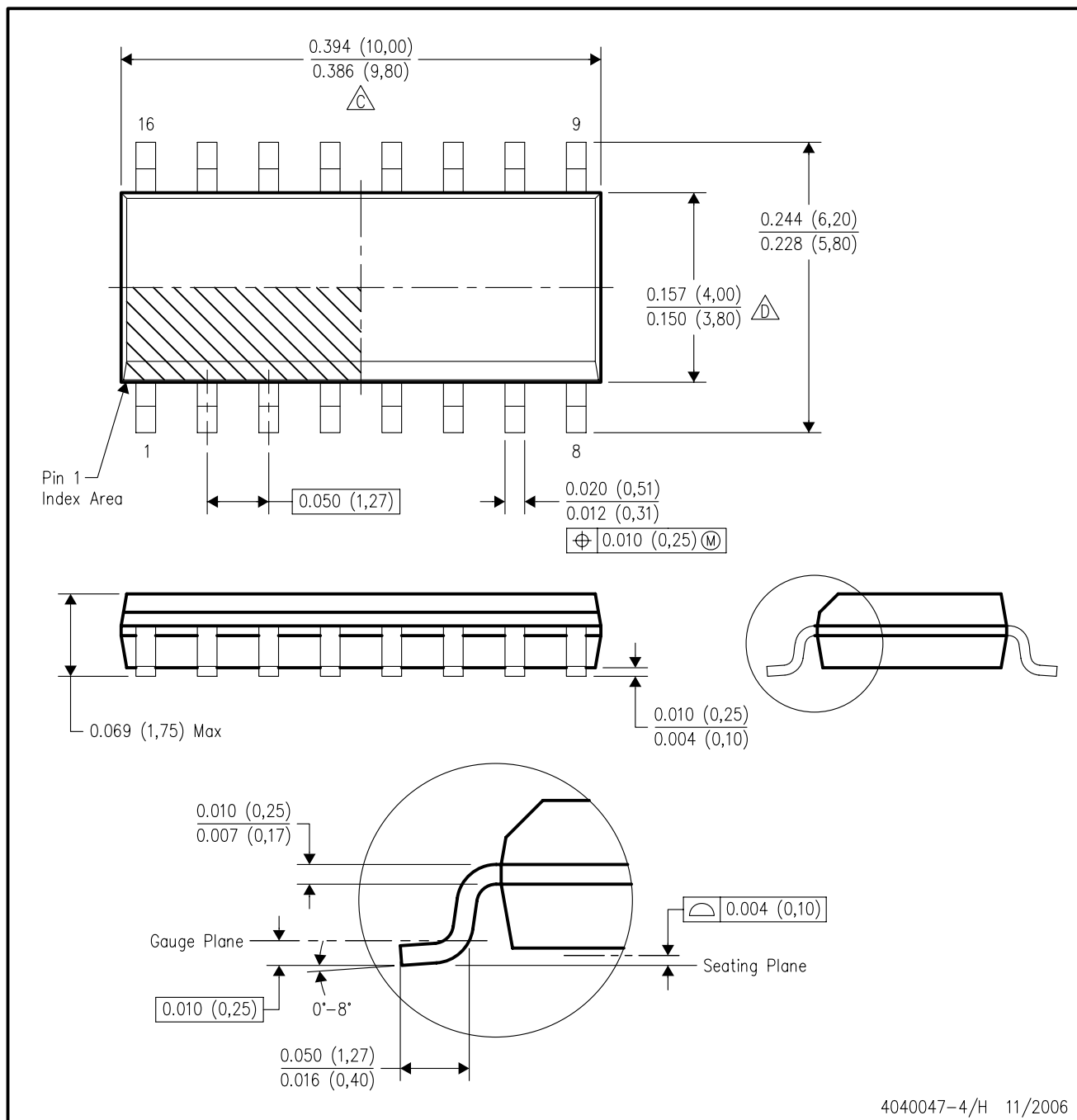
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

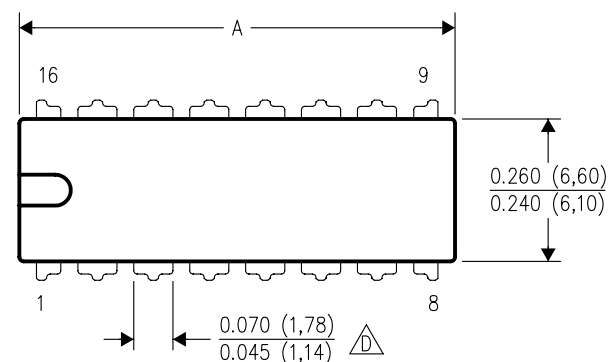
## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

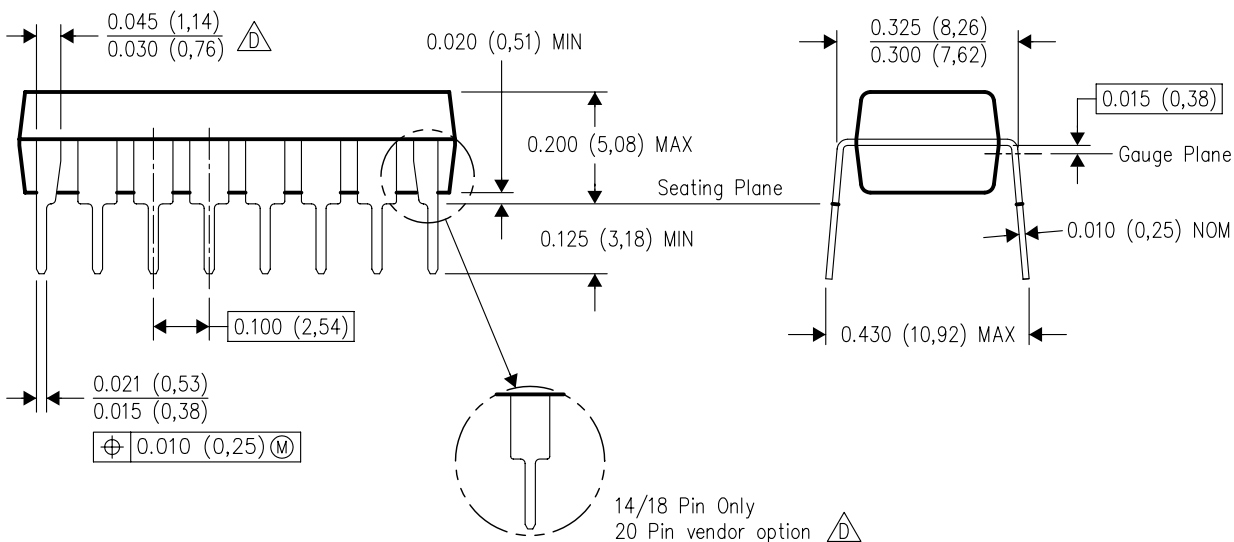
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE





PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.