1.2A USB-FRIENDLY Li-Ion BATTERY CHARGER AND POWER-PATH MANAGEMENT IC

FEATURES

- 28V Input Rating
- Integrated Dynamic Power Management Feature
- Supports up to 1.5A Output Current
- Integrated USB Charge Control With Selectable 100 mA and 500 mA Maximum Input Current
- Programmable Pre-Charge and Fast-Charge Safety Timers
- Thermal Regulation for Charge Control
- Reverse Current, Short-Circuit and Thermal Protection
- NTC Thermistor Input
- Soft-Start Feature to Reduce Inrush Current
- Status Indication – Charging/Done, Power Good
- Small 3 mm × 3 mm 16 Lead QFN Package

APPLICATIONS

- Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

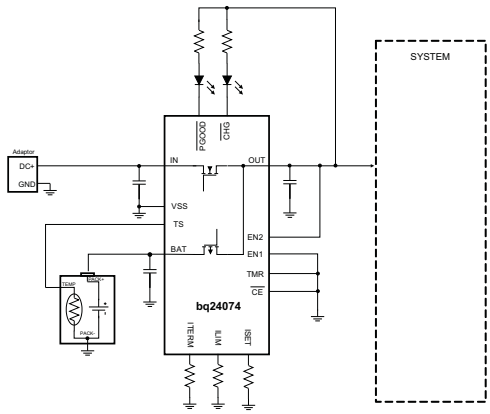
DESCRIPTION

The bq2407x series of devices are highly integrated Li-ion linear chargers and system power path management devices targeted at space-limited portable applications. The devices operate from either a USB port or AC adapter. The high input voltage range with input overvoltage protection supports low-cost unregulated adapters.

The bq2407x powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turn-on even with a totally discharged battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents, enabling the use of a smaller adapter.

The battery is charged in three phases: conditioning, constant current, and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if the internal temperature threshold is exceeded.

TYPICAL APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination. The input current limit and charge current are programmable using external resistors.

ORDERING INFORMATION

PART NUMBER (1)(2)	V_{OVP}	$V_{OUT(REG)}$	V_{DPM}	OPTIONAL FUNCTION	MARKING
bq24072RGTR	6.6 V	V_{BAT} + 200 mV	$V_{O(REG)}$ – 100 mV	TD	CKP
bq24072RGTT	6.6 V	V_{BAT} + 200 mV	$V_{O(REG)}$ – 100 mV	TD	CKP
bq24073RGTR	6.6 V	4.4 V	$V_{O(REG)}$ – 100 mV	TD	CKQ
bq24073RGTT	6.6 V	4.4 V	$V_{O(REG)}$ – 100 mV	TD	CKQ
bq24074RGTR	10.5 V	4.4 V	$V_{O(REG)}$ – 100 mV	ITERM	BZF
bq24074RGTT	10.5 V	4.4 V	$V_{O(REG)}$ – 100 mV	ITERM	BZF
bq24075RGTR	6.6 V	5.5 V	4.3 V	SYSOFF	CDU
bq24075RGTT	6.6 V	5.5 V	4.3 V	SYSOFF	CDU

(1) The RGT package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_I	Input Voltage	IN (with respect to VSS)	–0.3 to 28	V
		BAT (with respect to VSS)	–0.3 to 5	V
		OUT, EN1, EN2, $\overline{CE}$, TS, ISET, $\overline{PGOOD}$, $\overline{CHG}$, ILIM, TMR, ITERM, SYSOFF, TD (with respect to VSS)	–0.3 to 7	V
I_I	Input Current	IN	1.6	A
I_O	Output Current (Continuous)	OUT	5	A
		BAT (Discharge mode)	5	A
	Output Sink Current	$\overline{CHG}$, $\overline{PGOOD}$	15	mA
T_J	Junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS(1)

PACKAGE(2)	$R_{\theta JA}$	$R_{\theta JC}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR $T_A > 25°C$
RGT (1)	39.47 °C/W	2.4 °C/W	2.3 W	34.6 mW/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_I	IN voltage range		4.35	26	V
	IN operating voltage range	'72, '73, '75	4.35	6.6	V
		'74	4.35	10.5	
I_{IN}	Input current, IN pin			1.5	A
I_{OUT}	Current, OUT pin			4.5	A
I_{BAT}	Current, BAT pin (Discharging)			4.5	A
I_{CHG}	Current, BAT pin (Charging)			1.2	A
T_J	Junction Temperature		–40	125	°C
R_{ILIM}	Maximum input current programming resistor		1100	8000	Ω
R_{ISET}	Fast-charge current programming resistor		750	3000	Ω
R_{ITERM}	Termination current programming resistor		0	15	kΩ
R_{TMR}	Timer programming resistor		18	72	kΩ

ELECTRICAL CHARACTERISTICS

Over junction temperature range (0° ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
UVLO	Undervoltage lock-out	V_{IN}: 0 V → 4 V	3.2	3.3	3.4	V
V_{hys}	Hysteresis on UVLO	V_{IN}: 4 V → 0 V	200		300	mV
$V_{IN(DT)}$	Input power detection threshold	Input power detected when $V_{IN} > V_{BAT} + V_{IN(DT)}$ V_{BAT} = 3.6 V, VIN: 3.5 V → 4 V	55	80	130	mV
V_{hys}	Hysteresis on $V_{IN(DT)}$	V_{BAT} = 3.6 V, V_{IN}: 4 V → 3.5 V	20			mV
$t_{DGL(PGOOD)}$	Deglitch time, input power detected status	Time measured from V_{IN}: 0 V → 5 V 1 µs rise-time to $\overline{PGOOD}$ = LO		4		ms
V_{OVP}	Input overvoltage protection threshold	('72, '73, '75) V_{IN}: 5 V → 7 V	6.4	6.6	6.8	V
		('74) V_{IN}: 5 V → 11 V	10.2	10.5	10.8	
V_{hys}	Hysteresis on OVP	('72, '73, '75) V_{IN}: 7 V → 5V		110		mV
		('74) V_{IN}: 11 V → 5 V		175		
t_{BLK}	Input overvoltage blanking time			50		µs
t_{REC}	Input overvoltage recovery time	Time measured from V_{IN}: 11 V → 5 V with 1 µs fall-time to $\overline{PGOOD}$ = LO		2		ms
ILIM, TEST ISET SHORT CIRCUIT						
I_{SC}	Current source			1.3		mA
V_{SC}				520		mV
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Sleep current into BAT pin	$\overline{CE}$ = LO or HI, input power not detected, No load on OUT pin, T_J = 85°C			6.5	µA
I_{IN}	Standby current into IN pin	EN1= HI, EN2=HI, V_{IN} = 6 V, T_J=85°C			50	µA
		EN1= HI, EN2=HI, V_{IN} = 10 V, T_J=85°C			200	
I_{CC}	Active supply current, IN pin	$\overline{CE}$ = LO, V_{IN} = 6 V, no load on OUT pin, $V_{BAT} > V_{BAT(REG)}$, (EN1, EN2) ≠ (HI, HI)			1.5	mA
POWER PATH						
$V_{DO(IN-OUT)}$	$V_{IN} - V_{OUT}$	V_{IN} = 4.3 V, I_{IN} = 1A, V_{BAT} = 4.2V		300	475	mV
$V_{DO(BAT-OUT)}$	$V_{BAT} - V_{OUT}$	I_{OUT} = 1 A, V_{IN} = 0 V, V_{BAT} > 3 V		50	100	mV
$V_{O(REG)}$	OUT pin voltage regulation (bq24072)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$, V_{BAT} < 3.2 V		3.4		V
		$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$, $V_{BAT} \geq$ 3.2 V		V_{BAT} + 225mV		
	OUT pin voltage regulation (bq24073, bq24074)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	4.3	4.4	4.5	
	OUT pin voltage regulation (bq24075)	$V_{IN} > V_{OUT} + V_{DO(IN-OUT)}$	5.4	5.5	5.6	

ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range (0° ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IN}max	Maximum input current	EN1 = LO, EN2 = LO	90	95	100	mA
		EN1 = HI, EN2 = LO	450	475	500	
		EN2 = HI, EN1 = LO		K_{ILIM}/R_{ILIM}		A
K_{ILIM}	Maximum input current factor	I_{LIM} ≥ 500mA	1480	1550	1620	AΩ
		200mA < I_{LIM} < 500mA	1320	1470	1620	
I_{IN}max	Programmable input current limit range	EN2 = HI, EN1 = LO, R_{ILIM} = 8 kΩ to 1.1 kΩ	200		1500	mA
$V_{IN(LOW)}$	Input voltage threshold when input current is reduced	EN2 = LO, EN1 = X	4.35	4.5	4.63	V
V_{DPM}	Output voltage threshold when charging current is reduced	('72, '73, '74)		$V_{O(REG)}$ – 100mV		V
		('75)		4.3		V
V_{BSUP1}	Enter battery supplement mode			$V_{OUT} \le V_{BAT}$ –40		mV
V_{BSUP2}	Exit battery supplement mode			$V_{OUT} \ge V_{BAT}$–20		mV
$V_{O(SC1)}$	Output short-circuit detection threshold, power-on		0.8	0.9	1	V
$V_{O(SC2)}$	Output short-circuit detection threshold, supplement mode V_{BAT} – V_{OUT} > $V_{O(SC2)}$ indicates short-circuit		200	250	300	mV
$t_{DGL(SC2)}$	Deglitch time, supplement mode short circuit			250		µs
$t_{REC(SC2)}$	Recovery time, supplement mode short circuit			60		ms
BATTERY CHARGER						
I_{BAT}	Source current for BAT pin short-circuit detection		4	7.5	11	mA
V_{BAT}	BAT pin short-circuit detection threshold		1.6	1.8	2.0	V
$V_{BAT(REG)}$	Battery charge voltage		4.16	4.20	4.24	V
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.9	3	3.1	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I_{CHG}	Battery fast charge current range	$V_{BAT(REG)}$ > V_{BAT} > V_{LOWV}, V_{IN} = 5 V $\overline{CE}$ = LO, EN1 = LO, EN2 = HI	300		1200	mA
	Battery fast charge current	$\overline{CE}$ = LO, EN1= LO, EN2 = HI, V_{BAT} > V_{LOWV}, V_{IN} = 5 V, I_{IN}max > I_{CHG}, no load on OUT pin, thermal loop and DPM loop not active		K_{ISET}/R_{ISET}		A
K_{ISET}	Fast charge current factor		797	890	975	AΩ
I_{PRECHG}	Pre-charge current			K_{PRECHG}/R_{ISET}		A
K_{PRECHG}	Pre-charge current factor		70	88	106	AΩ
I_{TERM}	Termination comparator detection threshold (internally set)	$\overline{CE}$ = LO, (EN1, EN2) ≠ (LO, LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.09×I_{CHG}	0.1×I_{CHG}	0.11×I_{CHG}	A
		$\overline{CE}$ = LO, (EN1, EN2) = (LO, LO), V_{BAT} > V_{RCH}, t < t_{MAXCH}, V_{IN} = 5 V, DPM loop and thermal loop not active	0.027×I_{CHG}	0.033×I_{CHG}	0.040×I_{CHG}	
$I_{BIAS(ITERM)}$	Current for external termination-setting resistor		72	75	78	µA
I_{TERM}	Termination current threshold (externally set) (bq24074)			$K_{ITERM} \times R_{ITERM} / R_{ISET}$		A

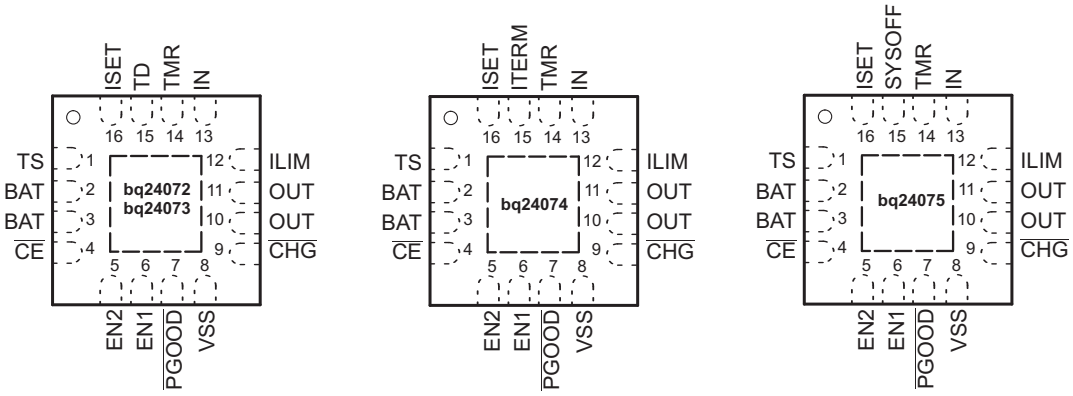
ELECTRICAL CHARACTERISTICS (continued)

Over junction temperature range (0° ≤ T_J ≤ 125°C) and the recommended supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{ITERM}	K Factor for termination detection threshold (externally set) (bq24074)	$\overline{CE}$ = LO, (EN1, EN2) ≠ (LO, LO), $V_{BAT} > V_{RCH}$, $t < t_{MAXCH}$, V_{IN} = 5 V, DPM loop and thermal loop not active	0.008	0.0100	0.012	A
		$\overline{CE}$ = LO, (EN1, EN2) = (LO, LO), $V_{BAT} > V_{RCH}$, $t < t_{MAXCH}$, V_{IN} = 5 V, DPM loop and thermal loop not active	0.0225	0.0300	0.0375	
$t_{DGL(TERM)}$	Deglitch time, termination detected		0	25		ms
V_{RCH}	Recharge detection threshold		$V_{BAT(REG)}$ –140	$V_{BAT(REG)}$ –100	$V_{BAT(REG)}$ –60	mV
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected			62.5		ms
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turn-off	V_{BAT} = 3.6 V. Time measured from V_{IN}: 5 V → 3 V 1 µs fall-time		20		ms
$I_{BAT(DET)}$	Sink current for battery detection		5	7.5	10	mA
t_{DET}	Battery detection timer			250		ms
BATTERY CHARGING TIMERS						
t_{PRECHG}	Pre-charge safety timer value	TMR = floating	1440	1800	2160	s
t_{MAXCHG}	Charge safety timer value	TMR = floating	14400	18000	21600	s
t_{PRECHG}	Pre-charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		$R_{TMR} \times K_{TMR}$		s
t_{MAXCHG}	Charge safety timer value	18 kΩ < R_{TMR} < 72 kΩ		10×RTMR ×K_{TMR}		s
K_{TMR}	Timer factor		36	48	60	s/kΩ
BATTERY-PACK NTC MONITOR(1)						
I_{NTC}	NTC bias current		72	75	78	µA
V_{HOT}	High temperature trip point	Battery charging	270	300	330	mV
$V_{HYS(HOT)}$	Hysteresis on high trip point	Battery charging		30		mV
V_{COLD}	Low temperature trip point	Battery charging	2000	2100	2200	mV
$V_{HYS(COLD)}$	Hysteresis on low trip point	Battery charging		300		mV
$t_{DGL(TS)}$	Deglitch time, pack temperature fault detection	Battery charging		50		ms
$V_{DIS(TS)}$	TS function disable threshold (bq24072, bq24073)			V_{IN} - 200mV		V
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit			125		°C
$T_{J(OFF)}$	Thermal shutdown temperature			155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON EN1, EN2, $\overline{CE}$, SYSOFF, TD						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6	V
I_{IL}		V_{IL}= 0V			1	µA
I_{IH}		V_{IH}= 1.4V			10	µA
LOGIC LEVELS ON $\overline{PGOOD}$, $\overline{CHG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5 mA			0.4	V

(1) These numbers set trip points of 0°C and 50°C while charging, with 3°C hysteresis on the trip points, with a Vishay Type 2 curve NTC with an R25 of 10 kΩ.

RGT PACKAGE
(Top View)



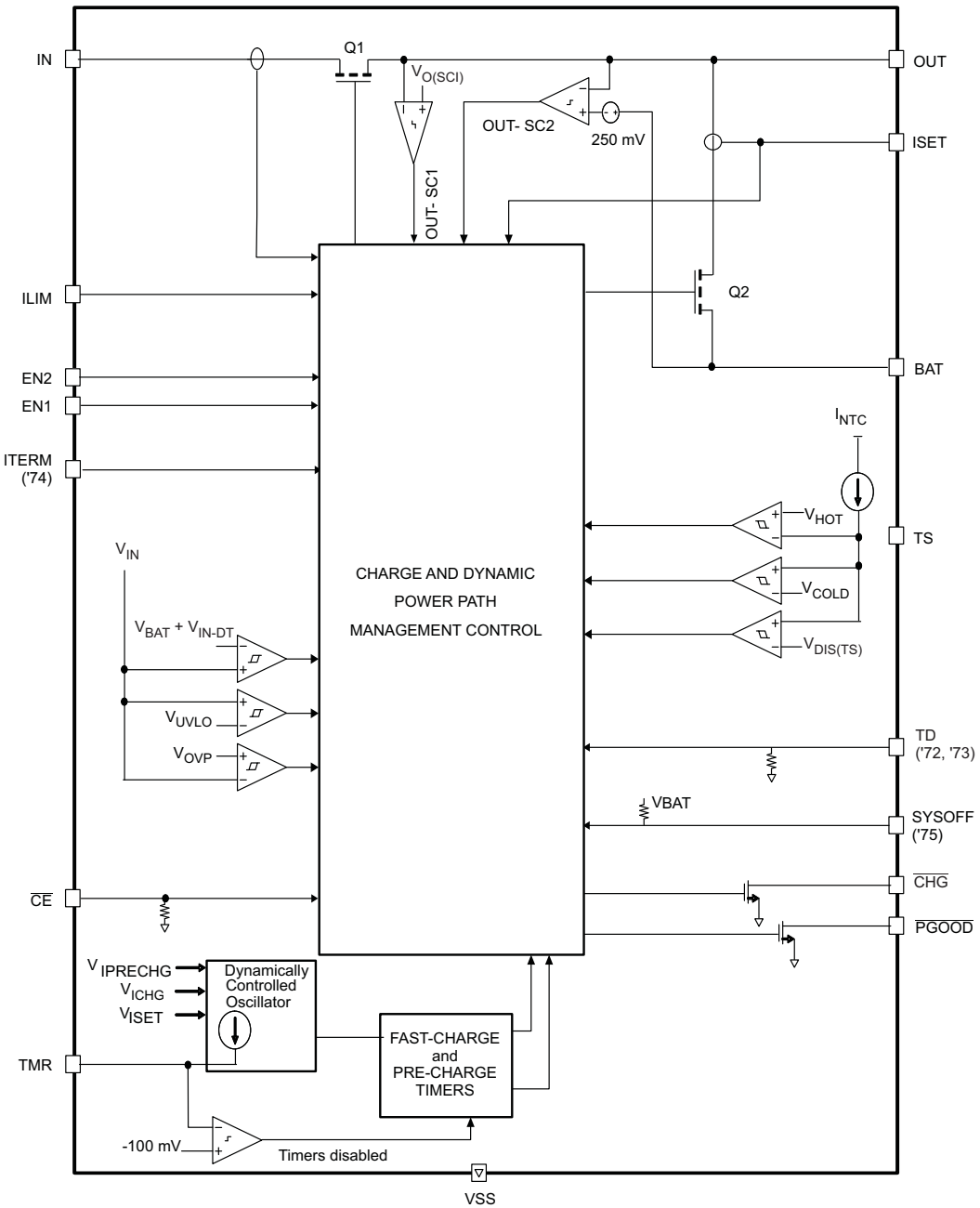
TERMINAL FUNCTIONS

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	'72, '73	'74	'75		
TS	1	1	1	I	External NTC Thermistor Input. Connect the TS input to the NTC thermistor in the battery pack. TS moniitors a 10kΩ NTC thermistor.To disable the external temperature sense circuitry, connect a 10kΩ resistor from TS to VSS.
BAT	2, 3	2, 3	2, 3	I/O	Charger Power Stage Output and Battery Voltage Sense Input. Connect BAT to the positive terminal of the battery. Bypass BAT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
$\overline{CE}$	4	4	4	I	Charge Enable Active-Low Input. Connect $\overline{CE}$ to a high logic level to place the battery charger in standby mode. In standby mode, OUT is active. Connect $\overline{CE}$ to a low logic level to enable the battery charger. $\overline{CE}$ is internally pulled down with ~285 kΩ.
EN2	5	5	5	I	Input Current Limit Configuration Inputs. Use EN1 and EN2 control the maximum input current and enable USB compliance. See Table 2 for the description of the operation states. EN1 and EN2 are internally pulled down with ~285 kΩ.
EN1	6	6	6	I	
$\overline{PGOOD}$	7	7	7	O	Open-drain Power Good Status Indication Output. $\overline{PGOOD}$ pulls to VSS when a valid input source is detected. $\overline{PGOOD}$ is high-impedance when the input power is not within specified limits. Connect $\overline{PGOOD}$ to the desired logic voltage rail using a 10kΩ-100kΩ resistor.
VSS	8	8	8	–	Ground. Connect to the thermal pad and to the ground rail of the circuit.
$\overline{CHG}$	9	9	9	O	Open-Drain Charging Status Indication Output. $\overline{CHG}$ pulls to VSS when the battery is charging. $\overline{CHG}$ is high impedance when charging is complete and when charger is disabled.
OUT	10, 11	10, 11	10, 11	O	System Supply Output. OUT provides a regulated output when the input is below the OVP threshold and above the regulation voltage. Connect OUT to the system load. Bypass OUT to VSS with a 4.7 µF to 47 µF ceramic capacitor.
ILIM	12	12	12	I	Adjustable Current Limit Programming Input. Connect a 1100 Ω to 8 kΩ resistor from ILIM to VSS to program the maximum input current (EN2=1, EN1=0). The input current includes the system load and the battery charge current.
IN	13	13	13	I	Input Power Connection. Connect IN to the connected to external DC supply (AC adapter or USB port). The input operating range is 4.35V to 6.6V (bq24072, bq24073, and bq24075) or 4.35V to 10.5V (bq23074). The input can accept voltages up to 26V without damage but operation is suspended. Connect bypass capacitor 1 µF to 10 µF to VSS.
TMR	14	14	14	I	Timer Programming Input. TMR controls the pre-charge and fast-charge safety timers. Connect TMR to VSS to disable all timers. Connect a 18 kΩ to 72 kΩ resistor between TMR and VSS to program the timers a desired length. Leave TMR unconnected to set the timers to the default values.
TD	15	–	–	I	Termination Enable Input. Connect TD to VSS to enable charger termination. Connect TD high to disable charger termination. See the TD section in this datasheet for a description of the behavior when termination is disabled. TD is internally pulled down to VSS with ~285 kΩ.
ITERM	–	15	–	I	Termination Current Programming Input. Connect a 0 Ω to 15 kΩ resistor from ITERM to VSS to program the termination current. Leave ITERM unconnected to set the termination current to the internal default value.
SYSOFF	–	–	15	I	System Enable Input. Connect SYSOFF high to disconnect OUT from the input power when . Internally pulled up to V_{BAT} through a large resistor (~5 MΩ).
ISET	16	16	16	I/O	Fast Charge Current Programming Input. Connect a 750 Ω to 3 kΩ resistor from ISET to VSS to program the fast charge current level.
Thermal Pad				–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

Table 1. EN1/EN2 Settings

EN2	EN1	Maximum input current into IN pin
0	0	100 mA. USB100 mode
0	1	500 mA. USB500 mode
1	0	Set by an external resistor from ILIM to VSS
1	1	Standby (USB suspend mode)

SIMPLIFIED BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

**ADAPTER REMOVAL
BATTERY CONNECTED
R_{OUT} = 6.6Ω**

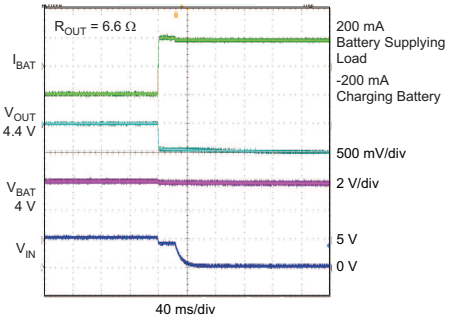


Figure 1.

**ADAPTER HOT-PLUG
NO BATTERY CONNECTED**

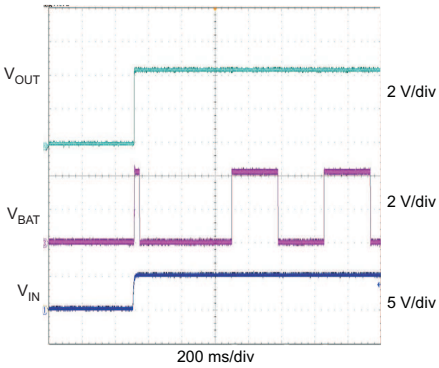


Figure 2.

**ADAPTER HOT-PLUG
BATTERY CONNECTED**

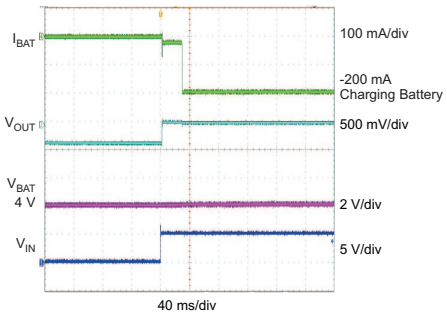


Figure 3.

**DROPOUT VOLTAGE
vs
TEMPERATURE**

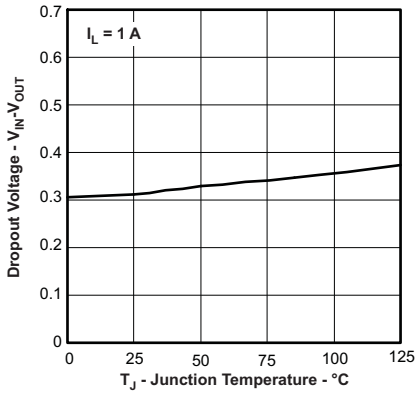


Figure 4.

**DROPOUT VOLTAGE
vs
TEMPERATURE
NO INPUT SUPPLY**

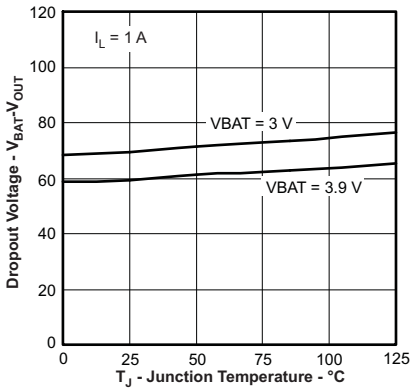


Figure 5.

**bq24072
OUTPUT REGULATION VOLTAGE
vs
BATTERY VOLTAGE**

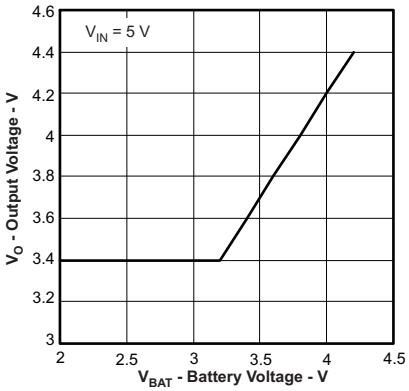


Figure 6.

**bq24072
OUTPUT REGULATION VOLTAGE
vs
TEMPERATURE**

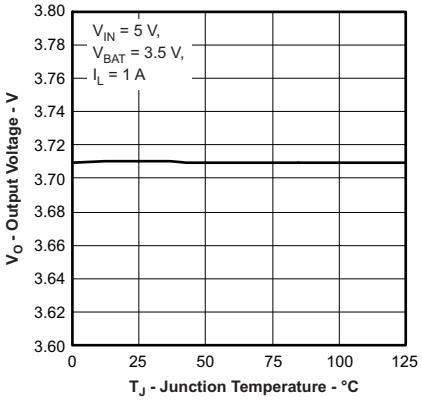


Figure 7.

**bq24073/ 74
OUTPUT REGULATION VOLTAGE
vs
TEMPERATURE**

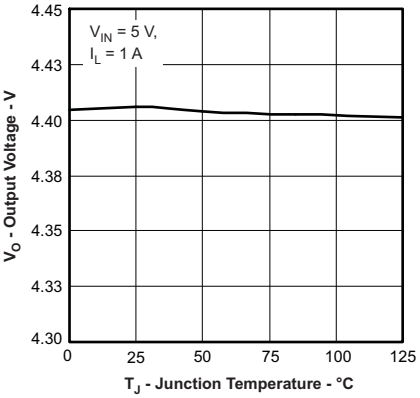


Figure 8.

**bq24075
OUTPUT REGULATION VOLTAGE
vs
TEMPERATURE**

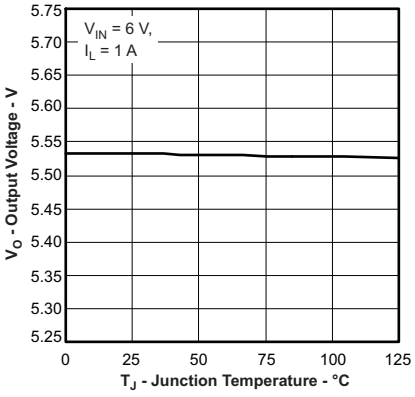


Figure 9.

TYPICAL CHARACTERISTICS (continued)

BAT REGULATION VOLTAGE vs TEMPERATURE

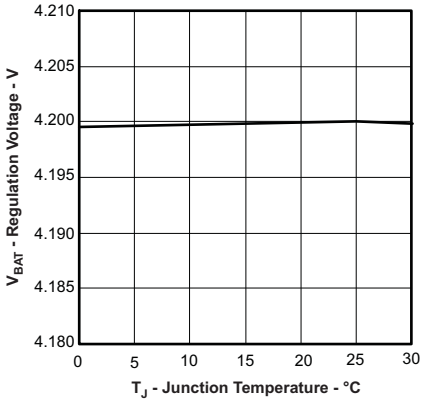


Figure 10.

bq24072/ 73/ 75 OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE

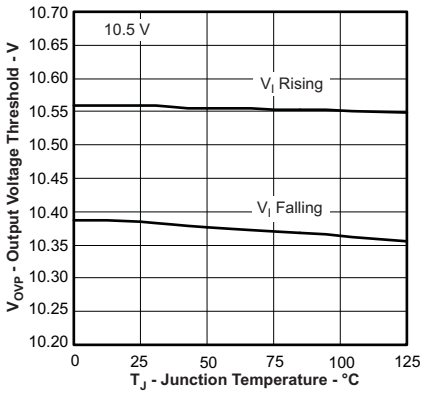


Figure 11.

bq24074 OVERVOLTAGE PROTECTION THRESHOLD vs TEMPERATURE

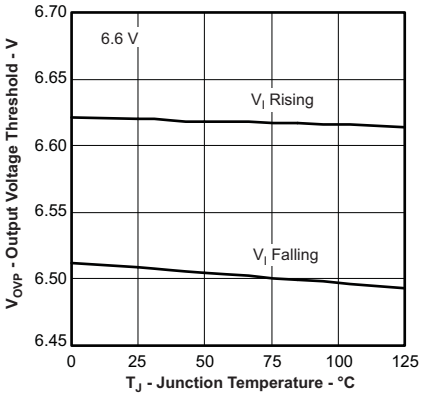


Figure 12.

bq24072/ 73/ 75 INPUT CURRENT LIMIT vs INPUT VOLTAGE

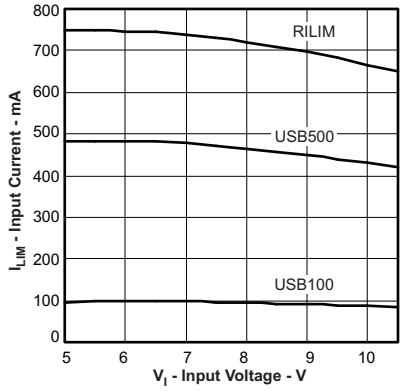


Figure 13.

bq24074 INPUT CURRENT LIMIT vs INPUT VOLTAGE

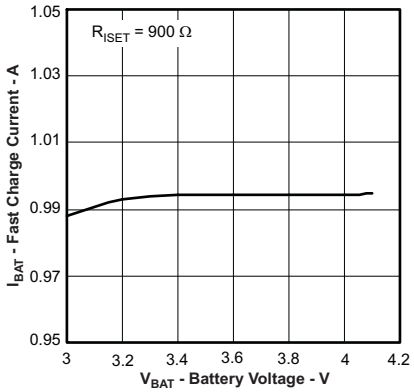


Figure 14.

FASTCHARGE CURRENT vs BATTERY VOLTAGE

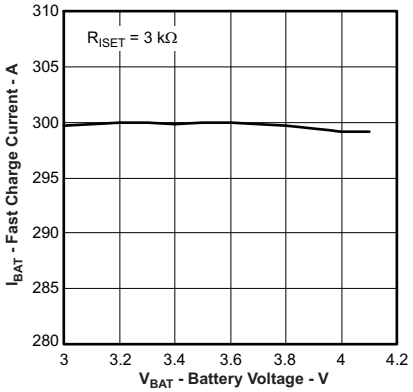


Figure 15.

FASTCHARGE CURRENT vs BATTERY VOLTAGE

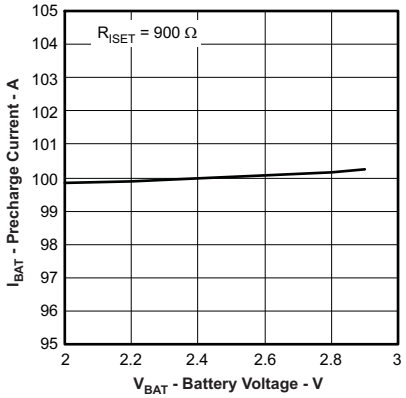


Figure 16.

PRECHARGE CURRENT vs BATTERY VOLTAGE

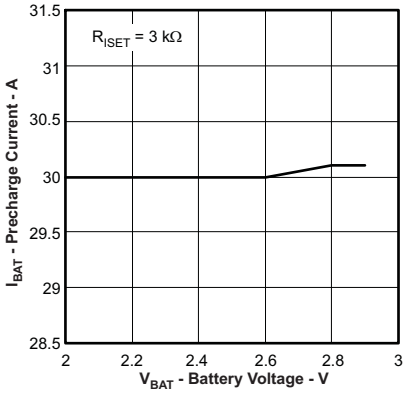


Figure 17.

EXPLANATION OF DEGLITCH TIMES AND COMPARATOR HYSTERESIS

Figures not to scale

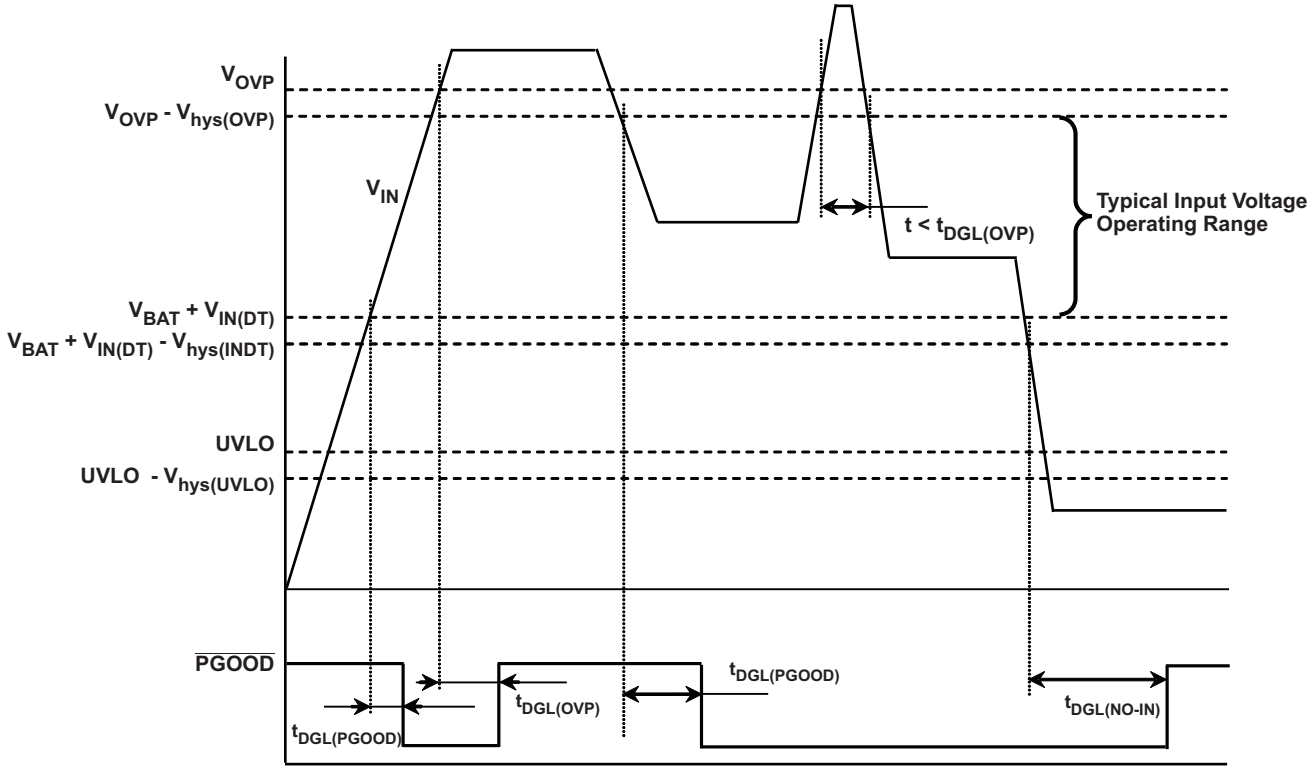


Figure 18. Power-Up, Power-Down

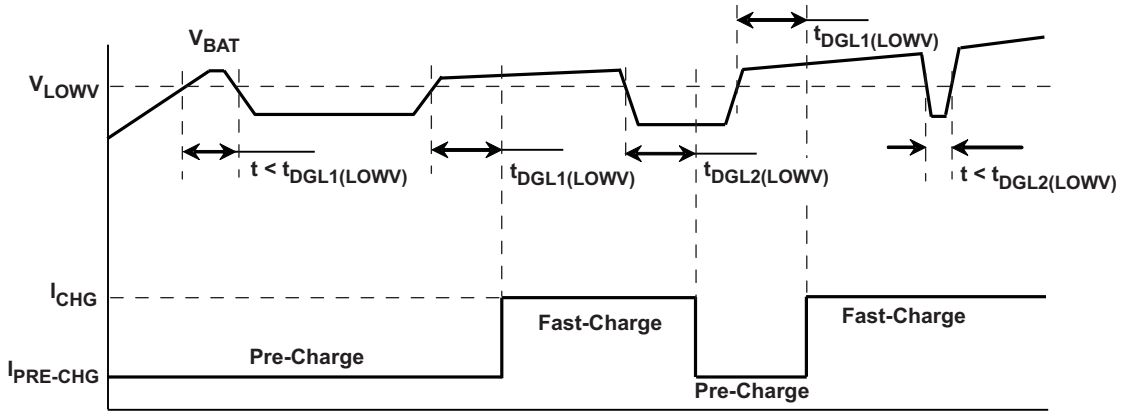


Figure 19. Pre- to Fast-Charge, Fast- to Pre-Charge Transition – $t_{DGL1(LOWV)}$, $t_{DGL2(LOWV)}$

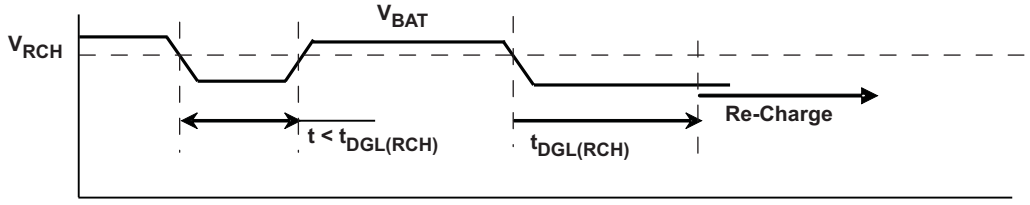


Figure 20. Recharge – $t_{DGL(RCH)}$

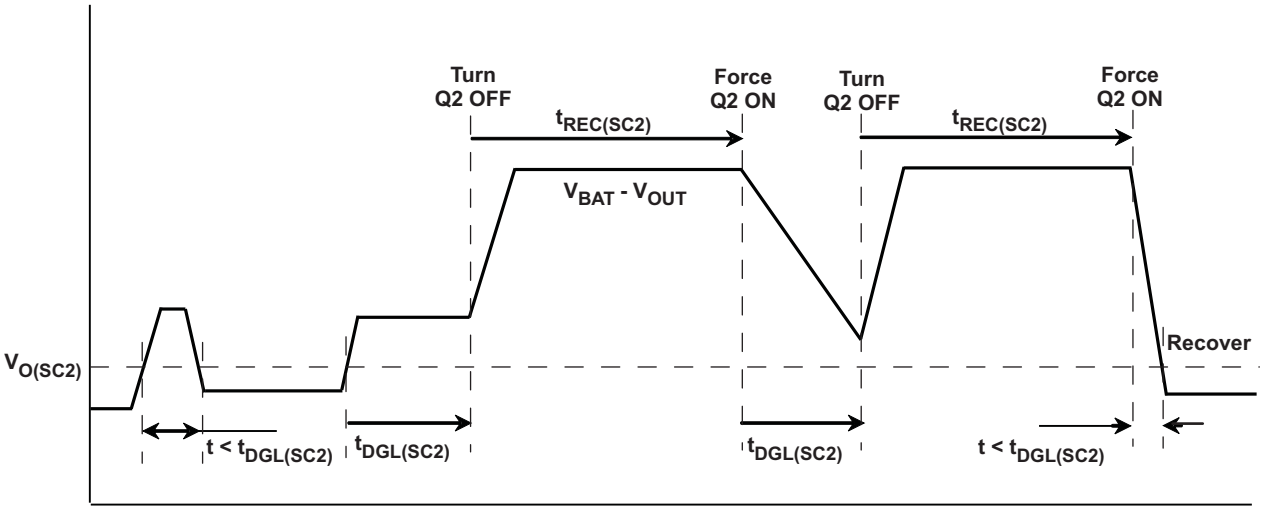


Figure 21. OUT Short-Circuit – Supplement Mode

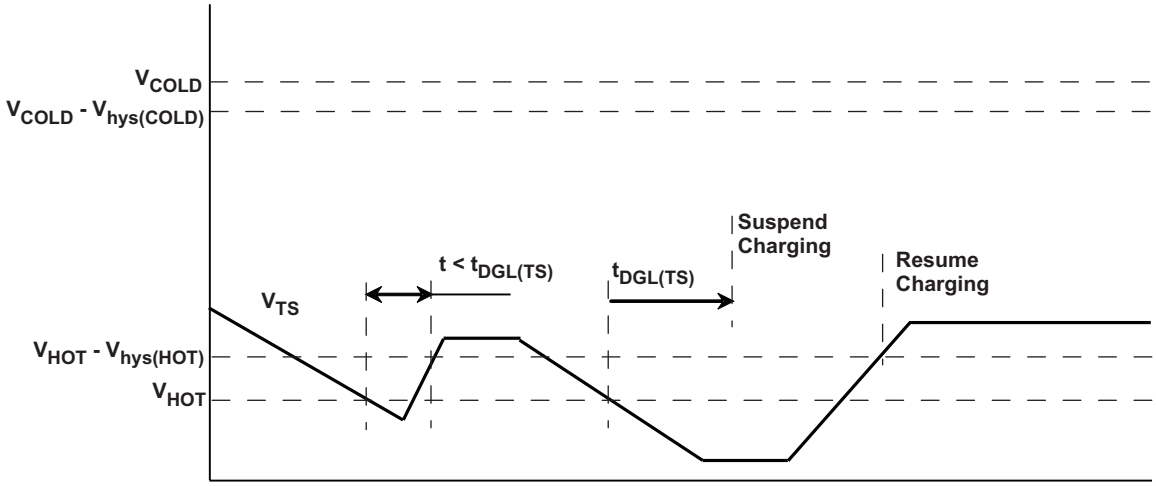


Figure 22. Battery Pack Temperature Sensing – TS Pin. Battery Temperature Increasing

DETAILED FUNCTIONAL DESCRIPTION

The bq2407x devices are integrated Li-Ion linear chargers and system power path management devices targeted at space-limited portable applications. The device powers the system while simultaneously and independently charging the battery. This feature reduces the number of charge and discharge cycles on the battery, allows for proper charge termination and enables the system to run with a defective or absent battery pack. It also allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be an AC adapter or a USB port. The devices feature Dynamic Power Management, which shares the source current between the system and battery charging, and automatically reduces the charging current if the system load increases. Additionally, when charging from a USB port, the device reduces the input current if the input voltage falls below a threshold, preventing the USB port from crashing. The power-path architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. The startup state diagram is shown in Figure 23.

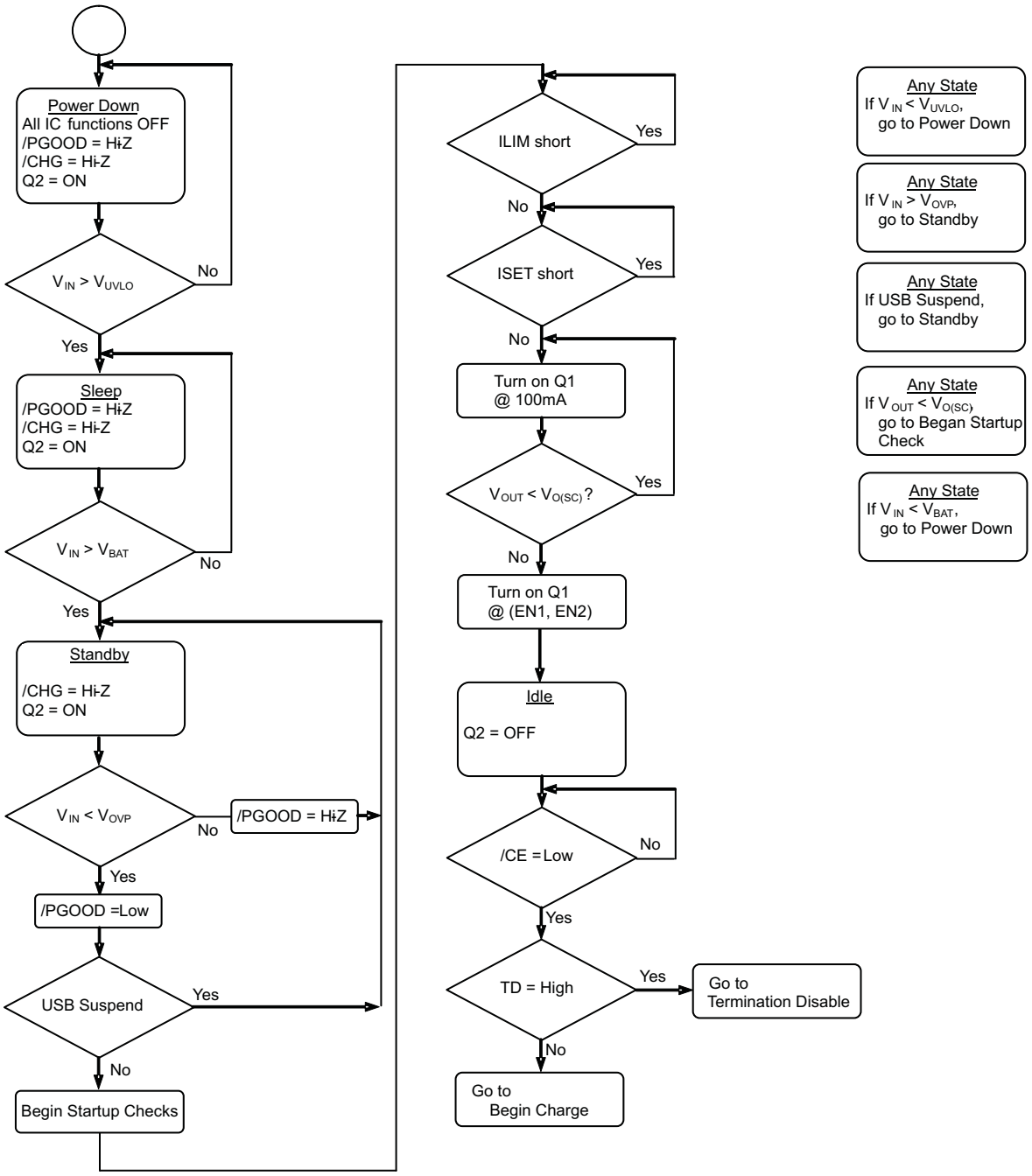


Figure 23. Startup State Diagram

UNDER-VOLTAGE LOCKOUT (UVLO)

The bq2407X family remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO).

During the power down mode the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During power down mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

POWER ON

When V_{IN} exceeds the UVLO threshold, the bq2407x powers up. While V_{IN} is below V_{BAT} + $V_{IN(DT)}$, the host commands at the control inputs ($\overline{CE}$, EN1 and EN2) are ignored. The Q1 FET connected between IN and OUT pins is off, and the status outputs $\overline{CHG}$ and $\overline{PGOOD}$ are high impedance. The Q2 FET that connects BAT to OUT is ON. (If SYSOFF is high, Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

Onve V_{IN} rises above V_{BAT} + $V_{IN(DT)}$, $\overline{PGOOD}$ is driven low to indicate the valid power status and the $\overline{CE}$, EN1, and EN2 inputs are read. The device enters standby mode if (EN1 = EN2 = HI) or if an input overvoltage condition occurs. In standby mode, Q1 is OFF and Q2 is ON so OUT is connected to the battery input. (If SYSOFF is high, FET Q2 is off). During this mode, the $V_{OUT(SC2)}$ circuitry is active and monitors for overload conditions on OUT.

When the input voltage at IN is within the valid range: V_{IN} > UVLO ***AND*** V_{IN} > V_{BAT} + $V_{IN(DT)}$ ***AND*** V_{IN} < V_{OVP}, and the EN1 and EN2 pins indicate that the USB suspend mode is not enabled [(EN1, EN2) ≠ (HI, HI)] all internal timers and other circuit blocks are activated. The device then checks for short-circuits at the ISET and ILIM pins. If no short conditions exists, the device switches on the input FET Q1 with a 100mA current limit to checks for a short circuit at OUT. If V_{OUT} rises above V_{SC}, the FET Q1 switches to the current limit threshold set by EN1, EN2 and R_{ILIM} and the device enters into the normal operation. During normal operation, the system is powered by the input source (Q1 is on), and the device continuously monitors the status of $\overline{CE}$, EN1 and EN2 as well as the input voltage conditions. Q2 is turned on to charge the battery and whenever the input source cannot deliver the required load current (supplement mode).

POWER-PATH MANAGEMENT

The bq2407x features an OUT output that powers the external load connected to the battery. This output is active whenever a source is connected to IN or BAT. The following sections discuss the behavior of OUT with a source connected to IN to charge the battery and a battery source only.

IN SOURCE CONNECTED

With a source connected, the power-path management circuitry of the bq2407x monitors the input current continuously. The OUT output for the bq24073/ 74/ 75 is regulated to a fixed voltage ($V_{O(REG)}$). For the bq24072, the OUT output is regulated to 200mV above the voltage at BAT. When the BAT voltage falls below 3.2V, OUT is clamped to 3.4V. Therefore, the minimum voltage at OUT with an adapter connected is 3.4V, allowing for proper startup of the system load. The current into IN is shared between charging the battery and powering the system load at OUT. The bq2407x has internal selectable current limits of 100mA (USB100) and 500mA (500mA) for charging from USB ports, as well as a resistor-programmable input current limit. The power path utilizes additional feature for operation from current-limited USB ports. When EN1 and EN2 are configured for USB100 (EN2=0, EN1=0) or USB500 (EN2=0, EN2=1) modes, the input voltage is monitored. If V_{IN} falls to V_{IN-LOW}, the input current limit is reduced to prevent the input voltage from falling further.

The input current limit selection is controlled by the state of the EN1 and EN2 pins as shown in Table 1. When using the resistor-programmable current limit, the input current limit is set by the value of the resistor connected from the ILIM pin to VSS, and is given by the equation:

$$I_{IN-MAX} = K_{ILIM}/R_{ILIM}$$

The input current limit is adjustable up to 1.5A. The valid resistor range is 1.1 kΩ to 8 kΩ.

When the IN source is connected, priority is given to the system load. The DPM and Battery Supplement modes are used to maintain the system load. Figure 24 and Figure 25 illustrate examples of the DPM and supplement modes. These modes are explained in detail in the following sections.

DPM Mode

When the sum of the charging and system load currents exceeds the preset maximum input current (programmed with EN1, EN2 and ILIM pins), the voltage at OUT decreases. Once the voltage on the OUT pin falls to V_{DPM}, the bq2407x enters DPM mode. In this mode, the charging current is reduced as the OUT current goes up in order to maintain the system output.

Battery Supplement Mode

While in DPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at OUT reduces further. When the OUT voltage drops below the V_{BSUP1} threshold, the battery supplements the system load. The battery stops supplementing the system load when the voltage at OUT rises above the V_{BSUP2} threshold.

During supplement mode, the battery supplement current is not regulated, however there is a short circuit protection circuit built in. If during battery supplement mode, the voltage at OUT drops 250mV below the BAT voltage, the OUT output is turned off if the overload exists after $t_{DGL(SC2)}$ and the device enters *Power-On Reset Mode*

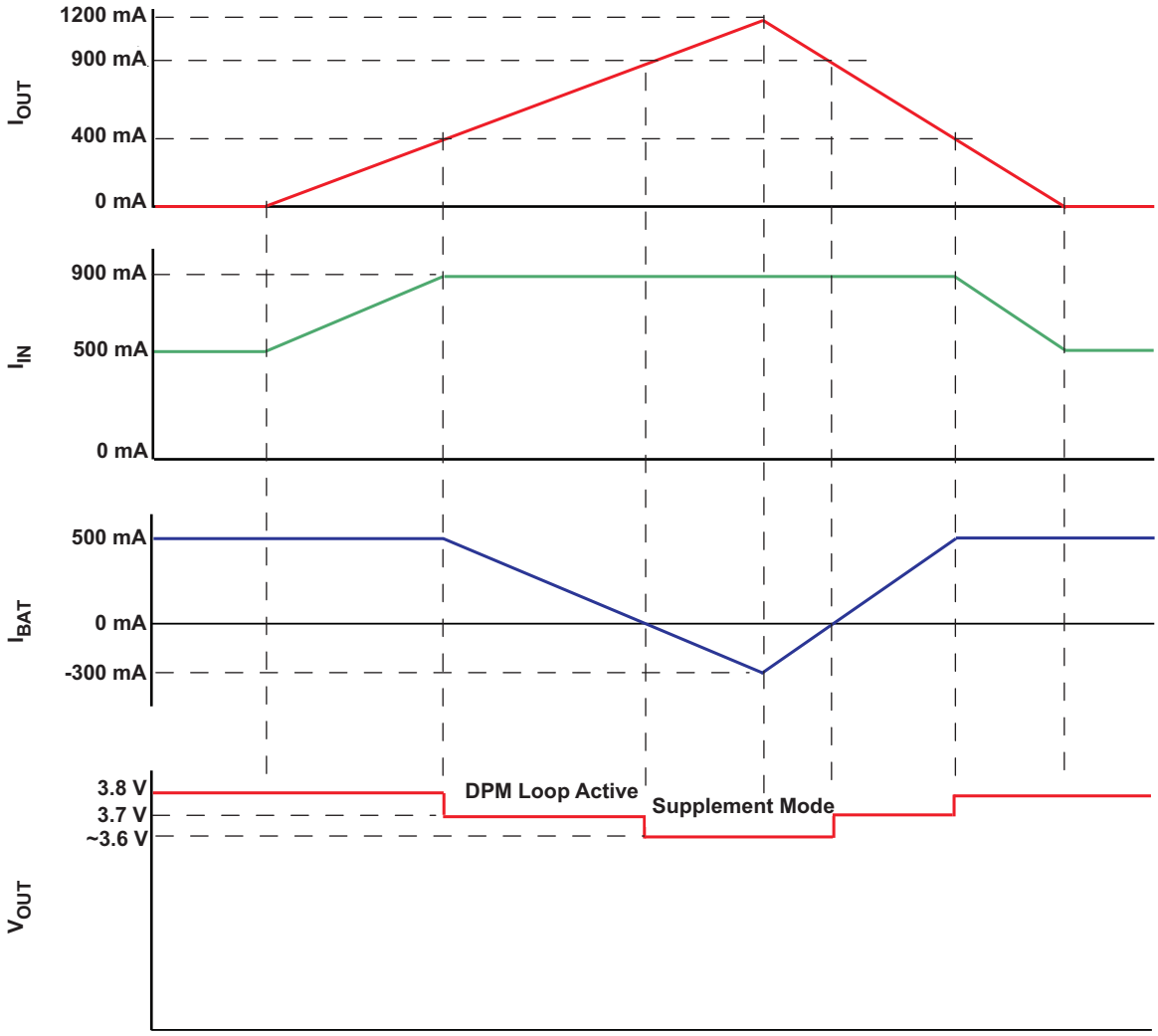


Figure 24. bq24072 DPM and Battery Supplement Modes (V_{OREG} = V_{BAT} + 200mV, V_{BAT} = 3.6V)

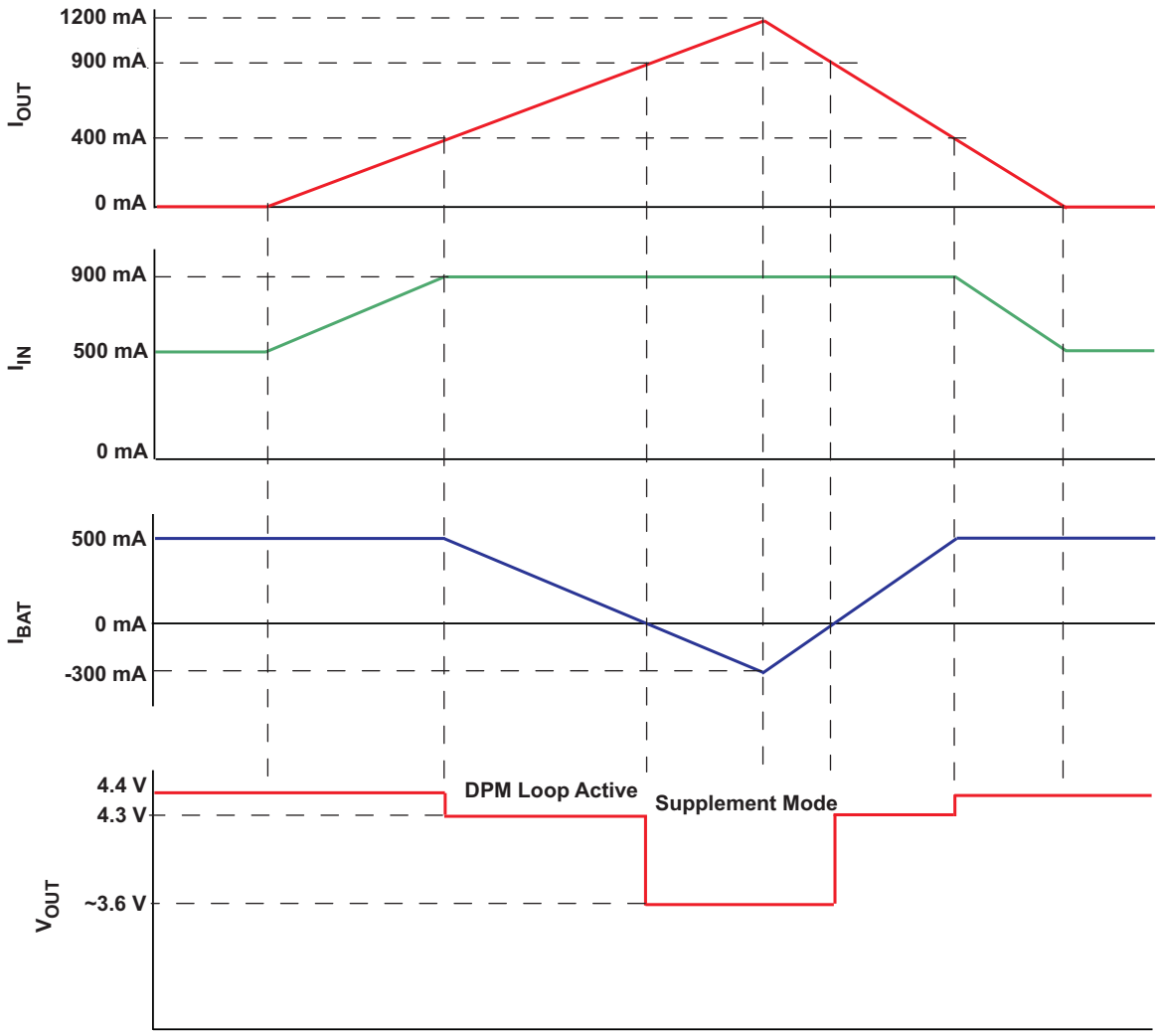


Figure 25. bq24073 DPM and Battery Supplement Modes (V_{OREG}=4.4V, V_{BAT} = 3.6V)

IN SOURCE NOT CONNECTED

When no source is connected to the IN input, OUT is powered strictly from the battery. During this mode the current into OUT is not regulated, similar to *Battery Supplement Mode*, however the short circuit circuitry is active. If the OUT voltage falls below the BAT voltage by 250mV for longer than $t_{DGL(SC2)}$, OUT is turned off. The short circuit recovery timer then starts counting. After $t_{REC(SC2)}$, OUT turns on and attempts to restart. If the short circuit remains, OUT is turned off and the counter restarts. This ON/OFF cycle continues until the overload condition is removed.

BATTERY CHARGING

Dive $\overline{CE}$ low after IC startup to initiate battery charging. First, the device checks for a short-circuit on the BAT pin by sourcing $I_{BAT(SC)}$ to the battery and monitoring the voltage. When the BAT voltage exceeds $V_{BAT(SC)}$, the battery charging continues. The battery is charged in three phases: conditioning pre-charge, constant current fast charge (current regulation) and a constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

Figure 26 illustrates a normal Li-Ion charge cycle using the bq2407x:

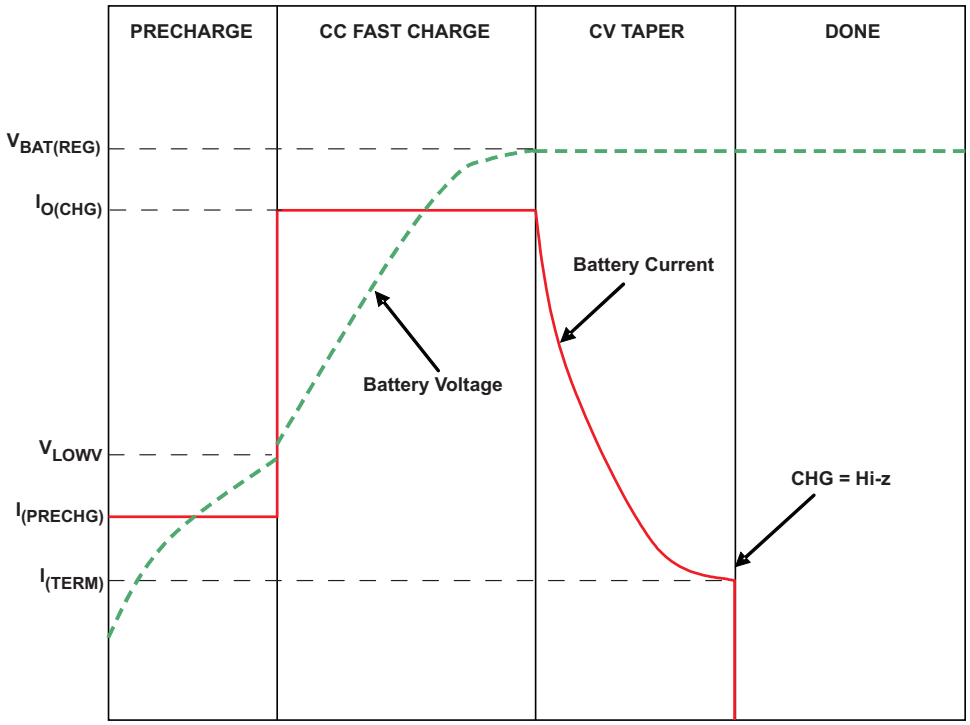


Figure 26. Typical Charge Cycle

In the pre-charge phase, the battery is charged at with the pre-charge current (I_{PRECHG}). Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged with the fast-charge current (I_{CHG}). As the battery voltage reaches $V_{BAT(REG)}$, the battery is held at a constant voltage of $V_{BAT(REG)}$ and the charge current tapers off as the battery approaches full charge. When the battery current reaches I_{TERM}, the $\overline{CHG}$ pin indicates *charging done* by going high-impedance.

Note that termination detection is disabled whenever the charge rate is reduced from the set point because of the actions of the thermal loop, the DPM loop or the $V_{IN(LOW)}$ loop.

The value of the fast-charge current is set by the resistor connected from the ISET pin to VSS, and is given by the equation

$$I_{CHG} = K_{ISET}/R_{ISET}$$

The charge current limit is adjustable up to 1.2A. The valid resistor range is 750Ω to 3 kΩ. Note that if I_{CHG} is programmed as greater than the input current limit, the battery will not charge at the rate of I_{CHG}, but at the slower rate of I_{IN}max (minus the load current on the OUT pin, if any). In this case, the charger timers will be proportionately slowed down. Figure 27 illustrates the battery charger state diagram.

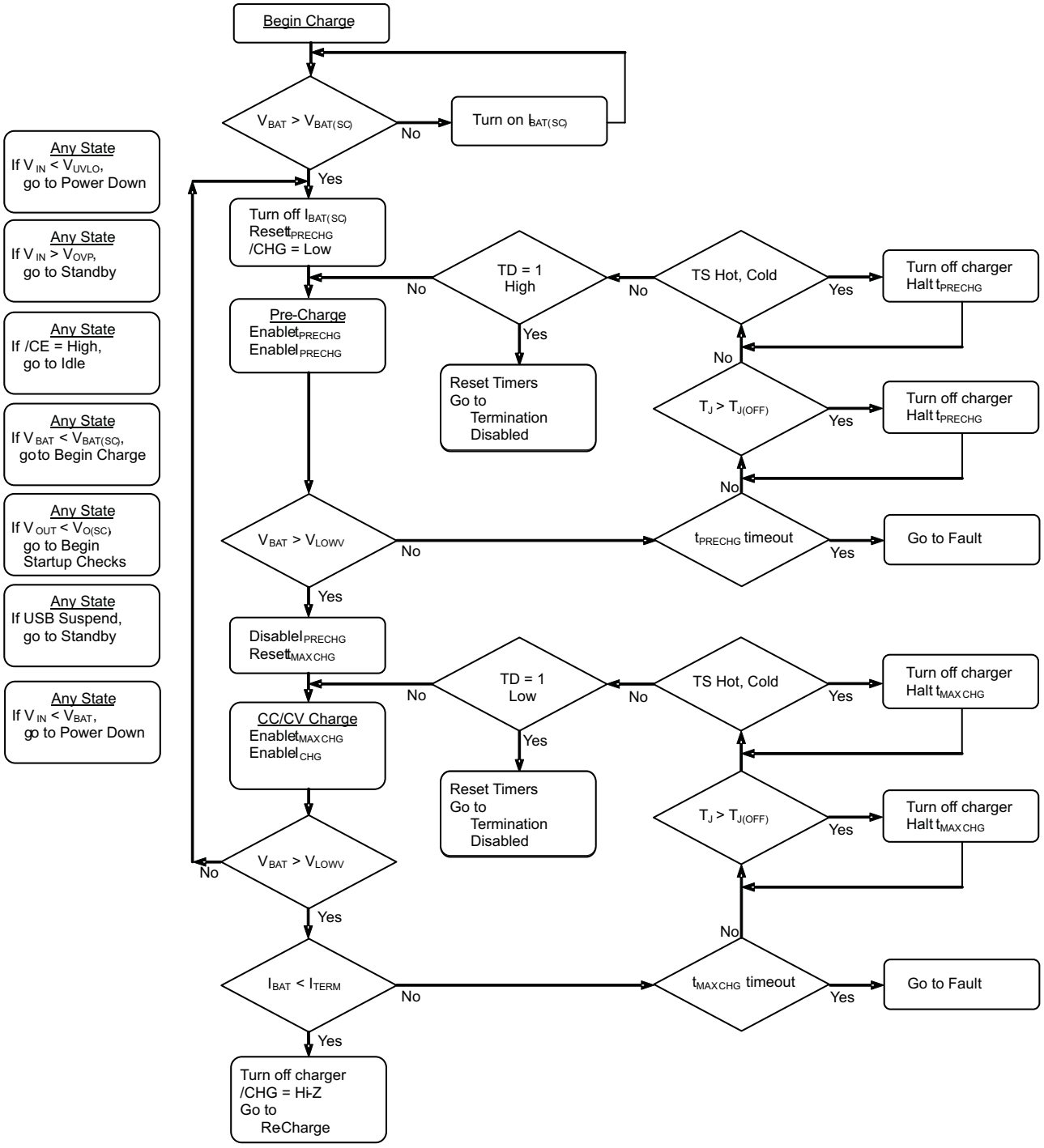


Figure 27. Charging State Diagram

ADJUSTABLE TERMINATION THRESHOLD (ITERM Input, bq24074)

The termination current threshold in the bq24074 is user-programmable. Set the termination current by connecting a resistor from ITERM to VSS. For USB100 mode (EN1 = EN2 = Low), the termination current value is calculated as:

$I_{TERM} = 0.01 \times R_{ITERM} / R_{ISET}$

In the other input current limit modes (EN1 ≠ EN2), the termination current value is calculated as:

$I_{TERM} = 0.03 \times R_{ITERM} / R_{ISET}$

The termination current is programmable up to 50% of the fastcharge current. The R_{ITERM} resistor must be less than 15 kΩ. Leave ITERM unconnected to select the default internally set termination current.

TERMINATION DISABLE (TD Input, bq24072, bq24073)

The bq24072 and bq24073 contain a TD input that allows termination to be enabled/ disabled. Connect TD to a logic high to disable charge termination. When termination is disabled, the device goes through the pre-charge, fast-charge and CV phases, then remains in the CV phase. During the CV phase, the charger maintains the output voltage at BAT equal to $V_{BAT(REG)}$, and charging current does not terminate. BAT sources currents up to I_{CHG} or I_{IN}max, whichever is less. Battery detection is not performed. The $\overline{CHG}$ output is high impedance once the current falls below I_{TERM} and does not go low until the input power is toggled. When termination is disabled, the pre-charge and fast-charge safety timers are also disabled. Battery pack temperature sensing (TS pin functionality) is disabled if the TD pin is high and the TS pin is unconnected or pulled up to V_{IN}.

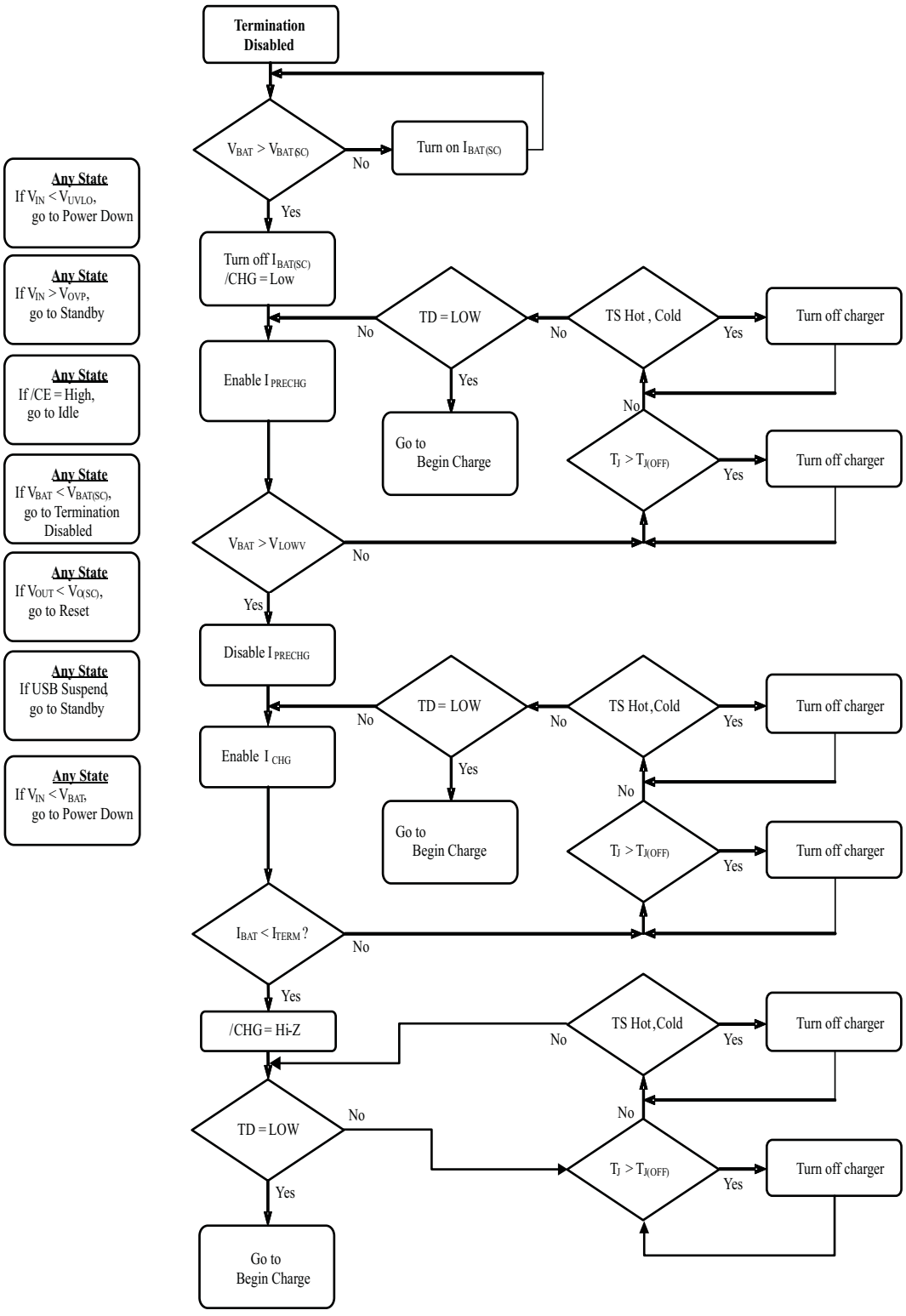


Figure 28. Termination State Diagram

BATTERY DETECTION AND RECHARGE

The bq2407x automatically detects if a battery is connected or removed. Once a charge cycle is complete, the battery voltage is monitored. When the battery voltage falls below V_{RCH}, the device determines whether the battery has been removed. A current, $I_{BAT(DET)}$, is pulled from the battery for a duration t_{DET}. If the voltage on the BAT pin remains above V_{LOWV}, it indicates that the battery is still connected, but has discharged. If $\overline{CE}$ is low, the charger is turned on again to top off the battery. During this recharge cycle, the $\overline{CHG}$ output remains high-impedance: Recharge cycles are not indicated by the $\overline{CHG}$ pin.

If the BAT voltage falls below V_{LOWV} during the battery detection test, it indicates that the battery has been removed. The device then checks for battery insertion. The FET Q2 is turned on and sources I_{PRECHG} out of BAT for the duration of t_{DET}. If the battery voltage does not rise above V_{RCH}, it indicates that a battery has been inserted, and a new charge cycle begins. If the voltage rises above V_{RCH}, it is possible that a fully charged battery has been inserted. To check for this, $I_{BAT(DET)}$ is pulled from the battery for t_{DET}. If the voltage falls below V_{LOWV}, a battery is not present. The device continuously checks for the presence of a battery.

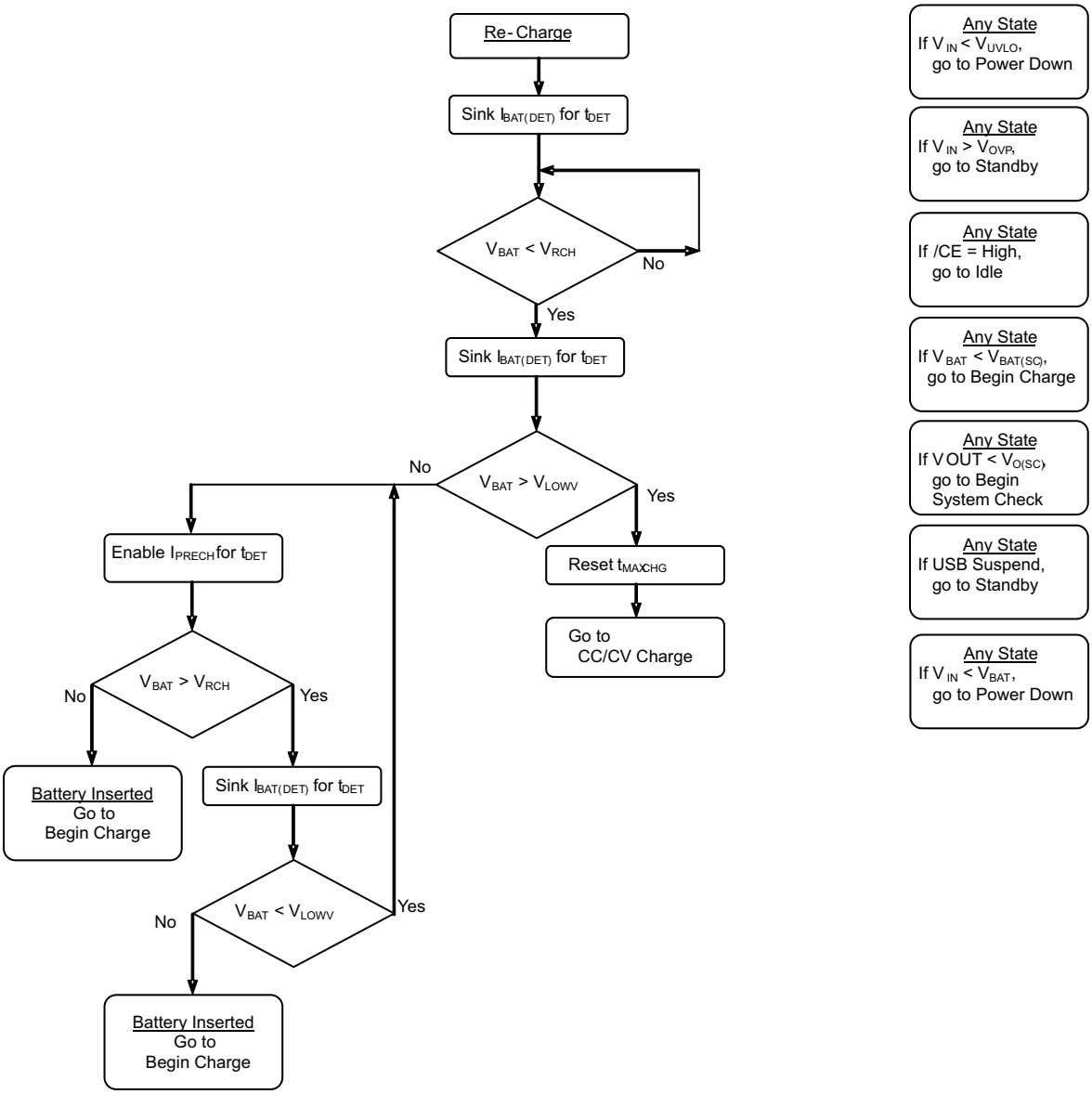


Figure 29. Re-Charge State Diagram

BATTERY DISCONNECT (SYSOFF Input, bq24075)

The bq24075 features a SYSOFF input that allows the user to turn the FET Q2 off and disconnect the battery from the OUT pin. This is useful for disconnecting the system load from the battery, factory programming where the battery is not installed or for host side charge monitoring where the OCV level must be monitored. The /CHG output remains low when SYSOFF is low. Connect SYSOFF to VSS, to turn Q2 on for normal operation. SYSOFF is internally pulled to VBAT through ~285 kΩ resistor.

DYNAMIC CHARGE TIMERS (TMR Input)

The bq2407x devices contain internal safety timers for the pre-charge and fast-charge phases to prevent potential damage to the battery and the system. The timers begin at the start of the respective charge cycles. The timer values are programmed by connecting a resistor from TMR to VSS. The resistor value is calculated using the following equation:

$t_{PRECHG} = K_{TMR} \times R_{TMR}$

$t_{MAXCHG} = 10 \times K_{TMR} \times R_{TMR}$

Leave TMR unconnected to select the internal default timers. Disable the timers by connecting TMR to VSS.

Note that timers are suspended when the device is in thermal shutdown, and the timers are slowed proportionally to the charge current when the device enters thermal regulation. For the bq24072 and bq24073, the timers are disabled when TD is connected to a high logic level.

During the fast charge phase, several events increase the timer durations.

1. The system load current activates the DPM loop which reduces the available charging current
2. The input current is reduced because the input voltage has fallen to $V_{IN(LOW)}$
3. The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$

During each of these events, the internal timers are slowed down proportionately to the reduction in charging current. For example, if the charging current is reduced by half, the fast charge timer is twice as long as long as programmed.

If the pre charge timer expires before the battery voltage reaches V_{LOWV}, the bq2407x indicates a fault condition. Additionally, if the battery current does not fall to I_{TERM} before the fast charge timer expires, a fault is indicated. The $\overline{CHG}$ output flashes at approximately 2 Hz to indicate a fault condition.

STATUS INDICATORS ($\overline{PGOOD}$, $\overline{CHG}$)

The bq2407x contains two open-drain outputs that signal its status. The $\overline{PGOOD}$ output signals when a valid input source is connected. $\overline{PGOOD}$ is low when $(V_{BAT} + V_{IN(DT)}) < V_{IN} < V_{OVP}$. When the input voltage is outside of this range, $\overline{PGOOD}$ is high impedance.

The $\overline{CHG}$ output signals when a new charge cycle is initiated. After a charge cycle is initiated, $\overline{CHG}$ goes low once the battery is above the short circuit threshold. $\overline{CHG}$ goes high impedance once the charge current falls below I_{TERM}. $\overline{CHG}$ remains high impedance until the input power is removed and reconnected or the $\overline{CE}$ pin is toggled. It does not signal subsequent recharge cycles. In additions, $\overline{CHG}$ signals timer faults by flashing at approximately 2Hz.

THERMAL REGULATION AND THERMAL SHUTDOWN

The bq2407x contain a thermal regulation loop that monitors the die temperature. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. In some cases, the die temperature continues to rise despite the operation of the thermal loop, particularly under high VIN and heavy OUT system load conditions. Under these conditions, if the die temperature increases to $T_{J(OFF)}$, the input FET Q1 is turned OFF. FET Q2 is turned ON to ensure that the battery still powers the load on OUT. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the input FET Q1 is turned on and the device returns to thermal regulation. Continuous overtemperature conditions result in the pulsing of the Q1 FET.

Note that this feature monitors the die temperature of the bq2407x. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm and the LDO associated with OUT. A modified charge cycle with the thermal loop active is shown in Figure 30:

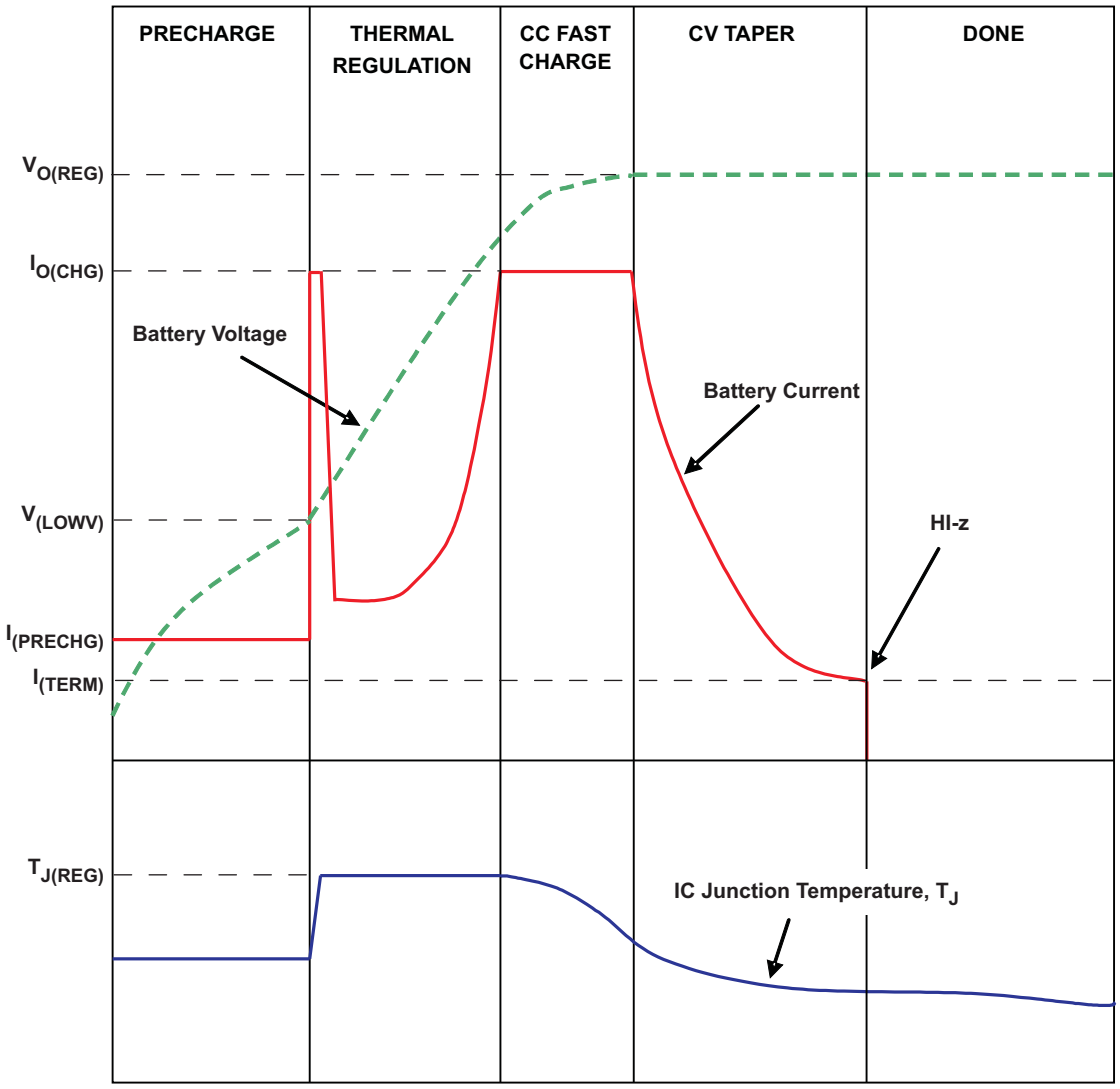


Figure 30. Charge Cycle Modified by Thermal Loop

BATTERY PACK TEMPERATURE MONITORING

The bq2407x features an external battery pack temperature monitoring input. The TS input connects to the NTC resistor in the battery pack to monitor battery temperature and prevent dangerous over-temperature conditions.

During charging, I_{NTC} is sourced to TS and the voltage at TS is continuously monitored. If, at any time, the voltage at TS is outside of the operating range (V_{COLD} to V_{HOT}), charging is suspended. The timers maintain their values but suspend counting. When the voltage measured at TS returns to within the operation window, charging is resumed and the timers continue counting. When charging is suspended due to a battery pack temperature fault, the $\overline{CHG}$ pin remains low and continues to indicate *charging*.

For the bq24072 and bq24073, battery pack temperature sensing is disabled when termination is disabled (TD = High) and the voltage at TS is greater than $V_{DIS(TS)}$. The battery pack temperature monitoring is disabled by connecting a 10 kΩ resistor from TS to VSS.

TYPICAL APPLICATION CIRCUITS

1) Charging a pack under host control, timers disabled

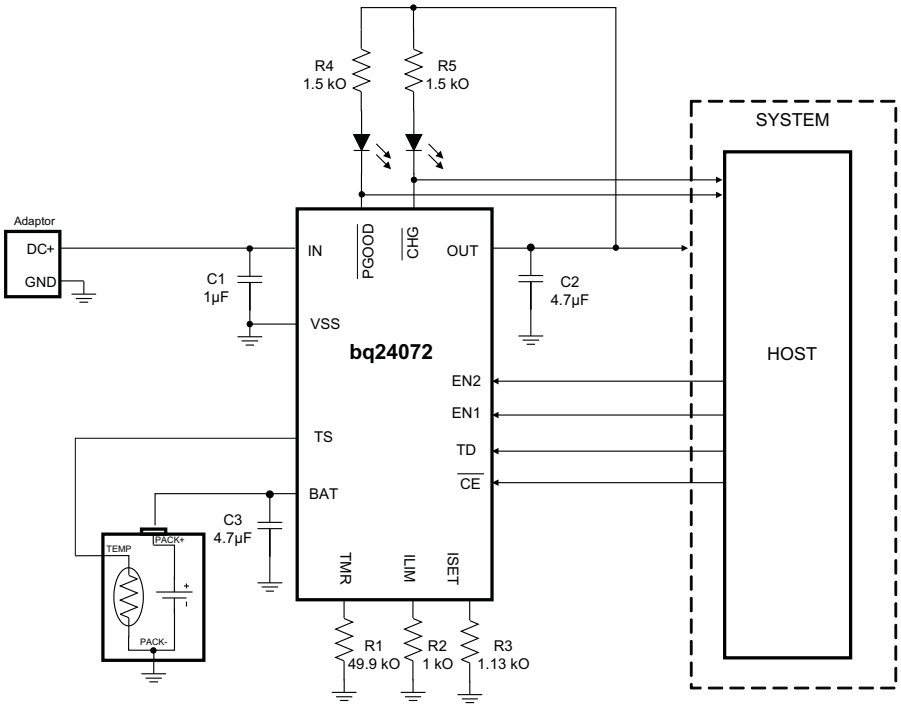


Figure 31. Host Controlled Charger Application Circuit

2) Stand-alone charger

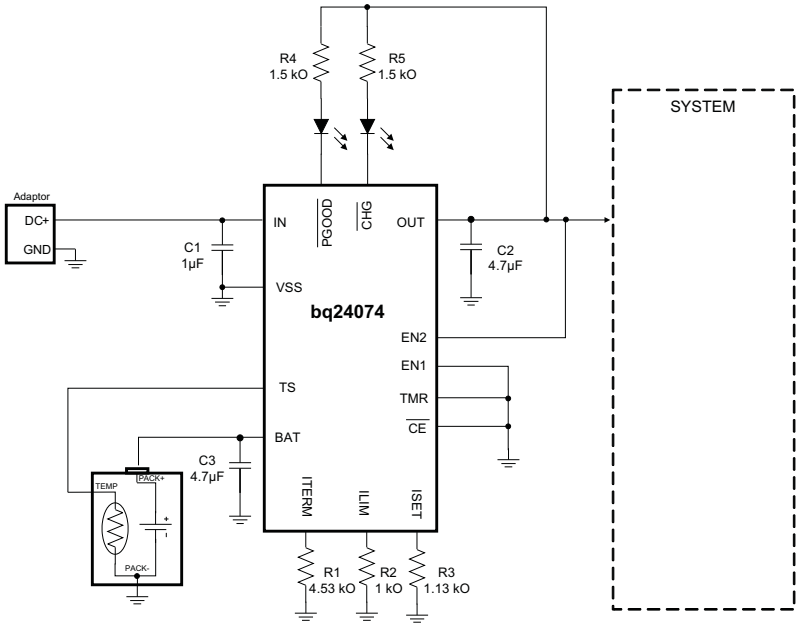


Figure 32. Stand Alone Charger Application Circuit

bq24074 CHARGER DESIGN EXAMPLE

Refer to Figure 32 for Schematic of Design Example.

Requirements

- Supply voltage = 5V
- Fast charge current of approximately 900 mA; ISET - pin 16
- Input Current Limit =1.5A; ILIM - pin 12
- Termination Current Threshold = 120mA; ITERM – pin 15
- Safety timer duration, Fast-Charge = 6.25 hours; TMR – pin 14
- TS – Battery Temperature Sense = 10kΩ NTC (103AT)

Calculations

Program the Fast Charge Current (ISET):

$R_{ISET} = K_{ISET} / I_{CHG}$
K_{ISET} = 900 AΩ fom the electrical characteristics table.
R_{ISET} = 900AΩ/0.8A = 1.125 kΩ

Select the closest standard value, which for this case is 1.13kΩ. Connect this resistor between ISET (pin 16) and V_{SS}.

Program the Input Current Limit (ILIM)

$R_{ILIM} = K_{ILMI} / I_{I\_MAX}$
K_{ILIM} = 1600 AΩ fom the electrical characteristics table.
R_{ISET} = 1600AΩ / 1.5A = 1.067 kΩ

Select the closest standard value, which for this case is 1 kΩ. Connect this resistor between ILIM (pin 12) and V_{SS}.

Program the Termination Current Threshold (I_{TERM})

$R_{ITERM} = I_{TERM} \times R_{ISET} / 0.030$
R_{ISET} = 1.13 kΩ fom the above calculation.
R_{ITERM} = 120mA × 1.13 kΩ / 0.030 = 4.52 kΩ

Select the closest standard value, which for this case is 4.53kΩ. Connect this resistor between ITERM (pin 15) and V_{SS}. Note that when in USB100 mode (EN1 = EN2 = V_{SS}), the termination threshold is 1/3 of the normal threshold.

Program 6.25-hour Fast-Charge Saftey Timer (TMR)

$R_{TMR} = t_{MAXCHG} / (10 \times K_{TMR})$
K_{TMR} = 45 s/kΩ fom the electrical characteristics table.
R_{TMR} = (6.25 hr × 3600 s/hr) / (10 × 45 s/kΩ) = 50 kΩ

Select the closest standard value, which for this case is 49.9 kΩ. Connect this resistor between TMR (pin 2) and V_{SS}.

TS Function

Use a 10kΩ NTC thermistor in the battery pack (103AT). To Disable the temp sense function, use a fixed 10kΩ resistor between the TS (Pin 1) and V_{SS}.

$\overline{CHG}$ and $\overline{PGOOD}$

LED Status: connect a 1.5kΩ resistor in series with a LED between OUT and $\overline{CHG}$ and OUT and $\overline{PGOOD}$.

Processor Monitoring Status: connect a pullup resistor (on the order of 100 kΩ) between the processor's power rail and $\overline{CHG}$ and $\overline{PGOOD}$

SELECTING IN, OUT AND BAT pin CAPACITORS

In most applications, all that is needed is a high-frequency decoupling capacitor (ceramic) on the power pin, input, output and battery pins. Using the values shown on the application diagram, is recommended. After evaluation of these voltage signals with real system operational conditions, one can determine if capacitance values can be adjusted toward the minimum recommended values (DC load application) or higher values for fast high amplitude pulsed load applications. Note if designed high input voltage sources (bad adaptors or wrong adaptors), the capacitor needs to be rated appropriately. Ceramic capacitors are tested to 2x their rated values so a 16V capacitor may be adequate for a 30V transient (verify tested rating with capacitor manufacturer).

THERMAL PACKAGE

The bq24072/3/4/5 family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). The power pad should be directly connected to the V_{SS} pin. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271). The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$\theta_{JA} = (T_J - T) / P$

Where:

T_J = chip junction temperature

T = ambient temperature

P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

1. Whether or not the device is board mounted
2. Trace size, composition, thickness, and geometry
3. Orientation of the device (horizontal or vertical)
4. Volume of the ambient air surrounding the device under test and airflow
5. Whether other surfaces are in close proximity to the device being tested

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. Typically after fast charge begins the pack voltage increases to ~3.4V within the first 2 minutes. The thermal time constant of the assembly typically takes a few minutes to heat up so when doing maximum power dissipation calculations, 3.4V is a good minimum voltage to use. This is easy to verify, with the system and a fully discharged battery, by plotting temperature on the bottom of the PCB under the IC (pad should have multiple vias), the charge current and the battery voltage as a function of time. The fast charge current will start to taper off if the part goes into thermal regulation.

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged : $P = [V_{(IN)} – V_{(OUT)}] \times I_{(OUT)} + [V_{(OUT)} – V_{(BAT)}] \times I_{(BAT)}$

The thermal loop feature reduces the charge current to limit excessive IC junction temperature. It is recommended that the design not run in thermal regulation for typical operating conditions (nominal input voltage and nominal ambient temperatures) and use the feature for non typical situations such as hot environments or higher than normal input source voltage. With that said, the IC will still perform as described, if the thermal loop is always active.

Half-Wave Adaptors

Some low cost adapters implement a half rectifier topology, which causes the adapter output voltage to fall below the battery voltage during part of the cycle. To enable operation with low cost adapters under those conditions the bq2407x family keeps the charger on for at least 20 msec (typical) after the input power puts the part in sleep mode. This feature enables use of external low cost adapters using 50 Hz networks.

Seep Mode

After entering sleep mode for >20mS the internal FET connection between the IN and OUT pin is disabled and pulling the input to ground will not discharge the battery, other than the leakage on the BAT pin. If one has a full 1000mAHr battery and the leakage is 10μA, then it would take 1000mAHr/10μA = 100000 hours (11.4 years) to discharge the battery. The battery's self discharge is typically 5 times higher than this.

Layout Tips

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq2407x, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces
- The bq2407x family is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: QFN/SON PCB Attachment Application Note (SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24072RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24072RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24072RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24072RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24073RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24073RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24073RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24073RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24074RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24074RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24074RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24074RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24075RGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24075RGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24075RGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24075RGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

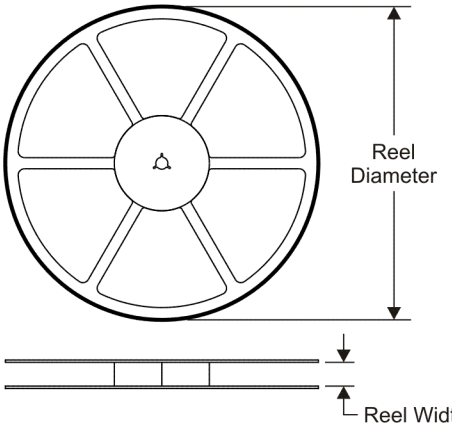
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

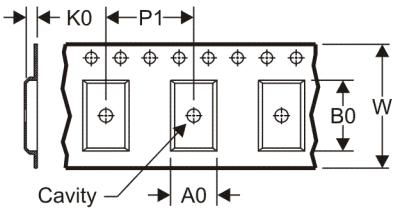
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

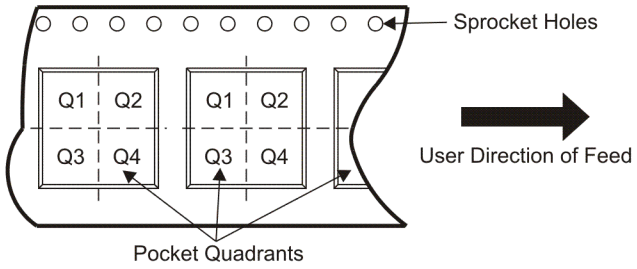


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

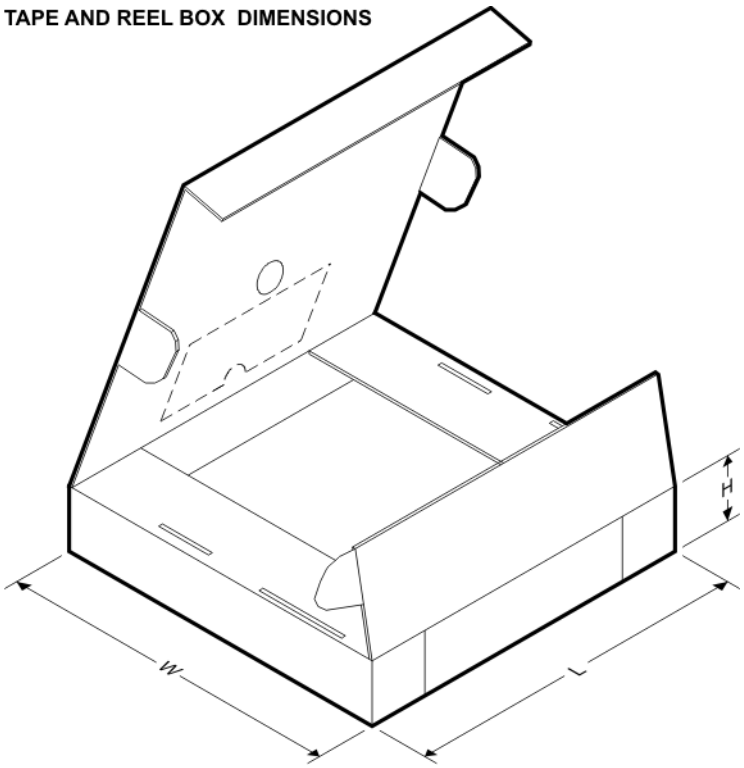
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24072RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24072RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24073RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24073RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24074RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24074RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075RGTR	QFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ24075RGTT	QFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

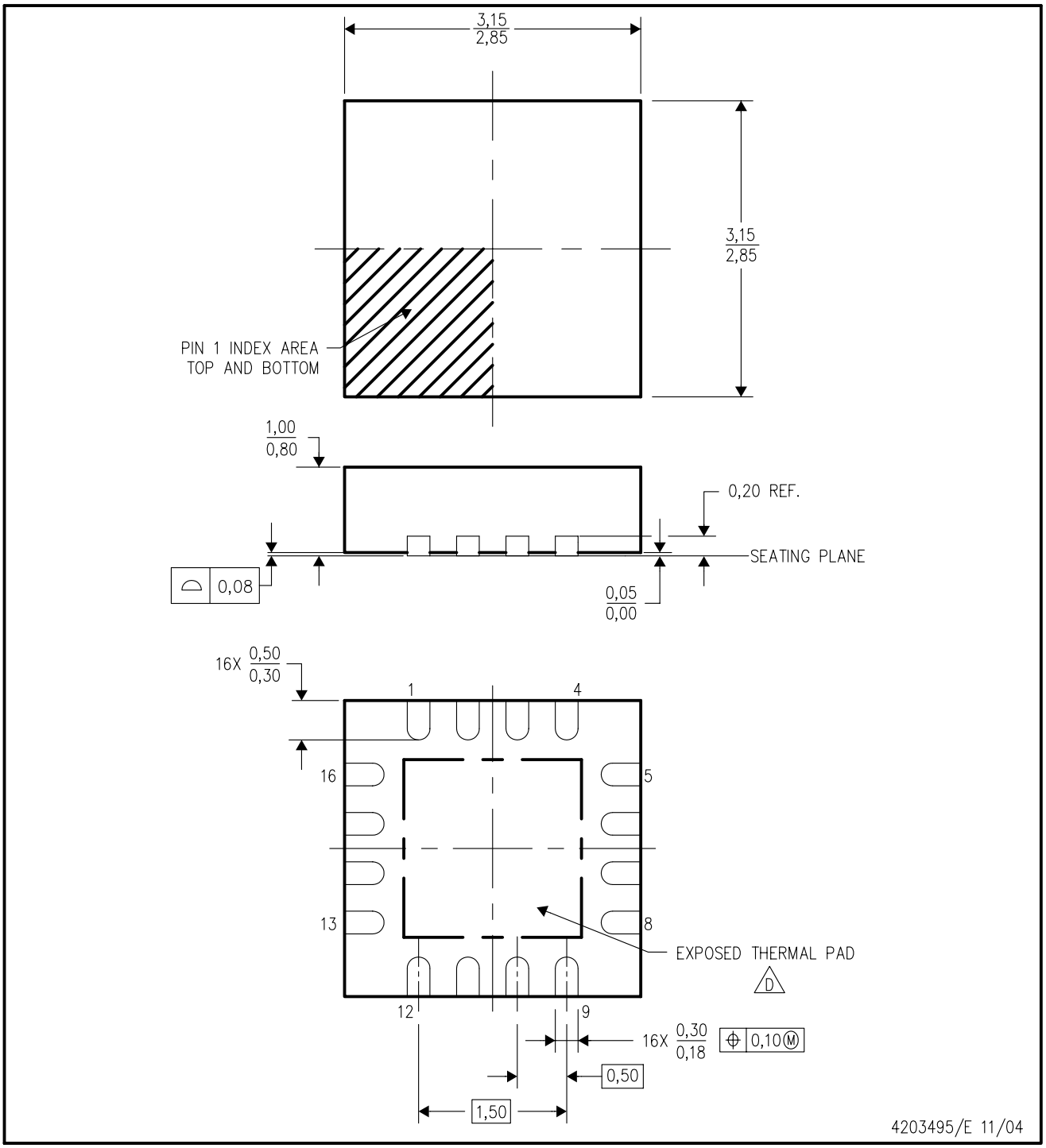
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24072RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
BQ24072RGTT	QFN	RGT	16	250	190.5	212.7	31.8
BQ24073RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
BQ24073RGTT	QFN	RGT	16	250	190.5	212.7	31.8
BQ24074RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
BQ24074RGTT	QFN	RGT	16	250	190.5	212.7	31.8
BQ24075RGTR	QFN	RGT	16	3000	346.0	346.0	29.0
BQ24075RGTT	QFN	RGT	16	250	190.5	212.7	31.8

RGT (S–PQFP–N16) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

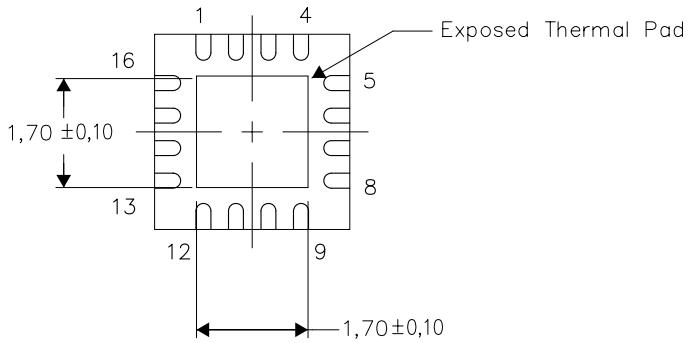
RGT (S–PQFP–N16)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

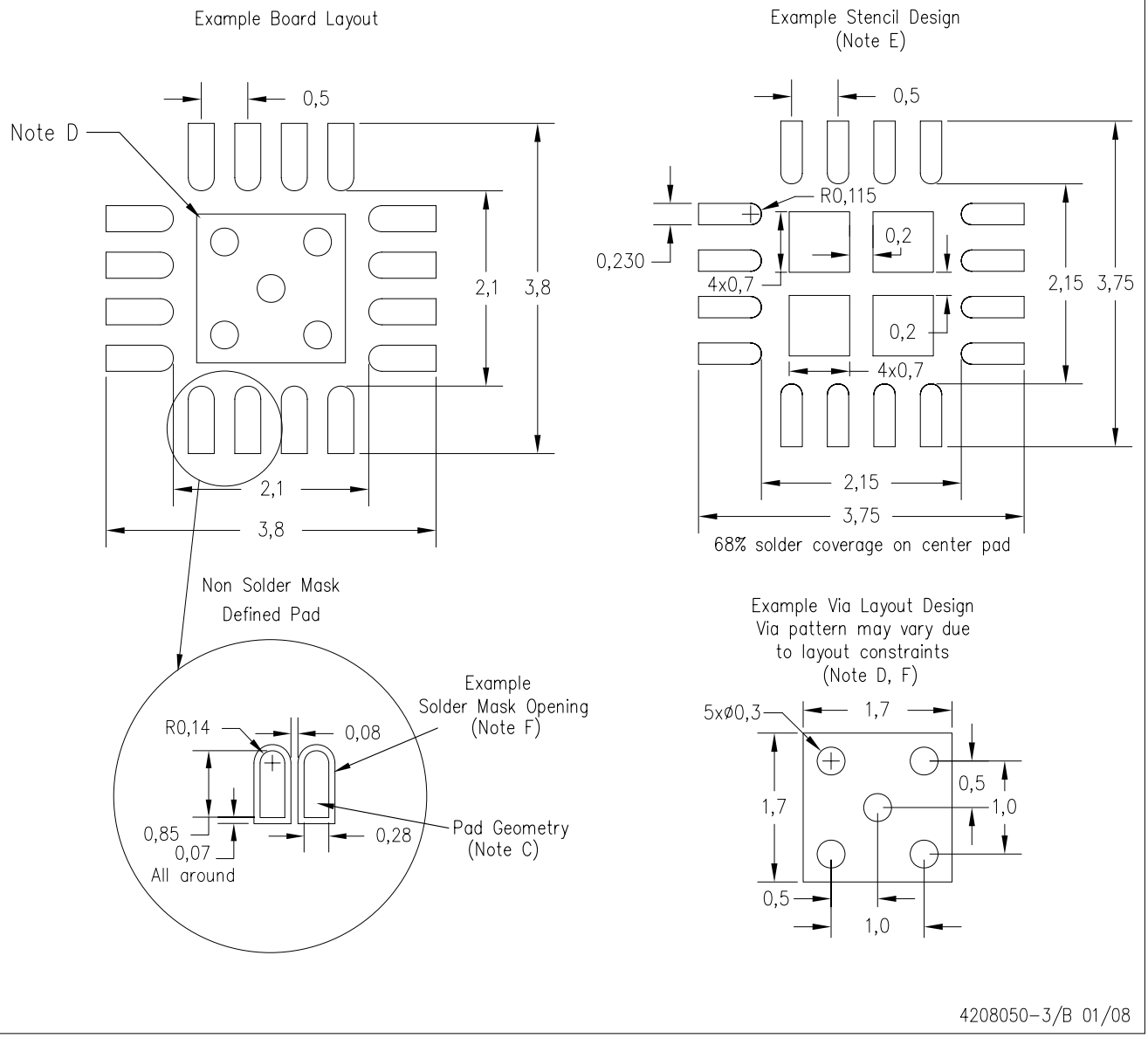


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGT (S–PQFP–N16)



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265