

- Member of the Texas Instruments Widebus™ Family
- Output Ports Have Series Damping Resistors, So No External Resistors Are Required
- Diodes on Inputs Clamp Overshoot
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

description/ordering information

This 1-bit to 2-bit address driver is designed for 2.3-V to 3.6-V V_{CC} operation.

Diodes to V_{CC} have been added on the inputs to clamp overshoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

The outputs, which are designed to sink up to 12 mA, include series damping resistors to reduce overshoot and undershoot.

The ALVCHS162830A is an improved version of the LVCHS162830 (non-A version) and has been optimized for lower power consumption and higher AC drive. Higher AC drive provides capability to drive loads with a faster edge rate.

To ensure the high-impedance state during power up or power down, the output-enable (\overline{OE}) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

DBB PACKAGE
(TOP VIEW)

2Y2	1	80	1Y3
1Y2	2	79	2Y3
GND	3	78	GND
2Y1	4	77	1Y4
1Y1	5	76	2Y4
V_{CC}	6	75	V_{CC}
A1	7	74	1Y5
A2	8	73	2Y5
GND	9	72	GND
A3	10	71	1Y6
A4	11	70	2Y6
GND	12	69	GND
A5	13	68	1Y7
A6	14	67	2Y7
V_{CC}	15	66	V_{CC}
A7	16	65	1Y8
A8	17	64	2Y8
GND	18	63	GND
A9	19	62	1Y9
$\overline{OE1}$	20	61	2Y9
$\overline{OE2}$	21	60	1Y10
A10	22	59	2Y10
GND	23	58	GND
A11	24	57	1Y11
A12	25	56	2Y11
V_{CC}	26	55	V_{CC}
A13	27	54	1Y12
A14	28	53	2Y12
GND	29	52	GND
A15	30	51	1Y13
A16	31	50	2Y13
GND	32	49	GND
A17	33	48	1Y14
A18	34	47	2Y14
V_{CC}	35	46	V_{CC}
2Y18	36	45	1Y15
1Y18	37	44	2Y15
GND	38	43	GND
2Y17	39	42	1Y16
1Y17	40	41	2Y16



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74ALVCHS162830A

1-BIT TO 2-BIT ADDRESS DRIVER

WITH 3-STATE OUTPUTS

SCES624 – FEBRUARY 2005

description/ordering information

ORDERING INFORMATION

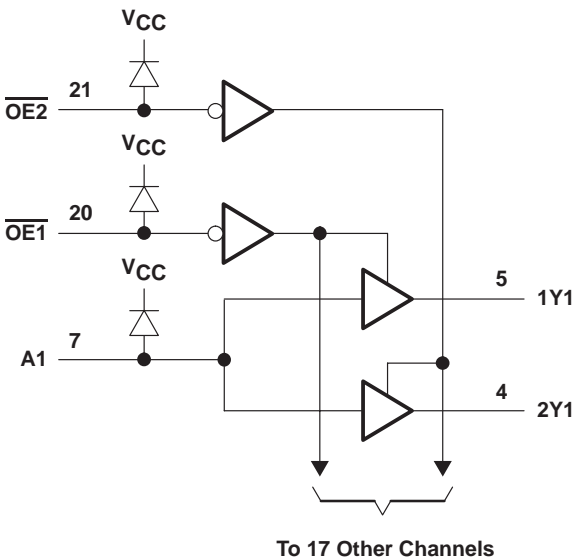
TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TVSOP – DBB	Tape and reel	74ALVCHS162830AGR	ALVCHS162830A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUTS	
OE1	OE2	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$, $V_I > V_{CC}$)	±50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3)	64°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 4.6 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.3$ V to 2.7 V	1.7		V
		$V_{CC} = 2.7$ V to 3.6 V	2		
V_{IL}	Low-level input voltage	$V_{CC} = 2.3$ V to 2.7 V		0.7	V
		$V_{CC} = 2.7$ V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2.3$ V		–6	mA
		$V_{CC} = 2.7$ V		–8	
		$V_{CC} = 3$ V		–12	
I_{OL}	Low-level output current	$V_{CC} = 2.3$ V		6	mA
		$V_{CC} = 2.7$ V		8	
		$V_{CC} = 3$ V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

74ALVCHS162830A
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS

SCES624 – FEBRUARY 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{IK}		I _I = -18 mA	2.3 V			-1.2	V
		I _I = 18 mA	2.3 V			V _{CC} + 1.2	
V _{OH}		I _{OH} = -100 µA	2.3 V to 3.6 V			V _{CC} - 0.2	V
		I _{OH} = -4 mA, V _{IH} = 1.7 V	2.3 V			1.9	
	I _{OH} = -6 mA	V _{IH} = 1.7 V	2.3 V			1.7	
		V _{IH} = 2 V	3 V			2.4	
		I _{OH} = -8 mA, V _{IH} = 2 V	2.7 V			2	
		I _{OH} = -12 mA, V _{IH} = 2 V	3 V			2	
V _{OL}		I _{OL} = 100 µA	2.3 V to 3.6 V			0.2	V
		I _{OL} = 4 mA, V _{IL} = 0.7 V	2.3 V			0.4	
	I _{OL} = 6 mA	V _{IL} = 0.7 V	2.3 V			0.55	
		V _{IL} = 0.8 V	3 V			0.55	
		I _{OL} = 8 mA, V _{IL} = 0.8 V	2.7 V			0.6	
		I _{OL} = 12 mA, V _{IL} = 0.8 V	3 V			0.8	
I _I		V _I = V _{CC} or GND	3.6 V			±5	µA
I _{I(hold)}		V _I = 0.7 V	2.3 V			45	µA
		V _I = 1.7 V	2.3 V			-45	
		V _I = 0.8 V	3 V			75	
		V _I = 2 V	3 V			-75	
		V _I = 0 to 3.6 V‡	3.6 V			±500	
I _{OZ}		V _O = V _{CC} or GND	3.6 V			±10	µA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	3.6 V			20	µA
ΔI _{CC}		One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	3 V to 3.6 V			500	µA
C _i	Control inputs	V _I = V _{CC} or GND	3.3 V			3.5	pF
	Data inputs					4.5	
C _O	Outputs	V _O = V _{CC} or GND	3.3 V			4.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

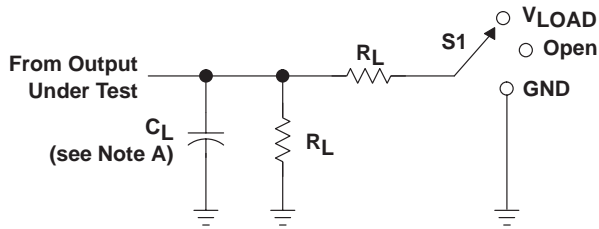
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.2	3.8		4	1.7	3.5	ns
t _{en}	$\overline{\text{OE}}$	Y	1	5.7		5.7	1	4.8	ns
t _{dis}	$\overline{\text{OE}}$	Y	1	4.9		5.4	1.7	5.2	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V _{CC} = 2.5 V	V _{CC} = 3.3 V	UNIT
				TYP	TYP	
C _{pd}	Power dissipation capacitance per bit (one output switching)	One $\overline{\text{OE}}$ enabled	C _L = 0, f = 10 MHz	17	17.5	pF
		All outputs disabled		0.4	0.5	



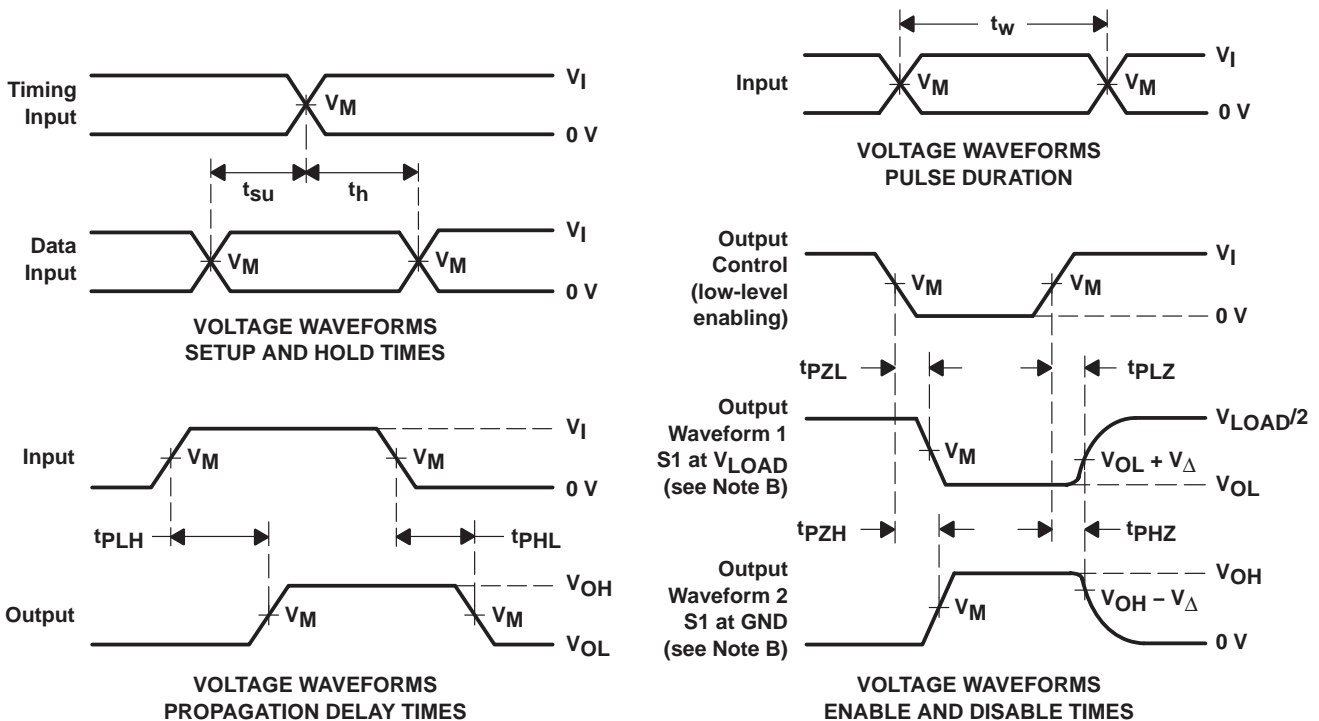
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{LOAD} GND

V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74ALVCHS162830AGR	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ALVCHS162830AGRE4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ALVCHS162830AGRG4	ACTIVE	TSSOP	DBB	80	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

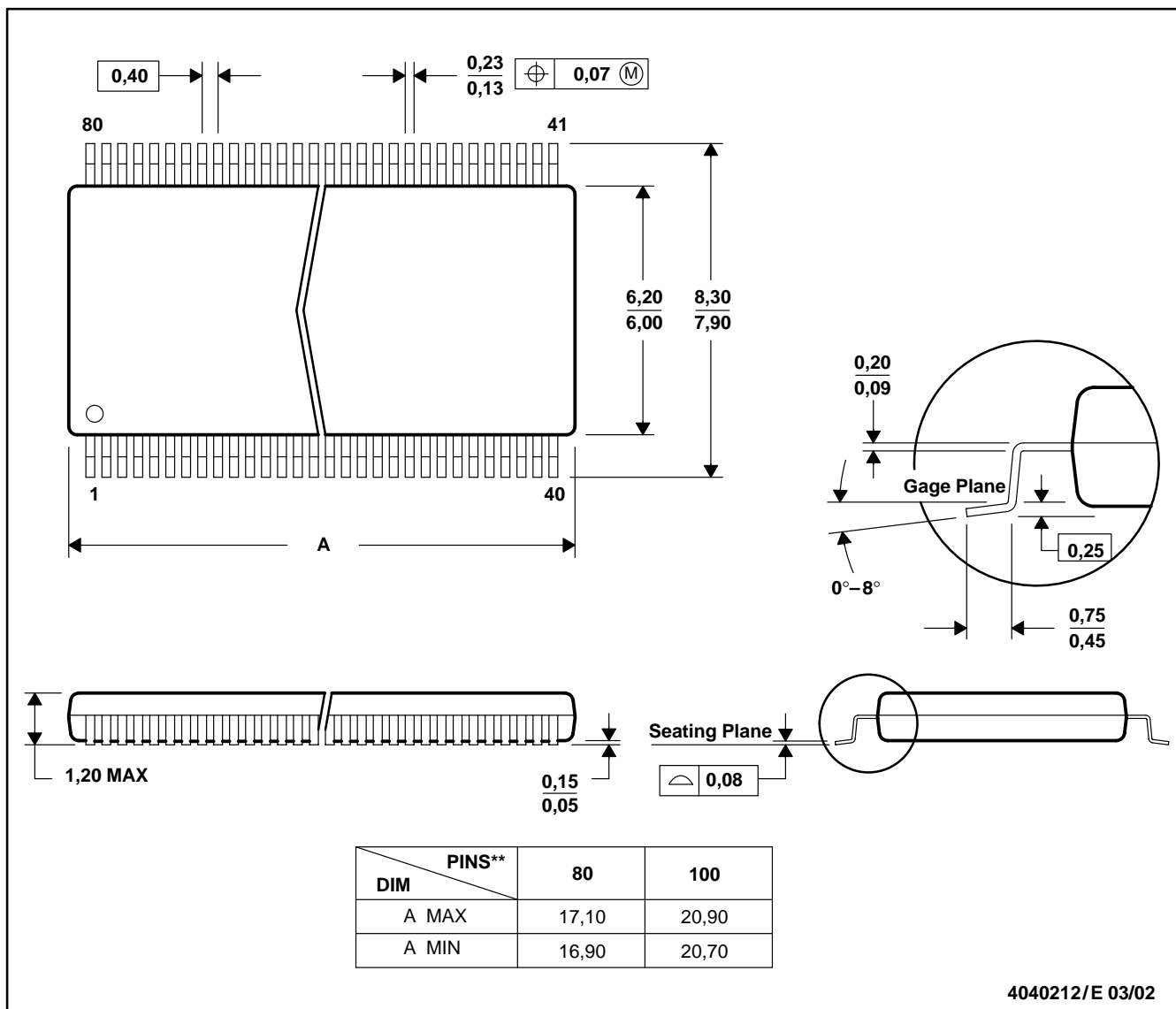
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DBB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

80 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC : 80 Pin – MO-153 Variation FF
 100 Pin – MO-194 Variation BB

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