T-46-07-(ス 54AC16822, 54ACT16822 74AC16822, 74ACT16822 20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS T10253-D3576, JUNE 1990

- Members of Texas Instruments Widebus™ Family
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Centerto-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed VCC and GND Pin Configuration.
 Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16822 and 'ACT16822 are inverting 20-bit D-type flip-flops composed of two 10-bit sections with separate control signals. For either 10-bit flip-flop section, the inverse of the data present at the corresponding D inputs is stored in the flip-flops on the rising edge of the clock input (1CLK or 2CLK) and appears on the appropriate Q outputs if the output enable $1\overline{OE}$ (or $2\overline{OE}$) is low. If $1\overline{OE}$ (or $2\overline{OE}$) is high, the outputs are in the high-impedance state. $1\overline{OE}$ (or $2\overline{OE}$) does not affect the operation of the flip-flops. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

54AC16822, 54ACT16822 ... WD PACKAGE 74AC16822, 74ACT16822 ... DL PACKAGE (TOP VIEW)

10E [T	U 56	□1CLK
1Q1[]2	55	1D1
102 [3	54	1 DZ
GND [4	53	GND
1Q3 [5	52	∏1 0 3
1Q4 [6	51	<u> </u>
V _{CC} [7	50	تي∨ٍc ⊡
1Q5 [8	49	105
1Q6 [9	48	1D6
1Q7 []10	47	1D7
GND [Įı,	46	GND
1Q8 [12	45	∐1 Ď8
1Q9 [13	44]1D̄9
1010	14	43]1D10
2Q1[15	42]2D1
202	16	41	_] 2D̃2
2Q3 [17	40	_] 2Ď3
GND [18	39	GND
2Q4 [19	38	□ 2D̄4
2Q5 [20	37] 2D5
2Q6 [21	36] 2D̃6
V _{CC}	22	35	ן ∨ _{cc}
2Q7 [23	34] 2D7
2Q8 [24	33] 2D̄8
GND [25	32	GND
2Q9 🗌		31	
2Q10 [27	30	
20E [28	29	2CLK

FUNCTION TABLE, EACH SECTION

INPUTS			1	
CLK	ŌĒ	FLIP-FLOP DATA	Q OUTPUTS	
1	Н	Current D Data	z	
Ļ	Н	Previous D Data	Z	
	L.	Current D Data	Inverse of Current D Data	
L	L	Previous D Data	Inverse of Previous D Data	

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54AC16822, 54ACT16822 74AC16822, 74ACT16822

20-BIT D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

D3576, JUNE 1990-TI0253

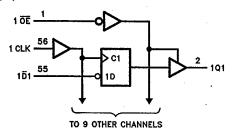
T-46-07-12

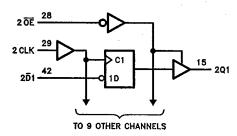
The 74AC16822 and 74ACT16822 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16822 has CMOS-compatible input thresholds. The 'ACT16822 has TTL-compatible input thresholds.

The 54AC16822 and 54ACT16822 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16822 and 74ACT16822 are characterized for operation from -40°C to 85°C.

logic diagram (positive logic)





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