# 73M1866B/73M1966B

# GUI User Guide

March 23, 2009
Rev. 1.1
UG_1x66B_002

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# 1 Introduction

The 73M1866B/73M1966B Graphical User Interface (GUI) provides control of the 73M1866B and 73M1966B registers. The GUI is used to configure the 73M1866B and 73M1966B demo boards and to read the status conditions of these boards. This document applies to GUI software version 1.3.

The GUI can be use with either the Demo Board or the Keychain Board. The GUI cannot be used if the SPI is connected to a host device. For example, if a Keychain Board is embedded in an application, use the appropriate driver (MIPS, ARM, etc.) to configure the Keychain Board.

Install the GUI on a PC running Microsoft Windows® versions XP, Me or 2000. The installation requires one megabyte of disk storage.

In this user guide, the 73M1866B and 73M1966B will be collectively referred to as the 73M1x66B.

The FPGA controls are not for customer use. Do not change the parameters on the FPGA tab.

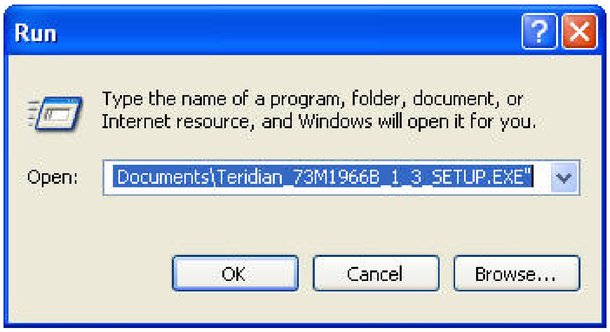
Similarly, do not select FPGA Functions from the Controls menu or use the functions on the FPGA Memory Functions screen.

# 2 Getting Started

This section describes how to install, start and use the GUI software.

## 2.1 GUI Installation

Load the GUI software from the CD onto the PC that will be used to control the configuration of the 73M1x66B Demo Board.



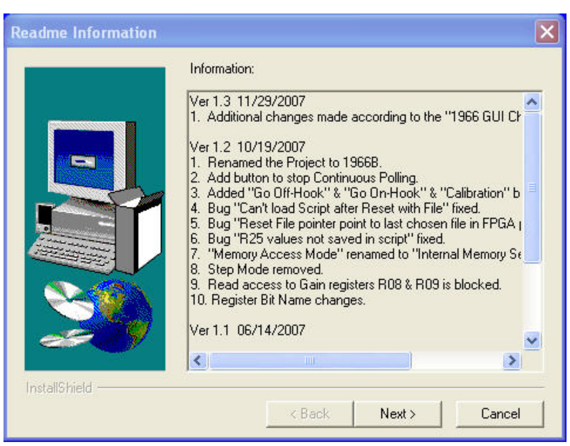

If the GUI software does not run automatically when the CD is installed, select Start → Run and browse the CD drive for Teridian_73M1966_1_3_SETUP.EXE.

Select OK. The following window appears.


Select Run.

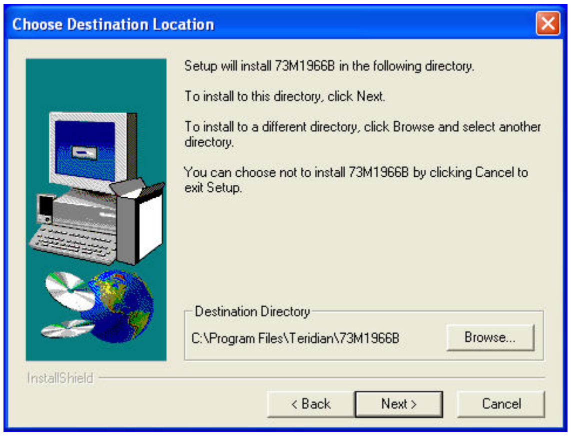

Select Yes to continue.

The following window appears.



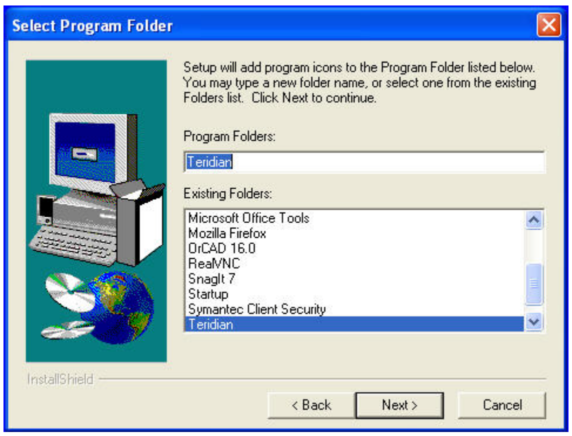

This window lists the revisions of the GUI software and the improvements made in each revision.

Select Next. The following window appears.

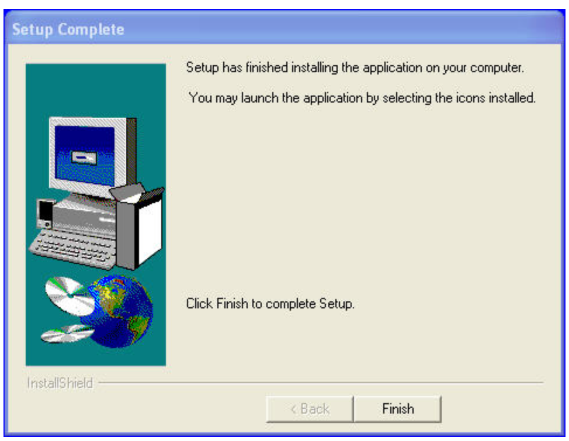



This window shows the default destination for the GUI software

Select Next. The following window appears.




The user can change the destination folder from the default. Change the destination folder or select Next to accept the default folder. The GUI software loads into the specified folder and the following window appears.




The setup is complete. Click Finish. The software is ready for use.

## 2.2 Using the GUI

The 73M1866B or 73M1966B Demo Board must be set up before using the GUI. See the *73M1866B/73M1966B Demo Board User Manual* for setup procedures.

To start the GUI using Windows XP, select Start → All Programs → Teridian → Teridian 73M1966B.

The Register Access screen appears (see Figure 1). The screen is divided into a top half and a bottom half. The first row of the top half consists of five tabs: R00-R09, R0A-R12, R13-R1B, R1C-R25 and FPGA.

The R00-R09 tab displays the register map for the first ten 73M1966B registers. The contents of each named bit can be changed by checking or un-checking the box next to it. A checked box means that the bit is set to 1 and an un-checked box means that the bit is set to 0. As boxes are checked and unchecked, the values in the bottom half reflect the changes and turn red. Select new values by checking and un-checking register bits. Click the Write Red button to set the values. Notice that after writing the values, all previously red values turn black. Polling can be done by double clicking on the lower register map for the register you are interested in or using the "Read All" radio button.

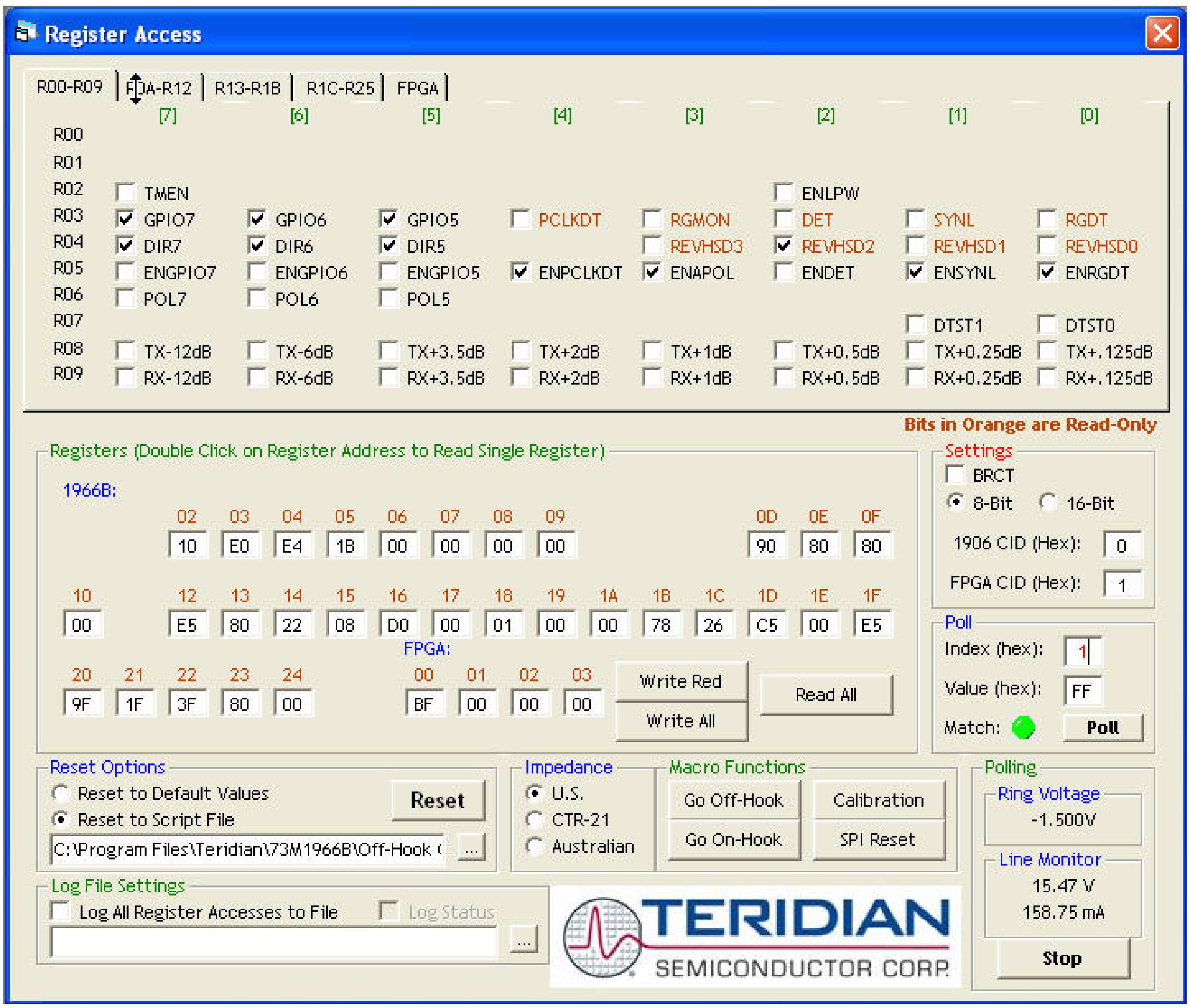
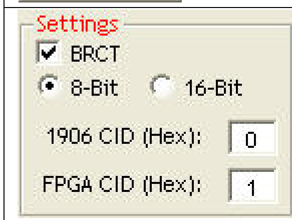
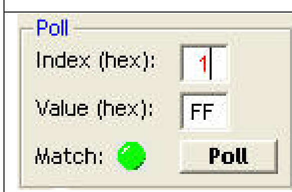


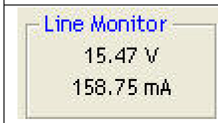

**Figure 1: Register Access Screen – R00-R09 Tab**

The bottom half of the Register Access screen shows the status of the entire 73M1x66B register set (in hex) and provides information and parameter controls.

Table 1 describes these controls.

**Table 1: GUI Controls**

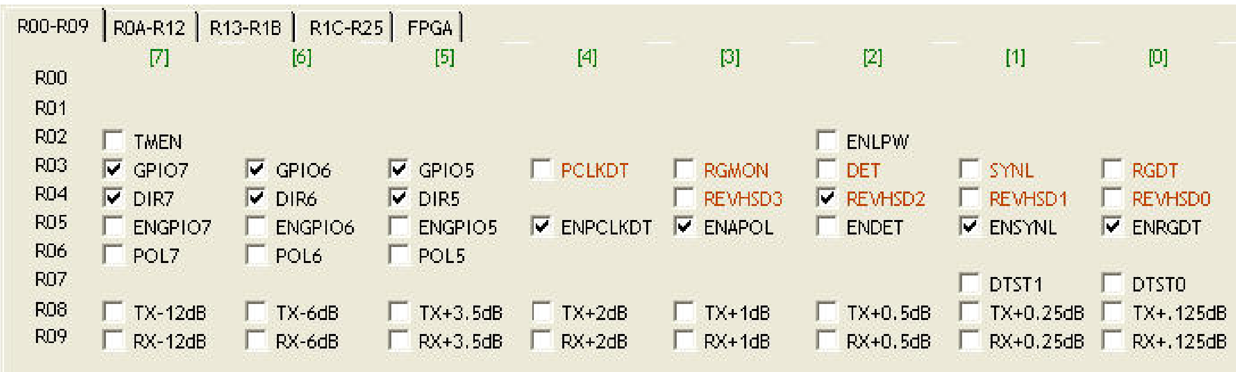
| | |
|---|---|
|  | Click Write Red to write all red values in the bottom half of the screen. Values become red when changed by checking or un-checking boxes in the top half of the screen. Click Write all to write all values (both read and black). After writing values, all values become black and remain black until another box is checked. |
|  | Click to read all current values from the board. |
|  | Select BRCT (BroadCasT) to send the same control data to all the 73M1966Bs in a daisy chain, ignoring their individual addresses. When using the 73M1966B in daisy chain mode, it is necessary to set the address of the 73M1966B that is being accessed. Each board has a 73M1906B and FPGA address. For example, the next downstream daisy chained 73M1966B board will have an address for its 73M1906B of 03h and its FPGA address will be 04h, and so on. See Section 5 of the *73M1866/73M1966 Data Sheet* for a description of the control byte and the BRCT bit. The radio buttons allow the selection of 8-bit or 16-bit SPI operations. |
|  | Implements the POLL function as described in Section 6.1 of the *73M1866B/73M1966B Data Sheet*. The Index field corresponds to the INDX field (Register 0x19[3:0]). The Value field corresponds to the POLVAL field (Register 0x1F[7:0]). Index is the offset address of the register to be manually polled with the results placed in POLVAL. The Index value ranges from 0 to 6 only. Index 0 refers to Register 0x12, Index 1 to Register 0x13, etc. The Value field returns the content of the register corresponding to the specified Index. Enter the index in the Index box. Select Poll. When this register is polled, the value is read back in the Value box. After selecting Poll, a red dot next to Match means that the register was not properly written. A green dot proves that the register was properly written. |
|  | Sets the registers to a default operating configuration. This is not the same as the default register settings after the 73M1x66 goes through a device reset. The default register settings may not be appropriate for all PCM test sets, so you may define your own default operating conditions. |

| | |
|---|---|
|  | Sets the registers to a user-defined configuration contained in a specified script file. This is used to quickly put the registers into a configuration and the 73M1x66 into operational mode without having to individually set the register bits. If you have a configuration that you will use again later, the configuration can be saved as a script. See Log All Register Accesses to File. |
|  | Used to keep a record of all register accesses performed by the user. Once turned on, user transactions are recorded in the file specified in the window. This is used to record a sequence of operations that can be edited and saved as a script. To use the recorded configuration, see Reset to Script File. |
|  | If Log Status is checked, all SPI transactions are recorded in the specified file, including those generated by the background line condition monitoring routine (line voltage, current, etc.). If Log Status is checked and line condition monitoring is activated, be aware that the log file is continuously increasing in size. |
|  | The settings for the three most common termination impedances. These are U.S. (600 Ω), CTR-21 (complex) and Australian (Australian complex). Select one to set the termination impedance. After activating the Read All radio button, the currently valid impedance is indicated only if it is one of the three choices. If the currently valid impedance is not one of the three choices, none of the options will be shown as active. |
|  | Goes Off-Hook. |
|  | Goes On-Hook. |
|  | Calibrates the receive channel of the chipset. |
|  | If the SPI transactions are corrupted for some reason, pressing this button resets the 73M1966B SPI state machine and restores proper communication between the 73M1966B and the GUI. |
|  | Updated with the most recent ring signal voltage as measured in R1A. This measurement is only valid during the on-hook state. |
|  | Displays the DC voltage and DC current from the CO or line emulator. The current reading is valid in off-hook mode only. |
|  | Stops the continuous line condition monitoring routine. Line voltage, current, etc. will not be written to the log file. |
|  | Starts the continuous line condition monitoring routine. Line voltage, current, etc. will be written to the log file. |

### 2.2.1 Controls for Registers R00 to R09

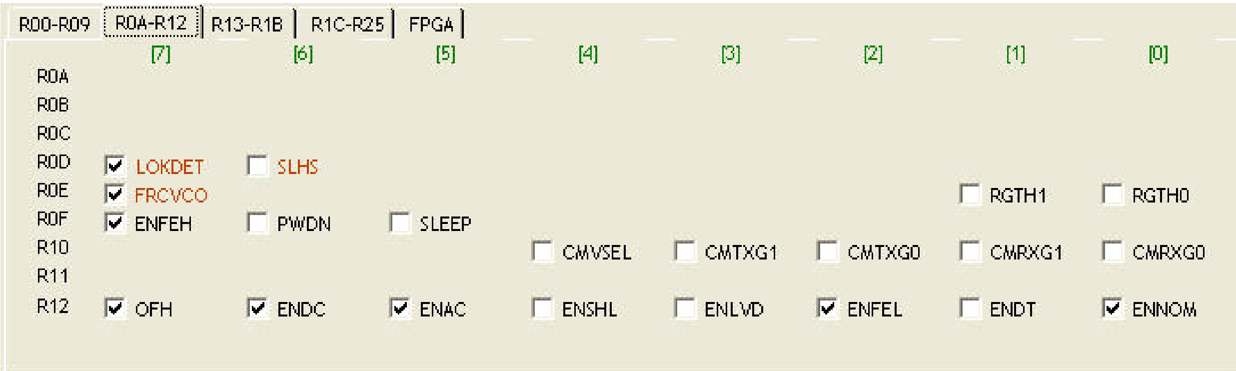
The GUI represents 73M1x66B registers in the form Rhh, where hh is the hexadecimal address. The *73M1866B/73M1966B Data Sheet* represents these same registers in the form 0xhh.

For detailed descriptions of 73M1x66B registers, see the *73M1866B/73M1966B Data Sheet*. The tables below list the section numbers in the *73M1866B/73M1966B Data Sheet* where additional information can be found about each bit.



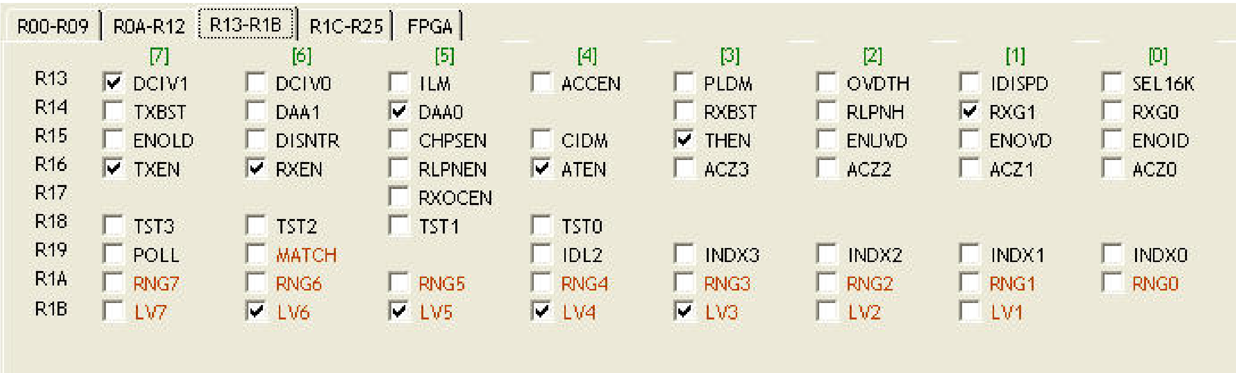

| Register | Bit Name | Summary Description | Data Sheet Section |
|---|---|---|---|
| R02[7] | TMEN | Test Mode Enable | 12.7 |
| R02[2] | ENLPW | Enable Line Power | 9.5 |
| R03[7:5] | GPIOn | GPIO Pin Enable | 7.5 |
| R03[4] | PCLKDT | PCLK Error Detected | 8.8 |
| R03[3] | RGMON | Ringing Monitor – 0 = silent, 1 = ringing | 11.12 |
| R03[2] | DET | Voltage Detection – 1 = detection of one of three conditions | 11.12 |
| R03[1] | SYNL | Barrier Synchronization Loss has occurred | 9.5 |
| R03[0] | RGDT | Ring or Line Reversal Detection – 1 = a Latched Ring or Line Reversal Detection event | 11.12 |
| R04[7:5] | DIRn | GPIO Input/Output Select – 0 = GPIO pin is an output,<br>1 = GPIO pin an input | 7.5 |
| R04[3:0] | REVHSDn | Host-Side Device Revision | 7.1 |
| R05[7:5] | ENGPIOn | GPIO Enable | 7.5 |
| R05[4] | ENPCLKDT | Enable PCLK Detection | 8.8 |
| R05[3] | ENAPOL | Enable Automatic Polling | 9.5 |
| R05[2] | ENDET | Enable Voltage Detection | 11.12 |
| R05[1] | ENSYNL | Enable Synch Loss Detection | 9.5 |
| R05[0] | ENRGDT | Enable Ring Detection Interrupt | 11.12 |
| R06[7:5] | POLn | GPIO Interrupt Edge Selection | 7.5 |
| R07[1:0] | DTSTn | Digital Test Mode Select | 12.7 |
| R08 | TXDGn | Transmitter Digital | 8.8 |
| R09 | RXDGn | Receiver Digital Gain | 8.8 |

### 2.2.2 Controls for Registers R0A to R12




| Register | Bit Name | Summary Description | Data Sheet Section |
|---|---|---|---|
| R0D[7] | LOKDET | Phase Locked Loop Lock Detect | 7.4 |
| R0D[6] | SLHS | Synchronized Lost Host Side | 9.5 |
| R0E[7] | FRCVCO | Force VCO | 7.4 |
| R0E[1:0] | RGTHn | Ring Detect Threshold | 11.12 |
| R0F[7] | ENFEH | Enable Front End Host | 7.3 |
| R0F[6] | PWDN | Power Down Mode | 7.3 |
| R0F[5] | SLEEP | Sleep Mode | 7.3 |
| R10[4] | CMVSEL | Call Progress Monitor Voltage Reference Select | 7.6 |
| R10[3:2] | CMTXGn | Transmit Path Gain Setting | 7.6 |
| R10[1:0] | CMRXGn | Receive Path Gain Setting | 7.6 |
| R12[7] | OFH | Off-Hook Enable | 10.6 |
| R12[6] | ENDC | Enable DC Transconductance Circuit | 10.6 |
| R12[5] | ENAC | Enable AC Transconductance Circuit | 10.6 |
| R12[4] | ENSHL | Enable Shunt Loading | 10.6 |
| R12[3] | $\overline{\text{ENLVD}}$ | LeV Detection (OVDET, UVDET, OIDET monitors) | 10.6 |
| R12[2] | ENFEL | Enable Front End Line-Side Circuit | 10.6 |
| R12[1] | ENDT | Enable Detectors | 11.12 |
| R12[0] | ENNOM | Enable Nominal Operation | 10.6 |

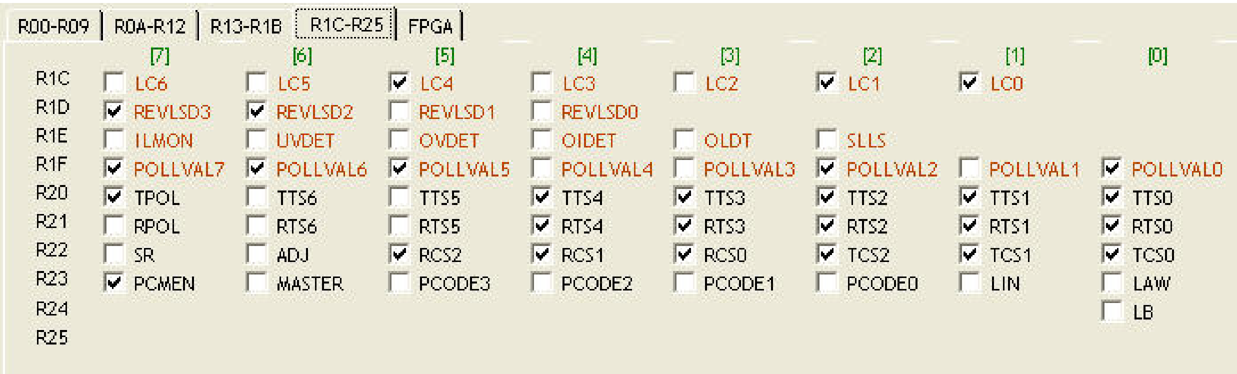
### 2.2.3 Controls for Registers R13 to R1C




| Register | Bit Name | Summary Description | Data Sheet Section |
|---|---|---|---|
| R13[7:6] | DCIVn | DC Current Voltage Characteristic Control | 10.6 |
| R13[5] | ILM | Current Limit Enable – 0 = no limit, 1 = 42 mA current limit | 10.6 |
| R13[4] | ACCEN | AC Cancellation Enable | 10.6 |
| R13[3] | PLDM | Pulse Dialing Enable | 10.6 |
| R13[2] | OVDTH | Over-Voltage Threshold | 11.12 |
| R13[1] | IDISPD | Discharge and Pulse Dialing | 10.6 |
| R13[0] | SEL16K | Sample Rate Mode Configuration Select | 8.8 |
| R14[7] | TXBST | Transmit Boost | 8.8 |
| R14[6:5] | DAAn | Data Access Arrangement<br>Used with TXBST to manage transmit level. | 8.8 |
| R14[3] | RXBST | Received Boost<br>If set to 1, receive signal is increased by 20 dB. | 8.8 |
| R14[2] | RLPNH | Receive Low Pass Notch<br>0 = Selects Receive Low Pass Notch (RLPN) at 12 kHz.<br>1 = Selects RLPN at 16 kHz. | 10.6 |
| R14[1:0] | RXGn | Receive Gain Control | 8.8 |
| R15[7] | ENOLD | Enable Over-Load Detector | 11.12 |
| R15[6] | DISNTR | Disable No-Transition Timer | 11.12 |
| R15[5] | CHPSEN | Enable Chopper Stabilization | 10.6 |
| R15[4] | CIDM | Caller ID Mode | 11.12 |
| R15[3] | THEN | Enable Transhybrid Circuit | 10.6 |
| R15[2] | ENUVD | Enable Under Voltage Detector | 11.12 |
| R15[1] | ENOVD | Enable Over-Voltage Detector | 11.12 |
| R15[0] | ENOID | Enable Over-Current Detector | 11.12 |
| R16[7] | TXEN | Transmit Path Enable | 8.8 |
| R16[6] | RXEN | Receive Path Enable | 8.8 |
| R16[5] | RLPNEN | Receive Low Pass Notch Enable | 10.6 |
| R16[4] | ATEN | Active Termination Loop Enable | 10.6 |
| R16[3:0] | ACZn | Active Termination Loops | 10.6 |
| R17[5] | RXOCEN | Rx DC Offset Calibrate Enable | 8.8 |
| R18[7:4] | TESTn | Enable Loopback Mode | 12.7 |
| R19[7] | POLL | Polling Enable | 6.1 |

| Register | Bit Name | Summary Description | Data Sheet Section |
|---|---|---|---|
| R19[6] | MATCH | Polling Match | 6.1 |
| R19[4] | IDL2 | Ring Detect Functions | 7.3 |
| R19[3:0] | INDXn | Index<br>Address of the register to be manually polled with the results placed in POLVAL. | 6.1 |
| R1A[7:0] | RNGn | Result of Auxiliary A/D measuring the attenuated ring voltage. | 11.12 |
| R1B[7:1] | LVn | Line Voltage Reading | 11.12 |

### 2.2.4 Controls for Registers R1D to R23




| Registers | | Description | Data Sheet Section |
|---|---|---|---|
| R1C[7:1] | LCn | Loop Current | 11.12 |
| R1D[7:4] | REVLSDn | Line-Side Device Revision | 7.1 |
| R1E[7] | ILMON | Current Limit Mode On | 10.6 |
| R1E[6] | UVDET | Under-Voltage Detector | 11.12 |
| R1E[5] | OVDET | Over-Voltage Detector | 11.12 |
| R1E[4] | OIDET | Over-Current (I) Detector | 11.12 |
| R1E[3] | OLDET | Over-Load Detector | 11.12 |
| R1E[2] | SLLS | Synchronization Loss Line Side | 9.5 |
| R1F[7:0] | POLLVALn | Polling Value<br>When polled, the content of the Line-Side Device Register | 6.1 |
| R20[7] | TPOL | Transmit Polarity | 8.8 |
| R20[6:0] | TTSn | Transmit Time Slot | 8.8 |
| R21[7] | RPOL | Receive Polarity | 8.8 |
| R21[6:0] | RTSn | Receive Time Slot | 8.8 |
| R22[7] | SR | Sampling Rate Mode | 8.8 |
| R22[6] | ADJ | Adjacent Time Slots | 8.8 |
| R22[5:3] | RCSn | Receive Clock Slot | 8.8 |
| R22[2:0] | TCSn | Transmit Clock Slot | 8.8 |
| R23[7] | PCMEN | PCM Transmit Enable | 8.8 |
| R23[6] | MASTER | Master/Slave Mode<br>0 = enables Slave Mode; 1 = enables Master Mode. | 8.8 |
| R23[5:2] | PCODEn | PCM Clock Code | 8.8 |
| R23[1] | LIN | Linear Mode Enable | 8.8 |
| R23[0] | LAW | Law Compression Mode<br>0 = selects A-law; 1 = selects μ-law. | 8.8 |
| R24[0] | LB | Enables PCM Loopback within the Host-Side Device. | 12.7 |

# 3 Scripts

If you have a configuration that will be used again later, the configuration can be saved by simple saving the current configuration by selecting “Save As Script” from the “File” drop-down menu. This will save ALL the register status information. Once the file has been saved, it can be edited so that only the registers you are interested in changing are contained in the file. The “Save As Script” function will save everything including all the read only registers.

Scripts can be used to set up any static state you wish, but are limited to just setting the registers. There is not a provision to do delays between the sequences of register settings. You cannot, for instance, pulse dial with a script. Usually this should not be a significant limitation since normally only one static configuration is used at a time. To load a saved configuration, select the button under the Reset radio button or Load Script from the File menu and select the file that you want to load.

The CD contains sample scripts that can be used to quickly configure the board for specific purposes. This is a listing of the “setup-wg-init_ofh.tsf” file. Everything necessary for operation is included in this script.

```
' 73M1966B Test Script File - setup-wg-init _ofh.tsf
' This script initializes the the 1966 registers
' after a hardware reset.  It selects time slot 0
' operation. Make sure hardware reset is performed
' first!  The 1966 will go off hook when executed.
'
' Script Format (All Values in Hex)
' Write Register: W,Mode,BRCT,CID,Address,Data
' Read Register:  R,Mode,CID,Address,Data
'                 Mode: 0=8-Bit, 1=16-Bit
'                 BRCT: Only used in Write
'                 CID, Address, Data: Hex Value
'
'      GPIO5-7 inputs set high
W,1,0,0,3,E0
'      GPIO5-7 =receivers
W,1,0,0,4,E4
'      Enable detectors, polling ID
W,1,0,0,5,1B
'      Enable line side device
W,1,0,0,F,80
'      Enable OFH, DC, AC, FE, ENNOM
W,1,0,0,12,E5
'      Set DCIV=10
W,1,0,0,13,80
'      Set DAA=01, RXG=10
W,1,0,0,14,22
'      Enable THEN
W,1,0,0,15,08
'      Enable TXEN, RXEN, ATEN
W,1,0,0,16,D0
'      Set DX polarity, timeslot 0
W,1,0,0,20,9F
'      Set DR polarity, timeslot 0
W,1,0,0,21,1F
'      Set clock slot for timeslot 0
W,1,0,0,22,3F
'      Enable PCM
W,1,0,0,23,80
```

This is a listing of the “ring-rev-set-up.tsf” file:

```
'   Script - ring-rev-set-up (ON hook)
' This script is used to enable the ring/line reversal
' detection or to go ON hook, no CID
' The time slot is not affected and will remain as
' previously programmed
' Script Format (All Values in Hex)
' Write Register: W,Mode,BRCT,CID,Address,Data
'      Write: W, Read: R
'      Mode: 0=8-Bit, 1=16-Bit
'      BRCT: Broadcast only used in Write
'      Chip ID, Address, Data: Hex Value
'
'      Enable detectors, polling ID bits
W,1,0,0,5,13
'      Set ring signal threshold to 15V
W,1,0,0,E,01
'      Enable barrier interface
W,1,0,0,F,80
'      Enable  line side device analog ckts
W,1,0,0,12,04
'      All off hook functions disabled
W,1,0,0,15,00
'      All off hook functions disabled
W,1,0,0,16,00
```

Note that the time slot is not being programmed in this case. This still would need to be done at some point, but it is not necessary to have a time slot selected if the PCM data is not being sent and received. There may also be cases where a specific time slot is being used other than time slot 0, so it would not be desirable to change to time slot zero every time the 73M1966B has a software reset.

In the following program example Caller ID can be received so the PCM receive channel must be configured. If the time slot is not programmed it will not be possible to receive the PCM data when the Caller ID signal is sent. It is not, however, necessary to program the PCMEN bit in register 23h since that is only required to send PCM. The receive analog channel must be turned on for the Caller ID path to be available, so the RXEN bit in register 16h must also be turned on. It was not really necessary to program the transmit channel time slot at this time, but it was done anyway so it won’t need to be done separately later.

```
'   Script - ring-rev-CID-set-up (ON hook)
' This script is used to enable the ring/line reversal
' detection and Caller ID reception
' Script Format (All Values in Hex)
' Write Register: W,Mode,BRCT,CID,Address,Data
'      Write: W, Read: R
'      Mode: 0=8-Bit, 1=16-Bit
'      BRCT: Broadcast only used in Write
'      Chip ID, Address, Data: Hex Value
'
'      Enable detectors, polling ID bits
W,1,0,0,5,13
'      Set ring signal threshold to 15V
W,1,0,0,E,01
'      Enable barrier device interface
W,1,0,0,F,80
'      Enable  line side device analog ckts
W,1,0,0,12,04
'      20dB boost on for CID
W,1,0,0,14,08
'      All off hook functions disabled; CID enabled
W,1,0,0,15,30
```

```
'      Disable off hook functions except RXEN for CID
W,1,0,0,16,40
'      Set DX polarity, timeslot 0 of WG
W,1,0,0,20,9F
'      Set DR polarity, timeslot 0 of WG
W,1,0,0,21,1F
'      Set clock slot for timeslot 0 of WG
W,1,0,0,22,3F
```

# 4 Related Documentation

The following 73M1x66B documents are available from Teridian Semiconductor Corporation:

*73M1866B/73M1966B Data Sheet*
*73M1966B Evaluation Kit User Manual*
*73M1866/73M1966B Demo Board User Manual*
*73M1866/73M1966B Keychain Demo Board User Manual*
*73M1966 Layout Guidelines*
*73M1x66B Worldwide Design Guide*

# 5 Contact Information

For more information about Teridian Semiconductor products or to check the availability of the 73M1866B or 73M1966B, contact us at:

6440 Oak Canyon Road
Suite 100
Irvine, CA 92618-5201

Telephone: (714) 508-8800
FAX: (714) 508-8878
Email: modem.support@teridian.com

For a complete list of worldwide sales offices, go to http://www.teridian.com.

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 1/25/2008 | First publication. |
| 1.1 | 3/23/2009 | Re-wrote Section 3, Scripts.<br>Updated Section 4, Related Documentation. |