

## High Voltage Liquid Crystal **Shutter Driver**

#### **Ordering Information**

| Device | HV <sub>№</sub> Maximum Voltage | Package Options |
|--------|---------------------------------|-----------------|
|        |                                 | SO-8            |
| HV508  | 45V                             | HV508LG         |

#### **Features**

- HVCMOS<sup>®</sup> technology for high performance
- Logic-selectable output voltage
- 100nF drive capability
- □ Up to 90V<sub>P-P</sub>
- 25µs response time

### **General Description**

The Supertex HV508 is a 45V liquid crystal shutter driver in an SO-8 surface mount package. It consist of two outputs that provide square waves of opposite phase. The liquid crystal shutter is connected between the two outputs. Its equivalent load can be approximated as a resistor in parallel with a capacitor. Minimum resistance is  $1.0M\Omega$  and maximum capacitance is  $0.1\mu$ F.

The HV508 has three input supply voltages,  $\mathrm{HV}_{\mathrm{IN}}, \mathrm{LV}_{\mathrm{IN}},$  and  $\mathrm{V}_{\mathrm{DD}}.$ The output's amplitude will be either LV<sub>IN</sub> or HV<sub>IN</sub>. A logic high on the HV<sub>EN</sub> input will set the output to operate from the HV<sub>IN</sub> supply. A logic low on the HV<sub>EN</sub> input will set the output to operate from the LV<sub>IN</sub> supply. The output frequency is set by the logic input frequency applied on the POL input.

# **Absolute Maximum\* Ratings**

| HV <sub>IN</sub> , high voltage input  | +60V            |
|--|-----------------|
| LV <sub>IN</sub> , low voltage input   | +7.5V           |
| V <sub>DD</sub> , logic supply voltage | +12V            |
| Continuous total power dissipation     | 700mW           |
| Operating temperature                  | -5°C to +60°C   |
| Storage temperature                    | -65°C to +150°C |
| Soldering temperature                  | +300°C          |

\* All voltages are referenced to GND.

For operation above 25°C ambient derate linearly at 6mW/°C.



#### 12/13/01

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#### Pin Configuration

## **Electrical Characteristics**

**DC Electrical Characteristics** (over operating supply voltages unless otherwise specified,  $T_A = -5^{\circ}C$  to  $+60^{\circ}C$ )

| Symbol            | Parameter                          | Min | Тур | Мах  | Unit | Conditions  |
|-------------------|------------------------------------|-----|-----|------|------|---|
| I <sub>HVQ</sub>  | HV <sub>IN</sub> quiescent current |     |     | 10   | μΑ   |   |
| I <sub>LVQ</sub>  | LV <sub>IN</sub> quiescent current |     |     | 10   | μΑ   |   |
| I <sub>DDQ</sub>  | V <sub>DD</sub> quiescent current  |     |     | 10   | μΑ   |   |
| I <sub>HV</sub>   | HV <sub>IN</sub> operating current |     |     | 2.8  | mA   | $\begin{array}{l} POL = 100Hz, \ HV_{EN} = high, \\ T_A = 25^{\circ}C, \ Load = 1M\Omega \ in \ parallel \\ with \ 0.1\mu F \ between \ HV_{OUT1} \ and \\ HV_{OUT2} \end{array}$ |
| I <sub>LV</sub>   | LV <sub>IN</sub> operating current |     |     | 380  | μA   | $\begin{array}{l} POL = 100Hz, \ HV_{EN} = low, \\ T_A = 25^{\circ}C, \ Load = 1M\Omega \ in \ parallel \\ with \ 0.1\mu F \ between \ HV_{OUT1} \ and \\ HV_{OUT2} \end{array}$  |
| I <sub>IL</sub>   | Logic input current low            | -5  |     |      | μA   |   |
| I <sub>IH</sub>   | Logic input current high           |     |     | 5.0  | μΑ   |   |
| C <sub>LOAD</sub> | Output capacitive load*            | 0   |     | 0.25 | μF   | $C_{\text{LOAD}}$ in parallel with a $1M\Omega$ resistor  |

\*The device can operate continuously without any damage within this range. AC limits are not implemented.

#### **AC Electrical Characteristics** (HV<sub>IN</sub> = 45V, LV<sub>IN</sub> = 6V, V<sub>DD</sub> = 5V, T<sub>A</sub> = -5°C to +60°C)

| Symbol               | Parameter                                   | Min | Тур | Max | Unit | Conditions  |  |
|----------------------|---|-----|-----|-----|------|---|--|
| f <sub>POL</sub>     | POL input frequency                         | 0   |     | 100 | Hz   |   |  |
| t <sub>HV(ON)</sub>  | Turn-on time when high voltage is enable    |     |     | 16  | μS   | Load = $1M\Omega$ in parallel with $0.1\mu$ F between HVours and HVours.  |  |
| t <sub>HV(OFF)</sub> | Turn-off time when high voltage is enabled  |     |     | 16  | μS   | $HV_{EN} = High.$ Outputs rise to $HV_{IN}$ .<br>See Fig. 1.  |  |
| t <sub>LV(ON)</sub>  | Turn-on time when high voltage is disabled  |     |     | 40  | μS   | Load = $1M\Omega$ in parallel with $0.1\mu$ F   |  |
| t <sub>LV(OFF)</sub> | Turn-off time when high voltage is disabled |     |     | 6.0 | μs   | $HV_{EN} = Low.$ Outputs rise to $LV_{IN}$<br>See Fig. 1.   |  |
| t <sub>EN(ON)</sub>  | Turn-on time from $HV_{EN}$ to $HV_{OUT}$   |     |     | 25  | μs   | Load = $1M\Omega$ in parallel with $0.1\mu$ F<br>between HV <sub>OUT1</sub> and HV <sub>OUT2</sub> .<br>See Fig. 2. |  |

#### **Recommended Operating Conditions**

| Symbol           | Parameter                  | Min                | Тур | Max             | Unit |
|------------------|----------------------------|--------------------|-----|-----------------|------|
| V <sub>DD</sub>  | Logic supply voltage       | 5.0                |     | 10.0            | V    |
| LV <sub>IN</sub> | Low output supply voltage  | 3.0                |     | 6.0             | V    |
| HV <sub>IN</sub> | High output supply voltage | 5.0                |     | 45              | V    |
| V <sub>IL</sub>  | Logic input voltage low    | 0                  |     | $0.3V_{DD}$     | V    |
| V <sub>IH</sub>  | Logic input voltage high   | 0.7V <sub>DD</sub> |     | V <sub>DD</sub> | V    |
| T <sub>A</sub>   | Ambient Temperature        | -5.0               |     | +60             | °C   |

#### Notes:

Power-up sequence should be the following:

1. Connect GND,  $V_{DD}$ , logic inputs,  $HV_{IN}$ , and  $LV_{IN}$ .

Power-down sequence should be the reverse of the above.

## Truth Table

| HV <sub>EN</sub> | POL | HV <sub>OUT1</sub> | HV <sub>OUT2</sub> |
|------------------|-----|--------------------|--------------------|
| н                | Н   | HV <sub>IN</sub>   | GND                |
| н                | L   | GND                | HV <sub>IN</sub>   |
| L                | Н   | LV                 | GND                |
| L                | L   | GND                | LV                 |

## **Timing Diagram**









## **Block Diagram**





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