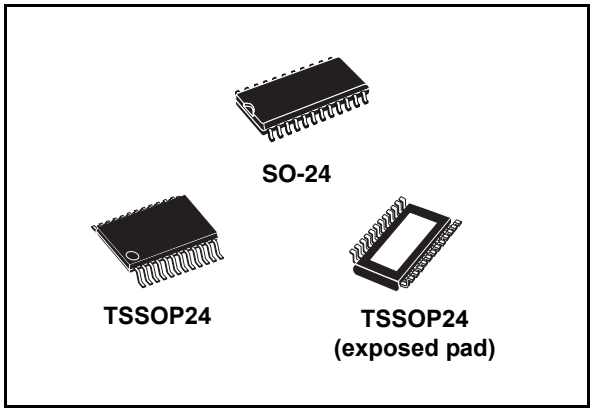
STP16CPS05

Low voltage 16-bit constant current LED sink driver with auto power saving

Features

- Low voltage power supply down to 3V
- 16 constant current output channels
- Adjustable output current through external resistor
- Serial Data IN/Parallel Data OUT
- Auto power-saving feature minimizes the quiescent current if no active data is detected on the latches
- Can be driven by a 3.3V microcontroller
- Output current: 5-100mA
- Max clock frequency 30MHz
- ESD protection 2.5kV HBM, 200V MM



Description

The STP16CPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPS05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 5mA to 100mA constant current to drive the LEDs.

The Auto Power Shut-Down and Auto Power-ON feature allows the device to save power without any external intervention.

The output current setup time is 40ns (typ), thus improving the system performance.

The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPS05 output current.

The STP16CPS05 guarantees a 20V output driving capability, allowing users to connect more LEDs in series.The high clock frequency, 30MHz, makes the device suitable for high data rate transmission. The 3.3V voltage supply is useful in applications that interface with a 3.3V microcontroller.

Table 1. Device summary

Order codes	Package	Packaging
STP16CPS05MTR	SO-24	1000 parts per reel
STP16CPS05TTR	TSSOP24	2500 parts per reel
STP16CPS05XTTR	TSSOP24 Exposed Pad	2500 parts per reel

Contents

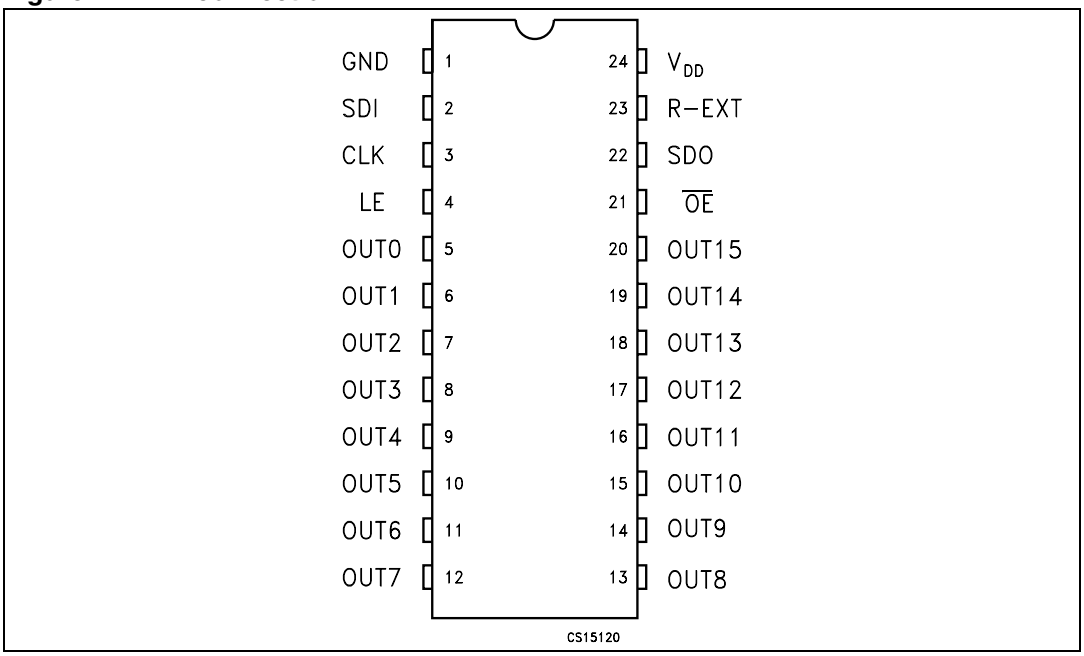
1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	temp.
	Between bits	Between ICs			
≥ 1.3V	±1.5%	±5%	≥20 to 100 mA	3.3V to 5V	25°C

1.1 Pin connection and description

Figure 1. Pin connection



Note: The exposed pad is electrically not connected

Table 3. Pin description

Pin N°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal of an external resistor for constant current programing
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}+0.4	V
I_{GND}	GND terminal current	1600	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJC}	Thermal resistance junction-case	DIP-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24(1) Exposed Pad	37.5	°C/W
		SO-24	75	°C/W

1. The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

Table 6. Recommended operating conditions at 25°C

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	3		100	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		$0.7V_{DD}$		$V_{DD}+0.3$	V
V_{IL}	Input voltage		-0.3		$0.3V_{DD}$	V
t_{wLAT}	LE pulse width	V_{DD} = 3.3V to 5.0V	20			ns
t_{wCLK}	CLK pulse width		16			ns
t_{wEN}	$\overline{OE}$ pulse width		200			ns
$t_{SETUP(D)}$	Setup time for DATA		20			ns
$t_{HOLD(D)}$	Hold time for DATA		15			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

1. If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please considered the timings carefully.

3 Electrical characteristics

Table 7. Electrical characteristics
(V_{DD}=3.3V to 5V, T = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high level		0.7V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20V			10	µA
V_{OL}	Output voltage (Serial-OUT)	I_{OL} = 1mA			0.4	V
V_{OH}	Output voltage (Serial-OUT)	I_{OH} = -1mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3V, R_{ext} = 3.9kΩ	4.25	5	5.75	mA
I_{OL2}		V_O = 0.3V, R_{ext} = 970Ω	19	20	21	
I_{OL3}		V_O = 1.3V, R_{ext} = 190Ω	96	100	104	
ΔI_{OL1}	Output current error between bit (All Output ON)	V_O = 0.3VR_{EXT} = 3.9kΩ		± 5	± 8	%
ΔI_{OL2}		V_O = 0.3VR_{EXT} = 970Ω		± 1.5	± 3	
ΔI_{OL3}		V_O = 1.3VR_{EXT} =190Ω		± 1.2	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	KΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	KΩ
$I_{DD(SH)}$	Shut-down current All Latched Data = L	V_{DD} = 3.3V		70	120	µA
		V_{DD} = 5V		100	150	µA
$I_{DD(OFF1)}$	Supply current (OFF)	R_{EXT} = 970 OUT 0 to 15 = OFF		4		mA
$I_{DD(OFF2)}$		R_{EXT} = 240 OUT 0 to 15 = OFF		11.2		
$I_{DD(ON1)}$	Supply current (ON)	R_{EXT} = 970 OUT 0 to 15 = ON		4.5		
$I_{DD(ON2)}$		R_{EXT} = 240 OUT 0 to 15 = ON		11.7		
Thermal	Thermal protection			170		°C

Table 8. Switching characteristics (V_{DD} = 5V, T = 25°C, unless otherwise specified.)

Symbol	Parameter	Test conditions			Min	Typ	Max	Unit
t_{PLH1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L	V_{DD} = 3.3 V V_{IL} = GND I_O = 20mA R_{EXT} = 1KΩ	$V_{IH} = V_{DD}$ C_L = 10pF V_L = 3.0 V R_L = 60 Ω	V_{DD} = 3.3V		50	70	ns
				V_{DD} = 5V		28	40	
t_{PLH2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L			V_{DD} = 3.3V		48	70	ns
				V_{DD} = 5V		25	40	
t_{PLH3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H			V_{DD} = 3.3V		55	75	ns
				V_{DD} = 5V		35	45	
t_{PLH}	Propagation delay time, CLK-SDO			V_{DD} = 3.3V		11	16	ns
				V_{DD} = 5V		8	12	
t_{PHL1}	Propagation delay time, CLK-$\overline{OUTn}$, LE = H, $\overline{OE}$ = L			V_{DD} = 3.3V		22	30	ns
				V_{DD} = 5V		17	25	
t_{PHL2}	Propagation delay time, LE-$\overline{OUTn}$, $\overline{OE}$ = L			V_{DD} = 3.3V		7	10	ns
				V_{DD} = 5V		4	6	
t_{PHL3}	Propagation delay time, $\overline{OE}$-$\overline{OUTn}$, LE = H			V_{DD} = 3.3V		18	30	ns
				V_{DD} = 5V		15	25	
t_{PHL}	Propagation delay time, CLK-SDO			V_{DD} = 3.3V		12	18	ns
				V_{DD} = 5V		8	12	
t_{ON}	Output rise time 10~90% of voltage waveform			V_{DD} = 3.3V		40	80	ns
				V_{DD} = 5V		22	35	
t_{OFF}	Output fall time 90~10% of voltage waveform			V_{DD} = 3.3V		11	15	ns
				V_{DD} = 5V		18	25	
t_r	CLK rise time (1)						5000	ns
t_f	CLK fall time (1)						5000	ns

1. In order to achieve high cascade data transfer,please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2. $\overline{OE}$ terminal

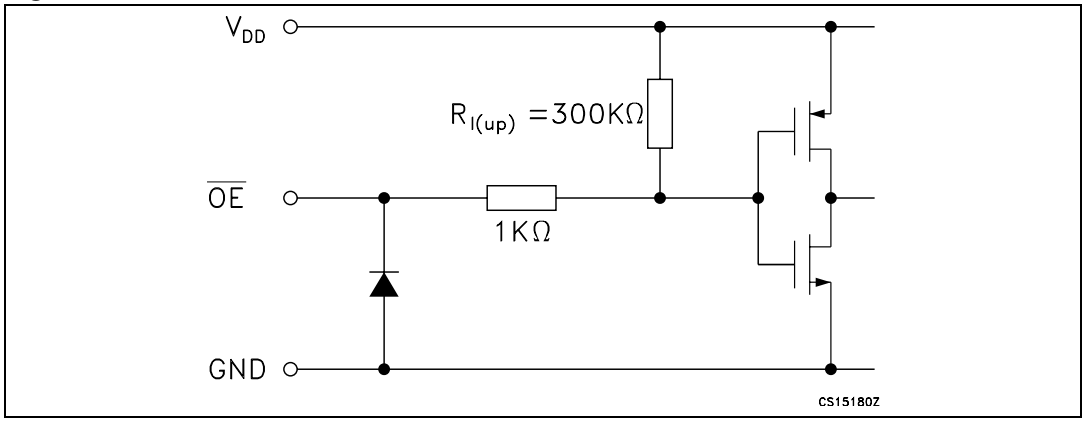


Figure 3. LE terminal

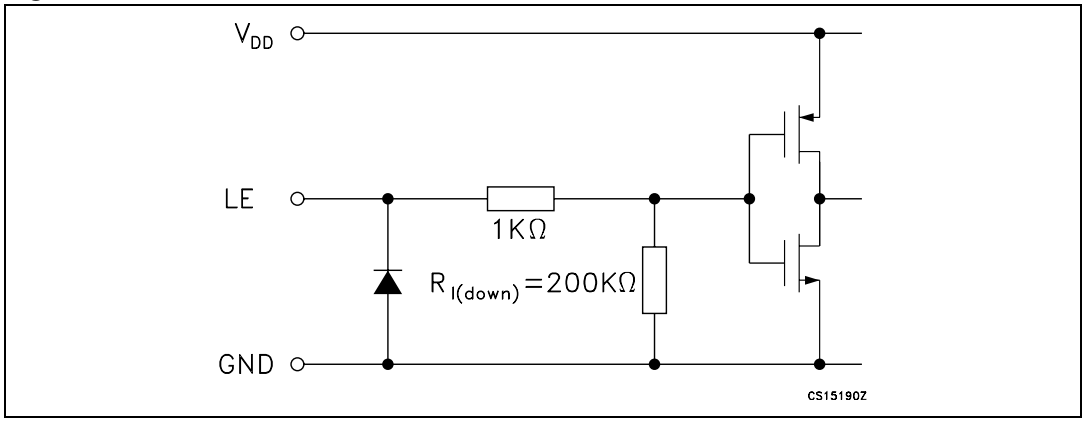


Figure 4. CLK, SDI terminal

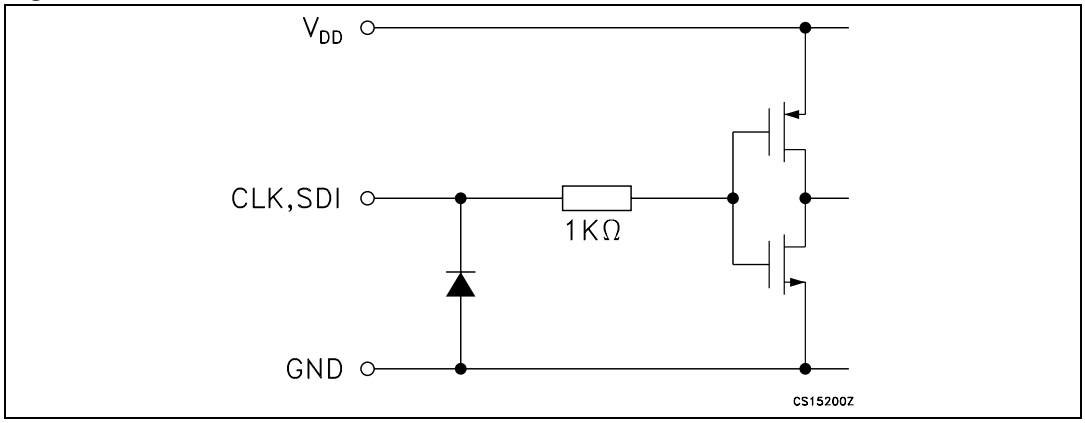


Figure 5. SDO terminal

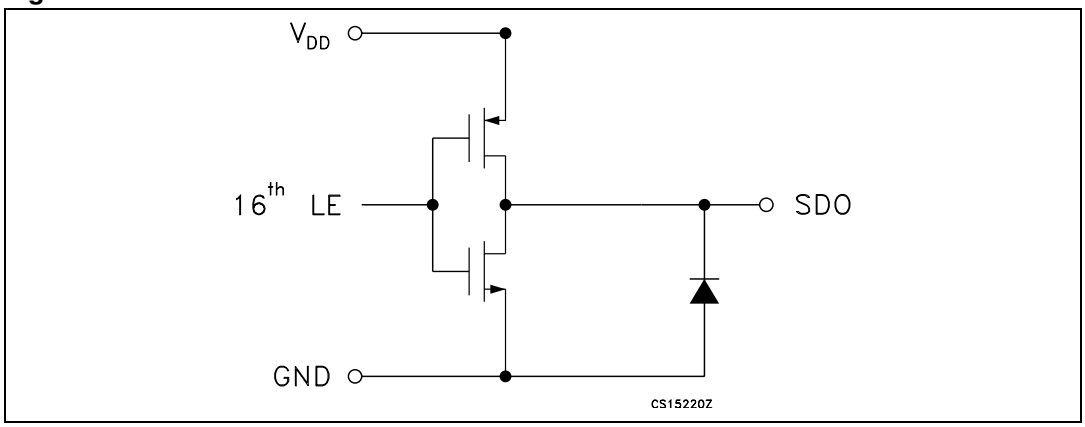
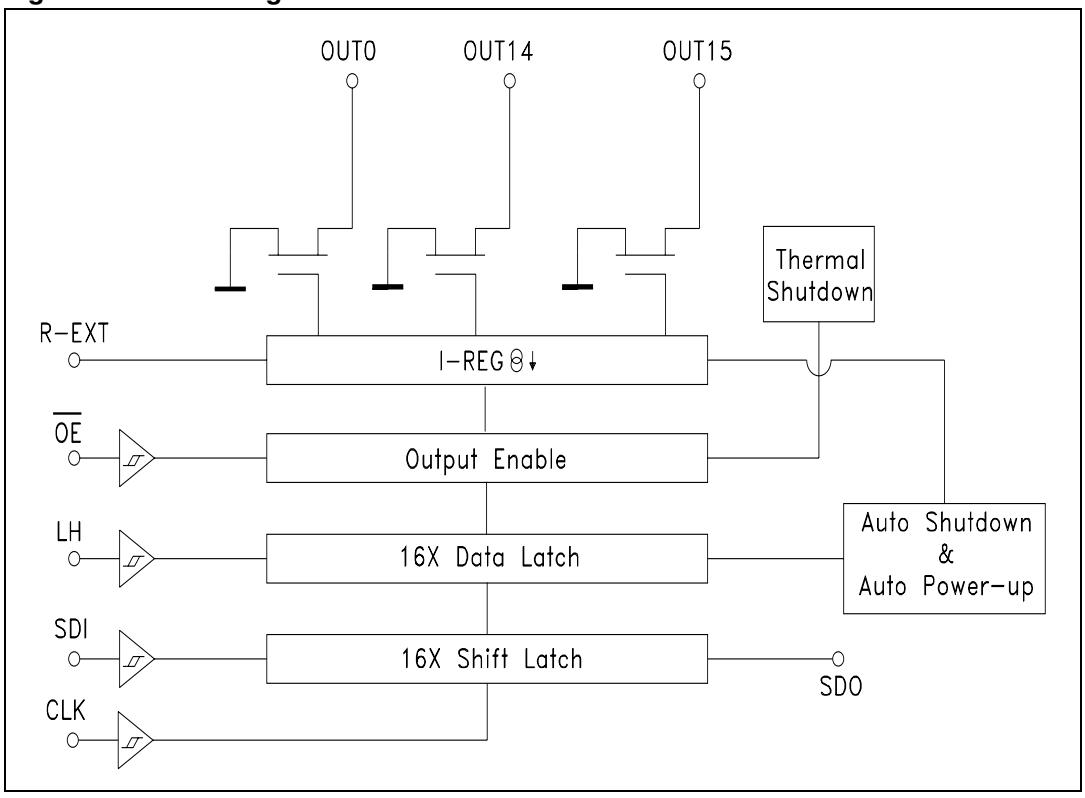


Figure 6. Block diagram



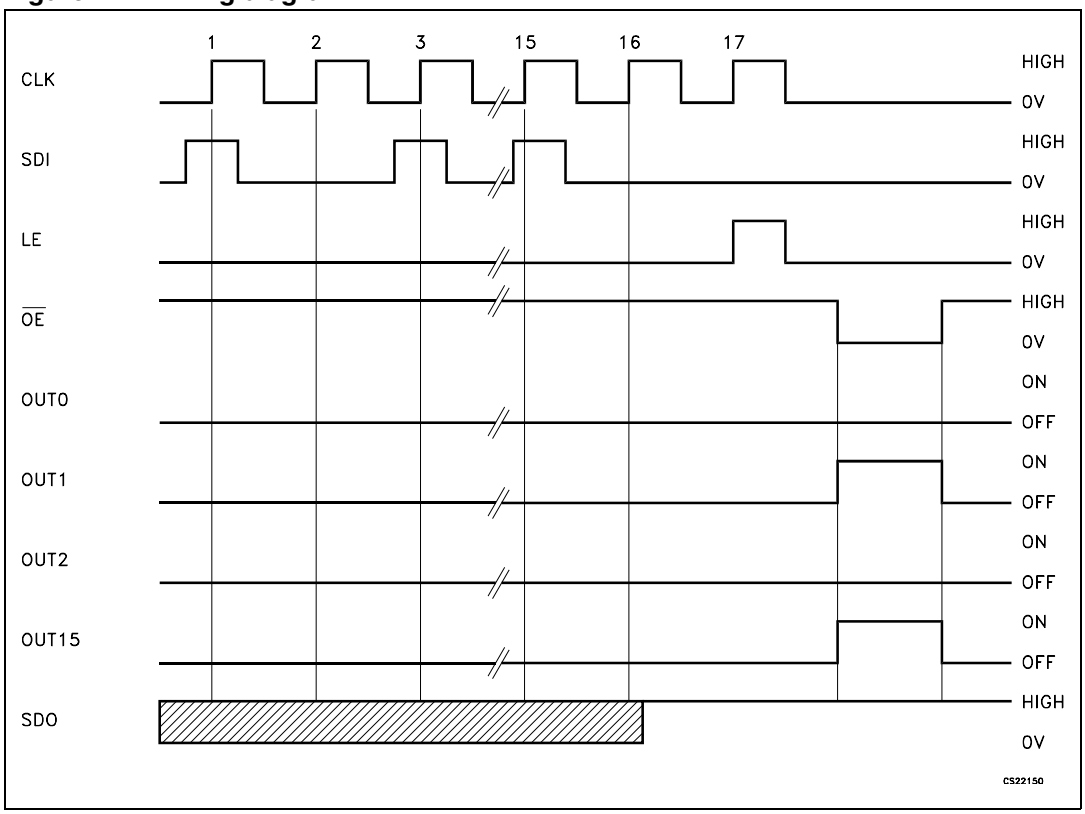
5 Timing diagrams

Table 9. Truth table

CLOCK	LE	$\overline{OE}$	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
⎍	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
⎍	L	L	Dn + 1	No Change	Dn - 14
⎍	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎎	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
⎎	X	H	Dn + 3	OFF	Dn - 13

Note: OUTn = ON when Dn = H OUTn = OFF when Dn = L

Figure 7. Timing diagram



Note: The latches circuit holds data when the LE terminal is Low.

1. *When LE terminal is at High level, latch circuit hold the data it passes from the input to the output.*
2. *When $\overline{OE}$ terminal is at Low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.*
3. *When $\overline{OE}$ terminal is at High level, it switches off all the data on the output terminal.*

Table 10. Enable IO: shut-down truth table

CLOCK	LE	SDI_0 ..... SDI_7 ..... SDI_{15}	SH	Auto Power-up	OUTn
⎍	H	All = L	Active	Not Active	OFF
⎍	L	No Change	No Change	No Change	No Change
⎍	H	One or more = H	Not Active	Active	X

Note: At the Power-up the device starts in Shut-Down mode.

Figure 8. Clock, serial-in, serial-out

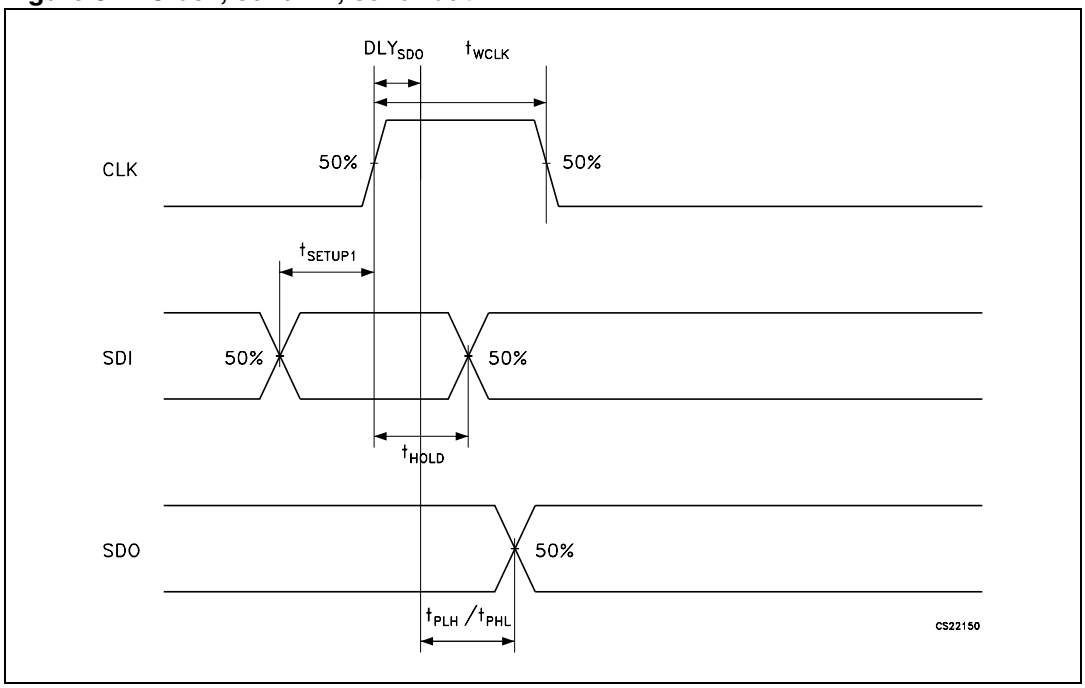


Figure 9. Clock, serial-in, latch, enable, outputs

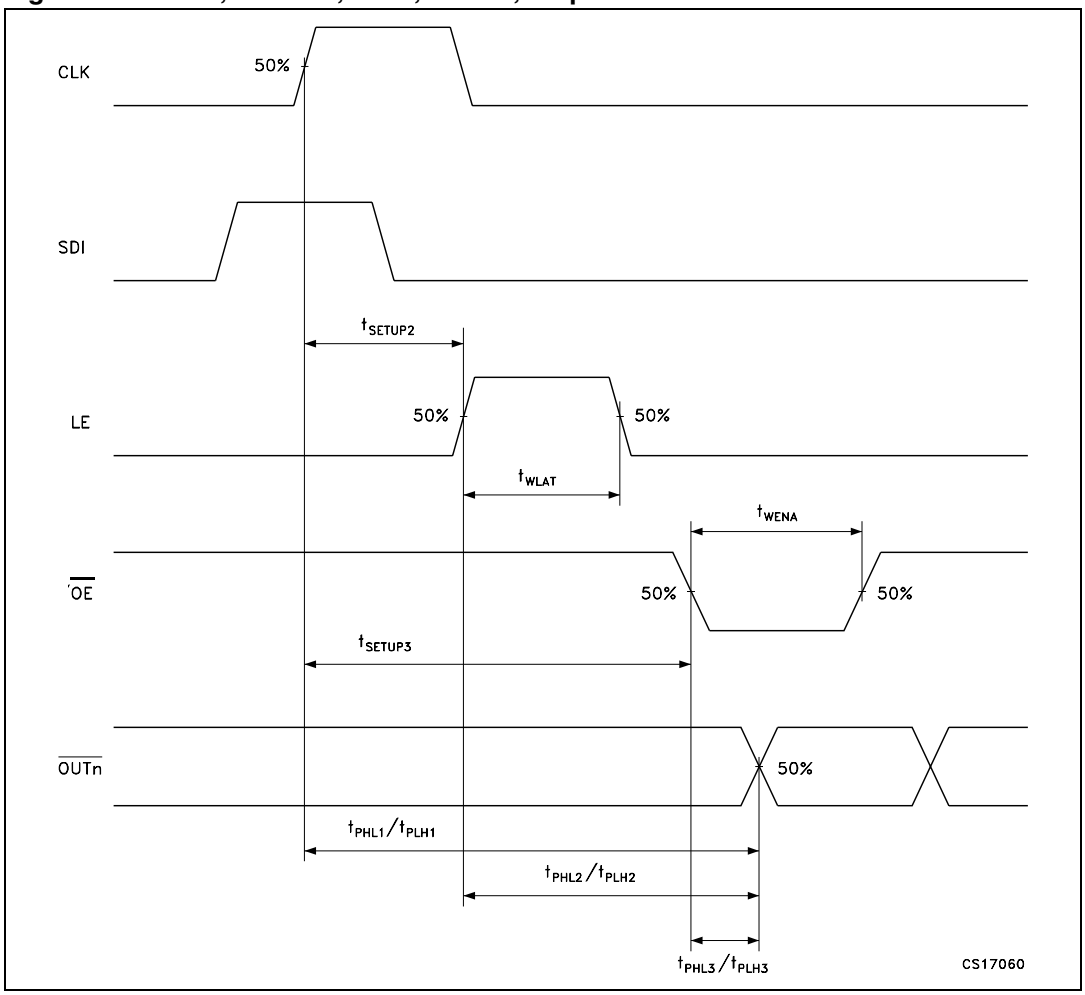
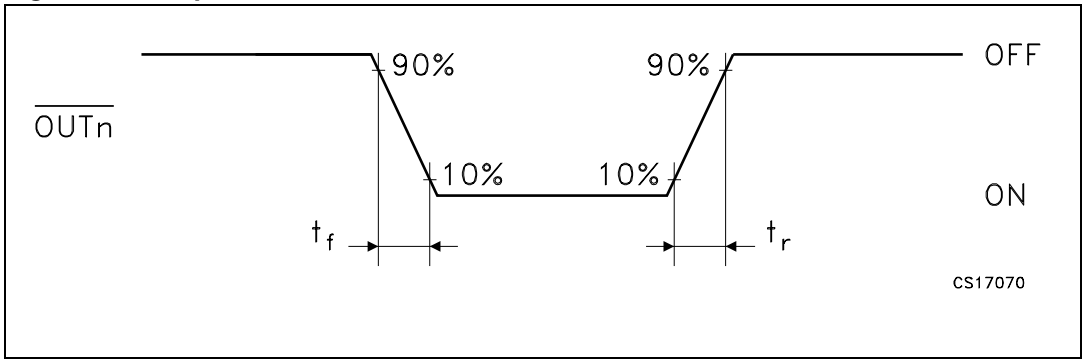


Figure 10. Outputs



6 Typical characteristics

Figure 11. Output current-R_{EXT} resistor

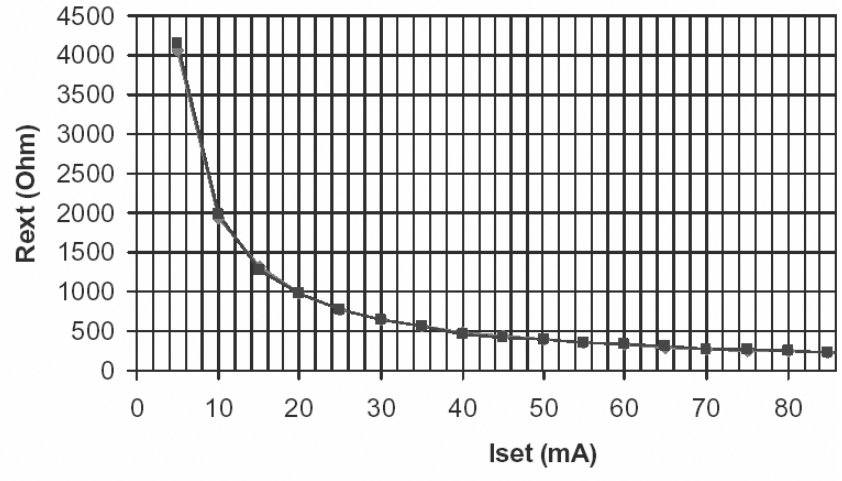


Table 11. Output current-R_{EXT} resistor

Rext (Ohm)	Output current (mA)
976	20
780	25
652	30
560	35
488	40
433	45
389	50
354	55
325	60
300	65
278	70
259	75
241	80
229	85
215	90

Figure 12. Output current vs $\pm \Delta I_{OL}(\%)$

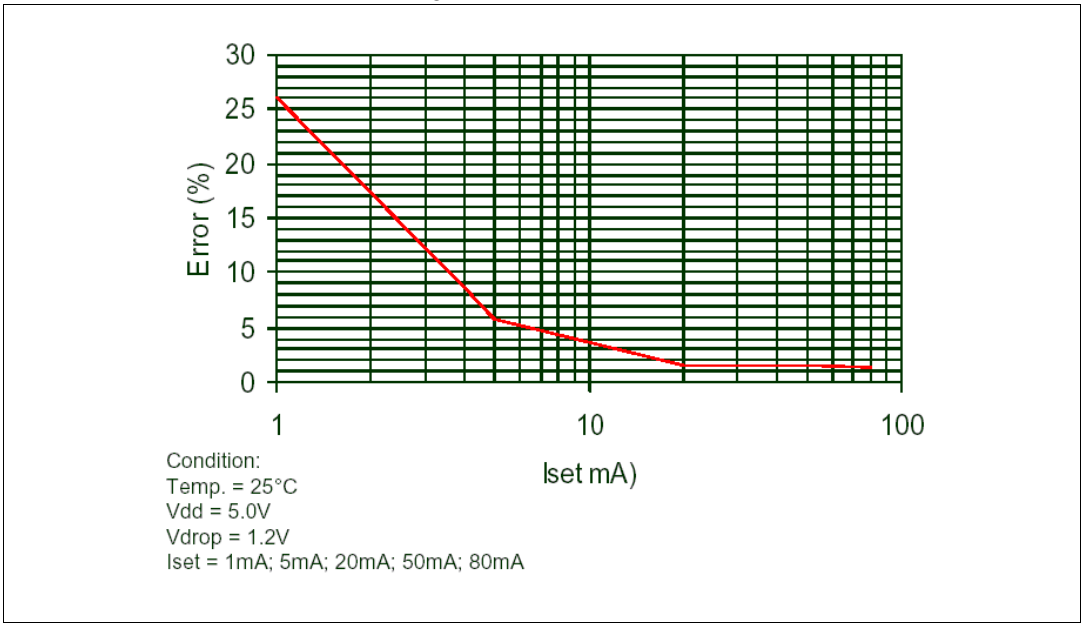
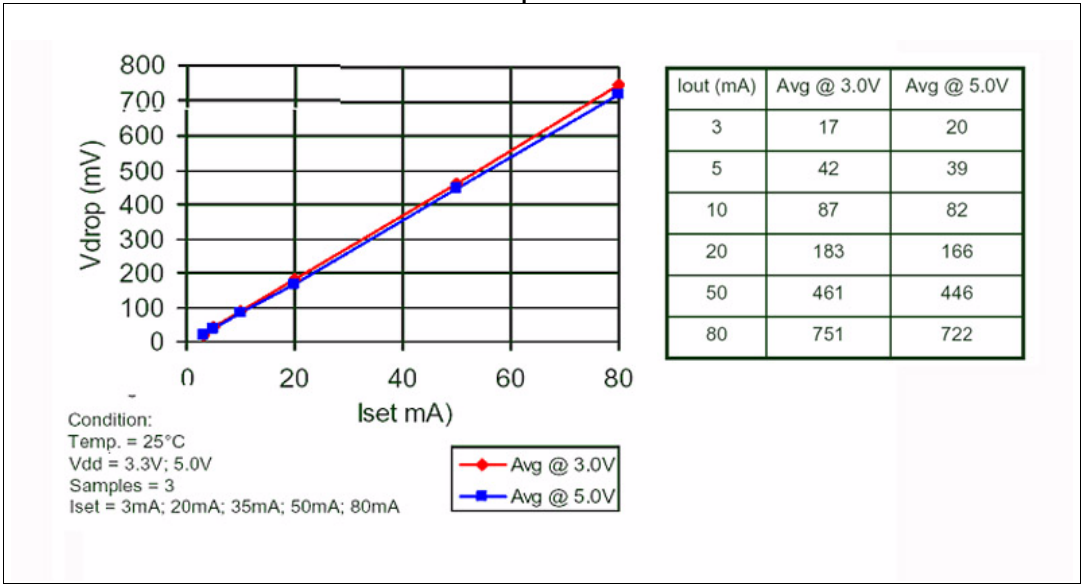


Figure 13. I_{SET} vs drop out voltage (V_{drop})



Iout (mA)	Avg @ 3.0V	Avg @ 5.0V
3	17	20
5	42	39
10	87	82
20	183	166
50	461	446
80	751	722

Figure 14. I_{DD} ON\OFF

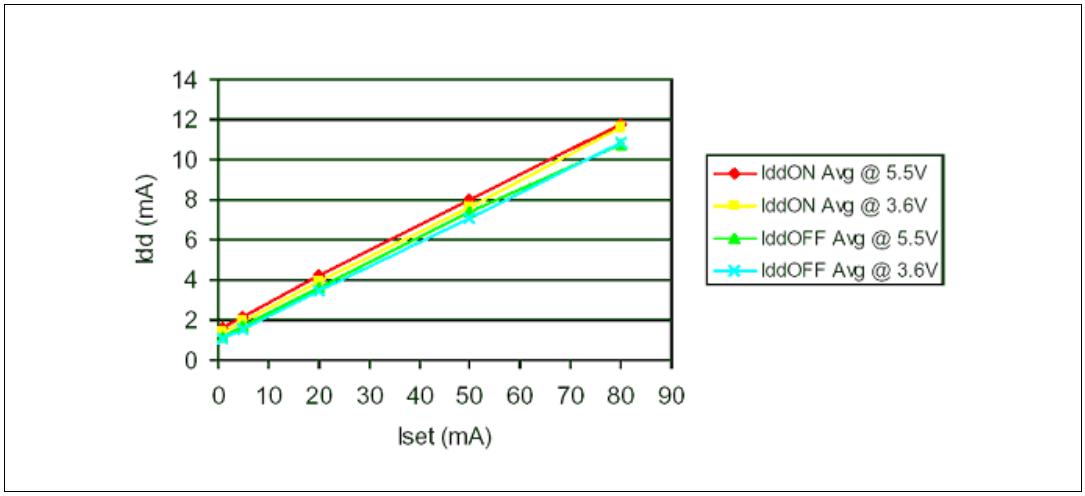
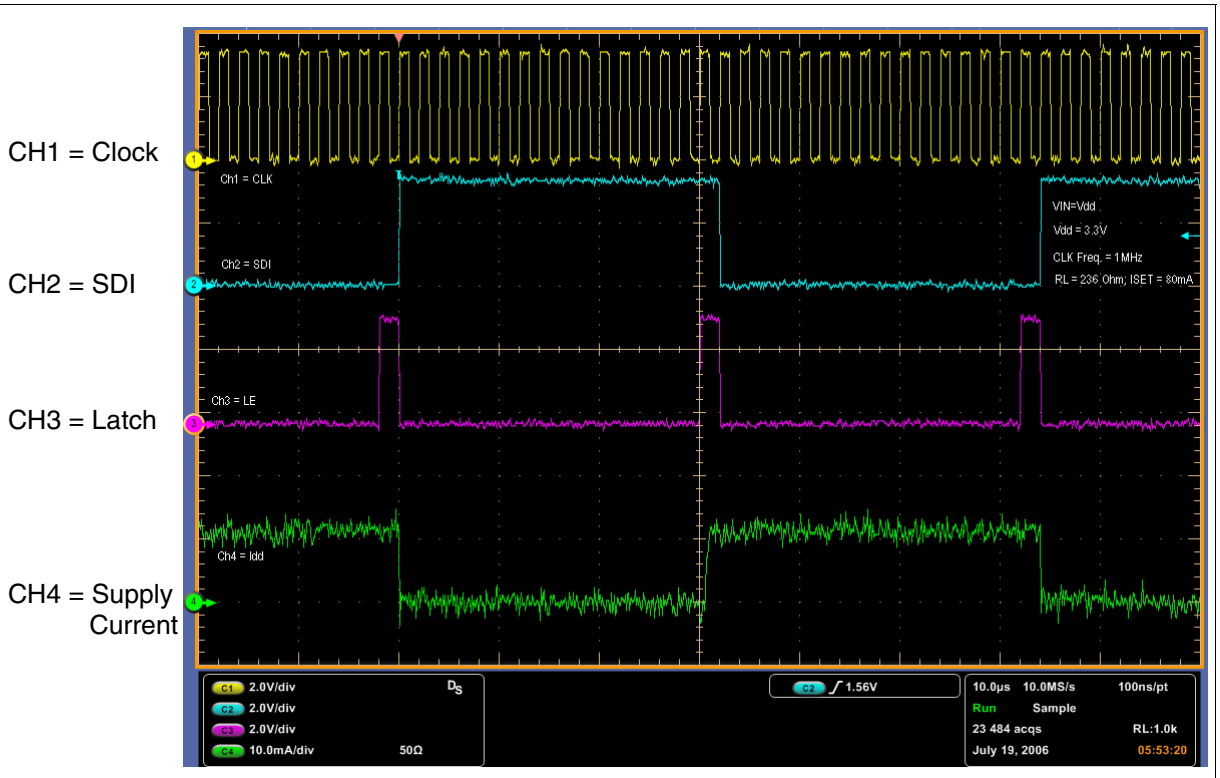


Figure 15. Auto power saving



Note: Auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto-power-up the device at fist active data latched.

7 Test circuit

Figure 16. DC characteristic

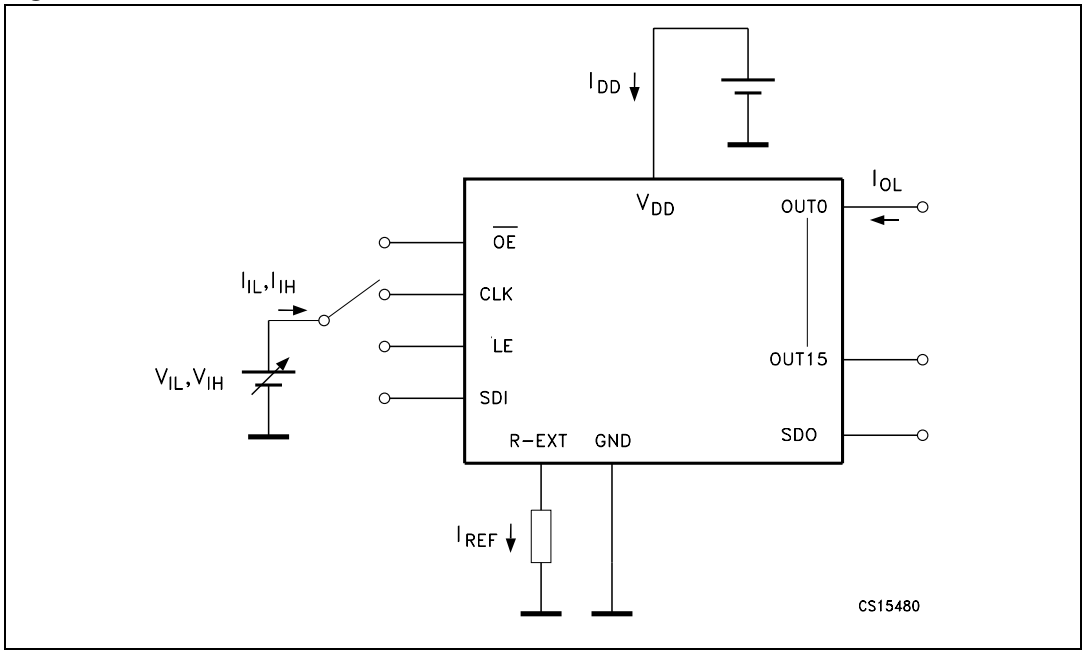


Figure 17. AC characteristic

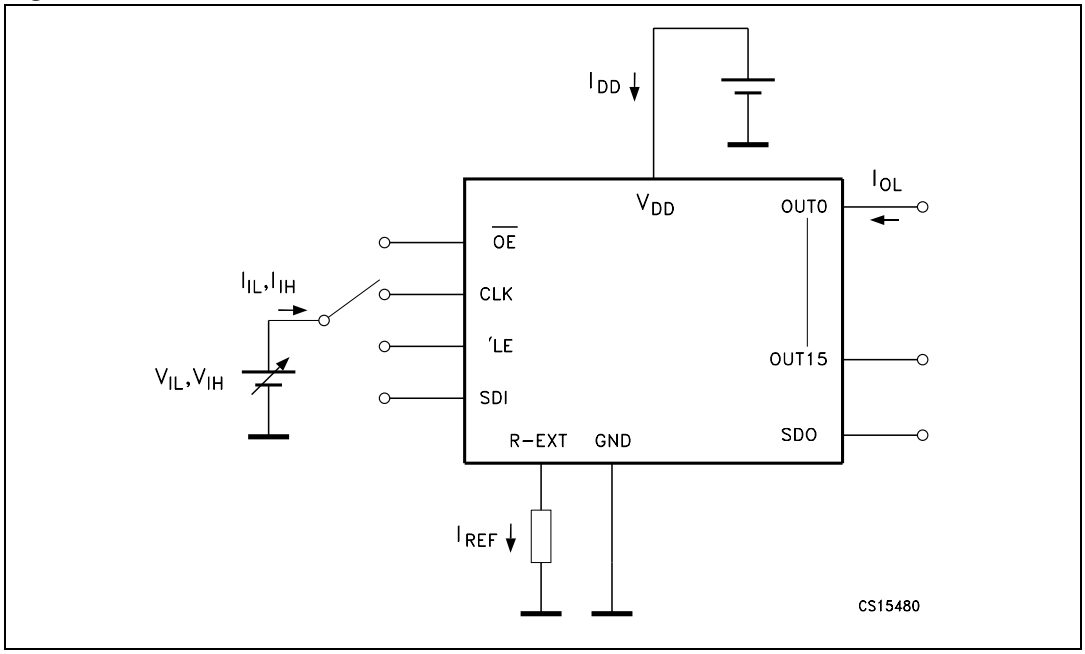
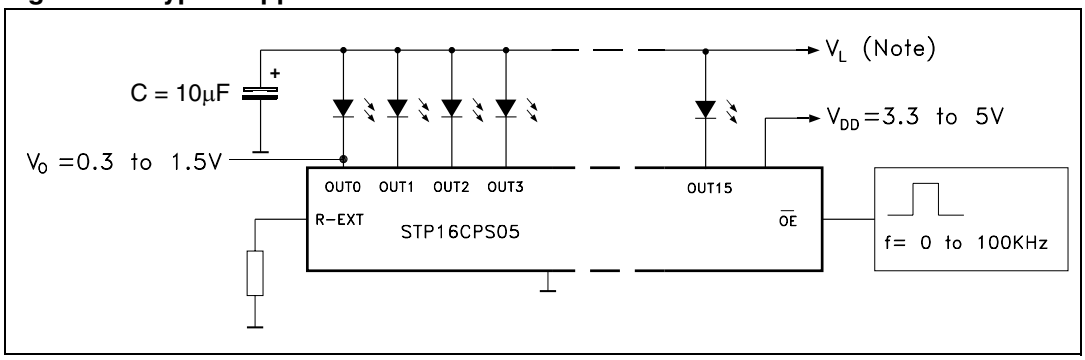


Figure 18. Typical application schematic



Note: V_L will be determined by the V_F of the LEDs

Test condition: Temp. = 25°C, V_{DD} = 3.0V, V_{IN} = V_{DD}, C_L = 10pF, Freq. = 1MHz, Ch1 = CLK, Ch2 = SDI, Ch3 = OUTn , Ch4 = V_{OUT}

Figure 19. Turn ON output current setup

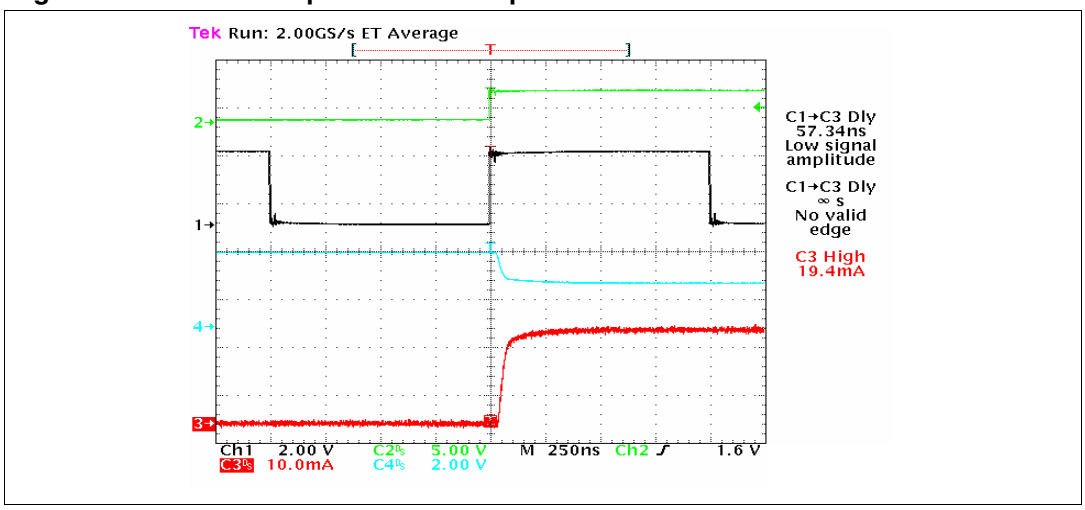
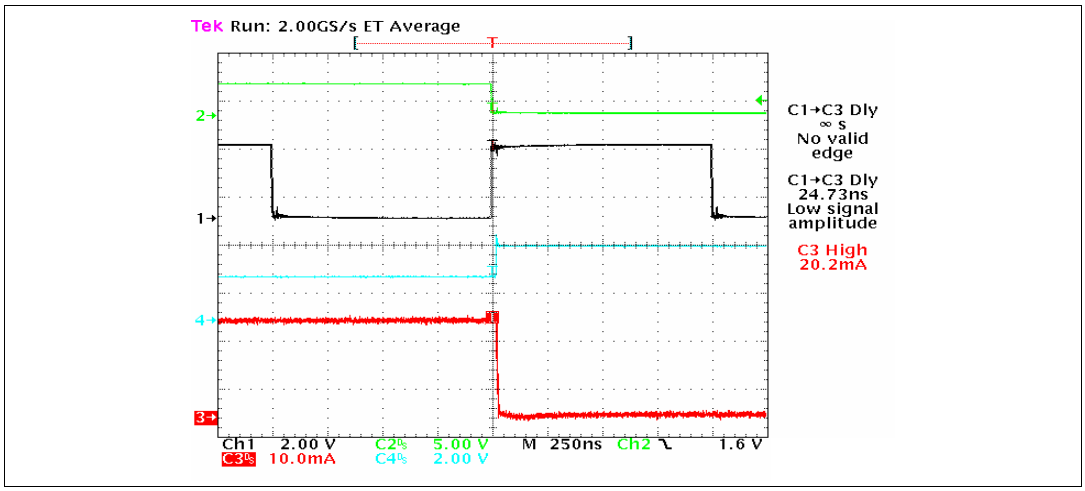


Figure 20. Turn OFF output current setup



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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Table 12. TSSOP24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 21. TSSOP24 package dimensions

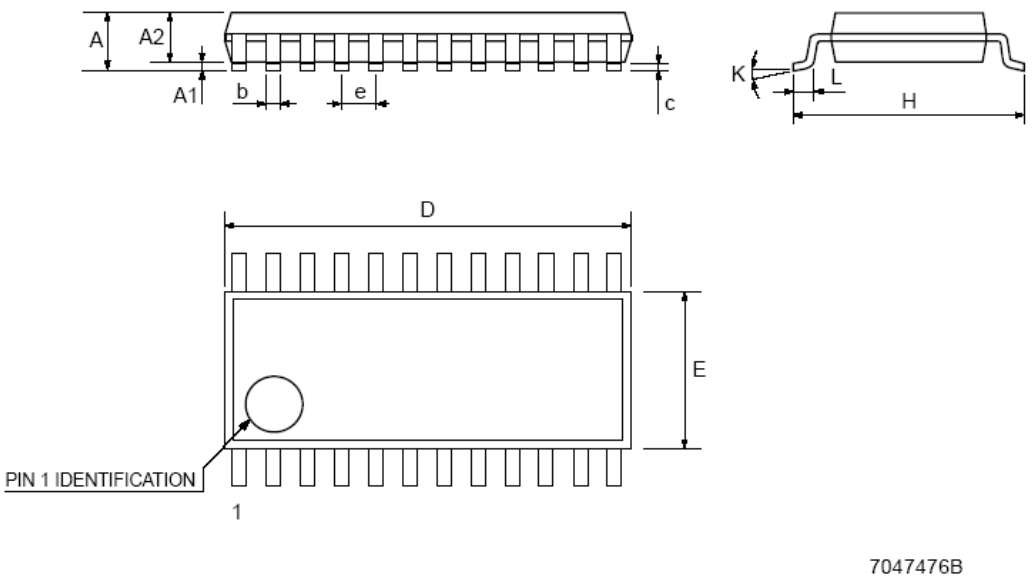


Table 13. Tape and reel TSSOP24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			2.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 22. Reel dimensions

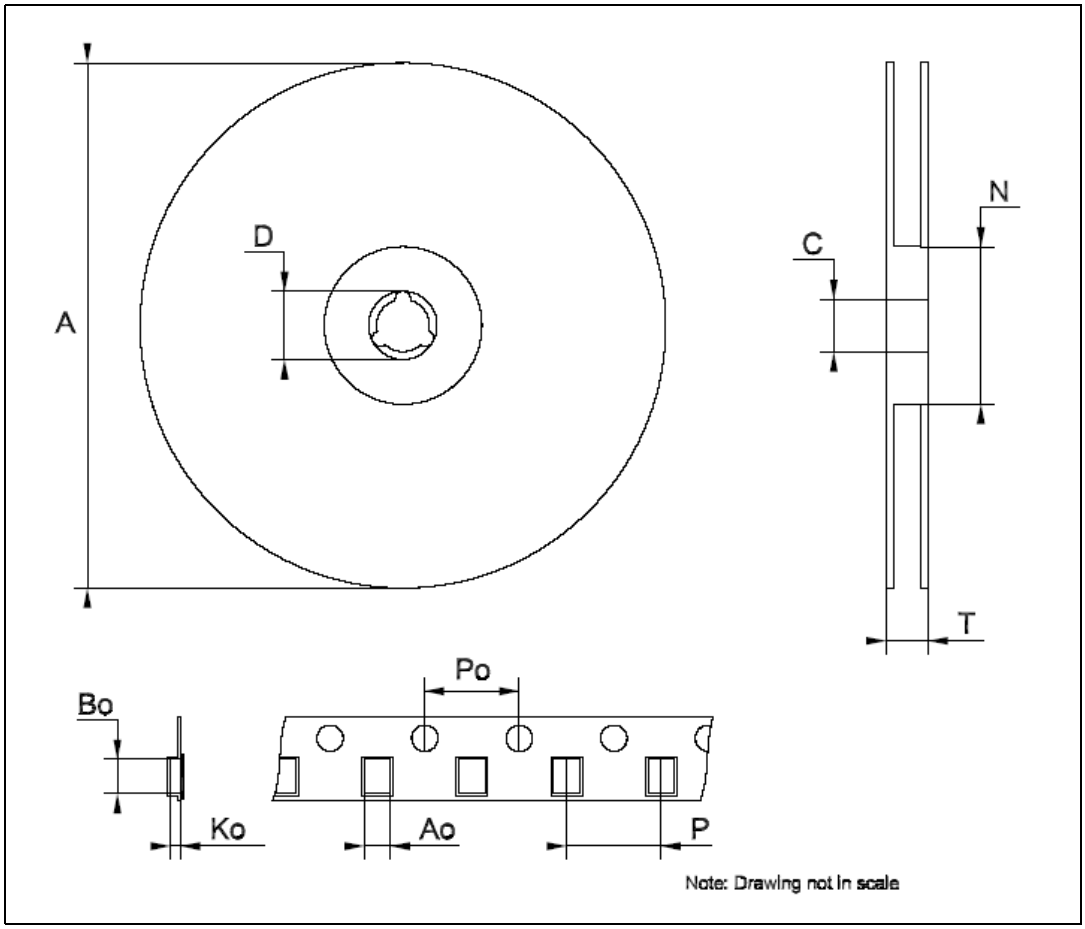


Table 14. SO-24 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 23. SO-24 package dimensions

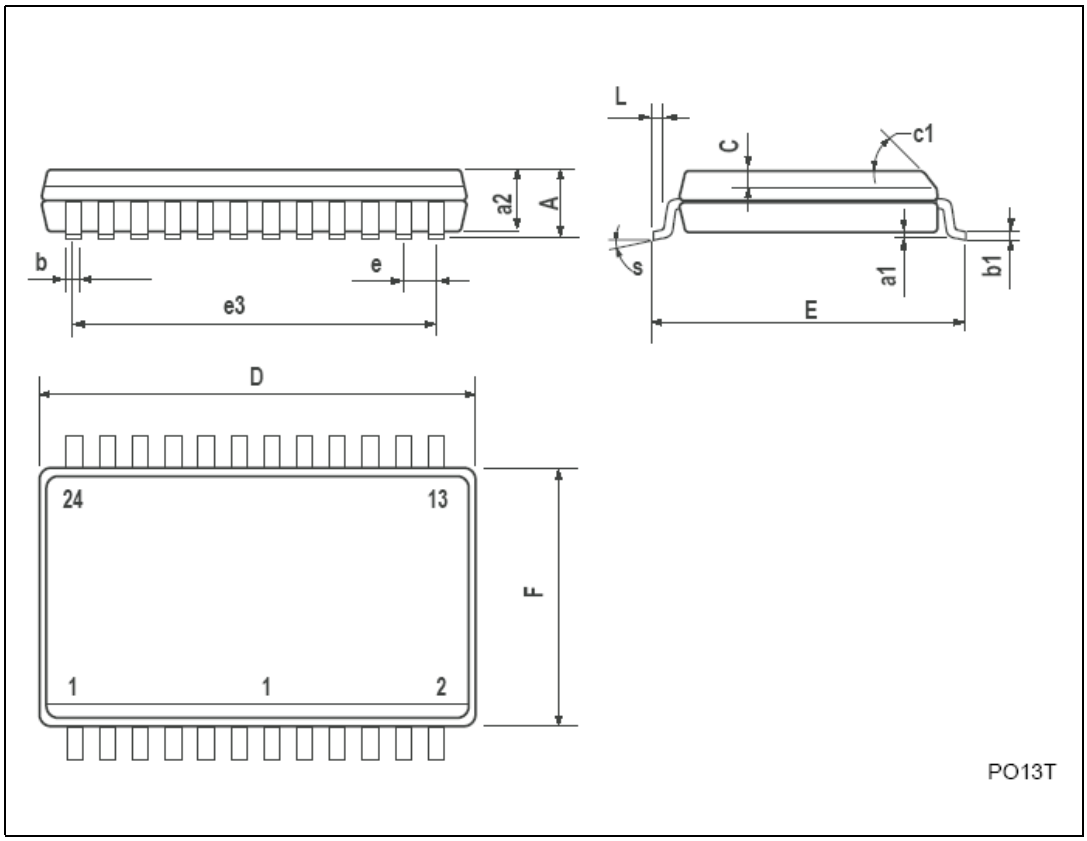


Table 15. Tape and reel SO-24

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 24. Reel dimensions

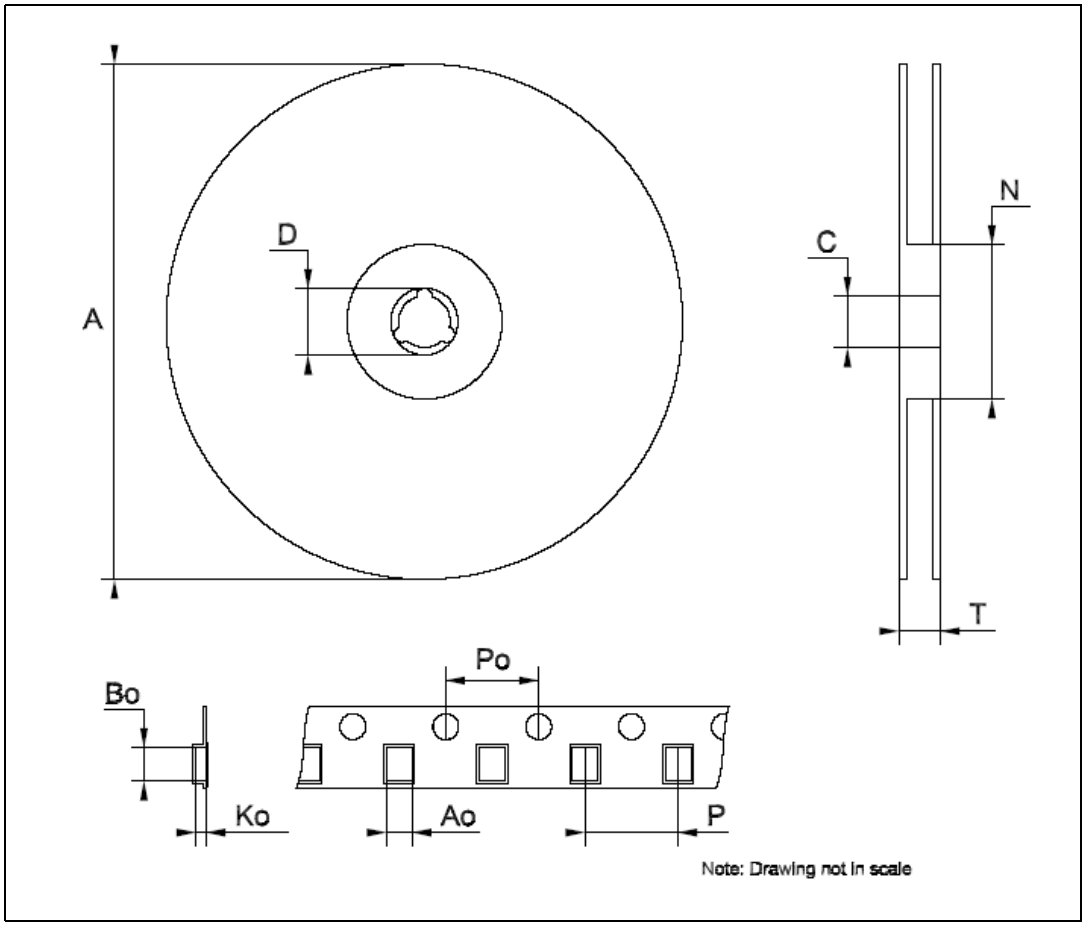
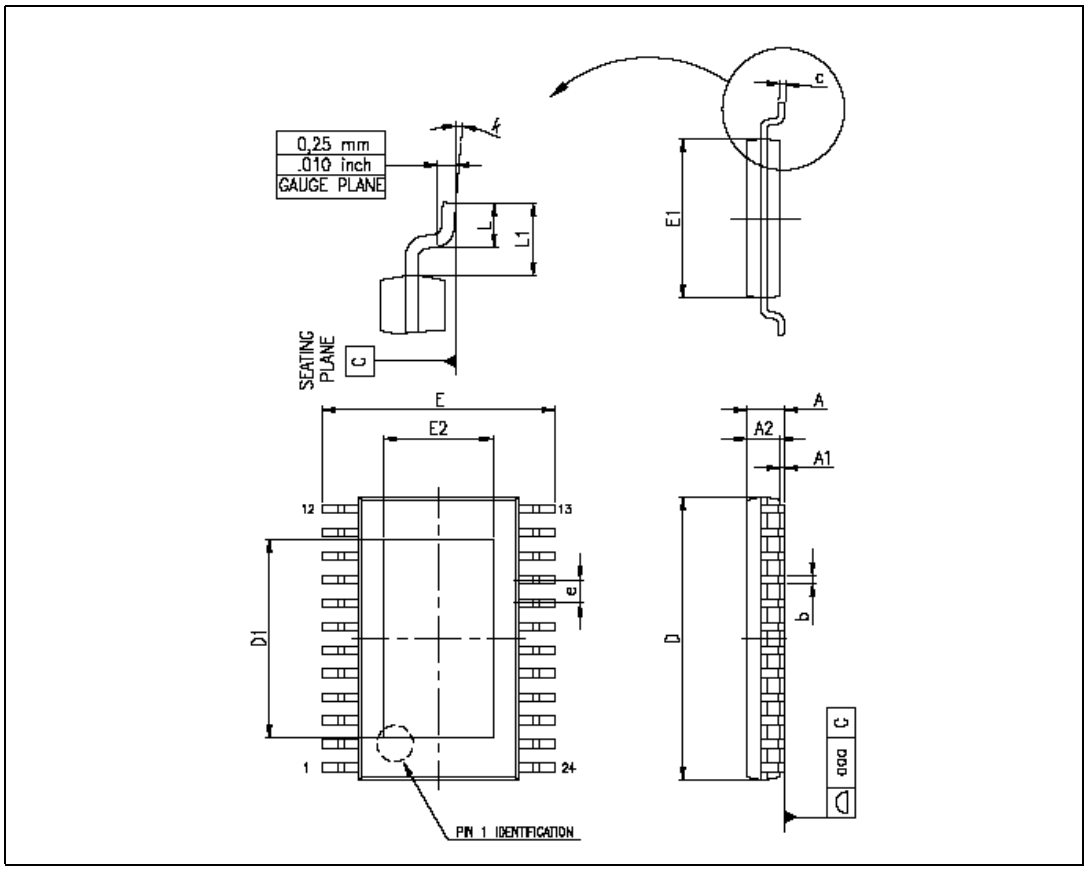


Table 16. TSSOP24 exposed-pad

Dim.	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1		2.7		0.106		
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2		1.5		0.059		
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 25. TSSOP24 dimensions



9 Revision history

Table 17. Revision history

Date	Revision	Changes
28-Jul-2006	1	First release
22-Dec-2006	2	Final datasheet
17-May-2007	3	Updated *Table 8 on page 7*
10-Jul-2007	4	Updated *Table 9: Truth table on page 10*

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