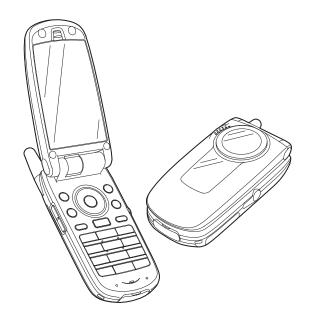
# SHARP SERVICE MANUAL

by Toko (toko@gsm-free.org)



# **DIGITAL MOBILE PHONE**

# MODEL TM200

(INTERNAL MODEL NAME: TM200)

 In the interests of user-safety the set should be restored to its original condition and only parts identical to those specified should be used.

#### Caution:

Risk of explosion if battery is replaced by an incorrect type, dispose of used batteries according to the instruction.

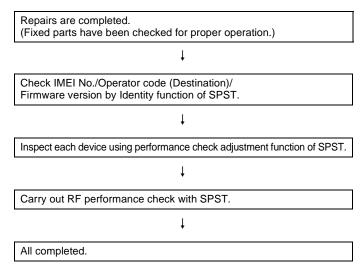
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Parts marked with "\_\textit{\Lambda}" are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

# **SERVICING CONCERNS**

- 1. When requested, back up user's handset data using SPST (SHARP Program Support Tool). Otherwise, before servicing, warn the user that data in the memory may be lost during repairs.
- 2. Upgrade the firmware to the latest version using SPST before returning the handset to the customer.
- 3. After repairs, inspect the handset according to the following flowchart.



- 4. When storing or transporting a PWB, put it into a conductive bag or wrap it in aluminum foil. (C-MOS IC may be damaged by electrostatic charges.)
- 5. Do not leave fingerprints, etc. on ornamental parts including a cabinet, especially clear windows for main and sub displays. Wear fingerstalls to avoid this.
  - Also, ensure not to leave fingerprints on the surface of main and external display panels.
- 6. To prevent oxidation which causes connection problems, do not touch any terminals on the electric board, microphone, vibrator, earpiece and speaker.
  - When handling these parts, wear fingerstalls. Should you touch these parts, clean them with a soft dry cloth.
  - Always wear fingerstalls when handling a shield case on the electric board.
  - Otherwise oxidation may occur causing handset performance deterioration.
- 7. The FPC is a precision device. Handle it carefully to prevent any damages.
- 8. Do not expose the moisture sensor to liquids.
  - If the sheet gets wet, red ink runs. In this case, replace the sheet with a new one.
  - Be careful about your perspiration.
- 9. Before you disassemble or reassemble handset, make sure to remove the Li-lon battery.
- 10. Be sufficiently careful with static electricity of integrated circuits and other circuits. Wear static electricity prevention bands while servicing.

# **CHAPTER 1. GENERAL DESCRIPTION**

FOR A COMPLETE DESCRIPTION OF THE OPERATION OF THIS UNIT, PLEASE REFER TO THE OPERATION MANUAL.

# 1. SPECIFICATIONS

Camera	Device	2 Megapixel CCD digital camera with LED flashlight				
	Autofocus	Autofocus mode, Semi-autofocus mode, Manual focus mode				
	Function	Max. 8x Digital zoom, Delay timer, Continuous shot, ±2 exposure correction				
	Image size	Still:       2 Megapixel       : 1,224 x 1,632 dots         1 Megapixel       : 858 x 1,144 dots         Large       : 768 x 1,024 dots (XGA)         Medium       : 480 x 640 dots (VGA)         Small       : 240 x 320 dots (QVGA)         Tiny       : 120 x 160 dots (QQVGA)         Video:       Large       : 176 x 144 dots         Small       : 128 x 96 dots				
Main display	Туре	2.2 inch Transmissive System LCDs (CG-Silicon)				
	Colour depth	262k*1 colours				
	Resolution	QVGA (240 x 320 dots)				
External display	Туре	1.06 inch Semi-Transmissive system LCDs				
	Colour depth	65k colours				
Resolution		96 x 64 dots				
Connections		Bluetooth <sup>™</sup> , SD memory card slot *2, Earphone/MIC, USB (Ver.1.1), RF connector				
Sound Chords		40 chord polyphonic ringtones				
Format		AAC, MP3, SMAF, MIDI, i-melody, WAVE, AMR				
Contacts list (Ph	onebook)	500 entries				
Messaging		SMS (Text message), MMS (Picture/Video messaging), E-mail with POP3 and SMTP supporting attachment				
WAP		Version 2.0				
Browser		Openwave 6.2.3				
JAVA TM	Version	MIDP2.0				
	Max. application size	200KB				
Language		11 languages (English, German, Dutch, Czech, Hungarian, French, Spanish, Italian, Greek, Portuguese, Turkish)				
Text input metho	od	T9, multi-tap				
Band		Tri-Band (900/1800/1900MHz)				
GPRS		Class B, Multislot Class10				
Battery		Li-lon (840 mAh)				
Continuous standby time		Approx. max. 220 hours *3 (TBD)				
Continuous talking time		Approx. max. 200 minutes *3 (TBD)				
Weight		Approx. 120g (TBD)				
Size (W x D x H)	)	Approx. 49.2 x 96.3 x 27.1mm (with shell closed and excluding protrusions)				

<sup>\*1)</sup> For JPEG wallpaper display only.

<sup>\*2)</sup> SD memory card is not included.

**<sup>\*</sup>**3) It varies depending on the condition.

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United Kingdom Pat. No. 2238414B; Hong Kong Sandard Pat. No. HK0940329; Republic of Singapore Pat. No.51383; Euro. Pat. No 0 842 463 (96927260.8) DE/DK, FI, FR, IT, NL, PT.ES, SE, GB;

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Please use discretion in privacy matters when taking photographs or sending images with a camera-equipped mobile phone.

Design and specifications are subject to change without prior notice.

The information contained in this sales manual is current as of December 2004 (product still under development).

All screen images are simulated.

# 2. NAMES OF PARTS



No.	Name
1	2-megapixel camera
2	LED flashlight
3	External display
4	Side-up/Side-down key
<b>⑤</b>	Camera/Music key
6	Voice mail key
7	Flashlight key
8	USB/charger connector
9	Earpiece
10	Main display
11)	Handsfree earphones & microphone (stereo)
12	Navigation key (Up/Down/Left/Right) You can programme the Navigation Key yourself.
13	Centre key
14)	Earphones connector
15)	Font Zoom key
16	The t-zones Key also gives you direct access to the t-zones Online Homepage.
17)	SD memory card slot

# 3. OPERATION MANUAL

(Page numbers refer to the user guide)

# [OPTIONAL ACCESSORIES]

· USB data cable

The above accessories may not be available in all regions. For details, please contact your dealer.

# CHAPTER 2. 1ADJUSTMENTS, PERFORMANCE CHECK, AND FIRMWARE UPGRADE

SPST (SHARP Program Support Tool) allows you to adjust settings, conduct performance checks, and upgrade the firmware.

# [1] SHARP PROGRAM SUPPORT TOOL (SPST)

# 1. SYSTEM REQUIREMENTS

 IBM PC compatible personal computer (standard COM1 115,200 bps serial port and USB required)

Supported OS: Windows 98/98SE/2000/XP (except for Windows 95/ME/NT)

(English, German, Italian, Spanish, French and Chinese versions)

· Data cable

<During RF adjustment>

• GSM tester: CMU150

• GPIB interface: National Instruments USB-GPIB cable

(Model No.: NI GPIB-USB-B)

# 2. INTRODUCTION

# 2-1. FUNCTIONS

SPST offers seven key functions:

- 1) Firmware download
- 2) User data transfer (processes all data at once but not individually.)
- 3) RF calibration check and test
- 4) Default setting
- 5) Identification
- 6) Performance check and adjustment
- 7) User password reset

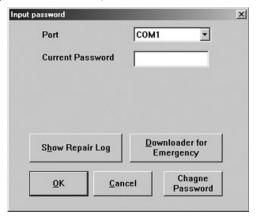
# 2-2. INSTALLATION

- Use Windows Explorer to execute the "setup.exe" file on the CD-ROM.
- The SPST TM200 setup wizard appears. Follow the installation instructions.
- After the installation is complete, shortcuts to SPST are created on the desktop and under the "Start"-"Programs"-"TM200" menu. Start SPST from the shortcuts.

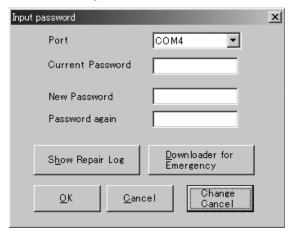
#### 2-3. STARTING UP

Connect TM200 to an operable serial port of the PC with the supplied data cable. Make sure that the battery is fully charged. Start SPST from the desktop.

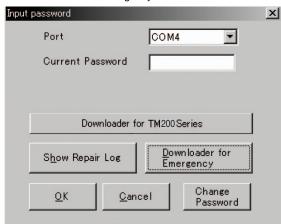
 The Input password dialog box appears. Enter the password, select a port where TM200 is connected from the list box, and click "OK".
 If you do not know SPC, click "Cancel" to exit.



To change the password, enter the current password in procedure 1, and then click "Change Password".

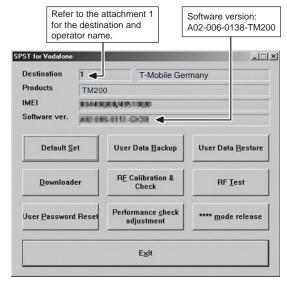


- 3. To check the usage status of tools, click "Show Repair Log" in procedure 1.
- 4. Click "Downloader for Emergency".



The above screen appears. Select a model to use and execute the Downloader. (Use this to initialize the flash, etc.)

When the password is correct, a connection is established and the following screen appears.



#### ■ Buttons

Default Set	Refer to "4-1. Default setting".
User Data Back-up	Refer to "4-2. User data back-up".
User Data Restore	Refer to "4-3. User data restore".
Downloader	Refer to "4-4. Downloader".
RF Calibration & Check	Refer to "4-5. RF calibration & check".
RF Test	Refer to "4-6. RF test tool".
User Password Reset	Refer to "4-7. Password reset".
Performance check adjustment	Refer to "4-8. Performance check and adjustment".
**** mode release	Refer to "4-9. ****mode release".
Exit	End SPST.

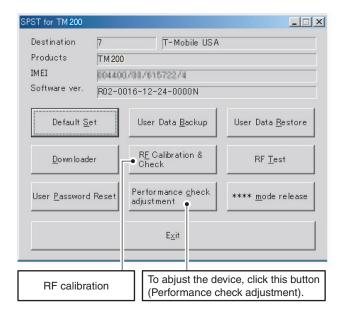
# 3. ADJUSTMENTS FOR TM200

1. Adjustments are required after replacing the following parts. ( O )

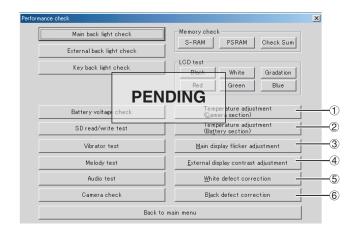
Parts	Temperature adjustment (Camera)	Temperature adjustment (Battery)	Main display flicker adjustment	White defect correction
TH101	×	0	×	×
TH701	0	×	×	×
Main display unit	×	×	0	×
Camera unit	×	×	×	0

When replacing other parts in the RF section, carry out RF calibration.

2. Click the buttons on the SPST screen for adjustments.



3. The following screen appears.



- ① Temperature adjustment (Camera section)
- 2 Temperature adjustment (Battery section)
- 3 Main display flicker adjustment
- 4 External display contrast adjustment
- ⑤ White defect correction
- 6 Black defect correction

# 4. FUNCTIONS

# 4-1. DEFAULT SETTING

SPST can restore the factory settings.

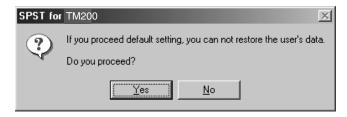
This function

- 1. Deletes all user data in the file system;
- 2. Restores all WAP settings to default; and
- 3. Restores the values set by the user to default;

(MEP\_LOCK settings and the destination and operator name do not change.)

# <Operation>

- 1) Set the COM port on the SPST initial screen and click "Default Set".
- 2) Click "Yes" to proceed. Click "No" to exit.



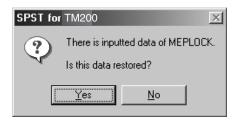
Click "Yes" to back-up the MEPLOCK data. Click "No" to restore default settings.



4) Communication starts.



 The following appears when you select "Yes" in step 3 and MEPLOCK data exists. Click "Yes" to restore the data.



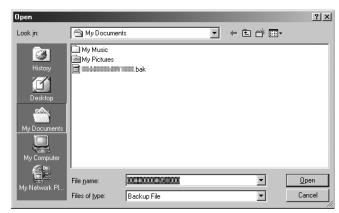
6) After the handset is turned on, the initialization is complete.



# 4-2. USER DATA BACK-UP

SPST saves all the data stored on the handset.

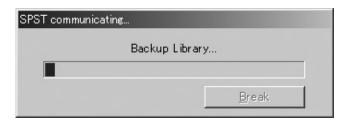
- Set the COM port on the SPST initial screen and click "User Data Back-up".
- 2. Specify the file name in the following dialog box and click "Save"



3. The communicating dialog box appears while processing.



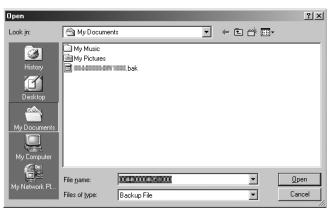
4. When completed, the following message appears. Click "OK".



# 4-3. USER DATA RESTORE

SPST completely restores the backed up data.

- Set the COM port on the SPST initial screen and click "User Data Restore".
- 2. Specify the file name in the following dialog box and click "Save".



3. The communicating dialog box appears while processing.



4. When the restore is complete, click "OK".



# 4-4. DOWNLOADER

#### 4-4-1. Introduction

Downloader allows you to upgrade the firmware.

# 1) System requirements

· Requirements for the upgrading tool:

OS : Windows 98, 98 SE, 2000, or XP

Download file : Only the Motorola format is supported.

Communication method : Asynchronous mode

Data length : 8 bits
Parity bit : None
Stop bit length : 1 bit

• Requirements for Loading loader

Handset : TM200

Communication method : Asynchronous mode

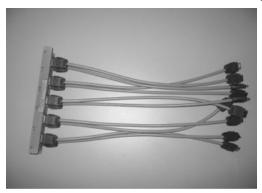
Data length : 8 bits
Parity bit : None
Stop bit length : 1 bit

# 2) Required devices

The following devices are required to rewrite MOT files using Communication Box.

# Conversion connector (16-pin → 10-pin)

This conversion connector is required to connect TM200 with Communication Box since the cable connector of Communication Box has 16 pins.



# 4-4-2. Getting started

This section describes how to install/uninstall the software and how to connect handset to a PC.

# 1) Installing/uninstalling the software

# [Installing the software]

Note: Downloader is installing/uninnstalling simultaneously with SPTP.

1. Double click the "setup.exe" icon in TM200 Install-E folder.



The Setup Wizard is activated. Click the "Next" button.



3. A location to install the software appears.

To install in the default location, click the "Next" button.

To change the location, click the "Browse" button, select a desired location and then click the "Next" button.

(See the description in "\* Changing the install location" below.)



\* Changing the install location

Click the "Browse" button in step 3 to browse folders.

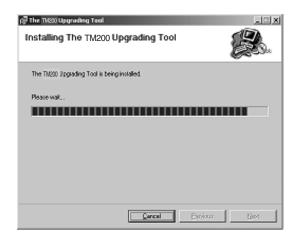
Click the "▼" button, select a folder and click the "OK" button.



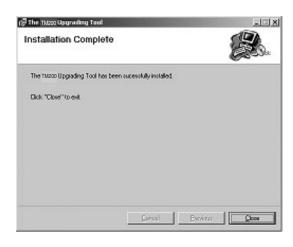
 A confirmation message appears. Click the "Next" button.



5. Installtion starts. The progress is displayed.



The installation is completed.Click the "Close" button to close the Setup Wizard.



7. The shortcut icon shown left is created on your desktop when the installation is completed.



#### Note:

 After installing the upgrading tool in Windows 98 or 98 SE, restart the operating system.

While installing the upgrading tool in Windows 98, 98 SE, or ME, a message may appear prompting to restart the operating system. In this case, restart your operating system follwoing the instruction. Even if the message does not appear, restart your operating system after the installation.

On Windows 98, if you start the upgrading tool without restarting the operation system, the following message may appear. Restart the operating system to ensure the proper operation of the upgrading tool.



 Uninstall the upgrading tool before installing the latest version or reinstalling the current version.

Otherwise, the upgrading tool may not function properly. To ensure the proper operation, uninstall and then reinstall the upgrading tool.

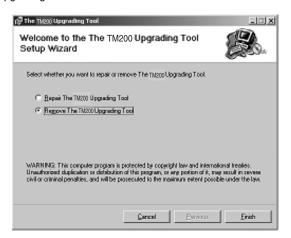
# [Uninstalling the software]

1. Double click "setup.exe" in TM200 Install-E folder.



secup.exe

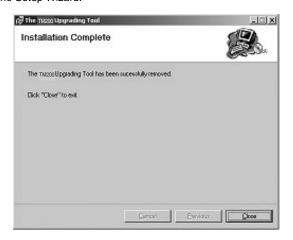
The Setup Wizard is activated. Select "Remove The TM200 Upgrading Tool" and click the "Finish" button.



3. Uninstalltion starts. The progress is displayed.



The uninstallation is completed. Click the "Close" button to close the Setup Wizard.



#### 2) Connecting handset to a PC

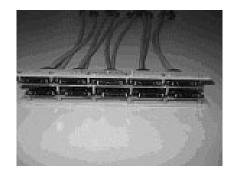
# A) Using a cable for upgrading

- 1. Connect the cable to a PC.
- 2. Connect the cable to handset.
- 3. The photo below shows handset connected to a PC.



# **B) Using Communication Box**

- 1. Connect a PC to Communication Box via a serial cable.
- Connect the AC charger to Communication Box and then plug it into the outlet.
  - All SET POWER SW on Communication Box must be turned off.
- Connect the conversion connector to Communication Box Cables.
   Connect the conversion connector in the following order, label side up.
   From upper right end: Cable No. 1, 3, 5, 7, and 9.
   From lower right end: Cable No. 2, 4, 6, 8, and 10.



4. The photo below shows the conversion connector connected to Communication Box Cable 1.

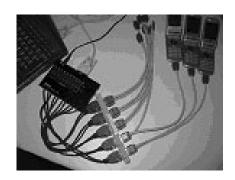


5. Connect the other end of the conversion connector to handset.



The photo below shows handset, Communication Box and a PC (all connected).

Make sure handset and Communication Box Cable 1 are connected via the conversion connector.



#### Note:

- Handset must be turned off before making any connections.
   Press and hold the Power key to turn off handset.
   Do not turn off in other ways. Malfunction may occur and the MOT file rewrite operation may fail.
- Make sure the handset battery is sufficiently charged.
   If the battery is low, the MOT file rewrite operation may fail.
   Charge the battery before the operation.
- Disconnect the AC charger from a cable for upgrading.

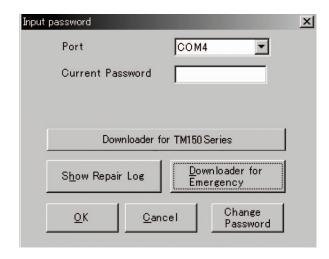
  When rewriting MOT files using the upgrading tool, do not connect the AC charger to the cable.

  If you connect the cable connected to the AC charger to banded.
  - If you connect the cable connected to the AC charger to handset, charging starts and the MOT file rewrite operation is interrupted.
- All SET POWER SW on Communication Box must be turned off.
   If handset is connected with SET POWER SW turned on, charging starts and the MOT file rewrite operation is interrupted.
- Make sure handset and Communication Box Cable 1 are connected via the conversion connector.
   (When using Communication Box, the only handset connected to Cable 1 can be operated on the PC.)

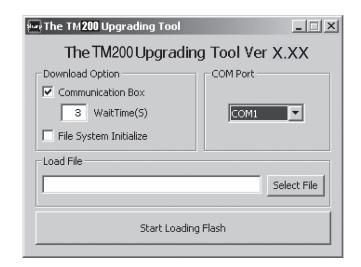
# 4-4-3. Rewriting MOT files

This section describes how to rewrite MOT files.

- 1) Downloader for Emergency
- 1. Click "Downloader for Emergency".



2. The upgrading tool is activated.

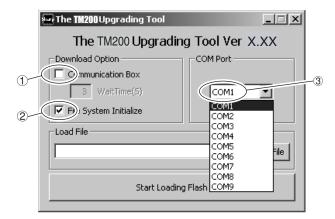


Note: Disable the power saving mode before rewriting MOT files.

If the power saving mode is active, the rewrite operation may fail depending on the PC.

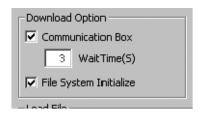
#### 2) Selecting options and COM port

- Uncheck the check box when using a cable for upgrading. Leave it checked when using Communication Box.
- ② To initialize user area, check the File System Initialize check box. (User data will be deleted and the handset status will return to the default.)
- ③ Click here and in the pull-down list, select a communications port where the cable or Communication Box is connected.



When using Communication Box, set Wait Time.

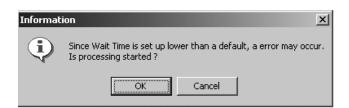
Check the Communication Box check box to adjust Wait Time (default: 3 seconds). The time to delete the program data varies between handsets. Handsets wait for the set Wait Time until the whole process is completed. If an error occurs, increase the value.



# [Notes for the Wait Time setting]

When the set value is smaller than the default (3), the message on the left appears alerting you a possible error.

Click the [OK] button to proceed, and click the [Cancel] button to change the value.



You can shorten time for the MOT rewrite operation by selecting a smaller value for Wait Time.

Example: Time to rewrite two MOT files at a time.

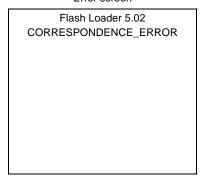
At the default setting (3 seconds), rewrite time is approximately 40 minutes. If the value is set to 1, the rewrite time will be reduced to approximately 30 minutes.

If an error occurs at 1, increase the value.

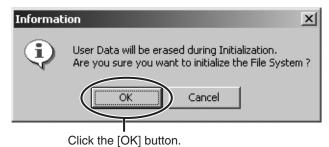
The error screen will appear on handsets No. 2 to No.10.

If this screen appears, increase Wait Time and retry.

# Error screen



When the File System Initialize check box is checked, a confirmation message appears.



Note: When you check File System Initialize check box and click the [OK] button, handset status returns to the default.

In this case, user data is initialized after the MOT file rewrite operation. Uncheck the check box to avoid this.

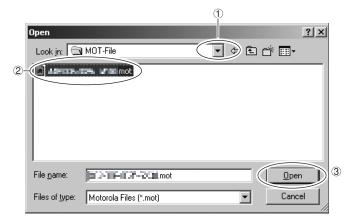
#### 3) Selecting a MOT file

Click the [Select File] button.
 The Open dialog box appears.



# [Open dialog box]

- ① Click the [▼] button to open a desired folder.
- ② A Motorola file (.mot) in the folder appears. Click a file to write in.
- 3 Click the [Open] button to open the file.



#### Note:

Make sure to select a MOT file.

If the File name field is blank, you cannot rewrite a MOT file.

• Use MOT files in the hard disk.

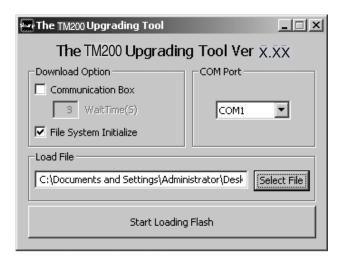
If the selected MOT file is stored in other locations, an error message appears and you cannot complete the rewrite operation.



To use MOT files on CDs or on the network, copy or download them to the hard disk first.

# 4) Rewriting a MOT file

Click the [Start Loading Flash] button to start rewriting.



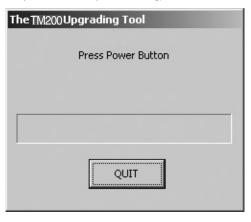
1. "Press Power Button" appears.

<When using a cable for upgrading>

Hold down the Power key.

<When using the Communication Box>

Turn on Communication Box SW from No.10 down to No.1 (turn on only the handsets you are using).



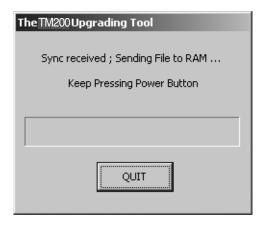
2. "Keep Pressing Power Button" appears.

<When using a cable for upgrading>

Hold down the Power key until the "Keep Pressing Power Button" disappears.

<When using the Communication Box>

Leave the Communication Box SW turned on.



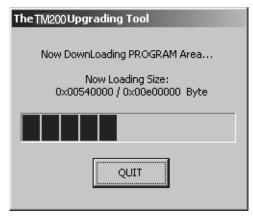
3. The MOT file rewrite operation starts.

<When using a cable for upgrading>

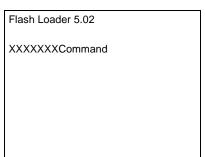
When "Keep Pressing Power Button" disappears, release the Power key.

<When using the Communication Box>

Leave the Communication Box SW turned on.



When the rewrite operation starts, handset display screen shows the software version and process of communications with the PC.



SUM also appears on handset.
<When using a cable for upgrading>
After 8 seconds, SUM disappears.
<When using Communication Box>
When SET POWER SW is turned off, SUM disappears.

Flash Loader 5.02	
SUM Check End	
SUM = 0xdb3d	

# Canceling the ongoing rewrite operation:

Click the [QUIT] button.

To rewrite MOT files later, remove and install the battery first.

# [Notes for the use of a cable for upgrading]

- Disconnect the AC charger from the cable. Otherwise charging starts and the MOT file rewrite operation is interrupted.
- Make sure the handset battery is sufficiently charged.If the battery is low, the rewrite operation may fail. Charge the battery before the operation.
- 3. If the ongoing rewrite operation is canceled, or interrupted by an error, remove and reinstall the battery and retry.

# [Notes for the use of the Communication Box]

- When "Press Power Button!" appears, turn on Communication Box SW from No.10 down to No.1. If the communication BoxSW No.1 is first turned on, the rewrite on communication BoxSW No. 2 to No. 10 operation will fail.
- The time to delete the program data varies between handsets. If the process fails at the default Wait Time (3 seconds), increase the value.
  - Consequently, this will increase the time to complete the rewrite operation.

# 5) Checking the value of SUM

When the rewrite operation is completed, a confirmation message appears with SUM.



# Make sure SUM is the same between the PC and handset.

The same SUM means that the rewrite operation is completed properly. If the value is different, try again to ensure completion of the operation.

# If the MOT file rewrite operation fails, an error message appears on handset.

**★**The screen shot on the left shows an error in erasing Flash data.

[ADR] and [STR] appear only when an error occurs in the FLASH-related operation.

Start over the MOT file rewrite operation.

<When other error messages appear>

Find the message in 4-4-4. 2)Error messages for Loading loader, and follow the instructions.

#### Error screen

Flash Loader 5.02 FLASH\_ERROR ERROR\_ERASE ADR = 0x1000000 STR = 0xA0

# 6) After the operation

Disconnect the cable for upgrading from handset.

When using the Communication Box, turn off SET POWER SW and then disconnect the cable from handset.

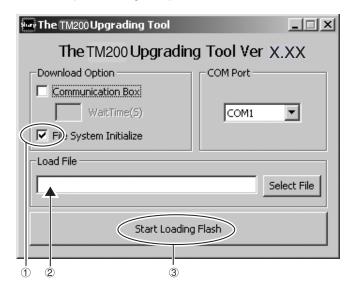
# 7) Initializing only the file system

Follow the instructions below to initialize only the file system.

(User data will be deleted and the handset status will return to the default.)

\*Perform this procedure when the handset does not turn on.

- ① Check the File System Initialize check box.
- 2 Leave the Load File text box blank.
- 3 Click the [Start Loading Flash] button.



For further operations, refer to [4-4-3. 4) Rewriting a MOT file] or [4-4-3. 5) Checking the value of SUM].

# 4-4-4. Error message list

Below is the list of error messages for the upgrading tool (on the PC side) and Loading loader (on the handset side).

# 1) Error messages for the upgrading tool (on the PC side)

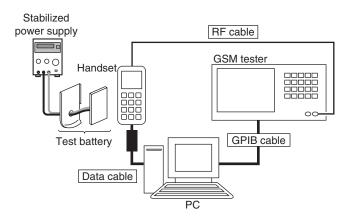
No.	Message	Descriptions/Instructions
1	Select a file for Downloading or check the box of Initializing.	Load File is not set. Select a MOT file.
2	Unable to open file.	Failed to open the MOT file. Start over the rewrite operation.
3	You need to set the Wait Time!	WaitTime (S) is not set. Set WaitTime (S) value.
4	The file you selected is unsuitable for Upgrading.	The selected file cannot be rewritten for upgrading. Select an appropriate MOT file.
5	Cannot Setup COM port.	The selected COM port does not exist or is used for other operations. Select a COM port connected to the PC cable.
6	RAM Loader not responding to Commands.	No response from Loading loader. Start over the rewrite operation.
7	RAM Loader responding Parameter Error.	Information sent from the PC is illegal. Reinstall the upgrading tool. Start over the rewrite operation.
8	RAM Loader responding Flash Error (XXXX).	Failed to initialize FLASH ROM in (XXXX). Start over the rewrite operation.
9	Correspondence Error.	Undefined response from Loading loader. Start over the rewrite operation.

2) Error messages for Loading loader (on the handset side)

		· · · · · · · · · · · · · · · · · · ·
No.	Message	Descriptions/Instructions
1	FLASH_ERROR	An error in Flash Rom. Start over the rewrite operation.
2	ERROR_PARAM	The upgrading tool is damaged. Uninstall and reinstall the upgrading tool, and start over the rewrite operation.
3	ERROR_WPROTECT	Flash Rom is protected. Battery may be too low. Use a sufficiently charged battery and start over the rewrite operation.
4	ERROR_READ	Failed to read Flash Rom data and the operation was aborted. Start over the rewrite operation.
5	ERROR_WRITE	Failed to write to Flash Rom and the operation was aborted. Start over the rewrite operation.
6	ERROR_ERASE	Failed to erase Flash Rom data and the operation was aborted. Start over the rewrite operation.
7	ERROR_VERIFY	The rewrite operation was aborted since there was a mismatch between data written to Flash Rom and that written to handset.  Start over the rewrite operation.
8	ERROR_RWE_TMOUT	Communication was terminated since there was no response from Flash Rom for a certain period of time. Start over the rewrite operation.
9	CORRESPONDENCE _ERROR	Communication was terminated since serial data communication failed. Start over the rewrite operation.
10	ADR = XXXXXXXX	Indicates the address of Flash (the error source).
11	STR = XX	Indicates the status of Flash (the error source).

\*When No.1 occurs, handset screen shows error messages for No.2 to No.8 as well as the address (No.10) and status (No.11) of the error source at the same time.

# 4-5. RF CALIBRATION & CHECK

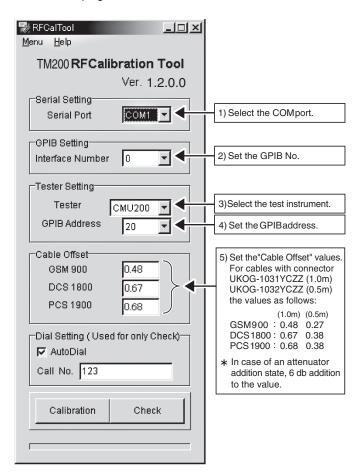


# 4-5-1. Preparation

- Connect PC and GSM tester with a GPIB cable.
- Connect PC and handset with a Data cable. (Use a test battery or one close.)
- Connect a RF cable of GSM tester to handset.

# 4-5-2. Default setting for the program.

• Activate the program and set defaults.



5. Make sure the handset is on and click "OK". (Adjustment starts.)



6. Click "OK".



7. The initial screen returns.

# 4-5-4. RF performance check (Insert SIM card)

- 1. Apply 4 V using a stabilized power supply and turn on the handset.
- 2. Start "RF calibration & check" on SPST and click "Calibration".
- 3. When initialization is complete, click "OK".



# 4-5-3. RF calibration (Remove SIM card)

- 1. Apply 4 V using a stabilized power supply and turn on the handset.
- 2. Start "RF calibration & check" on SPST and click "Calibration".
- 3. When initialization is complete, click "OK".



Apply 4 V using a stabilized power supply and turn on the handset.
 After the handset enters Standby mode, lower the voltage to 3.7 V.



Apply 4 V using a stabilized power supply and turn on the handset.
 After the handset enters Standby mode, lower the voltage to 3.7 V.



5.Make sure the handset is in the idle mode and click "OK"...



6. Press the keys 1, 2, 3 and Send and click "OK".



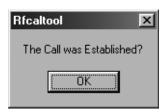
 Make sure the terminal display is "In Call" and click "OK". (RF performance check starts.)



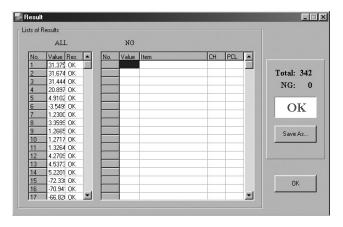
 The following message appears during the check. Press the keys 1, 2, 3 and Send again and click "OK".



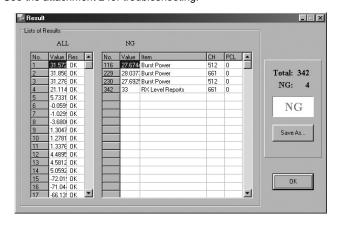
9. Make sure the terminal display is "In Call" and click "OK".



10. RF performance check is complete. Click "Save As..." and name the file to save the result. Click "OK" to exit.



The following will be displayed in case of failure. See the attachment 2 for troubleshooting.



11. Click "OK".



12. The initial screen returns.

# Attachment 2

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL			
GSM900	Tx	1	Burst Power	37CH	PCL5			
		2	Burst Power	975CH	PCL5			
		3	Burst Power	124CH	PCL5			
		4	Burst Power	37CH	PCL11			
		5	Burst Power	37CH	PCL19			
		6	Frequency Error	37CH	PCL5			
		7	Frequency Error	975CH	PCL5			
		8	Frequency Error	124CH	PCL5			
		9	Phase Error (RMS)	37CH	PCL5			
		10	Phase Error (RMS)	975CH	PCL5			
		11	Phase Error (RMS)	124CH	PCL5			
		12	Phase Error (Peak)	37CH	PCL5			
		13	Phase Error (Peak)	975CH	PCL5			
		14	Phase Error (Peak)	124CH	PCL5			
		15	Mod_spectrum -800	37CH	PCL5			
		16	Mod_spectrum -600	37CH	PCL5			
		17	Mod spectrum -400	37CH	PCL5			
		18	Mod spectrum -250	37CH	PCL5			
		19	Mod_spectrum -200	37CH	PCL5			
		20	Mod_spectrum +200	37CH	PCL5			
		21	Mod_spectrum +250	37CH	PCL5			
		22	Mod_spectrum +400	37CH	PCL5			
		23	Mod_spectrum +600	37CH	PCL5			
		24	Mod_spectrum +800	37CH	PCL5			
			25	Mod_spectrum -800	975CH	PCL5		
			26	Mod_spectrum -600	975CH	PCL5		
							27	Mod_spectrum -400
		28	Mod_spectrum -250	975CH	PCL5			
		29	Mod_spectrum -200	975CH	PCL5			
		30	Mod_spectrum +200	975CH	PCL5 PCL5			
			31	Mod_spectrum +250	975CH			
			32	Mod_spectrum +400	975CH	PCL5		
		33	Mod_spectrum +600	975CH	PCL5			
		34	Mod_spectrum +800	975CH	PCL5			
		35	Mod_spectrum -800	124CH	PCL5			
		36	Mod_spectrum -600	124CH	PCL5			
		37	Mod_spectrum -400	124CH	PCL5			
		38	Mod_spectrum -250	124CH	PCL5			
		39	Mod_spectrum -200	124CH	PCL5			
		40	Mod_spectrum +200	124CH	PCL5			
		41	Mod_spectrum +250	124CH	PCL5			
		42	Mod_spectrum +400	124CH	PCL5			
					43	Mod_spectrum +600	124CH	PCL5
		44	Mod_spectrum +800	124CH	PCL5			
					45	Mod_spectrum -800	37CH	PCL11
		46	Mod_spectrum -600	37CH	PCL11			
		47	Mod_spectrum -400	37CH	PCL11			

Receive	No.	inspected	Channel	PCL
Tx	48	Mod_spectrum -250	37CH	PCL11
	49	Mod_spectrum -200	37CH	PCL11
	50	Mod_spectrum +200	37CH	PCL11
	51	Mod_spectrum +250	37CH	PCL11
	52	Mod_spectrum +400	37CH	PCL11
	53	Mod_spectrum +600	37CH	PCL11
	54	Mod_spectrum +800	37CH	PCL11
ľ	55	Mod_spectrum -800	37CH	PCL19
ľ	56	Mod_spectrum -600	37CH	PCL19
	57	Mod_spectrum -400	37CH	PCL19
	58	Mod_spectrum -250	37CH	PCL19
ľ	59	Mod_spectrum -200	37CH	PCL19
ľ	60	Mod_spectrum +200	37CH	PCL19
ľ	61	Mod_spectrum +250	37CH	PCL19
	62	Mod_spectrum +400	37CH	PCL19
	63	Mod_spectrum +600	37CH	PCL19
	64	Mod_spectrum +800	37CH	PCL19
	65	Switch_Spectrum -1800	37CH	PCL5
	66	Switch_Spectrum -1200	37CH	PCL5
	67	Switch_Spectrum -600	37CH	PCL5
	68	Switch_Spectrum -400	37CH	PCL5
	69	Switch_Spectrum +400	37CH	PCL5
	70	Switch_Spectrum +600	37CH	PCL5
	71	Switch_Spectrum +1200	37CH	PCL5
	72	Switch_Spectrum +1800	37CH	PCL5
	73	Switch_Spectrum -1800	975CH	PCL5
	74	Switch_Spectrum -1200	975CH	PCL5
	75	Switch_Spectrum -600	975CH	PCL5
	76	Switch_Spectrum -400	975CH	PCL5
	77	Switch_Spectrum +400	975CH	PCL5
	78	Switch_Spectrum +600	975CH	PCL5
	79	Switch_Spectrum +1200	975CH	PCL5
	80	Switch_Spectrum +1800	975CH	PCL5
	81	Switch_Spectrum -1800	124CH	PCL5
	82	Switch_Spectrum -1200	124CH	PCL5
	83	Switch_Spectrum -600	124CH	PCL5
	84	Switch_Spectrum -400	124CH	PCL5
	85	Switch_Spectrum +400	124CH	PCL5
	86	Switch_Spectrum +600	124CH	PCL5
	87	Switch_Spectrum +1200	124CH	PCL5
	88	Switch_Spectrum +1800	124CH	PCL5
	89	Switch_Spectrum -1800	37CH	PCL11
	90	Switch_Spectrum -1200	37CH	PCL11
ļ	91	Switch_Spectrum -600	37CH	PCL11
ļ	92	Switch_Spectrum -400	37CH	PCL11
	ıx	49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91	49 Mod_spectrum +200 50 Mod_spectrum +250 51 Mod_spectrum +400 53 Mod_spectrum +400 53 Mod_spectrum +800 54 Mod_spectrum +800 55 Mod_spectrum -800 56 Mod_spectrum -800 57 Mod_spectrum -250 59 Mod_spectrum -250 59 Mod_spectrum -200 60 Mod_spectrum +250 61 Mod_spectrum +250 62 Mod_spectrum +250 63 Mod_spectrum +400 63 Mod_spectrum +400 64 Mod_spectrum +800 65 Switch_Spectrum -1800 66 Switch_Spectrum -1200 67 Switch_Spectrum -400 68 Switch_Spectrum +400 70 Switch_Spectrum +400 71 Switch_Spectrum +1200 72 Switch_Spectrum +1200 73 Switch_Spectrum -1800 74 Switch_Spectrum -1200 75 Switch_Spectrum -1200 76 Switch_Spectrum -400 77 Switch_Spectrum +400 78 Switch_Spectrum +400 79 Switch_Spectrum +400 78 Switch_Spectrum +400 79 Switch_Spectrum +400 80 Switch_Spectrum +1200 81 Switch_Spectrum +1200 82 Switch_Spectrum -1200 83 Switch_Spectrum -1200 84 Switch_Spectrum -1200 85 Switch_Spectrum -1200 86 Switch_Spectrum -1200 87 Switch_Spectrum -1200 88 Switch_Spectrum +400 89 Switch_Spectrum +400 80 Switch_Spectrum -1200 81 Switch_Spectrum -1200 82 Switch_Spectrum -1200 83 Switch_Spectrum +400 84 Switch_Spectrum +400 85 Switch_Spectrum +400 86 Switch_Spectrum +400 87 Switch_Spectrum +400 88 Switch_Spectrum +400 89 Switch_Spectrum +1200 80 Switch_Spectrum +1200 81 Switch_Spectrum +400 82 Switch_Spectrum +400 83 Switch_Spectrum +400 84 Switch_Spectrum +400 85 Switch_Spectrum +1200 86 Switch_Spectrum +1200 87 Switch_Spectrum +1200 88 Switch_Spectrum +1200 89 Switch_Spectrum +1200 80 Switch_Spectrum +1200 80 Switch_Spectrum +1200	49 Mod_spectrum -200

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL
GSM900	Tx	93	Switch_Spectrum +400	37CH	PCL11
		94	Switch_Spectrum +600	37CH	PCL11
		95	Switch_Spectrum +1200	37CH	PCL11
		96	Switch_Spectrum +1800	37CH	PCL11
		97	Switch_Spectrum -1800	37CH	PCL19
		98	Switch_Spectrum -1200	37CH	PCL19
		99	Switch_Spectrum -600	37CH	PCL19
		100	Switch_Spectrum -400	37CH	PCL19
		101	Switch_Spectrum +400	37CH	PCL19
		102	Switch_Spectrum +600	37CH	PCL19
		103	Switch_Spectrum +1200	37CH	PCL19
		104	Switch_Spectrum +1800	37CH	PCL19
		105	Burst Timing	37CH	PCL5
		106	Burst Timing	975CH	PCL5
		107	Burst Timing	124CH	PCL5
		108	Burst Timing	37CH	PCL11
		109	Burst Timing	37CH	PCL19
	Rx	110	Rx Sensitivity	37CH	PCL5
		111	Rx Sensitivity	975CH	PCL5
		112	Rx Sensitivity	124CH	PCL5
		113	Usable Receiver Level	37CH	PCL5
		114	Rx Level Reports	37CH	PCL5
DCS	Tx	115	Burst Power	699CH	PCL0
		116	Burst Power	512CH	PCL0
		117	Burst Power	855CH	PCL0
		118	Burst Power	699CH	PCL5
		119	Burst Power	699CH	PCL15
		120	Frequency Error	699CH	PCL0
		121	Frequency Error	512CH	PCL0
		122	Frequency Error	885CH	PCL0
		123	Phase Error (RMS)	699CH	PCL0
		124	Phase Error (RMS)	512CH	PCL0
		125	Phase Error (RMS)	885CH	PCL0
		126	Phase Error (Peak)	699CH	PCL0
		127	Phase Error (Peak)	512CH	PCL0
		128	Phase Error (Peak)	855CH	PCL0
		129	Mod_spectrum -800	699CH	PCL0
		130	Mod_spectrum -600	699CH	PCL0
		131	Mod_spectrum -400	699CH	PCL0
		132	Mod_spectrum -250	699CH	PCL0
		133	Mod_spectrum -200	699CH	PCL0
		134	Mod_spectrum +200	699CH	PCL0
		135	Mod_spectrum +250	699CH	PCL0
		136	Mod_spectrum +400	699CH	PCL0
		137	Mod_spectrum +600	699CH	PCL0
		138	Mod_spectrum +800	699CH	PCL0
		139	Mod_spectrum -800	512CH	PCL0

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL
DCS	Tx	140	Mod_spectrum -600	512CH	PCL0
		141	Mod_spectrum -400	512CH	PCL0
		142	Mod_spectrum -250	512CH	PCL0
		143	Mod_spectrum -200	512CH	PCL0
		144	Mod_spectrum +200	512CH	PCL0
		145	Mod_spectrum +250	512CH	PCL0
		146	Mod_spectrum +400	512CH	PCL0
		147	Mod_spectrum +600	512CH	PCL0
		148	Mod_spectrum +800	512CH	PCL0
		149	Mod_spectrum -800	885CH	PCL0
		150	Mod_spectrum -600	885CH	PCL0
		151	Mod_spectrum -400	885CH	PCL0
		152	Mod_spectrum -250	885CH	PCL0
		153	Mod_spectrum -200	885CH	PCL0
		154	Mod_spectrum +200	885CH	PCL0
		155	Mod_spectrum +250	885CH	PCL0
		156	Mod_spectrum +400	885CH	PCL0
		157	Mod_spectrum +600	885CH	PCL0
		158	Mod_spectrum +800	885CH	PCL0
		159	Mod_spectrum -800	699CH	PCL5
		160	Mod_spectrum -600	699CH	PCL5
		161	Mod_spectrum -400	699CH	PCL5
		162	Mod_spectrum -250	699CH	PCL5
		163	Mod_spectrum -200	699CH	PCL5
		164	Mod_spectrum +200	699CH	PCL5
		165	Mod_spectrum +250	699CH	PCL5
		166	Mod_spectrum +400	699CH	PCL5
		167	Mod_spectrum +600	699CH	PCL5
		168	Mod_spectrum +800	699CH	PCL5
		169	Mod_spectrum -800	699CH	PCL15
		170	Mod_spectrum -600	699CH	PCL15
		171	Mod_spectrum -400	699CH	PCL15
		172	Mod_spectrum -250	699CH	PCL15
		173	Mod_spectrum -200	699CH	PCL15
		174	Mod_spectrum +200	699CH	PCL15
		175	Mod_spectrum +250	699CH	PCL15
		176	Mod_spectrum +400	699CH	PCL15
		177	Mod_spectrum +600	699CH	PCL15
		178	Mod_spectrum +800	699CH	PCL15
		179	Switch_Spectrum -1800	699CH	PCL0
		180	Switch_Spectrum -1200	699CH	PCL0
		181	Switch_Spectrum -600	699CH	PCL0
		182	Switch_Spectrum -400	699CH	PCL0
		183	Switch_Spectrum +400	699CH	PCL0
		184	Switch_Spectrum +600	699CH	PCL0
		185	Switch_Spectrum +1200	699CH	PCL0
		186	Switch_Spectrum +1800	699CH	PCL0
		187	Switch_Spectrum -1800	512CH	PCL0

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL
DCS	Tx	188	Switch_Spectrum -1200	512CH	PCL0
		189	Switch_Spectrum -600	512CH	PCL0
		190	Switch_Spectrum -400	512CH	PCL0
		191	Switch_Spectrum +400	512CH	PCL0
		192	Switch_Spectrum +600	512CH	PCL0
		193	Switch_Spectrum +1200	512CH	PCL0
		194	Switch_Spectrum +1800	512CH	PCL0
		195	Switch_Spectrum -1800	885CH	PCL0
		196	Switch_Spectrum -1200	885CH	PCL0
		197	Switch_Spectrum -600	885CH	PCL0
		198	Switch_Spectrum -400	885CH	PCL0
		199	Switch_Spectrum +400	885CH	PCL0
		200	Switch_Spectrum +600	885CH	PCL0
		201	Switch_Spectrum +1200	885CH	PCL0
		202	Switch_Spectrum +1800	885CH	PCL0
		203	Switch_Spectrum -1800	699CH	PCL5
		204	Switch_Spectrum -1200	699CH	PCL5
		205	Switch_Spectrum -600	699CH	PCL5
		206	Switch_Spectrum -400	699CH	PCL5
		207	Switch_Spectrum +400	699CH	PCL5
		208	Switch_Spectrum +600	699CH	PCL5
		209	Switch_Spectrum +1200	699CH	PCL5
		210	Switch_Spectrum +1800	699CH	PCL5
		211	Switch_Spectrum -1800	699CH	PCL15
		212	Switch_Spectrum -1200	699CH	PCL15
		213	Switch_Spectrum -600	699CH	PCL15
		214	Switch_Spectrum -400	699CH	PCL15
		215	Switch_Spectrum +400	699CH	PCL15
		216	Switch_Spectrum +600	699CH	PCL15
		217	Switch_Spectrum +1200	699CH	PCL15
		218	Switch_Spectrum +1800	699CH	PCL15
		219	Burst Timing	699CH	PCL0
		220	Burst Timing	512CH	PCL0
		221	Burst Timing	885CH	PCL0
		222	Burst Timing	699CH	PCL5
		223	Burst Timing	699CH	PCL15
	Rx	224	Rx Sensitivity	699CH	PCL0
		225	Rx Sensitivity	512CH	PCL0
		226	Rx Sensitivity	885CH	PCL0
		227 Usable Receiver L		699CH	PCL0
		228	Rx Level Reports	699CH	PCL0
PCS	Tx	229	Burst Power	661CH	PCL0
. 00		230	Burst Power	512CH	PCL0
		231	Burst Power	810CH	PCL0

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL
PCS	Tx	232	Burst Power	661CH	PCL5
	2		Burst Power	661CH	PCL15
		234	Frequency Error	661CH	PCL0
	235		Frequency Error	512CH	PCL0
		236	Frequency Error	810CH	PCL0
		237	Phase Error (RMS)	661CH	PCL0
		238	Phase Error (RMS)	512CH	PCL0
		239	Phase Error (RMS)	810CH	PCL0
		240	Phase Error (Peak)	661CH	PCL0
		241	Phase Error (Peak)	512CH	PCL0
		242	Phase Error (Peak)	810CH	PCL0
		243	Mod_spectrum -800	661CH	PCL0
		244	Mod_spectrum -600	661CH	PCL0
		245	Mod_spectrum -400	661CH	PCL0
		246	Mod_spectrum -250	661CH	PCL0
		247	Mod_spectrum -200	661CH	PCL0
		248	Mod_spectrum +200	661CH	PCL0
		249	Mod_spectrum +250	661CH	PCL0
		250	Mod_spectrum +400	661CH	PCL0
		251	Mod_spectrum +600	661CH	PCL0
		252	Mod_spectrum +800	661CH	PCL0
		253	Mod_spectrum -800	512CH	PCL0
		254	Mod_spectrum -600	512CH	PCL0
		255	Mod_spectrum -400	512CH	PCL0
		256	Mod_spectrum -250	512CH	PCL0
		257	Mod_spectrum -200	512CH	PCL0
		258	Mod_spectrum +200	512CH	PCL0
		259	Mod_spectrum +250	512CH	PCL0
		260	Mod_spectrum +400	512CH	PCL0
		261	Mod_spectrum +600	512CH	PCL0
		262	Mod_spectrum +800	512CH	PCL0
		263	Mod_spectrum -800	810CH	PCL0
		264	Mod_spectrum -600	810CH	PCL0
	265		Mod_spectrum -400	810CH	PCL0
		266	Mod_spectrum -250	810CH	PCL0
		267	Mod spectrum -200	810CH	PCL0
		268	Mod_spectrum +200	810CH	PCL0
		269	Mod_spectrum +250	810CH	PCL0
		270	Mod_spectrum +400	810CH	PCL0
		271	Mod_spectrum +600	810CH	PCL0
	272		Mod_spectrum +800	810CH	PCL0
		273	Mod_spectrum -800	661CH	PCL5
	274		Mod_spectrum -600	661CH	PCL5
	275		Mod_spectrum -400	661CH	PCL5
		276	Mod_spectrum -250	661CH	PCL5
		277	Mod_spectrum -200	661CH	PCL5
		278	Mod_spectrum +200	661CH	PCL5
		279	Mod_spectrum +250	661CH	PCL5
		280	Mod_spectrum +400	661CH	PCL5
			•		

Band	Sending/	No.	Item to be	Channel	PCL
PCS	Receive	281	inspected Mod_spectrum +600	661CH	PCL5
1 00	1^				PCL5
		282	Mod_spectrum +800	661CH	
		283	Mod_spectrum -800	661CH	PCL15
		284	Mod_spectrum -600	661CH	PCL15
		285	Mod_spectrum -400	661CH	PCL15
		286	Mod_spectrum -250	661CH	PCL15
		287	Mod_spectrum -200	661CH	PCL15
		288	Mod_spectrum +200	661CH	PCL15
		289	Mod_spectrum +250	661CH	PCL15
		290	Mod_spectrum +400	661CH	PCL15
		291	Mod_spectrum +600	661CH	PCL15
		292	Mod_spectrum +800	661CH	PCL15
		293	Switch_Spectrum -1800	661CH	PCL0
		294	Switch_Spectrum -1200	661CH	PCL0
		295	Switch_Spectrum -600	661CH	PCL0
		296	Switch_Spectrum -400	661CH	PCL0
		297	Switch_Spectrum +400	661CH	PCL0
		298	Switch_Spectrum +600	661CH	PCL0
		299	Switch_Spectrum +1200	661CH	PCL0
		300	Switch_Spectrum +1800	661CH	PCL0
		301	Switch_Spectrum -1800	512CH	PCL0
		302	Switch_Spectrum -1200	512CH	PCL0
		303	Switch_Spectrum -600	512CH	PCL0
		304	Switch_Spectrum -400	512CH	PCL0
		305	Switch_Spectrum +400	512CH	PCL0
		306	Switch_Spectrum +600	512CH	PCL0
		307	Switch_Spectrum +1200	512CH	PCL0
		308	Switch_Spectrum +1800	512CH	PCL0
		309	Switch_Spectrum -1800	810CH	PCL0
		310	Switch_Spectrum -1200	810CH	PCL0
		311	Switch_Spectrum -600	810CH	PCL0
		312	Switch_Spectrum -400	810CH	PCL0
		313	Switch Spectrum +400	810CH	PCL0
		314	Switch_Spectrum +600	810CH	PCL0
			Switch_Spectrum +1200		PCL0
		315	_ ·	810CH	
		316	Switch_Spectrum +1800	810CH	PCL0
		317	Switch_Spectrum -1800	661CH	PCL5
		318	Switch_Spectrum -1200	661CH	PCL5
		319	Switch_Spectrum -600	661CH	PCL5
		320	Switch_Spectrum -400	661CH	PCL5
		321	Switch_Spectrum +400	661CH	PCL5
		322	Switch_Spectrum +600	661CH	PCL5
		323	Switch_Spectrum +1200	661CH	PCL5
		324	Switch_Spectrum +1800	661CH	PCL5

Band	Sending/ Receive	No.	Item to be inspected	Channel	PCL
PCS	Tx	325	Switch_Spectrum -1800	661CH	PCL15
		326	Switch_Spectrum -1200	661CH	PCL15
		327	Switch_Spectrum -600	661CH	PCL15
		328	Switch_Spectrum -400	661CH	PCL15
		329	Switch_Spectrum +400	661CH	PCL15
		330	Switch_Spectrum +600	661CH	PCL15
		331	Switch_Spectrum +1200	661CH	PCL15
	332		Switch_Spectrum +1800	661CH	PCL15
		333	Burst Timing	661CH	PCL0
		334	Burst Timing	512CH	PCL0
		335	Burst Timing	810CH	PCL0
		336	Burst Timing	661CH	PCL5
		337	Burst Timing	661CH	PCL15
	Rx	338	Rx Sensitivity	661CH	PCL0
		339	Rx Sensitivity	512CH	PCL0
		340	Rx Sensitivity	810CH	PCL0
		341	Usable Receiver Level	661CH	PCL0
		342	Rx Level Reports	661CH	PCL0

# **■** Troubleshooting list

Test items	Check parts for GSM900	Check parts for DCS	Check parts for PCS
Tx			
Burst Power	IC802, IC803, FL905	IC802, IC803, FL905	IC802, IC803, FL905
Frequency Error	TCX801	TCX801	TCX801
Phase Error	IC801	IC801	IC801
Mod_spectrum	IC801, TCX801	IC801, TCX801	IC801, TCX801
Switch_Spectrum	IC801, IC802 IC803	IC801, IC802 IC803	IC801, IC802, IC803
Burst Timing	IC802	IC802	IC802
Rx			
Rx Sensitivity	IC801, IC803, FL902, FL905	IC801, IC803, FL902, FL905	IC801, IC803, FL903, FL905
Usable Receiver Level	IC801	IC801	IC801
Rx Level Reports	IC801, IC803, FL902, FL905	IC801, IC803, FL902, FL905	IC801, IC803, FL903, FL905

# 4-6. RF TEST TOOL

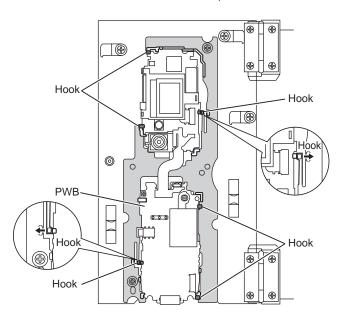
# 4-6-1. Requirements

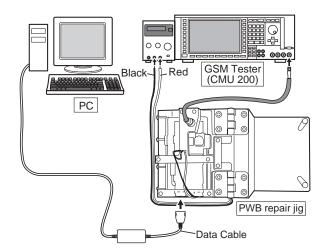
For repairs, this test checks the condition of an electric board (especially the RF section).

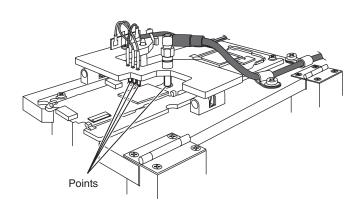
- PC with COM port
- TM200 Data Cable
- PWB repair jig
- GSM Tester (CMU200)

# 4-6-2. Setup

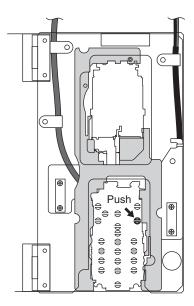
Set PWB and make connections as shown below.
 Make sure connections are correct at the points shown below.



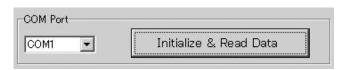




2. Apply 4 V using a stabilized power supply and turn on the handset.



- 3. Start RF test tool.
- 4. Select a COM port to which Data Cable is connected.
- 5. Press the "Initialize & Read Data" button.



6. The figre shown below appears (wait a few seconds).

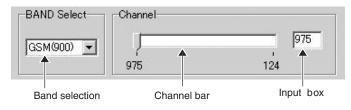


7. Click "OK" to proceed.

# 4-6-3. Tests

# 1) BAND Select & Channel

Select a band and a channel to test. Settings are applied to all tests.

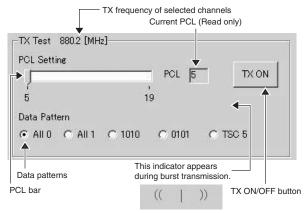


# [Procedure]

- 1. Select a band. (GSM900, DCS or PCS)
- 2. Select or enter a channel using Channel bar or Input box.

# 2) TX test

Test burst transmission.



# [Procedure]

- 1. Select a band and channel. [See 4-6-13. 1)]
- 2. Select PCL (Power Control Level) using PCL bar.
- 3. Select Data pattern.
- 4. Click TX ON to start burst transmission. (You can check each part in this state.)
- 5. Click TX OFF to end burst transmission.
- \*Data pattern (TSC 5) includes Training Sequence GSM 5, and other part is pseudo random data.

TM200 TX power Table (25°C, voltage: 3.7[V])

# **■ GSM900 Band**

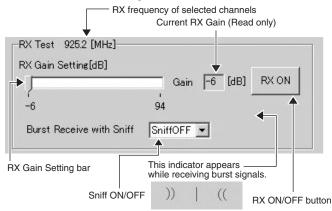
PCL	GSM900	Tolerance
FCL	[dBm]	Tolerance
5	33	+/- 2 dB
6	31	+/- 3 dB
7	29	+/- 3 dB
8	27	+/- 3 dB
9	25	+/- 3 dB
10	23	+/- 3 dB
11	21	+/- 3 dB
12	19	+/- 3 dB
13	17	+/- 3 dB
14	15	+/- 3 dB
15	13	+/- 3 dB
16	11	+/- 5 dB
17	9	+/- 5 dB
18	7	+/- 5 dB
19	5	+/- 5 dB

**■ DCS/PCS Band** 

PCL	DCS/PCS	Tolerance
FCL	[dBm]	Tolerance
0	30	+/- 2 dB
1	28	+/- 3 dB
2	26	+/- 3 dB
3	24	+/- 3 dB
4	22	+/- 3 dB
5	20	+/- 3 dB
6	18	+/- 3 dB
7	16	+/- 3 dB
8	14	+/- 3 dB
9	12	+/- 4 dB
10	10	+/- 4 dB
11	8	+/- 4 dB
12	6	+/- 4 dB
13	4	+/- 4 dB
14	2	+/- 5 dB
15	0	+/- 5 dB

# 3) RX test

The handset receives burst signals in this test.





#### [Procedure]

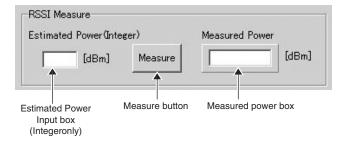
- 1. Select a channel and band. [see 4-6-3.1)]
- 2. Select RX Gain using RX Gain Setting bar.
- 3. Choose Sniff ON or OFF.
- 4. Click "RX ON" to start receiving burst signals.
- From GSM tester, send burst signals in the specified channel. (You can check each part in this state.)
- 6. Click "RX OFF" to end receiving burst signals.
  - ★In this test, the reception timing cannot be synchronized with burst signals from Signal Generator or GSM tester.
  - ★The standard RX Gain Setting is:

(Input power at the aerial connector of the handset) + (RX Gain)

Excessive Input power or RX Gain may cause damage to the handset.

# 4) RSSI Measure

The handset notifies you of input power value at the aerial connector.



#### [Procedure]

- 1. Connect the handset and GSM tester (or Signal Generator) with RF cable.
- 2. Select a band and channel. [see 4-6-3. 1)]
- 3. Send signals (\*) from GSM tester.
- Enter the value of input power from GSM tester in integers (from -10 to -110) considering RF cable loss.
- 5. Press the [Measure] button.
- 6. The result appears in Measured Power box.

**★**The signal type from GSM tester must be either of two:

 Continuous sine wave (without modulation) with the frequency as follows:

(Frequency of the measured channel) + 67.708kHz. (Ex. channel: GSM 37ch  $\rightarrow$  the result: 942.467708 MHz)

2. BCCH signal of the measured channel Power: -110 to -10 dBm

Power: -110 to -10 dBm

# Result

When the handset is properly calibrated, the error between "Estimated Power" and "Measured Power" is less than 3dB.

#### 4-6-4. Termination

Turn off the handset to ensure proper operations.

# 4-6-5. Trouble information

When switching DCS and PCS, change the channel number as well. Or the band does not change properly.

Example: If you change DCS 512 CH to PCS 512 CH, the band remains DCS.

#### 4-7. Password reset

SPST resets the password (handset code is set to "0000").

#### <Operation>

Set the COM port on the SPST initial screen and click "User Password Reset". Click "Yes" to reset. Click "No" to exit.



2) When completed, the following appears.



# 4-8. Performance check and adjustment

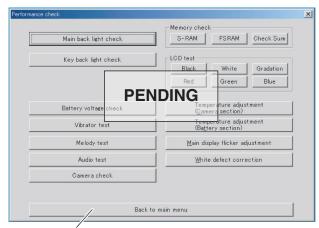
With this function, SPST checks the performance of the handset and makes adjustments.

# <Operation>

 Set the COM port on the SPST initial screen and click "Performance check and adjustment". The following dialog box appears while processing.



When completed, the following is displayed.
 Click "Back to main menu" to exit.



The functions of each button are described below.

# 4-8-1. Main back light check

The main display backlight turns on and the message appears on the PC.



Check the backlight and press "OK".

• If a failure occurs, see "10. Back Light does not turn on." in [3] Troubleshooting.

# 4-8-2. External back light check

The external display back light turns on and the message appears on the PC. Check the back light and press "OK".

If a failure occurs, see "10. Back Light does not turn on." in [3] Troubleshooting.

# 4-8-3. Key back light check

The keypad back light turns on and the message appears on the PC. Check the back light and press "OK".

#### 4-8-4. LED check

The LED lights up in a specified color and the message appears on the PC. Check the LED and press "OK".

If a failure occurs, see "15. Flash light does not work." in [3] Trouble-shooting.

# 4-8-5. Battery voltage check

Click to display the current battery voltage.

• If a failure occurs, see "1. Power is not turned on." in [3] Troubleshooting.

#### 4-8-6. SD read/write test

Insert an SD card (otherwise a message prompts you to do so and click the button to perform the SD card read/write test.

 If a failure occurs, see "17. SD (Memory) card is not recognized." in [3] Troubleshooting.

#### 4-8-7. Vibrator test

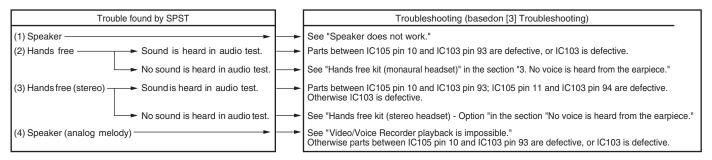
Click to vibrate the handset. Click "OK" to exit.

If a failure occurs, see "5. Vibrator does not work." in [3] Trouble-shooting.

#### 4-8-8. Melody test

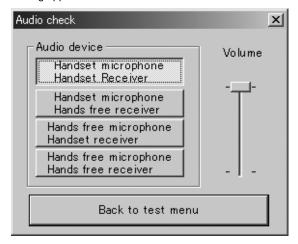
A message describes test items. Click "Yes" to proceed and "No" to exit. The order of the test items:

speaker → hands free → hands free (stereo) → speaker (analog melody)

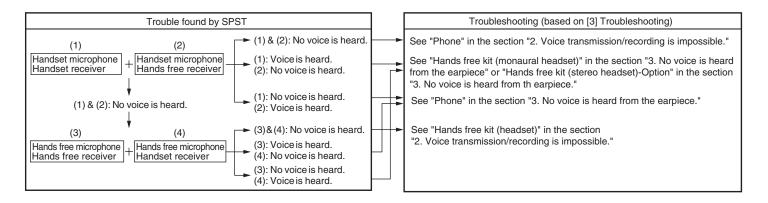


# 4-8-9. Audio test

The following appears.

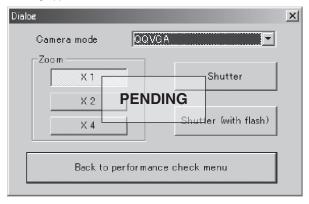


Select a test item from Audio device. Check the output sound from the receiver by speaking to the microphone, etc. Click "Back to test menu" to return to the previous screen.



#### 4-8-10. Camera check

The following appears.



Select a Camera mode from the pull-down menu. Click "Shutter" to check that the camera operates properly. Click "Back to performance check menu" to return to the previous screen.

If a failure occurs, see "10. Pictures cannot be taken." in [3] Trouble-shooting.

# 4-8-11. Memory check

Click "S-RAM" and "PSRAM" to see each test result.

For "Check Sum", the calculation appears after the SPST communicating dialog box.

# 4-8-12. LCD test

Check that the specified color appears on the main display.

If a failure occurs, see "12. The display does not appear on Main Display." and "13. The display does not appear on External Display (in 65K color mode)." in [3] Troubleshooting.

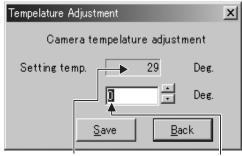
# 4-8-13. Temperature adjustment

The following appears.

Setting temp. indicates the current temperature. The relative temperature is displayed in the text box below.

(Only the relative temperature is adjustable.)

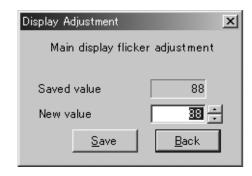
If displayed Setting temp. value differs from the current temperature, click [▲] or [▼] to set a correction value in the range of -99 to +99 and click "Save"



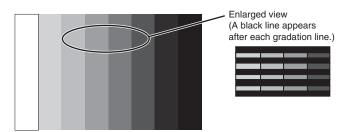
Correction value = (Setting temp.) - (current temp.) + (displayed correction value)

# 4-8-14. Main display flicker adjustment

The following is displayed.



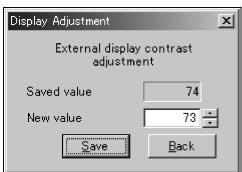
Check a main display visually within a distance of 20 cm from a fluorescent light, and adjust the value to minimize flicker on the display with the [▲] and [▼] buttons. Click "Save" and confirm that the main display does not flicker. (Fine adjustment for DC voltage between display electrodes)



8-level graduation pattern with alternate black and gradation lines (black and white)

# 4-8-15. External display contrast adjustment

Click the "External display contrast adjustment" button. The following screen appears.



# DEN: 075

8-level gradation pattern (black & white pattern)

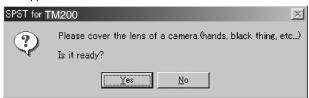
Comparing with an adjusted handset, click "\( \Lambda \)" or "\( \nabla \)" to adjust the value so that the same gradation pattern is displayed. Click "Save" and confirm the pattern on the external display.

#### 4-8-16. White defect correction

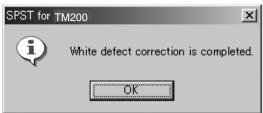
#### \*White defect correction:

Defective pixels in a camera light sensor appear as bright points in the display even when light is blocked completely (display is all black). Perform white defect correction to eliminate errors in these pixels.

- 1. Protect the handset camera from light completely with a black cover.
- Click the "White defect correction" button. The following screen appears.



Click the "Yes" button and leave it for about 20 seconds. When completed, the following message appears.



When an error occurs, the corresponding message appears. Solve the problem according to "Solution".

• Error 1

Error message : "There are too many white cracks."

Cause : The light is not sufficiently blocked.

Solution : Block the light completely and perform white

defect correction again.

• Error 2

Error message : "There are many white cracks."

Cause : The light is not sufficiently blocked.

Solution : Block the light completely and perform white

defect correction again.

• Error 3

Error message : "There are too many white cracks cannot be

rectified."

Cause : There is a hardware error.
Solution : Replace the camera unit.

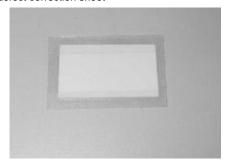
#### 4-8-17. Black defect correction

# \*Black defect correction:

Defective pixels in a camera light sensor appear as black points in the display even when a captured image is completely white (display is all white). Perform black defect correction to eliminate errors in these pixels.

# 1) Requirements

- · Desk top type of fluorescent lamp
- · Black defect correction sheet



• Illuminance meter

#### 2) Procedure

 Cover the camera section with the black defect correction sheet as shown in Figure 96.



Check the distance from the fluorescent lamp by using an illuminance meter.

In the proper position for black defect correction, illuminance is between 8,000 and 10,000 lux.



3. Hold the handset in the proper position.



4. Click the "Black defect correction" button. The following message is displayed.



5. Click the "Yes" button. Communication starts.



6. The result is displayed within a minute as follows.



When an error occurs, the corresponding message appears. Solve the problem according to "Solution".

• Error 1

Error message : "There are too many black cracks."

Cause : The light is too weak or strong.

Solution : At the proper distance from the light source (8,000-

10,000 lux), perform black defect correction again.

• Error 2

Error message : "There are many black cracks."

Cause : The light is too weak or strong.

Solution : At the proper distance from the light source

(8,000 - 10,000 lux), perform black defect correction again.

• Error 3

Error message : "There are too many black cracks cannot be rectified."

Cause : There is a hardware error.
Solution : Replace the camera unit.

# 4-9. \*\*\*\*MODE RELEASE

When the handset does not turn on and enter the normal mode, use this function to change \*\*\*\* mode to the normal mode.

<Operation>

 Select the COM port on the SPST initial screen and click "\*\*\*\* mode release". The following dialog box appears.



If SPST cannot communicate with the handset, the following message is displayed. Make sure the handset is turned on and click "Retry". To exit, click "Cancel".



3) When complete, the following message appears.



# 5. OTHER TESTS

SPST does not provide tests of Bluetooth/USB communication. Check them according to the following instructions.

# 5-1. USB

Connect TM200 and a PC with a USB cable. Check that TM200 is recognized as a device.

If the USB driver for TM200 (SHARP GSM GPRS USB Driver) is not installed on the PC, "Found New Hardware" window appears and "Found New Hardware Wizard" starts (the handset is recognized).

# 5-2. BLUETOOTH

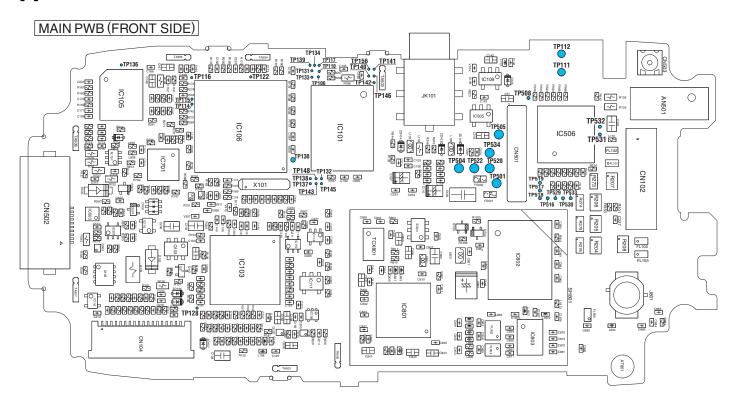
Connect TM200 to the network and check that a conversation (talking and listening) is possible using a Bluetooth headset.

Recommended Bluetooth headset:

JABRA BT200

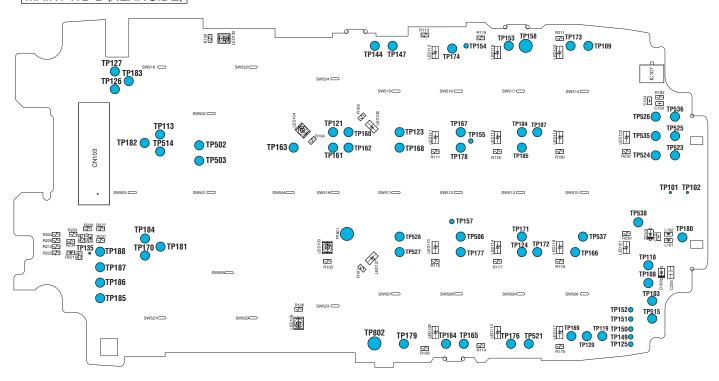
PLANTRONICS M1000 PLANTRONICS M3000

# [2] TEST POINTS

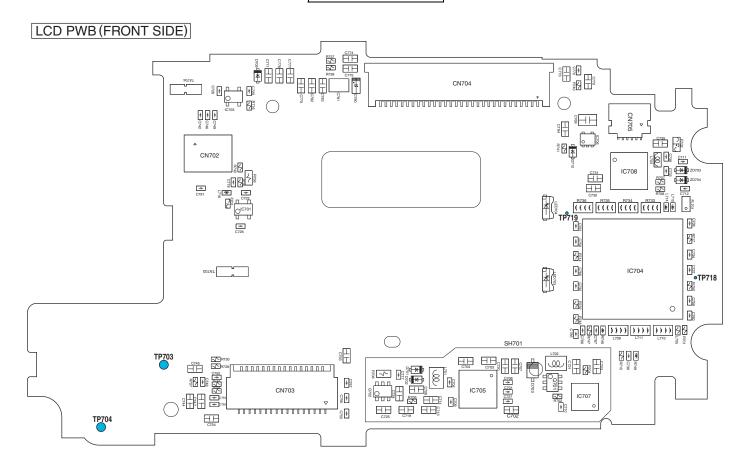


TP No.	Signal name	TP No.	Signal name
TP111	VVIB	TP505	DGND
TP112	DGND	TP520	BATT
TP501	BATT	TP522	POWONKEY
TP504	DGND	TP534	BATT_SENSE

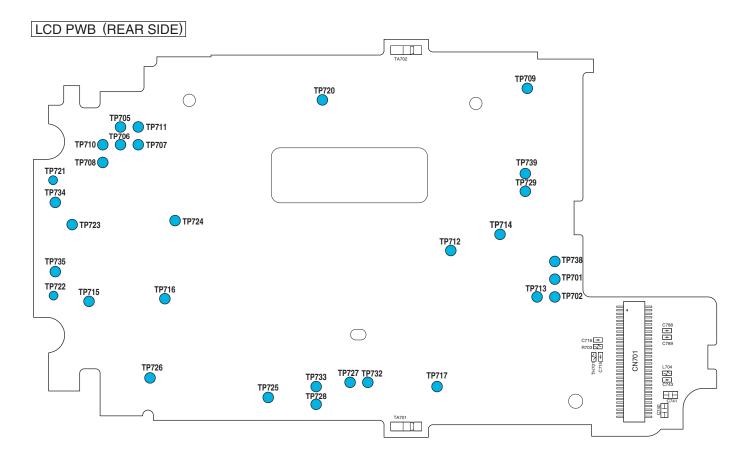
# MAIN PWB-B (REAR SIDE)



TP No.	Signal name	TP No.	Signal name
TP103	USC [0]	TP171	VCORE (1.8V)
TP104	USC [1]	TP172	VAPP
TP105	USC [2]	TP173	VINT (3V)
TP107	USC [4]	TP174	LIGHT3 (KEYLED)
TP108	USC [5]	TP176	VMIC
TP109	USC [6]	TP177	AUXADC1
TP113	VVIB	TP178	TEMP
TP118	USC [3]	TP179	AUXADC1
TP119	MIC	TP180	CHGIN_A (5.2V)
TP120	AUDIO_IN	TP181	Flexible PWB insert check terminal 1
TP121	JACK_L	TP182	Flexible PWB insert check terminal 2
TP123	RESET	TP183	Flexible PWB insert check terminal 3
TP124	PWRON	TP184	Flexible PWB insert check terminal 4
TP126	SP1	TP502	VBAT
TP127	SP2	TP503	VBAT
TP144	Terminal for STACK MEMORY adhesion check 1	TP506	BATT_SENSE
TP147	Terminal for STACK MEMORY adhesion check 2	TP514	BT_VCC (3.0V)
TP153	VPP Flash	TP515	VBUS_IN
TP157	Analog Power Supply IC INT	TP521	POWONKEY
TP158	VINT (3V)	TP523	USB D+
TP160	HEDSET_DET	TP524	USB D-
TP161	STEREO_SW	TP525	RTS
TP162	REMOTE_SW	TP526	CTS
TP163	JACK_R	TP527	DGND
TP164	VABB	TP528	DGND
TP165	VT (2.75V)	TP535	Reserved
TP166	VUSB	TP536	ManufactUre Specific
TP167	VRTC (1.8V)	TP537	CHGIN
TP168	VBACK (3V)	TP801	VTCXO (2.9V)
TP169	VSIM (2.85V)	TP802	VRF (2.9V)
TP170	VMEM (2.8V)		



TP No.	Signal name	TP No.	Signal name
TP703	SP1	TP704	SP2



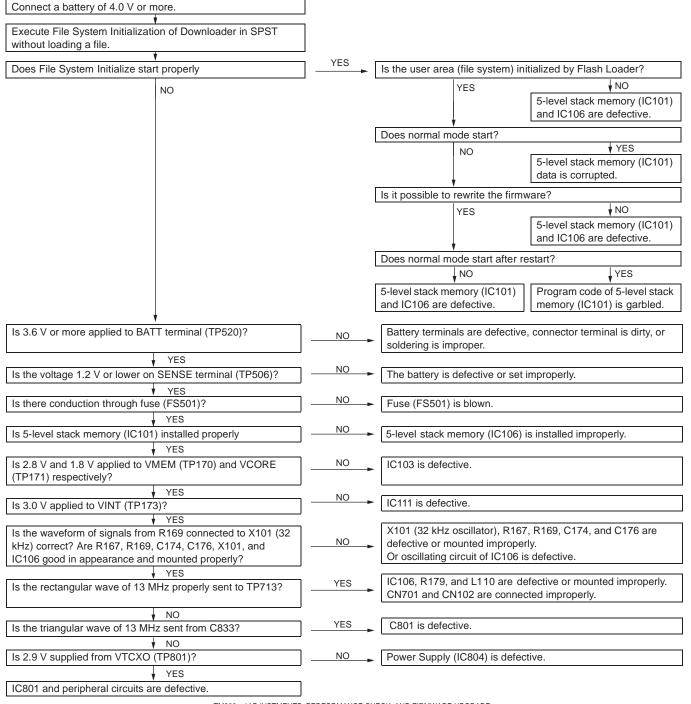
TP No.	Signal name	TP No.	Signal name
TP701	SP1	TP720	VDD2
TP702	SP2	TP721	RECIVER_OUT+
TP705	Backlight 4	TP722	RECIVER_OUT-
TP706	Backlight 3	TP723	Terminal for LCDC adhesion check 3
TP707	Backlight 2	TP724	Terminal for LCDC adhesion check 4
TP708	Flash (LED-)	TP725	Terminal for APPLICATION POWER adhesion check
TP709	VLCD_INT (3.0V)	TP726	Power supply for camera (-8 V)
TP710	Backlight & Flash (LED+)	TP727	Power supply for camera (+15V)
TP711	Backlight 1	TP728	VDD2 (3V)
TP712	CAMCLK	TP729	VBAT
TP713	13MHzCLK	TP733	VDD1 (1.8V)
TP714	VLCD (1.8V)	TP734	RECIVER_OUT+
TP715	Terminal for LCDC adhesion check 1	TP735	RECIVER_OUT-
TP716	Terminal for LCDC adhesion check 2	TP738	VBAT
TP717	VOUT (External Display)		

# [3] TROUBLESHOOTING

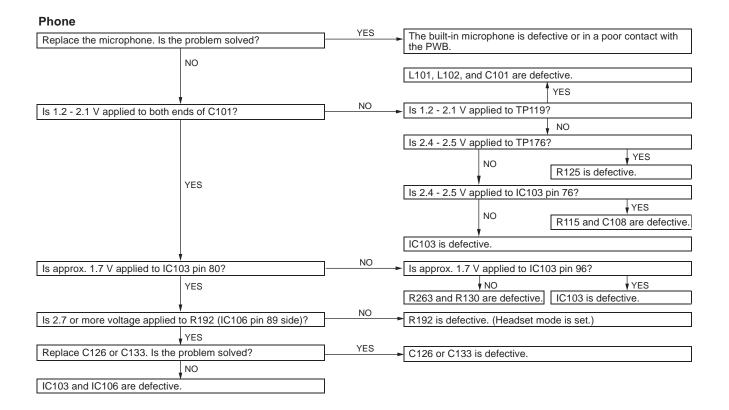
- 1. Power is not turned on.
- 2. Voice transmission/recording is impossible.
- 3. No voice is heard from the earpiece.
- 4. Battery does not charge.
- 5. Vibrator does not work.
- 6. Clock Settings are reset.
- 7. Speaker does not work.
- 8. MP3 cannot be played.
- 9. Video/Voice Recorder playback is impossible.
- 10. Back Light does not turn on.

- 11. Out of range and incoming/outgoing calls are impossible.
- 12. The display does not appear on Main Display.
- The display does not appear on External Display (in 65K color mode).
- 14. Pictures cannot be taken.
- 15. AF does not move.
- 16. SIM card is not recognized.
- 17. SD (Memory) card is not recognized.
- 18. USB connection is impossible.
- 19. Bluetooth communication is impossible.

# 1. POWER IS NOT TURNED ON.

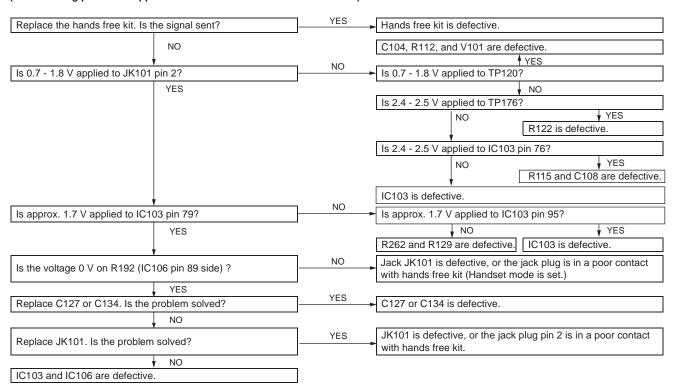


# 2. VOICE TRANSMISSION/RECORDING IS IMPOSSIBLE.

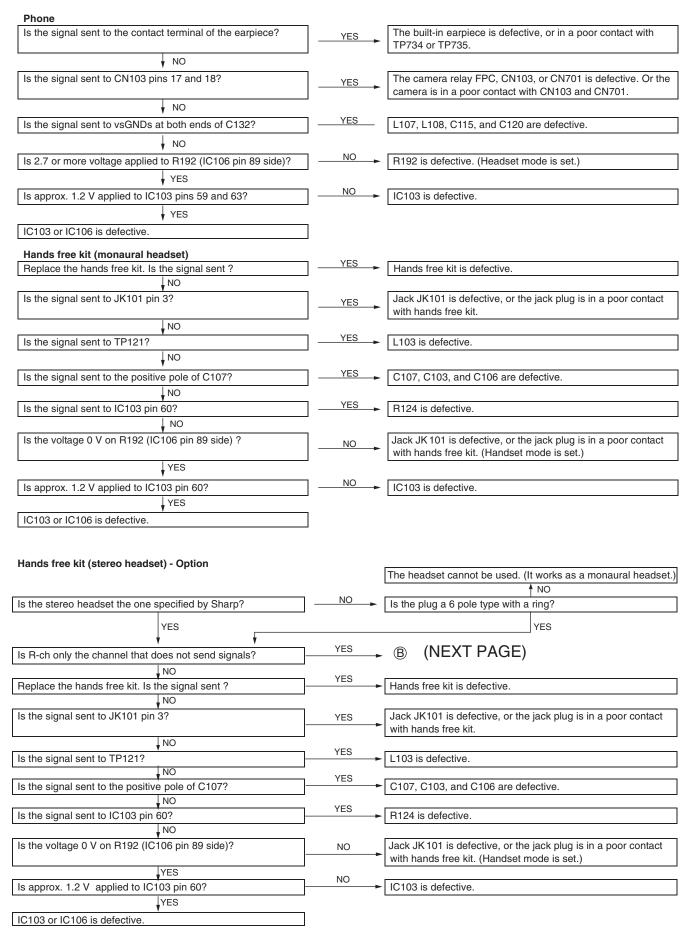


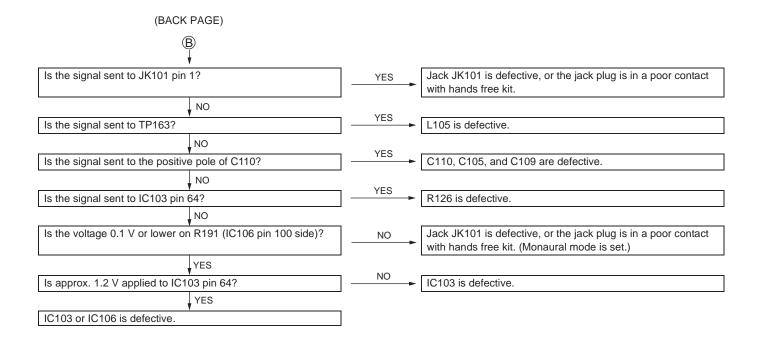
#### Hands free kit (headset)

(The following procedure applies to both monaural and stereo headsets.)

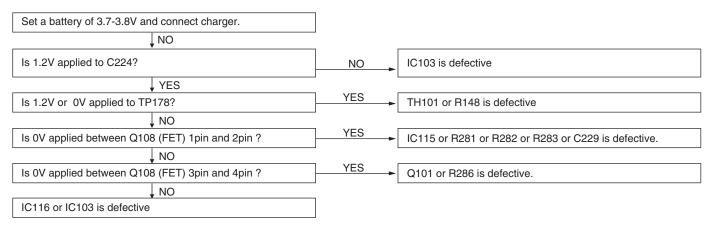


# 3. NO VOICE IS HEARD FROM THE EARPIECE.

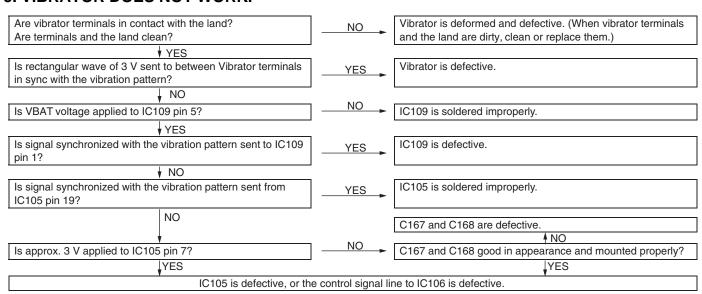




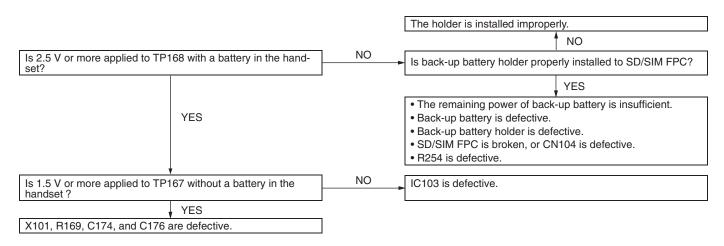
# 4. BATTERY DOES NOT CHARGE.



# 5. VIBRATOR DOES NOT WORK.

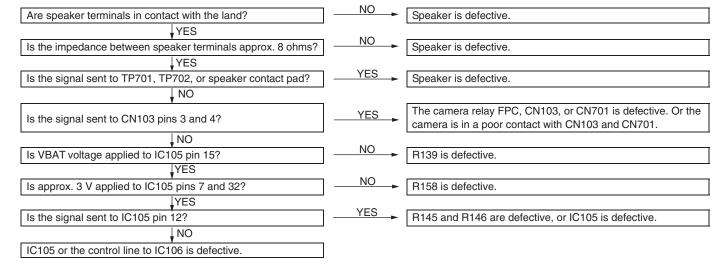


### 6. CLOCK SETTING ARE RESET.

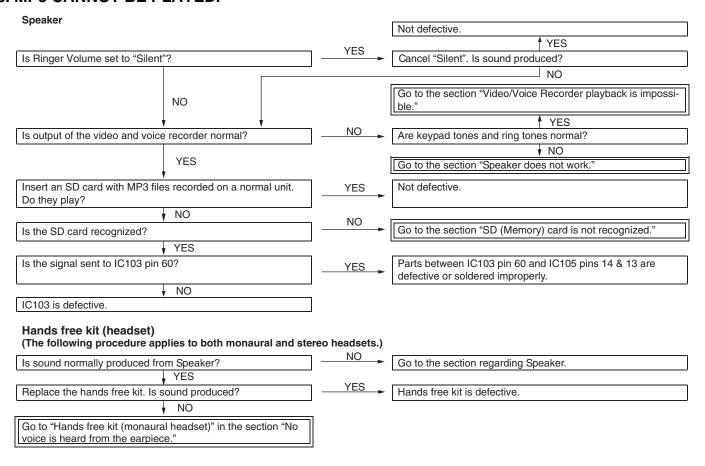


#### 7. SPEAKER DOES NOT WORK.

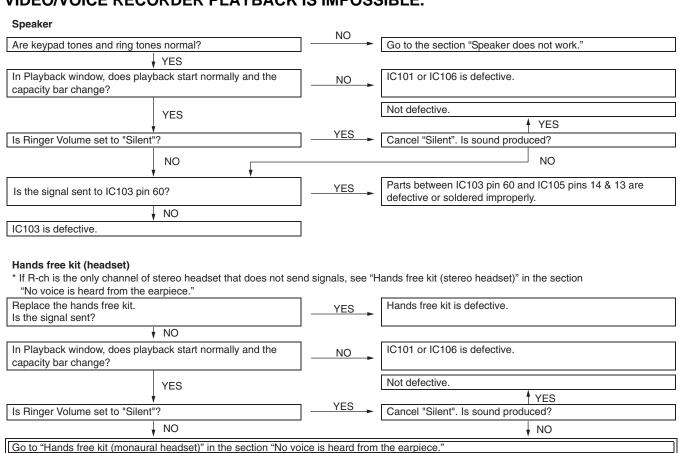
- \* When ring tones sound, but keypad tones do not, "Keypad Tones" is set to Off.
- \* When Ringer Volume is set to "Silent":
- · Voice Recorder playback sound is not produced.
- · Playback sound of Video and MP3 can be heard by increasing the volume during playback.



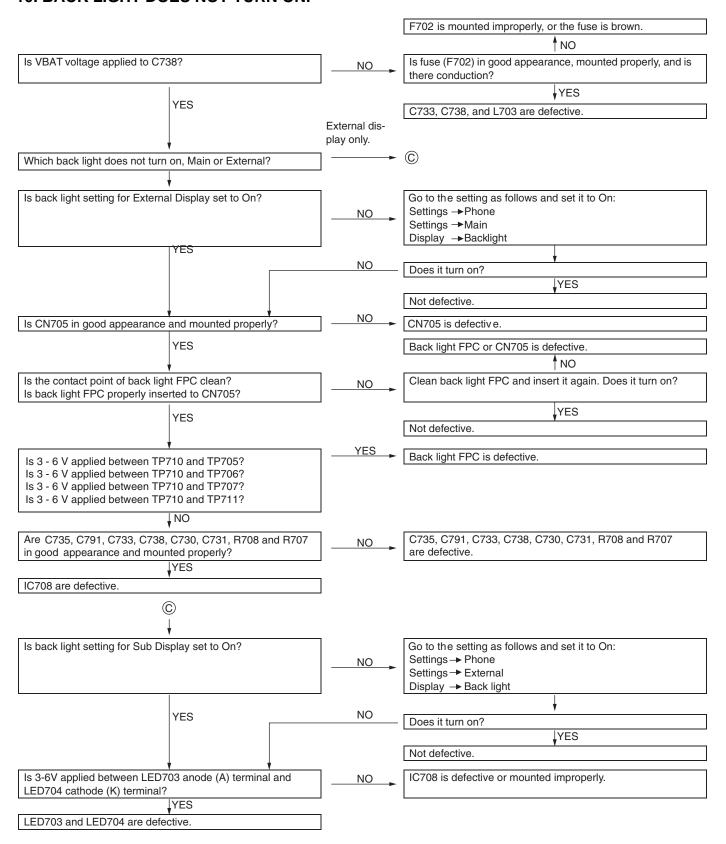
#### 8. MP3 CANNOT BE PLAYED.



#### 9. VIDEO/VOICE RECORDER PLAYBACK IS IMPOSSIBLE.



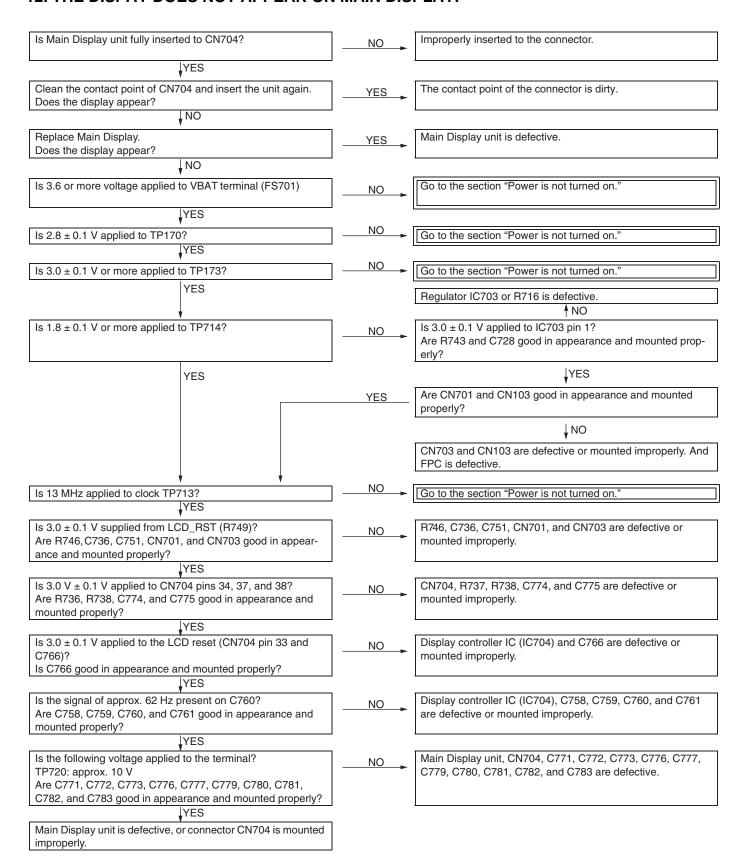
### 10. BACK LIGHT DOES NOT TURN ON.



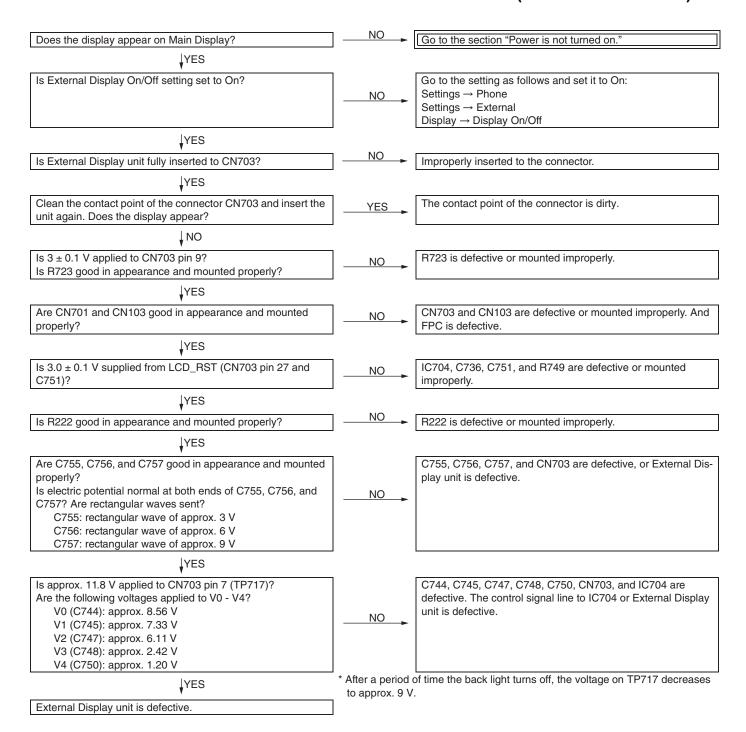
### 11. OUT OF RANGE AND INCOMING/OUTGOING CALLS ARE IMPOSSIBLE.

[Checkpoint s in RF Test Tool] Is transmission possible using RF Test Tool? YES [Sender] IC804 is defective. Is voltage (applox. 2.9 V) supplied to pin 6 of IC804? YES Is IQ signal supplied to pins 23, 24, 25, and 26 of IC801? IC103, IC106, or PWB is defective. YES Is frequency signal sent? IC801 is defective. NO GSM900 bands ...... IC801 pin 17 DCS1800/PCS1900 bands ......IC801 pin 19 IC802 is defective. Is frequency signal supplied? NO GSM900 bands ...... IC803 pin 16 DCS1800/PCS1900 bands ..... IC803 pin 14 YES IC803 is defective. Is frequency signal supplied to pin 1 of FL905? **↓**YES NO FL905 is defective. Is frequency signal supplied to pin 1 of J801? **YES** J801 is defective. [Receiver] -70 dBm input. Is frequency signal supplied? IC801 is defective. GSM900 bands ...... IC801 pins 9, 10 YES DCS1800 band ...... IC801 pins 6, 7 PCS1900 band ...... IC801 pins 3, 4 NO FL902, or FL903 is defective. Is frequency signal supplied? YES GSM900 band ...... FL902 pin 4 DCS1800 band ...... FL902 pin 1 PCS1900 band ...... FL903 pin 1 ↓ NO IC803 is defective. Is frequency signal supplied to pin 10 of IC803 \_ NO FL905 or J801 is defective.

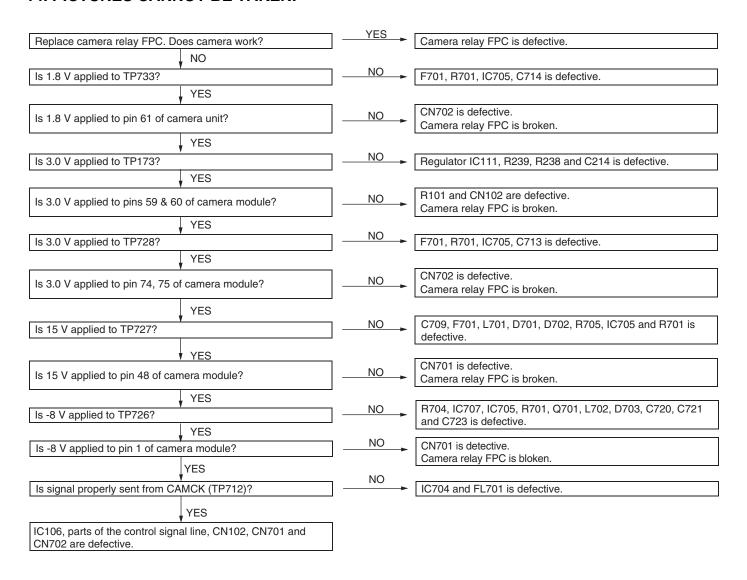
### 12. THE DISPAY DOES NOT APPEAR ON MAIN DISPLAY.



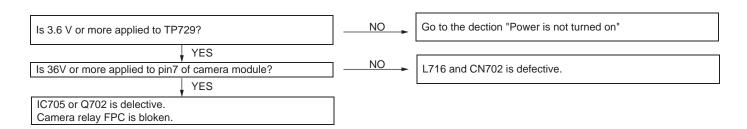
## 13. THE DISPLAY DOES NOT APPEAR ON EXTERNAL DISPLAY (IN 65K COLOR MODE).



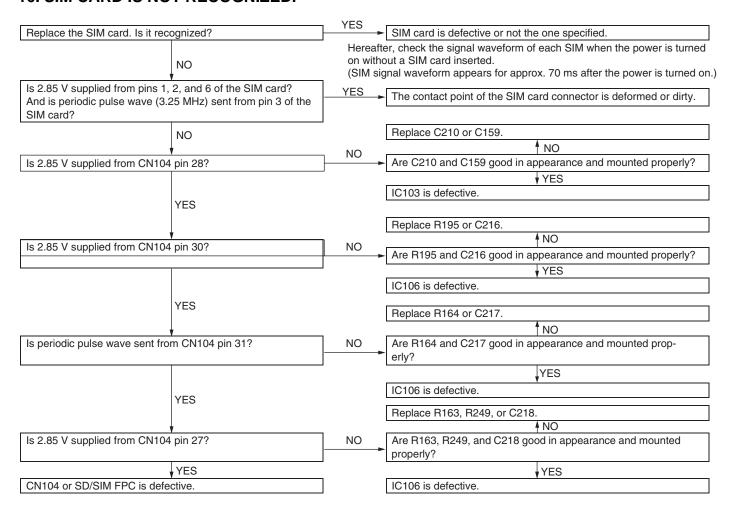
### 14. PICTURES CANNOT BE TAKEN.



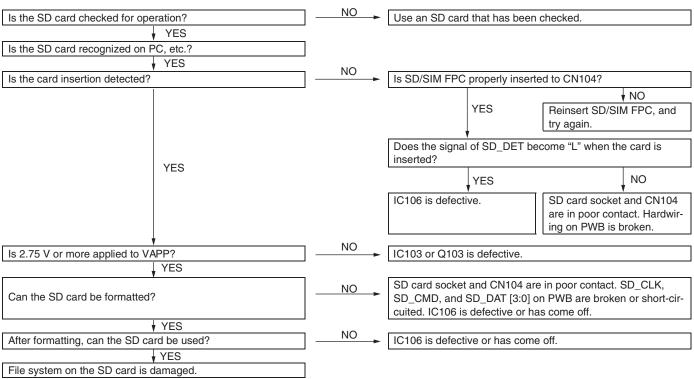
### 15. AF DOES NOT MOVE



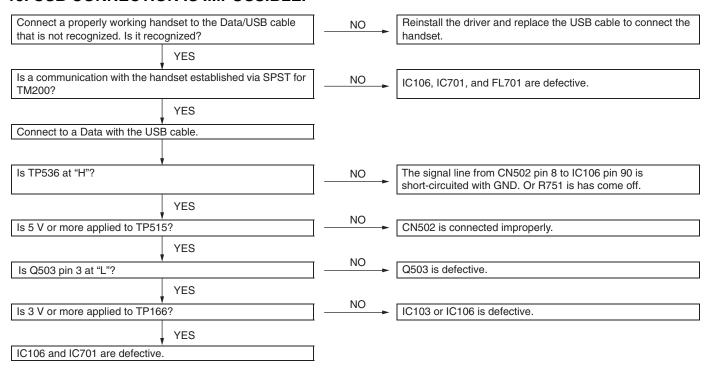
### 16. SIM CARD IS NOT RECOGNIZED.



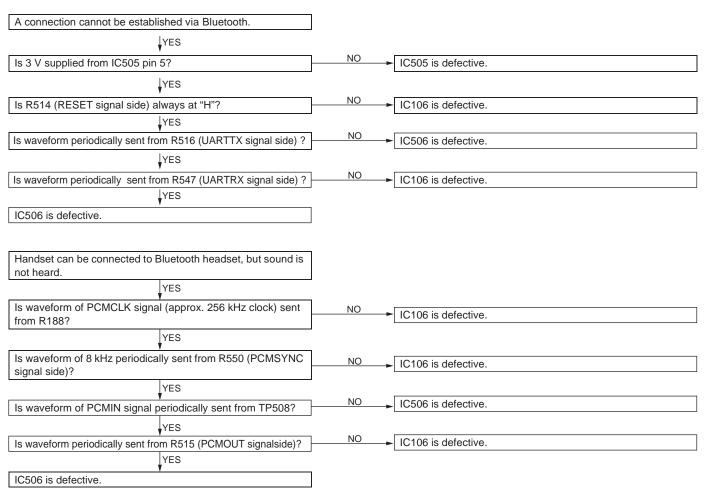
## 17. SD (MEMORY) CARD IS NOT RECOGNIZED.



#### 18. USB CONNECTION IS IMPOSSIBLE.



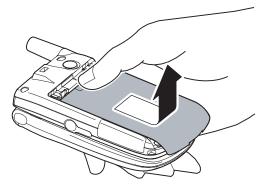
### 19. BLUETOOTH COMMUNICATION IS IMPOSSIBLE.



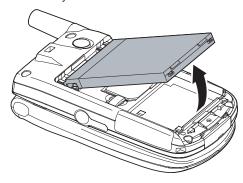
## **CHAPTER 3. DISASSEMBLY AND REASSEMBLY**

#### A. BATTERY REMOVAL

1) Remove the battery cover.

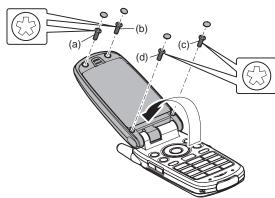


2) Remove the battery.

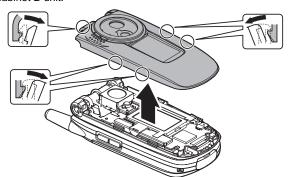


#### **B. SPEAKER REMOVAL**

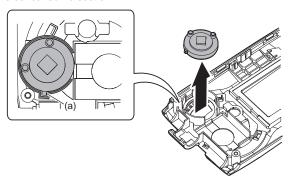
- Open the display section. Remove the screw cover, and remove the special screw.
- \* When removing the special screw, use the exclusive tool.
- When tightening the screws, follow the tightening sequence of (a), (b), (c), and (d).



Close the display section. Disengage the pawls, and remove the cabinet B unit.

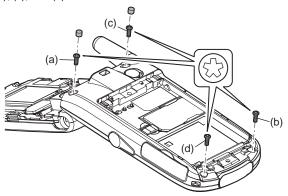


- 3) Remove the speaker from the cabinet B unit.
- \* When installing the speaker, fit the speaker projection (a) with the concaved rib section.

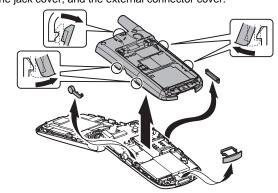


#### C. VIBRATING MOTOR REMOVAL

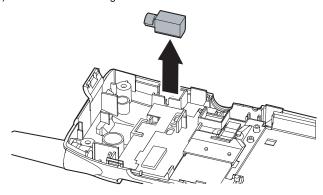
- Open the display section. Remove the screw cover, and remove the special screw.
- \* When removing or installing the special screw, use the exclusive tool.
- When tightening the screws, follow the tightening sequence of (a), (b), (c), and (d).



2) Disengage the pawls, and cabinet D unit. Remove the side key, the jack cover, and the external connector cover.

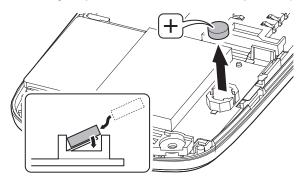


3) Remove the vibrating motor from the cabinet D unit.



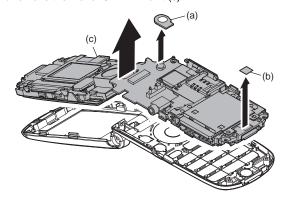
#### D. BACKUP BATTERY REMOVAL

- 1) Remove the backup battery from the main/LCD PWB unit.
- \* When installing the battery, be careful of the installing direction and install it diagonally from the lower side of the battery holder spring.

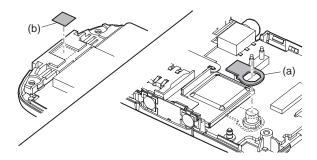


#### E. MAIN/LCD PWB UNIT REMOVAL

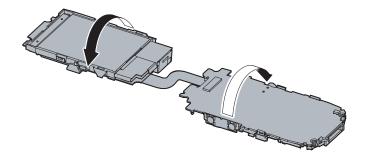
 Remove the ANT dust-proof sheet (a) and the submersion sheet (b), and remove the main/LCD PWB unit (c).



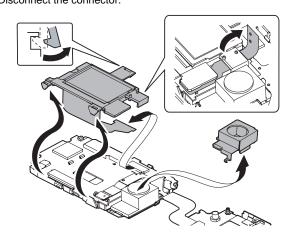
- When attaching the ANT dust-proof sheet (a), fit it with the RF external antenna connector with the main/LCD PWB silk section as the reference
- \* When attaching the submersion sheet (b), attach it inside the bump area.



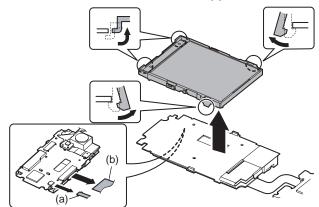
When attaching the PWB unit, rotate the main PWB and the LCD PWB 180 degrees in the arrow direction to wind the flat cable.



 Remove the camera shield case unit from the main/LCD PWB unit, and remove the camera flexible unit.
 Disengage the pawl, and remove the sub LCD unit.
 Disconnect the connector.

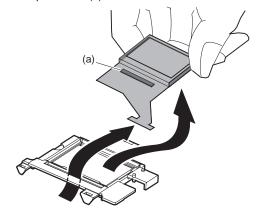


 Remove the connector (a). Disengage the pawl, and remove the main/LCD unit. Disconnect the connector (b).



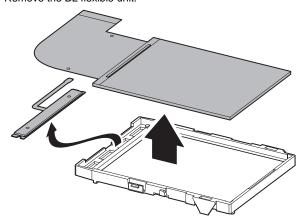
#### F. SUB LCD REMOVAL

- 1) Remove the sub LCD from the sub LCD holder unit.
- Hold the both ends of the sub LCD as shown in the figure, and never press TAB (a).

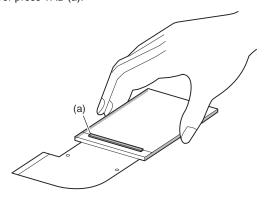


### G. MAIN LCD, BL FLEXIBLE UNIT REMOVAL

 Remove the main LCD from the main LCD holder unit. Remove the BL flexible unit.

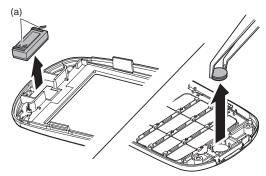


\* Hold the both ends of the main LCD as shown in the figure, and never press TAB (a).

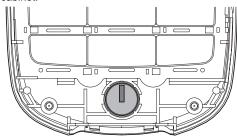


#### H. RECEIVER AND MIC REMOVAL

- 1) Remove the receiver and the mic from the cabinet A/C unit.
- \* When attaching the receiver, be sure to face the terminal (a) tip toward the inside without covering over the rib.
- \* When handling the mic, use a pair of tweezers to hold the peripheral of the mic, and be careful not to touch the front and the rear of the mic.

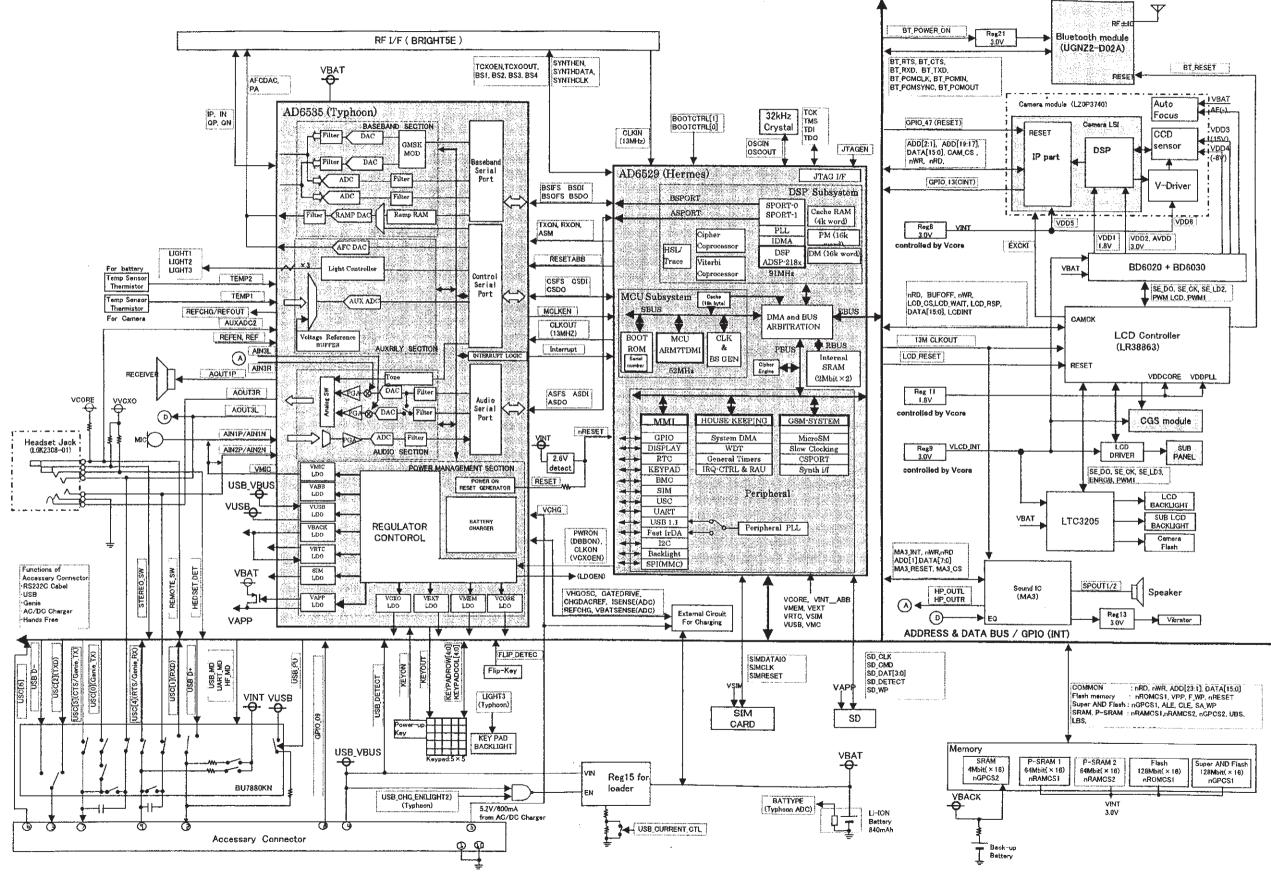


\* When attaching the mic, be sure to set the spring direction vertically to the cabinet.

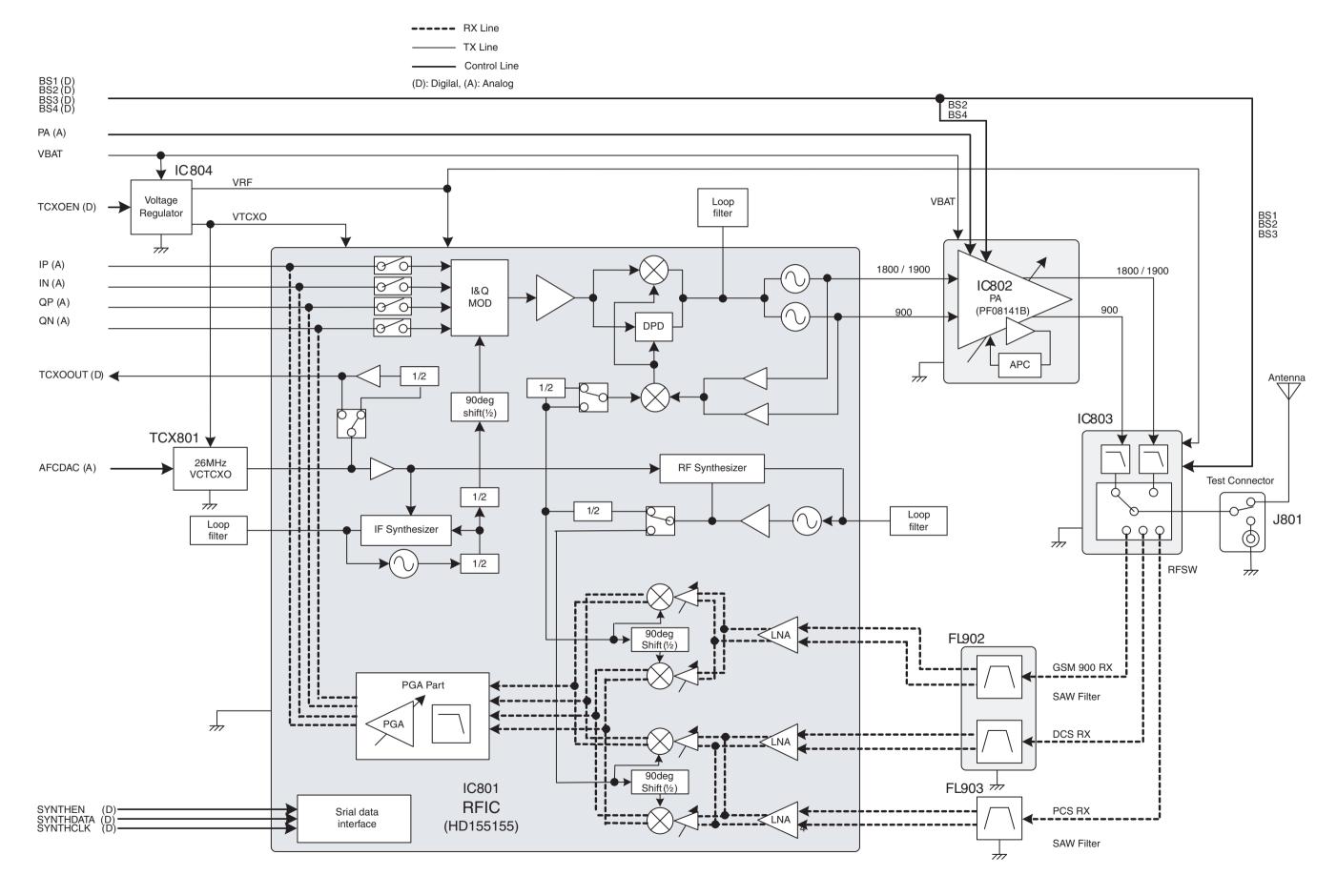


## **CHAPTER 4. DIAGRAMS**

[1] Block diagram
[Main]



[RF]

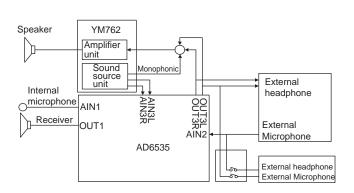


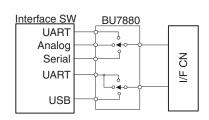
TM200 DIAGRAM
4 - 3

4 - 4

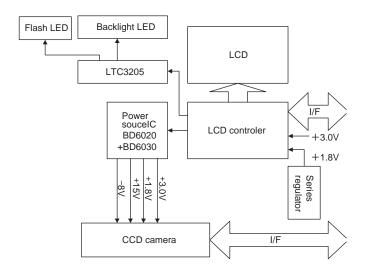
### (1) Sound signal system

## (4) Interface

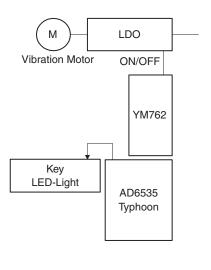




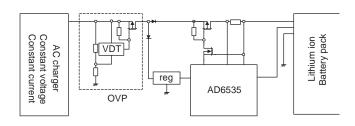
### (2) LCD & camera system



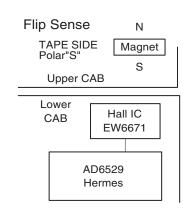
### (5) Vibration Motor & LED Driver



### (3) Battery charge system



## (6) Sense Flip



### CHAPTER 5. SCHEMATIC DIAGRAM AND WIRING SIDE OF P.W.BOARD

## [1] NOTES ON SCHEMATIC DIAGRAM

· Resistor:

To differentiate the units of resistors, the symbols K and M are used. The symbol K means 1000 ohm and the symbol M means 1000 kohm. The resistor without any symbol is an ohm resistor.

- · Capacitor:
- To indicate the unit of capacitor, the symbol is used.
- The symbol P means pico-farad and the unit of the capacitor without such a symbol is microfarad. As to electrolytic capacitor, the expression "capacitance/withstand voltage" is used.

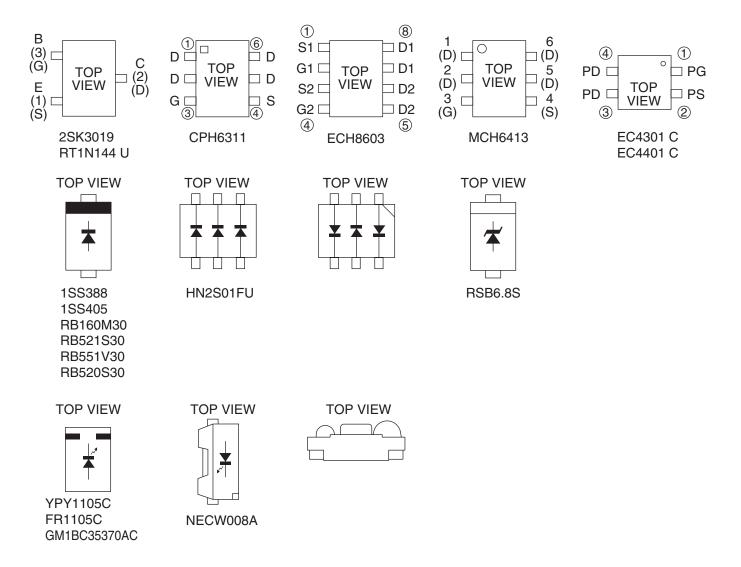
(CH), (RH), (UJ): Temperature compensation

(ML) : Mylar type(S) : Styrol type

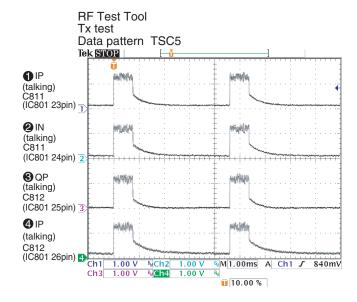
(PP) : Polypropylene type

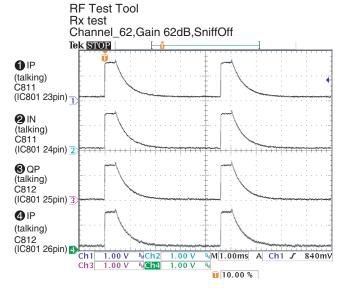
- The indicated voltage in each section is the one measured by Digital Multimeter between such a section and the chassis with no signal given.
- Conditions: SIM card inserted, power on, in stand-by mode (opened)
- Schematic diagram and Wiring Side of P.W. Board for this model are subject to change for improvement without prior notice.
- Parts marked with "^ " are important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

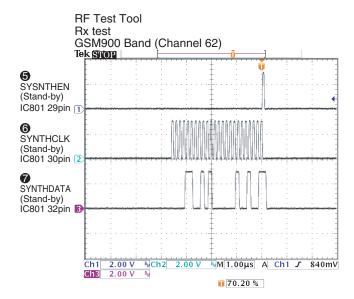
### [2] TYPES OF TRANSISTOR AND LED

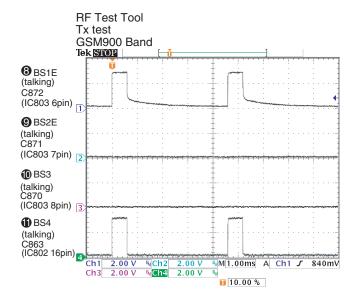


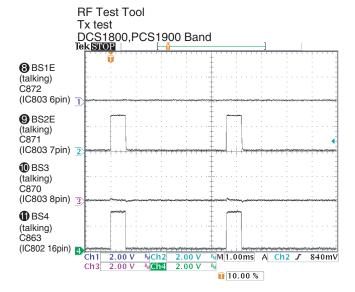
## [3] WAVEFORMS OF CIRCUIT

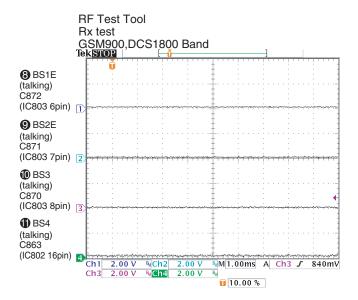


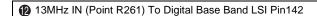


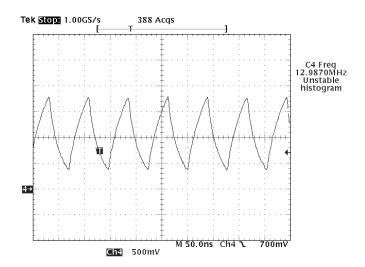




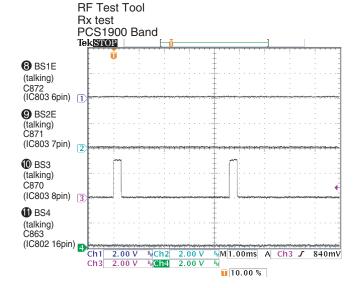


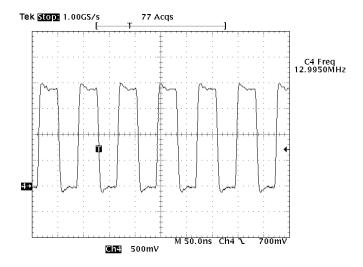




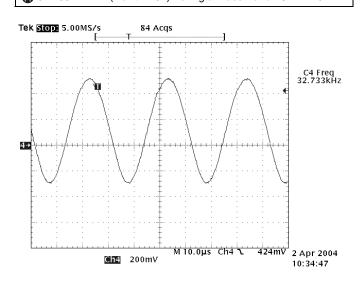


#### (3) 13MHz OUT (Point R166) from Digital Base Band LSI Pin84

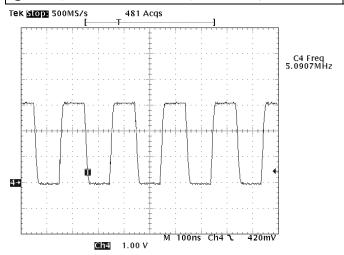




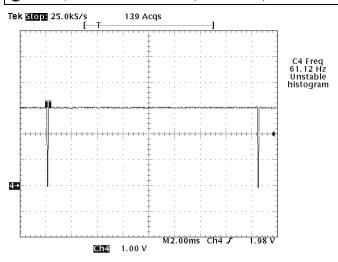
### (A) 32.768KHz IN (Point-R152) To Digtal Base Band LSI Pin49



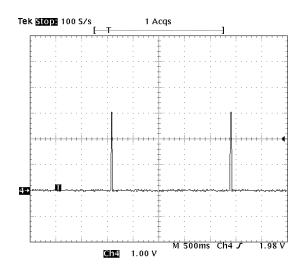


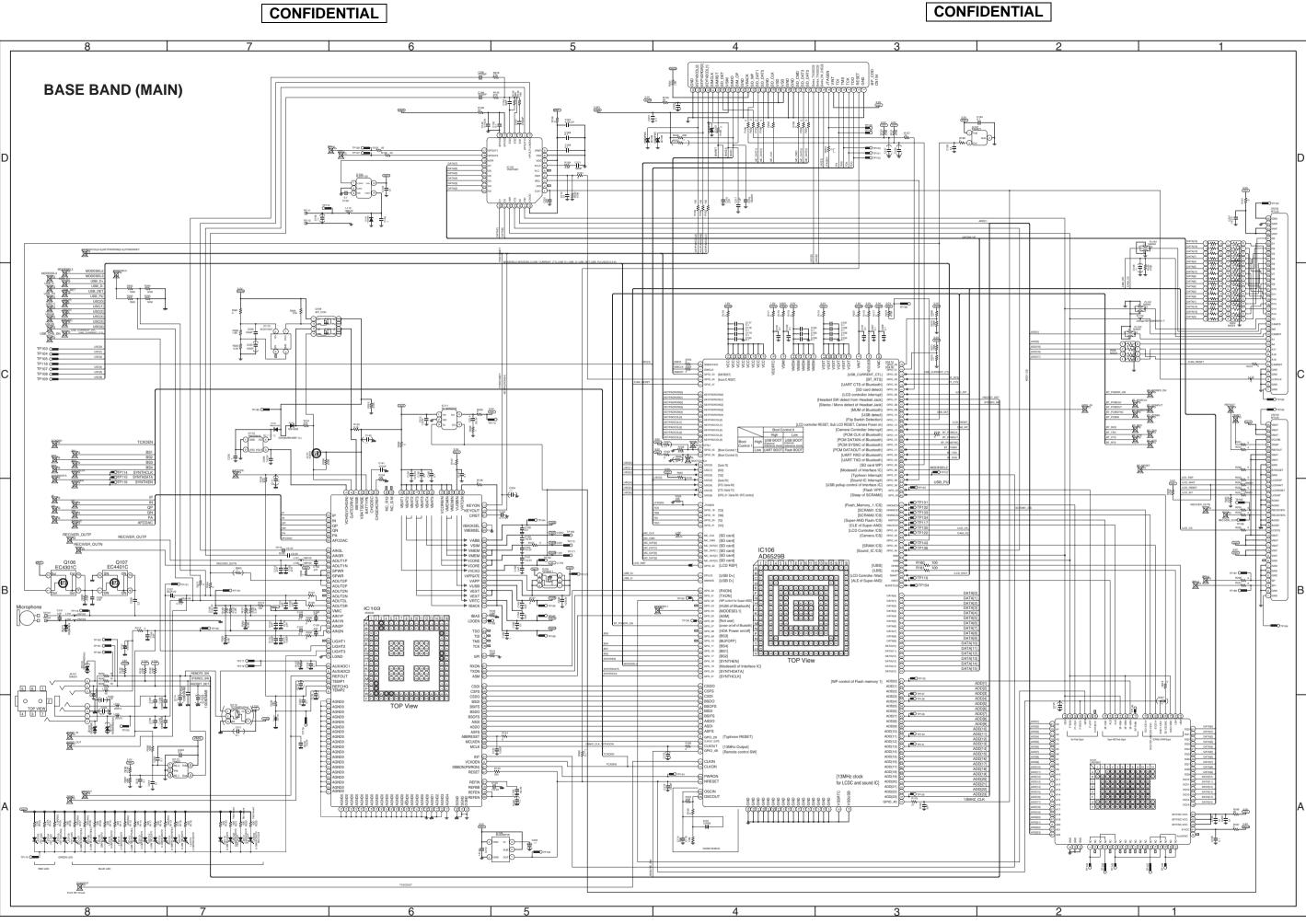


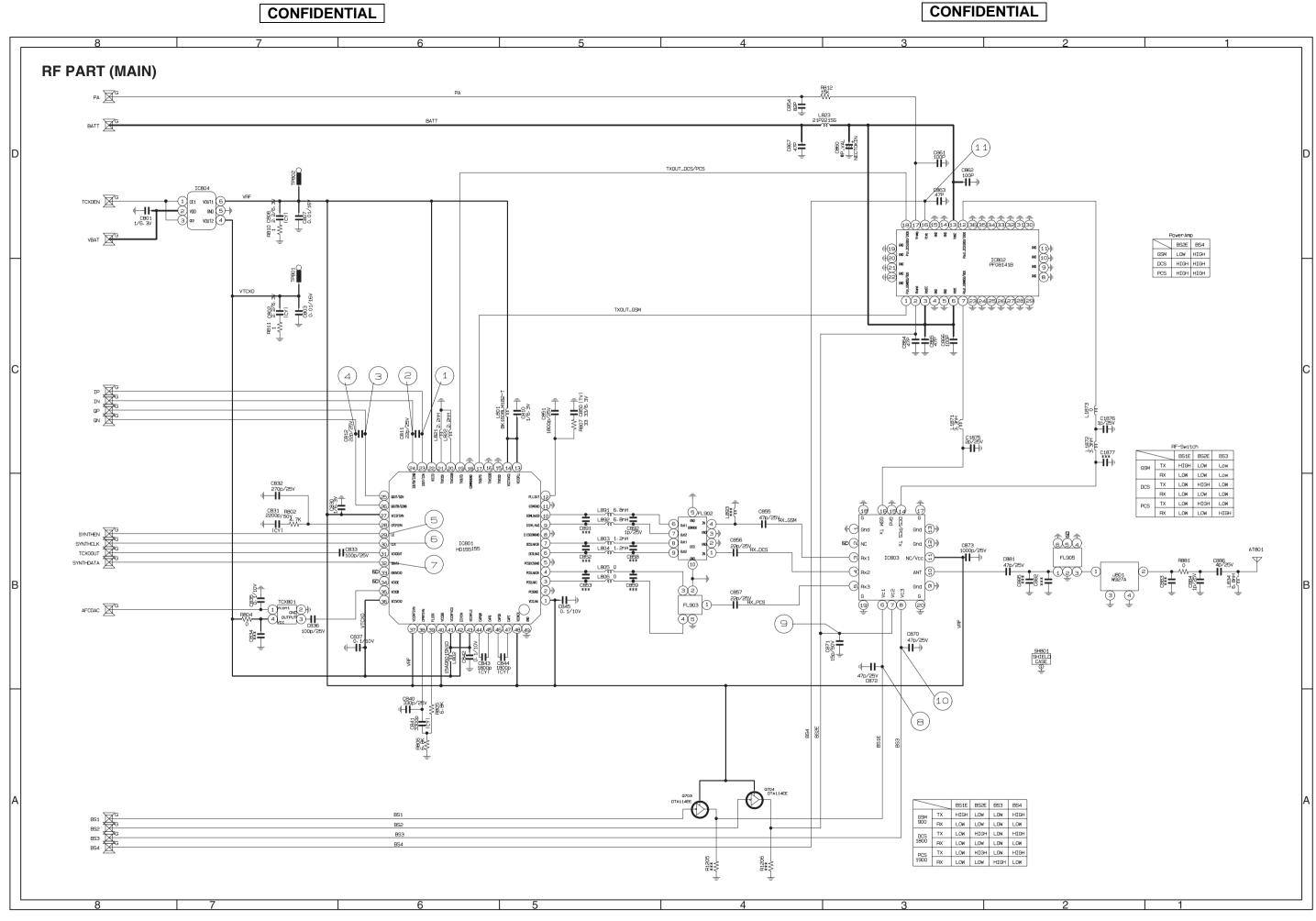
### **(b**VSYNC (Point-C760 on LCDC\_PCB) To LCD Unit pin28



### TCXOEN (Point-IC804 pin 1) From Analog Base Band LSI Pin 2



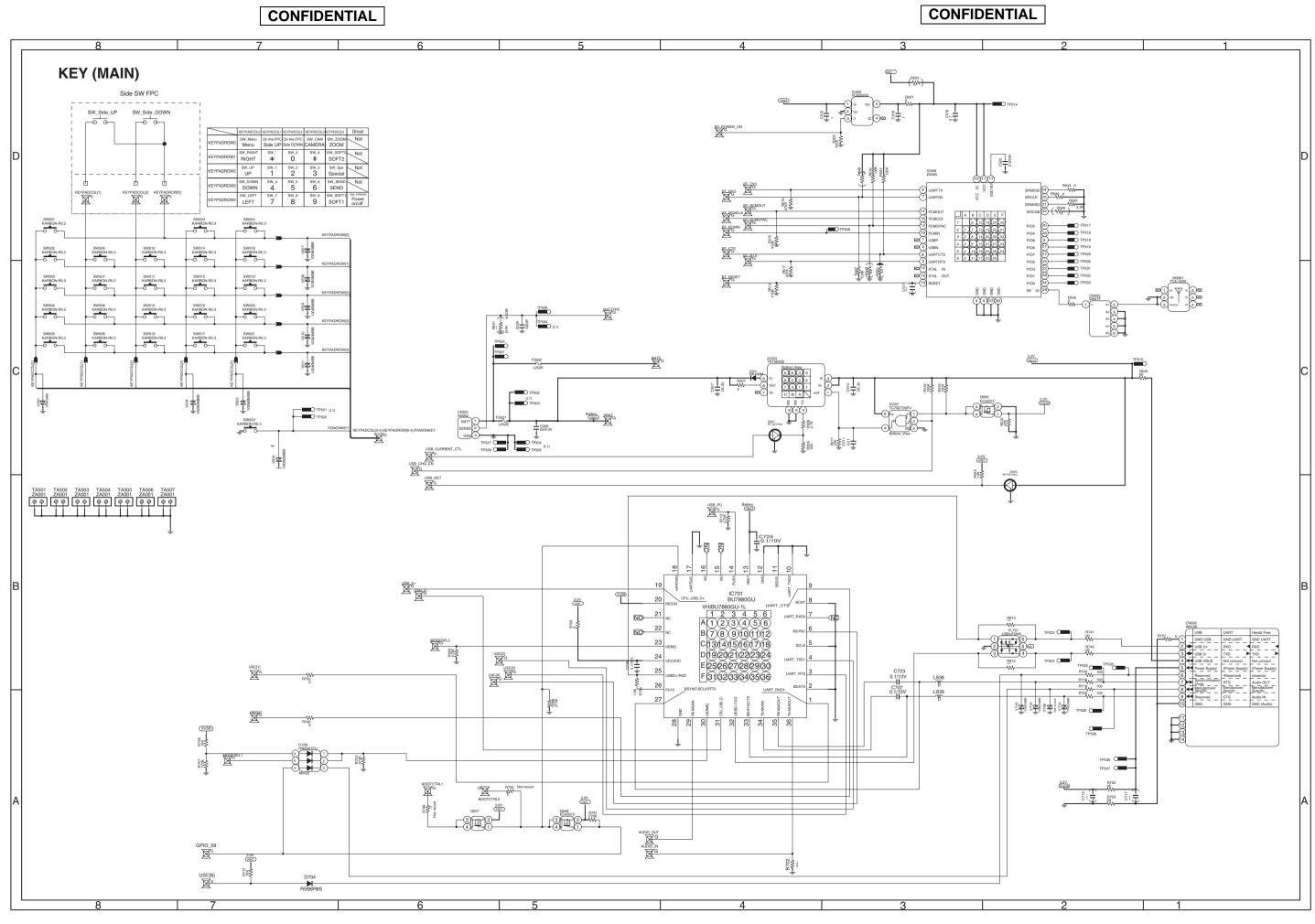




TM200 CIRCUIT DIAGRAM AND PWB LAYOUT

5 - 7

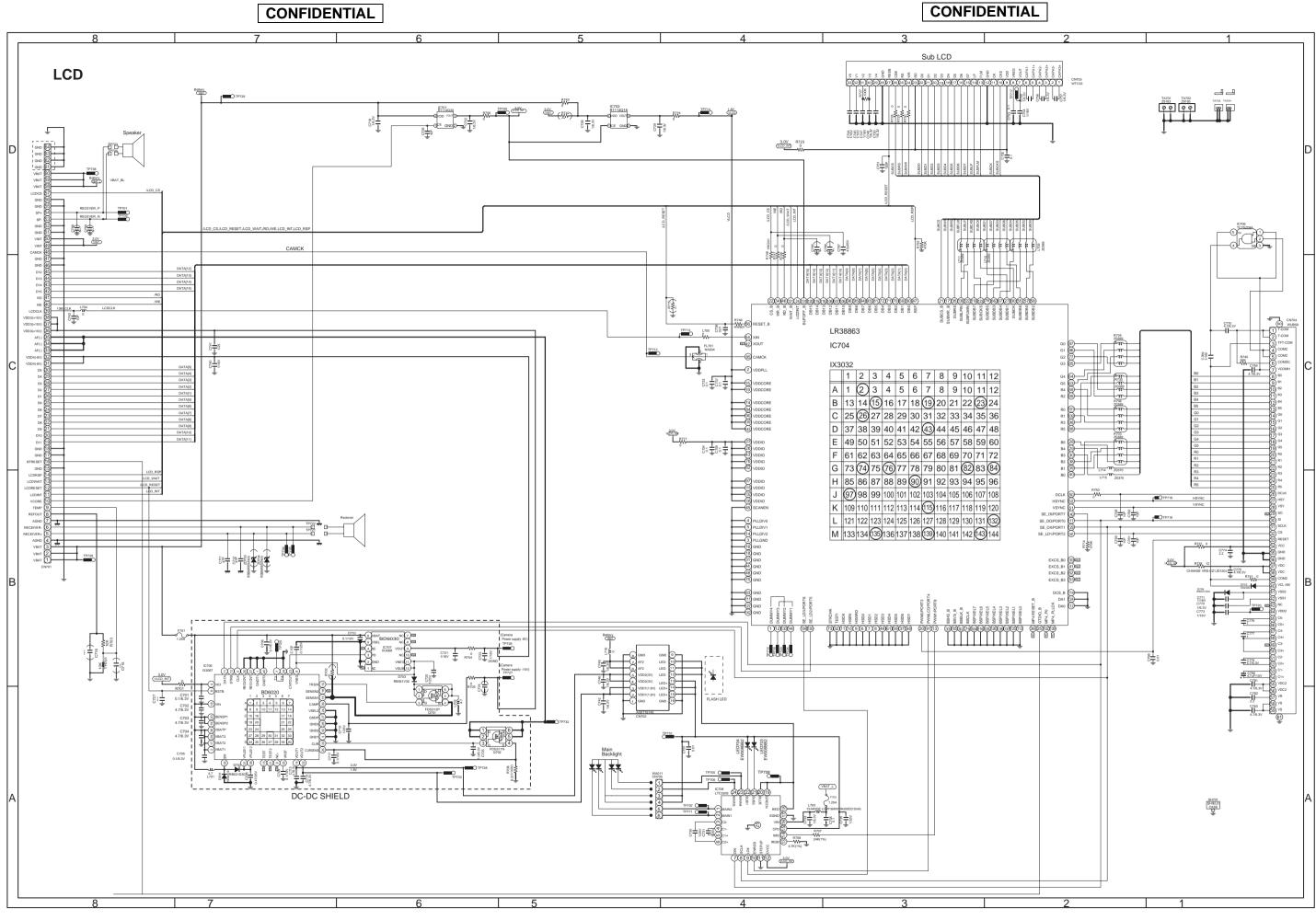
5 - 8

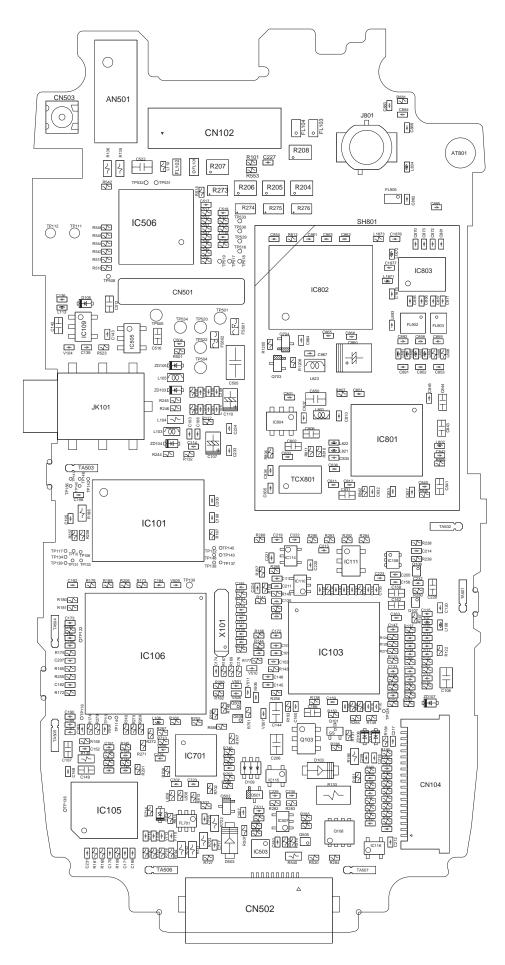


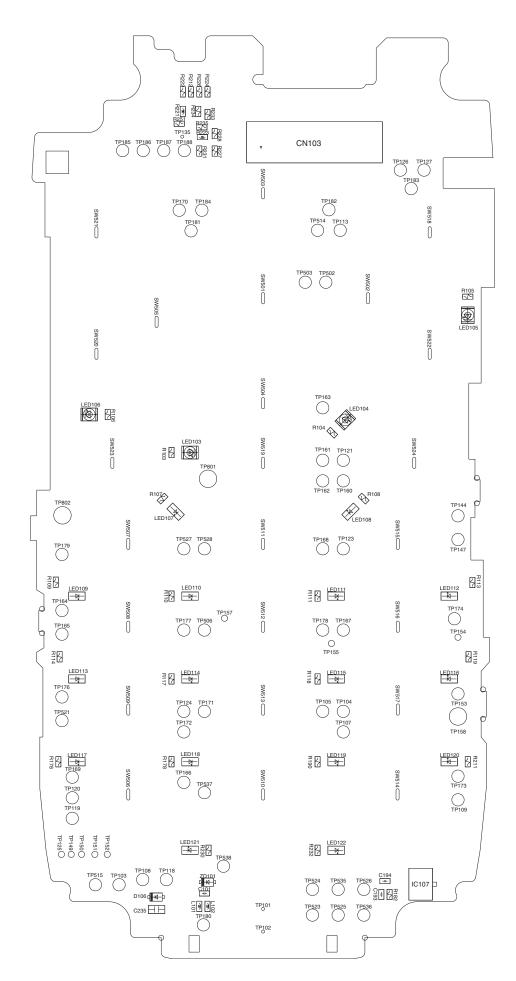
TM200 CIRCUIT DIAGRAM AND PWB LAYOUT

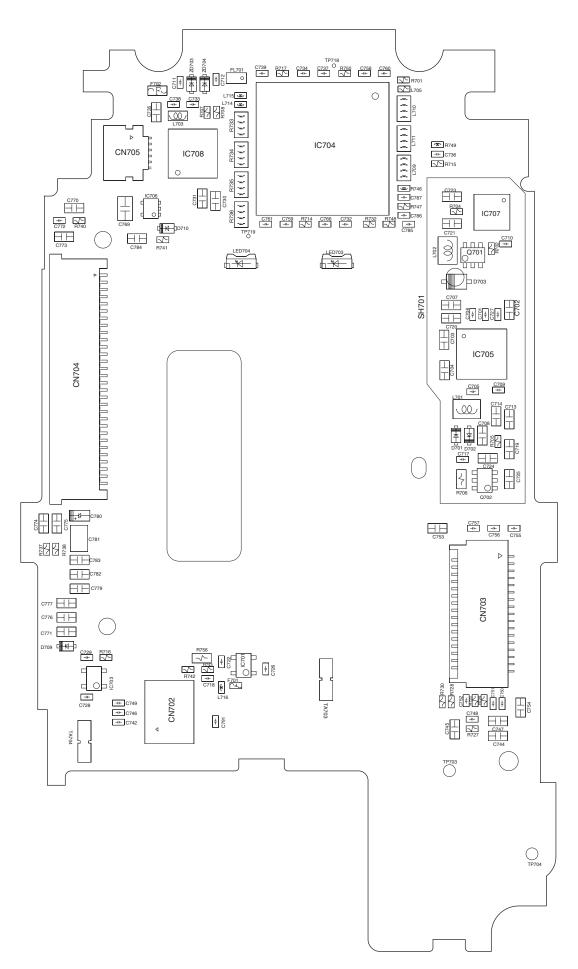
5 -9

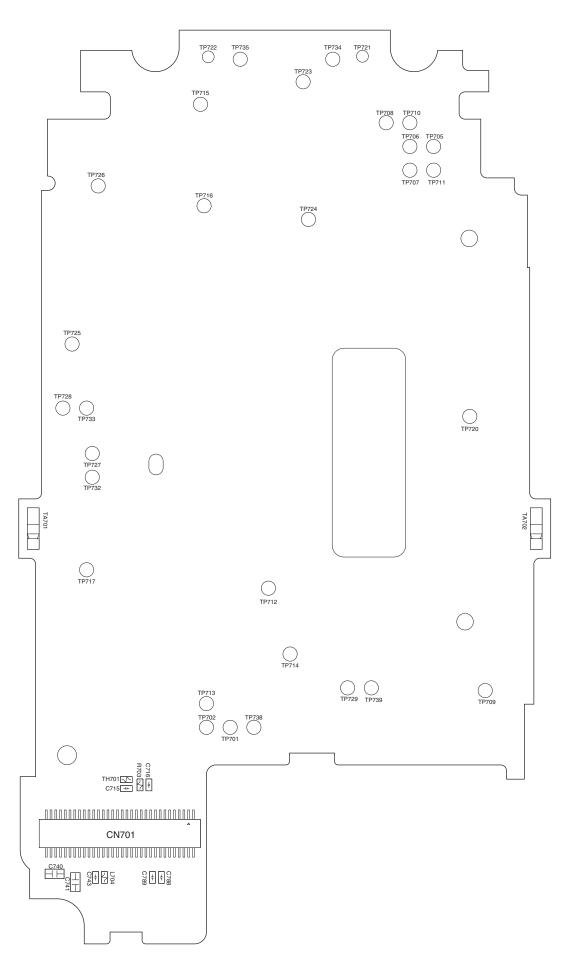
5 - 10



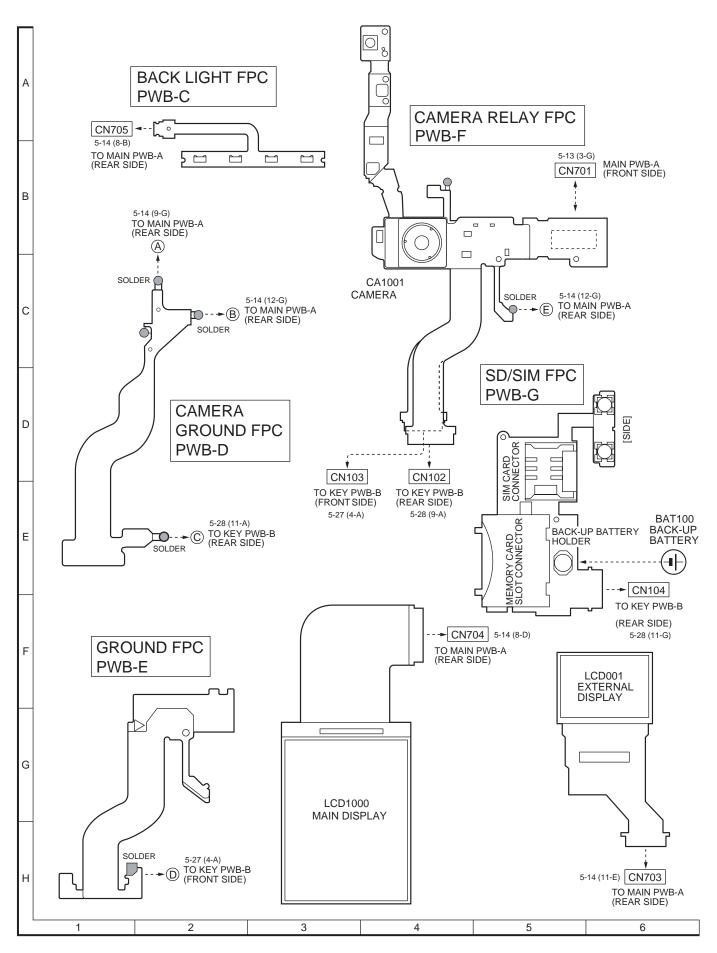








■ LCD PWB\_REAR



Conditions: SIM card inserted, power on (battery=3.7V), in stand-by mode (opened) Measuring instrument: Digital multimeter : Unmeasurable IC105 IC503 IC111 IC505 IC701 IC801 IC802 PIN NO. VOLTAGE 0V 2.89V 1.41V 3.69V 1.8V 0V 2 0V 2 2 0.03V 2 0V 2 2 0V 0V 2 0V 3 0.03V 3 2.98V 3 3 0V 3 3.0V 3 0V 3 3.70V 4 4 2.98V 4 0V 4 Not used 4 0V 4 4 3.69V 0V 5 5 5 ٥V 5 5 0V 5 0V 6 0V 6 IC703 6 3.70V В 0V 0V 6 7 2.98V IC114 7 Not used PIN NO. VOLTAGE 7 0V 7 0V 8 3.68V PIN NO. VOLTAGE IC506 8 8 0V 0V 8 3.0V 0V PIN NO. VOLTAGE 9 0V 9 2.25V 2 0V 9 0V 9 0V 10 10 Not used 1.13V 2 0V 3 1.8V 10 0V 11 0.27V 3 2 Not used 4 3.69V 11 0V 11 0V 3 ٥V 4 0V 12 12 12 2.44V 13 0V 5 4 0V 13 2.89V 13 3.70V IC706 5 14 0V 14 0V 2.89V 14 0V PIN NO. VOLTAGE 6 0.01V 15 15 3.69V IC115 0V 15 0V 3.58V С PIN NO. VOLTAGE 16 0V 7 0V 16 0V 16 0V 2 1.82V 8 0.01V 17 0V 0V 17 0V 17 0V 3 0V 18 0V 2 0V 9 0V 18 0V 18 0V 4 1.78V 3 Not used 10 0V 19 0V 19 0V 19 ٥V 5 3.58V 20 0.49V 4 0V 11 0V 20 0V 20 0V 12 0.01V 21 0.7V 21 0V 21 0V 22 0.91V IC116 13 0V 22 2.89V 22 0V 14 23 0.95V PIN NO. VOLTAGE Not used 23 0.21V 23 0V 24 15 Not used 24 0.21V 1.01V 0V 24 0V D 25 25 16 0V 1.08V 2 0.14V 0.21V 25 0V 26 0.73V 3 0V 17 0V 26 0.21V 26 0V 27 1.36V 4 0.14V 18 0V 27 2.89V 27 0V 19 0V 28 2.39V 28 0.27V 28 0V 20 1.87V 29 2.97V 29 0V 29 0V 21 30 1.79V 0V 30 0V 30 ٥V 31 2.07V 22 1.8V 31 1.14V 31 0V 32 23 0V 2.98V 32 0V 32 0V 24 0V 33 0V 33 0V Ε 25 0V 34 0V 34 0V IC107 26 1.8V 35 1.82V 35 0V PIN NO. VOLTAGE 27 0V 36 2.89V 36 0V 1 2.98V 28 2.78V 37 2.89V 2 0V IC804 29 0V 38 0.26V PIN NO. VOLTAGE 3 2.98V 30 0V 39 0V 31 2.96V 0V 40 2.89V 32 2 3.80V 1.7V 41 2.89V IC108 3 2.96V 33 7.75V 42 2.89V PIN NO. VOLTAGE 34 1.75V 43 2.89V 4 2.89V 5 0V 44 2.87V 2 6 2.89V IC507 45 2.87V 3 PIN NO. VOLTAGE 46 2.87V 4 0V 47 1 2.87V 2 48 2.89V 0V 3 49 0V 0V IC109 4 0V PIN NO. VOLTAGE 5 0V G 0V 2 0V 3 0V 4 0V 5 3.69V Η • NOTES ON SCHEMATIC DIAGRAM can be found on page 5-1. 2 3 4 5 6

# **CHAPTER 6. OTHERS**

# [1] FUNCTION TABLE OF IC

## ■ IC101 (LRS1B27): 5-LEVEL STACK MEMORY

Pin No.	Terminal name	Input/Output	Description of terminal
1	NC	_	Not used
2*	A20	Input	Address input (NOR Flash, Smartcombo RAM)
3	A11	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
4	A15	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
5	A14	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
6	A13	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
7	A12	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
8	GND	_	Ground
9	NC	_	Not used (VCC IO/NC)
10*	NC	_	Not used
11*	NC	_	Not used
12*	NC	_	Not used
13*	SF-RY/BY	Output	Ready busy output (Smartcombo Flash)
14	A16	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
15	A8	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
16	A10	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
17	A9	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
18	DQ15	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
19	S/SC-/WE	Input	Write enable input (SRAM, Smartcombo RAM)
20	DQ14	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
21	DQ7	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
22	NC	_	Not used
23*	NC	_	Not used
24*	SF-/RE	Input	Read enable input (Smartcombo Flash)
25	F-/WE	Input	Write enable input (NOR Flash)
26*	F-RY/-BY	Output	Ready busy output (NOR Flash) When deleting/writing: VOL When interrupting block delete/ write: High-Z (High impedance)
27	A21	Input	Address input (NOR Flash, Smartcombo RAM 2)

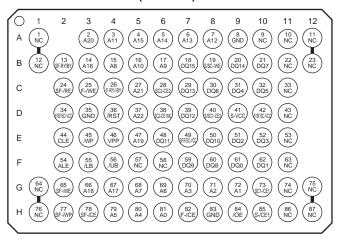
Pin	Tarminal		
No.	Terminal name	Input/Output	Description of terminal
28	SC2-CE2	Input	Sleep state input (Smartcombo RAM 2)
29	DQ13	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
30	DQ6	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
31	DQ4	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
32	DQ5	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
33*	NC	_	Not used
34	SF/F/SC-VCC		Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)
35	GND	_	Ground
36	/RST	Input	Reset input (NOR Flash) (F-/RST) When deleting block/writing: VIH When reading : VIH Reset : VIL
37	A22	Input	Address input (NOR Flash)
38	SC2-/CE1/NC (F2-/CE)	Input	Chip enable input (Smartcombo RAM 2)
39	DQ12	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM)
			Command, Address, and Data input/output (Smartcombo Flash)
40	S/SC1-CE2	Input	Command, Address, and Data
40	S/SC1-CE2 S-VCC	Input —	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep
		Input — —	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)
41 42 43	S-VCC	Input — — — —	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo
41 42	S-VCC SF/F/SC-VCC	Input — — — Input	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)
41 42 43	S-VCC SF/F/SC-VCC	<u> </u>	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)  Not used  Command latch enable input
41 42 43 44*	S-VCC SF/F/SC-VCC NC CLE	——————————————————————————————————————	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)  Not used  Command latch enable input (Smartcombo Flash)
41 42 43 44* 45	S-VCC SF/F/SC-VCC NC CLE /WP (F-/WP)	——————————————————————————————————————	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)  Not used  Command latch enable input (Smartcombo Flash)  Write protect input (NOR Flash)  Power voltage detect terminal (NOR Flash)  When deleting/writing: VPP = VPPH When deleting/writing is prohibited:
41 42 43 44* 45 46	S-VCC SF/F/SC-VCC NC CLE /WP (F-/WP) VPP (F-VPP)	Input Input	Command, Address, and Data input/output (Smartcombo Flash)  Chip enable input (SRAM), sleep state input (Smartcombo RAM 1)  Power (SRAM)  Power (NOR Flash ,Smartcombo Flash, Smartcombo RAM)  Not used  Command latch enable input (Smartcombo Flash)  Write protect input (NOR Flash)  Power voltage detect terminal (NOR Flash)  When deleting/writing: VPP = VPPH When deleting/writing is prohibited: VPP < VPPLK  Address input

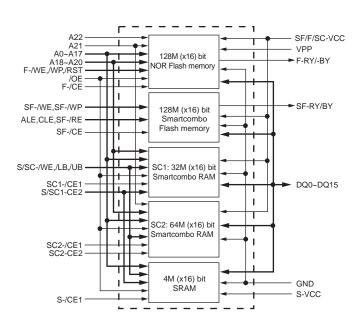
			•
Pin No.	Terminal name	Input/Output	Description of terminal
50	DQ10	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM)
			Command, Address, and Data input/output (Smartcombo Flash)
51	DQ2	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM)
			Command, Address, and Data input/output (Smartcombo Flash)
52	DQ3	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
53*	NC	_	Not used
54	ALE	Input	Address latch enable input (Smartcombo Flash)
55	/LB	Input	Byte enable input (DQ0-DQ7) (Smartcombo RAM, SRAM)
56*	/UB	Input	Byte enable input (DQ8-DQ15) (Smartcombo RAM, SRAM)
57	NC	_	Not used
58*	NC	_	Not used
59	DQ9	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
60	DQ8	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
61	DQ0	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
62	DQ1	Input/Output	Data input/output (NOR Flash, Smartcombo RAM, SRAM) Command, Address, and Data input/output (Smartcombo Flash)
63*	NC	_	Not used
64*	NC	_	Not used
65	SF-/WE	Input	Write enable input (Smartcombo Flash)
66	A18	Input	Address input (NOR Flash, Smartcombo RAM)
67	A17	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
68	A7	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
69	A6	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
70	A3	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
71	A2	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
72	A1	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
73	SC1-/CE1	Input	Chip enable input (Smartcombo RAM 1)
74*	NC	_	Not used
75*	NC		Not used

Pin No.	Terminal name	Input/Output	Description of terminal
77	SF-/WP	Input	Write protect input (Smartcombo Flash)
78	SF-/CE	Input	Chip enable input (Smartcombo Flash)
79	A5	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
80	A4	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
81	A0	Input	Address input (NOR Flash, Smartcombo RAM, SRAM)
82	F-/CE (F1-/CE)	Input	Chip enable input (NOR Flash)
83	GND	_	Ground
84	/OE	Input	Output enable input (NOR Flash, Smartcombo RAM, SRAM)
85	S-/CE1	Input	Chip enable input (SRAM)
86*	NC	_	Not used
87*	NC	_	Not used

In this unit, the terminal with asterisk mark (\*) is (open) terminal which is not connected to the outside.

#### (TOPVIEW)





### ■ IC103 (AD6535): ANALOG BASEBAND

No.	Terminal name	Input/ Output	Description of terminal
1 *	TDI	Input	Not used
2	VCXOEN	Input	VCXO supply
3	VBAT3	Input	External interface regulator input
4 *	VEXT	Output	Not used
5	VCHG	Input	Charge supply
6	GATEDRIVE	Output	Charge DAC (FET) output control
7	ISENSE	Input	Charge current sense input
8	TEMP2	Input	Temp sensor input for battery
9*	AUXADC2	Input	Not used
10	REFBB	Output	Baseband transmit & receive voltage reference
11	AGND2		Analog baseband ground
12	IP .	Input/Output	I-channel positive input/output
13	IN	Input/Output	I-channel negative input/output
14	QN	Input/Output	Q-channel positive input/output
			' ' '
15	QP	Input/Output	Q-channel negative input/output
16 *	RSVD_A16	_	Not used
17*	TMS	Input	Not used
18 *	TCK	Input	Not used
19	VBAT3	Input	External interface regulator input
20*	VEXT	Output	Not used
21	CHGOSC	Input	Charge oscillator capacitor
22	BATTYPE	Input	Battery type identification input
23	CHGDACREF	Output	Charge DAC reference
24	VBATSENSE	Input	Battery voltage sense input
25	TEMP1	Inpsut	Temp sensor input for camera
26	AUXADC1	Input	Auxiliary ADC input for temp. sensor adjustment
27	REFOUT	Output	Voltage reference output
28	PA	Output	Power amplifier control output
29	AGND0	_	Analog ground
30	AFCDAC	Output	Automatic frequency control DAC output
31	REF	Output	Voltage reference
32	AGND1		Analog ground
33 *	TDO	Output	Not used
34 *	GPI	Input	Not used
35	VBAT1	Input	Voltage controlled crystal oscillator regulator input
36 *	RSVD_C16	_	Not used
37	INT	Output	Digital BB interrupt
38	ASDO	Output	Audio serial port data output
39	REFCHG	Output	Voltage reference output
40	VVCXO	Output	Voltage controlled crystal oscillator supply 2.71 - 2.79 V (VT)
41	ASDI	Input	Audio serial port data input
42	BSDO	Output	Baseband serial port data output
43	VUSB	Output	USB interface supply 3.0 - 3.6 V
43	VAPPGATE	Output	Application regulator pass device gate control
44		l .	-
44	BSIFS	Input	Baseband serial port input framing signal
44 45	BSIFS ASES	Input	
44 45 46	ASFS	Output	Audio serial port framing signal
44 45 46 47	ASFS VUSBIN	Output Input	Audio serial port framing signal USB interface regulator input
44 45 46	ASFS	Output	

D:	T	1	
Pin No.	Terminal name	Input/ Output	Description of terminal
50	BSDI	Input	Baseband serial port data input
51	VBAT2	Input	Analog baseband regulator input
52*	NC_G16	_	Not used
53	CSDO	Output	Control serial port data output
54	CSDI	Input	Control serial port data input
55	VBAT2	Input	Analog baseband regulator input
56	VABB	Output	Analog baseband supply
57	ASM	Input	Advanced state machine
58	MCLKEN	Output	Master clock enable
59	AOUT1P	Output	Receiver audio positive output
60	AOUT3L	Output	Headset receiver audio L-channel output
61	RXON	Input	Baseband receive section control
62	TXON	Input	Baseband transmit section control
63	AOUT1N	Output	Receiver audio negative output
64	AOUT3R	Output	Headset receiver audio R-channel output
65	MCLK	Input	Master clock
66	CSFS	Input	Control serial port framing signal
67	AGND3	_	Analog audio ground
68	LIGHT1	Output	Charge LED control
69	ABBRESET	Input	Reset input
70	DGND	_	Digital ground
71	LIGHT2	Output	USB charge enable
72	LIGHT3	Output	Key-pad LED control
73	VCORE	Output	Digital core supply 1.72 - 1.9 V
74	VCOREIN	Input	Digital core regulator input
75	LGND	_	Light driver ground
76	VMIC	Output	Microphone supply 2.4 - 2.6 V
77	VCORE	Output	Digital core supply 1.72 - 1.9 V
78	VMEMIN	Input	Memory interface regulator input
79	AIN2P	Input	Headset mic audio positive input
80	AIN1P	Input	Mic audio positive input
81	CRST	Output	Power-on reset capacitor
82	VMEMIN	Input	Memory interface regulator input
83	VMEMSEL	Input	Memory supply voltage selection
84	VBAT5	Input	Back-up battery regulator input
85	VBAT4	Input	SIM interface regulator input
86	VRTCIN	Input	Real-time clock regulator input
87	DBBON	Input	Digital BB supply regulator on signal
88	SGND	_	AOUT2P/N ground
89*	AOUT2N	Output	Not used
90*	SPWR	Input	Not used
91*	AOUT2P	Output	Not used
92*	NC_R12		Not used
93	AIN3L	Input	Sound IC audio L-channel input
94	AIN3R	Input	Sound IC audio R-channel input
95	AIN2N	Input	Headset mic audio negative input
96	AIN1N	Input	Mic audio negative input
97	RESET	Output	Reset output
98	VMEM	Output	Memory interface supply 2.75 - 3.05 V
99	VMEM	Output	Memory interface supply 2.75 - 3.05 V
100	VBACK	Output	Backup battery supply 2.72 - 3.05 V
101	VBACKSEL	Input	Backup battery supply voltage selection

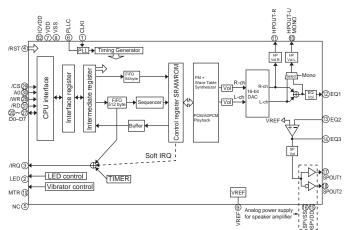
Pin No.         Terminal name         Output         Description of terminal           102         VSIM         Output         SIM interface supply 2.75 - 2.95 V           103         VRTC         Output         Real-time clock supply 1.6 - 2.0 V           108*         AOUT2N         Output         Not used           108*         SPWR         Input         Not used           107*         AOUT2P         Output         Not used           108         LDOEN         Output         Regulator enable output           109         KEYOUT         Output         Power-on key input           110         KEYON         Input         Power-on key input           111         IBIAS         Output         Regulator bias current reference           112         AGND4         — Power management analog ground           113         AGND0         — Thermal ground for power supply           114         AGND0         — Thermal ground for power supply           115         AGND0         — Thermal ground for power supply           116         AGND0         — Thermal ground for power supply           117         AGND0         — Thermal ground for power supply           118         AGND0         — Thermal ground for power		I	T	
103         VRTC         Output         Real-time clock supply 1.6 - 2.0 V           104         SGND         — AOUT2P/N ground           108**         AOUT2N         Output         Not used           107**         AOUT2P         Output         Not used           107**         AOUT2P         Output         Regulator enable output           108         LDOEN         Output         Power-on key output           110         KEYON         Input         Power-on key input           111         IBIAS         Output         Regulator bias current reference           112         AGND4         — Power management analog ground           113         AGND0         — Thermal ground for power supply           114         AGND0         — Thermal ground for power supply           115         AGND0         — Thermal ground for power supply           116         AGND0         — Thermal ground for power supply           117         AGND0         — Thermal ground for power supply           118         AGND0         — Thermal ground for power supply           129         AGND0         — Thermal ground for power supply           121         AGND0         — Thermal ground for power supply           122				Description of terminal
SGND	102	VSIM	Output	SIM interface supply 2.75 - 2.95 V
106* AOUT2N	103	VRTC	Output	Real-time clock supply 1.6 - 2.0 V
Input	104	SGND	_	AOUT2P/N ground
Not used   LDOEN	105*	AOUT2N	Output	Not used
LODEN	106*	SPWR	Input	Not used
NEYOUT   Output   Power-on key output	107*	AOUT2P	Output	Not used
Input	108	LDOEN	Output	Regulator enable output
111   IBIAS	109	KEYOUT	Output	Power-on key output
112 AGND4	110	KEYON	Input	Power-on key input
Thermal ground for power supply Thermal ground for power suppl	111	IBIAS	Output	Regulator bias current reference
Thermal ground for power supply Thermal ground for power suppl	112	AGND4	_	Power management analog ground
Thermal ground for power supply	113	AGND0	_	Thermal ground for power supply
Thermal ground for power supply	114	AGND0	_	Thermal ground for power supply
Thermal ground for power supply	115	AGND0	_	Thermal ground for power supply
Thermal ground for power supply 19 AGND0 — Thermal ground for power supply 120 AGND0 — Thermal ground for power supply 121 AGND0 — Thermal ground for power supply 122 AGND0 — Thermal ground for power supply 123 AGND0 — Thermal ground for power supply 124 AGND0 — Thermal ground for power supply 125 AGND0 — Thermal ground for power supply 126 AGND0 — Thermal ground for power supply 127 AGND0 — Thermal ground for power supply 128 AGND0 — Thermal ground for power supply 129 AGND0 — Thermal ground for power supply 130 AGND0 — Thermal ground for power supply 131 AGND0 — Thermal ground for power supply 132 AGND0 — Thermal ground for power supply 133 AGND0 — Thermal ground for power supply 134 AGND0 — Thermal ground for power supply 135 AGND0 — Thermal ground for power supply 136 AGND0 — Thermal ground for power supply 137 AGND0 — Thermal ground for power supply 138 AGND0 — Thermal ground for power supply 139 AGND0 — Thermal ground for power supply 140 AGND0 — Thermal ground for power supply 141 AGND0 — Thermal ground for power supply 142 AGND0 — Thermal ground for power supply 143 AGND0 — Thermal ground for power supply 144 AGND0 — Thermal ground for power supply 145 AGND0 — Thermal ground for power supply 146 AGND0 — Thermal ground for power supply 147 AGND0 — Thermal ground for power supply 148 AGND0 — Thermal ground for power supply 149 AGND0 — Thermal ground for power supply 140 AGND0 — Thermal ground for power supply 141 AGND0 — Thermal ground for power supply 142 AGND0 — Thermal ground for power supply 143 AGND0 — Thermal ground for power supply 144 AGND0 — Thermal ground for power supply 145 AGND0 — Thermal ground for power supply 146 AGND0 — Thermal ground for power supply 147 AGND0 — Thermal ground for power supply 148 AGND0 — Thermal ground for power supply	116	AGND0	_	Thermal ground for power supply
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147 AGND0 — Thermal ground for power supply	145	AGND0	_	Thermal ground for power supply
	146	AGND0	_	Thermal ground for power supply
148 AGND0 — Thermal ground for power supply	147	AGND0	_	Thermal ground for power supply
3	148	AGND0	_	Thermal ground for power supply

In this unit, the terminal with asterisk mark (\*) is (open) terminal which is not connected to the outside.

### ■ IC105 VHIYMU762C+-1L (YMU762C): SOUND

Pin. No.         Terminal name         Input/Output         Description of terminal           1         CLKI         Input         Clock input terminal           2         LED         Output         External LED control terminal           3         //RQ         Output         Interrupt output terminal           4         //RST         Input         Hardware reset input terminal           5*         NC         —         Not used           6         PLLC         —         Built-in PLL capacitor terminal           7         VDD         —         Power supply (Typ + 3.0 V)           8         VSS         —         Ground           9         VREF         —         Analog reference voltage terminal           10         HPOUT-L/MONO         Output         Headphone output L-ch           11         HPOUT-L/MONO         Output         Headphone output R-ch           12         EQ1         —         Equalizer terminal           13         EQ2         —         Equalizer terminal 1           14         EQ3         —         Equalizer terminal 2           15         SPVDD         —         Analog power supply for speaker amplifier (Typ + 3.6 V)           16		■ IC105 VHITMU/62C+-1L (TMU/62C): SOUND				
2 LED Output External LED control terminal 3 /IRQ Output Interrupt output terminal 4 /RST Input Hardware reset input terminal 5* NC — Not used 6 PLLC — Built-in PLL capacitor terminal 7 VDD — Power supply (Typ + 3.0 V) 8 VSS — Ground 9 VREF — Analog reference voltage terminal 10 HPOUT-L/MONO Output Headphone output L-ch 11 HPOUT-R Output Headphone output R-ch 12 EQ1 — Equalizer terminal 1 13 EQ2 — Equalizer terminal 2 14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 4 22 D5 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 0 27 D0 Input/Output CPU I/F data bus 0 28 WRR Input CPU I/F data bus 0 29 I/CS Input CPU I/F data bus 0 29 I/CS Input CPU I/F data bus 0 29 I/CS Input CPU I/F in pselect input 30 A0 Input CPU I/F address signal 31 I/RD Input CPU I/F read enable			Input/Output	Description of terminal		
A	1	CLKI	Input	Clock input terminal		
4 /RST Input Hardware reset input terminal 5* NC — Not used 6 PLLC — Built-in PLL capacitor terminal 7 VDD — Power supply (Typ + 3.0 V) 8 VSS — Ground 9 VREF — Analog reference voltage terminal 10 HPOUT-L/MONO Output Headphone output L-ch 11 HPOUT-R Output Headphone output R-ch 12 EQ1 — Equalizer terminal 1 13 EQ2 — Equalizer terminal 2 14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F address signal	2	LED	Output	External LED control terminal		
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8 VSS — Ground 9 VREF — Analog reference voltage terminal 10 HPOUT-L/MONO Output Headphone output L-ch 11 HPOUT-R Output Headphone output R-ch 12 EQ1 — Equalizer terminal 1 13 EQ2 — Equalizer terminal 2 14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 2 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 I/WR Input CPU I/F write enable 29 I/CS Input CPU I/F write enable 29 I/CS Input CPU I/F chip select input 30 A0 Input CPU I/F chip select input 31 I/RD Input CPU I/F read enable	6	PLLC	_	Built-in PLL capacitor terminal		
9 VREF — Analog reference voltage terminal 10 HPOUT-L/MONO Output Headphone output L-ch 11 HPOUT-R Output Headphone output R-ch 12 EQ1 — Equalizer terminal 1 13 EQ2 — Equalizer terminal 2 14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 1 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 I/WR Input CPU I/F write enable 29 I/CS Input CPU I/F chip select input 30 A0 Input CPU I/F chip select input 31 I/RD Input CPU I/F read enable	7	VDD	_	Power supply (Typ + 3.0 V)		
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11 HPOUT-R  Output Headphone output R-ch  12 EQ1 — Equalizer terminal 1  13 EQ2 — Equalizer terminal 2  14 EQ3 — Equalizer terminal 3  15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V)  16 SPVSS — Analog ground for speaker amplifier  17 SPOUT1 Output Speaker terminal 1  18 SPOUT2 Output Speaker terminal 2  19 MTR Output External motor control terminal  20 D7 Input/Output CPU I/F data bus 7  21 D6 Input/Output CPU I/F data bus 6  22 D5 Input/Output CPU I/F data bus 5  23 D4 Input/Output CPU I/F data bus 4  24 D3 Input/Output CPU I/F data bus 3  25 D2 Input/Output CPU I/F data bus 2  26 D1 Input/Output CPU I/F data bus 1  27 D0 Input/Output CPU I/F data bus 0  28 /WR Input CPU I/F data bus 0  29 /CS Input CPU I/F chip select input  30 A0 Input CPU I/F address signal  31 /RD Input CPU I/F read enable	9	VREF	_	Analog reference voltage terminal		
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13 EQ2 — Equalizer terminal 2 14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F read enable	11	HPOUT-R	Output	Headphone output R-ch		
14 EQ3 — Equalizer terminal 3 15 SPVDD — Analog power supply for speaker amplifier (Typ + 3.6 V) 16 SPVSS — Analog ground for speaker amplifier 17 SPOUT1 Output Speaker terminal 1 18 SPOUT2 Output Speaker terminal 2 19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F read enable	12	EQ1	_	Equalizer terminal 1		
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19 MTR Output External motor control terminal 20 D7 Input/Output CPU I/F data bus 7 21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	17	SPOUT1	Output	Speaker terminal 1		
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21 D6 Input/Output CPU I/F data bus 6 22 D5 Input/Output CPU I/F data bus 5 23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	19	MTR	Output	External motor control terminal		
22D5Input/OutputCPU I/F data bus 523D4Input/OutputCPU I/F data bus 424D3Input/OutputCPU I/F data bus 325D2Input/OutputCPU I/F data bus 226D1Input/OutputCPU I/F data bus 127D0Input/OutputCPU I/F data bus 028/WRInputCPU I/F write enable29/CSInputCPU I/F chip select input30A0InputCPU I/F read enable	20	D7	Input/Output	CPU I/F data bus 7		
23 D4 Input/Output CPU I/F data bus 4 24 D3 Input/Output CPU I/F data bus 3 25 D2 Input/Output CPU I/F data bus 2 26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	21	D6	Input/Output	CPU I/F data bus 6		
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26 D1 Input/Output CPU I/F data bus 1 27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	24	D3	Input/Output	CPU I/F data bus 3		
27 D0 Input/Output CPU I/F data bus 0 28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	25	D2	Input/Output	CPU I/F data bus 2		
28 /WR Input CPU I/F write enable 29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	26	D1	Input/Output	CPU I/F data bus 1		
29 /CS Input CPU I/F chip select input 30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	27	D0	Input/Output	CPU I/F data bus 0		
30 A0 Input CPU I/F address signal 31 /RD Input CPU I/F read enable	28	/WR	Input	CPU I/F write enable		
31 /RD Input CPU I/F read enable	29	/CS	Input	CPU I/F chip select input		
	30	A0	Input	CPU I/F address signal		
32 IOVDD — Power supply for terminal	31	/RD	Input	CPU I/F read enable		
	32	IOVDD	_	Power supply for terminal		

In this unit, the terminal withasterisk mark (\*) is (open) terminal which is not connected to the outside.



### ■ IC106 (AD6529B): DIGITAL BASEBAND

Pin No.	Terminal name	Input/ Output	Description of terminal
1	ASDO	Output	Audio serial port data output to analog BB
2	BSDI	Input	Baseband serial port data input from analog BB
3	BSOFS	Output	Baseband serial port output framing signal output to analog BB
4	GPIO_48	Input	Hook switch of hands free kit (earphone) detection
5	VINT	Input	Analog BB interface power supply 1.7 - 3.3 V (VCORE)
6	GPO_29	Output	Analog BB reset output (ABBRESET)
7	GPO_5	Output	Advanced state machine of analog BB
8	VDDRTC	Input	RTC power supply 1.0 - 1.9 V (VRTC)
9	VSSRTC	_	RTC ground
10	MC_DAT[0]	Input/ Output	SD interface data bus 0
11	GPIO_22	Output	RSP for main LCD controller
12	GPIO_56	Input	Boot control 2 (Hardware version select)
13	KEYPADCOL[4]	Output	KEYIN signal output 4
14	KEYPADCOL[1]	Output	KEYIN signal output 1
15	KEYPADROW[4]	Input	KEYIN signal input 4
16	KEYPADROW[2]	Input	KEYIN signal input 2
17	GPIO_38	Input	Interrupt input from sound generator IC
18	GPIO_36	Output	Mode select 2 for interface IC/ AOUT3 bias control
19	ASDI	Input	Audio serial port data input from analog BB
20	GPIO_35	Input	SD card interface write protect
21	ADD[0]	Output	Write protect control for flash memory 2
22	ASFS	Input	Audio serial port framing signal input from analog BB
23	BSIFS	Input	Baseband serial port input framing signal input from analog BB
24	BSDO	Output	Baseband serial port data output to analog BB
25	CSDI	Input	Control serial port data input from analog BB
26*	GPO_6	Output	Not used
27	GPO_0	Output	Analog baseband receive section control (RXON)
28	OSCOUT	Output	32.768 kHz crystal oscillator output
29	MC_DAT[2]	Input/ Output	SD interface data bus 2
30	VMC	Input	SD card interface power supply 1.7 - 3.3 V (VAPP)
31	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
32	KEYPADCOL[3]	Output	KEYIN signal output 3
33	KEYPADCOL[2]	Output	KEYIN signal output 2
34	GPIO_39	Output	USB PU control for interface IC
	GPIO_37	Input	Interrupt input from analog BB

Pin No. name   Input   Description of terminal   Output   36   GPIO_34   Output   UART_TXD for Bluetooth module   37   ADD[4]   Output   Processor address bus 4   38   ADD[2]   Output   Processor address bus 2   39   GND	_	T T		I
37         ADD[4]         Output         Processor address bus 4           38         ADD[2]         Output         Processor address bus 2           39         GND         —         Ground           40         KEYPADROW[0]         Input         KEYIN signal input 0           41         VEXT         Input         System interface power supply 2.4 - 3.3 V (VINT)           42         GPO_23         Output         SLEEP control for SRAM 2           43         ADD[7]         Output         Processor address bus 7           44         VMEM         Input         Memory power supply 2.7 - 3.3 V (VMEM)           45         ADD[1]         Output         Processor address bus 1           46         CSDO         Output         Processor address bus 1           47         CLKOUT_GATE         Input         Master clock enable from analog BB (MCLKEN)           48         GPO_1         Output         Serial port data output to analog BB (MCLKEN)           49         OSCIN         Input         32.768 kHz crystal oscillator input           50         MC_CMD         Input         Sp. Input         Mescrip of Serial port data output to analog BB (MCLKEN)           51         GPIO_55         Input         Boot control 1 (Hardware version select		Terminal name	•	Description of terminal
38 ADD[2] Output Processor address bus 2 39 GND — Ground 40 KEYPADROW[0] Input KEYIN signal input 0 41 VEXT Input System interface power supply 2.4 - 3.3 V (VINT) 42 GPO_23 Output SLEEP control for SRAM 2 43 ADD[7] Output Processor address bus 7 44 VMEM Input Memory power supply 2.7 - 3.3 V (VMEM) 45 ADD[1] Output Processor address bus 1 46 CSDO Output Control serial port data output to analog BB (MCLKEN) 48 GPO_1 Output Analog baseband transmit section control (TXON) 49 OSCIN Input 32.768 kHz crystal oscillator input SD interface CMD (SD_CMD) 50 MC_CMD Input/ Output SD interface CMD (SD_CMD) 51 GPIO_55 Input Boot control 1 (Hardware version select) 52 GND — Ground 53 KEYPADROW[3] Input KEYIN signal input 1 54 KEYPADROW[1] Input KEYIN signal input 1 55 GPIO_33 Input UART_RXD for Bluetooth module 56 GPIO_17 Output Processor address bus 11 58 ADD[9] Output Processor address bus 5 59 ADD[5] Output Processor address bus 3 61 GND — Ground 62 VCC Input Core power supply 1.7 - 1.9 V (VCORE) 63 PWRON Output System power control for analog BB 64 MC_DAT[1] Input/ Output System power control for analog BB 66 VEXT Input KEYIN signal output 0 67 KEYPADCOL[0] Output KEYIN signal output 0 68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input Processor address bus 1 70 GPIO_16 Output Processor address bus 13 71 ADD[13] Output Processor address bus 13 72 ADD[13] Output Processor address bus 13 74 ADD[13] Output Processor address bus 13 75 ADD[15] Output Processor address bus 13 76 GPIO_16 Output Processor address bus 13 77 ADD[17] Output Processor address bus 13 78 ADD[18] Output Processor address bus 13	36	GPIO_34	Output	UART_TXD for Bluetooth module
39 GND	37	ADD[4]	Output	Processor address bus 4
40	38	ADD[2]	Output	Processor address bus 2
41	39	GND	_	Ground
Input	40	KEYPADROW[0]	Input	KEYIN signal input 0
43 ADD[7] Output Processor address bus 7  44 VMEM Input (VMEM)  45 ADD[1] Output Processor address bus 1  46 CSDO Output analog BB  47 CLKOUT_GATE Input Master clock enable from analog BB (MCLKEN)  48 GPO_1 Output Analog baseband transmit section control (TXON)  49 OSCIN Input SD interface CMD (SD_CMD)  50 MC_CMD Input Output SEYNORD)  51 GPIO_55 Input HEYPADROW[3] Input KEYIN signal input 3  52 GND — Ground  53 KEYPADROW[3] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module PCM data output for Bluetooth module  56 GPIO_17 Output Processor address bus 11  58 ADD[9] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output BB Output Output Output SIM power supply 2.4 - 3.3 V (VINT)  65 GPIO_15 Input KEYIN signal output 0  66 VEXT Input Core power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_16 Output PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output PCM SYNC output for Bluetooth module  72 ADD[13] Output PCM SYNC output for Bluetooth module  73 ADD[8] Output PCM SYNC output for Bluetooth module	41	VEXT	Input	System interface power supply 2.4 - 3.3 V (VINT)
44 VMEM Input (VMEM) 45 ADD[1] Output Processor address bus 1 46 CSDO Output Control serial port data output to analog BB 47 CLKOUT_GATE Input Master clock enable from analog BB (MCLKEN) 48 GPO_1 Output Analog baseband transmit section control (TXON) 49 OSCIN Input SD interface CMD (SD_CMD) 50 MC_CMD Input/ Output 51 GPIO_55 Input Boot control 1 (Hardware version select) 52 GND — Ground 53 KEYPADROW[3] Input KEYIN signal input 3 54 KEYPADROW[1] Input UART_RXD for Bluetooth module 55 GPIO_33 Input UART_RXD for Bluetooth module 56 GPIO_17 Output Processor address bus 11 58 ADD[9] Output Processor address bus 5 59 ADD[5] Output Processor address bus 3 61 GND — Ground 62 VCC Input Core power supply 1.7 - 1.9 V (VCORE) 63 PWRON Output BB Output Output Output SIM power supply 2.4 - 3.3 V (VINT) 65 GPIO_15 Input KEYIN signal output 0 66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 67 KEYPADCOL[0] Output REYIN signal output 0 68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input PCM data input for Bluetooth module 70 GPIO_16 Output PCM SYNC output for Bluetooth module 71 ADD[13] Output PCM SYNC output for Bluetooth module 72 ADD[13] Output PCM SYNC output for Bluetooth module	42	GPO_23	Output	SLEEP control for SRAM 2
Input   (VMEM)	43	ADD[7]	Output	Processor address bus 7
46 CSDO Output Control serial port data output to analog BB  47 CLKOUT_GATE Input Master clock enable from analog BB (MCLKEN)  48 GPO_1 Output Analog baseband transmit section control (TXON)  49 OSCIN Input SD interface CMD (SD_CMD)  50 MC_CMD Input Output SD interface CMD (SD_CMD)  51 GPIO_55 Input Hardware version select)  52 GND — Ground  53 KEYPADROW[3] Input KEYIN signal input 3  54 KEYPADROW[1] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module  56 GPIO_17 Output Processor address bus 11  58 ADD[9] Output Processor address bus 9  59 ADD[5] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output System power control for analog BB  64 MC_DAT[1] Input/ Output SU interface data bus 1  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM SYNC output for Bluetooth module  70 GPIO_16 Output PCCSSOR address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	44	VMEM	Input	
AT CLKOUT_GATE Input Master clock enable from analog BB (MCLKEN)  48 GPO_1 Output Analog baseband transmit section control (TXON)  49 OSCIN Input 32.768 kHz crystal oscillator input SD interface CMD (SD_CMD)  50 MC_CMD Input SD interface CMD (SD_CMD)  51 GPIO_55 Input Boot control 1 (Hardware version select)  52 GND Ground  53 KEYPADROW[3] Input KEYIN signal input 3  54 KEYPADROW[1] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module  56 GPIO_17 Output PCM data output for Bluetooth module  57 ADD[11] Output Processor address bus 11  58 ADD[9] Output Processor address bus 9  59 ADD[5] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output System power control for analog BB  64 MC_DAT[1] Input/ Output SD interface data bus 1  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 8	45	ADD[1]	Output	Processor address bus 1
Input BB (MCLKEN)  48 GPO_1 Output Analog baseband transmit section control (TXON)  49 OSCIN Input 32.768 kHz crystal oscillator input  50 MC_CMD Input Output SD interface CMD (SD_CMD)  51 GPIO_55 Input Boot control 1 (Hardware version select)  52 GND — Ground  53 KEYPADROW[3] Input KEYIN signal input 3  54 KEYPADROW[1] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module  56 GPIO_17 Output PCM data output for Bluetooth module  57 ADD[11] Output Processor address bus 11  58 ADD[9] Output Processor address bus 9  59 ADD[5] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output System power control for analog BB  64 MC_DAT[1] Input/Output SIM power supply 2.4 - 3.3 V (VINT)  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	46	CSDO	Output	
Section control (TXON)  49 OSCIN Input 32.768 kHz crystal oscillator input  50 MC_CMD Input/Output  51 GPIO_55 Input Boot control 1 (Hardware version select)  52 GND — Ground  53 KEYPADROW[3] Input KEYIN signal input 3  54 KEYPADROW[1] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module  56 GPIO_17 Output PCM data output for Bluetooth module  57 ADD[11] Output Processor address bus 11  58 ADD[9] Output Processor address bus 9  59 ADD[5] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output BB  64 MC_DAT[1] Input/Output  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	47	CLKOUT_GATE	Input	
50 MC_CMD Input/Output SD interface CMD (SD_CMD)  51 GPIO_55 Input Boot control 1 (Hardware version select)  52 GND — Ground  53 KEYPADROW[3] Input KEYIN signal input 3  54 KEYPADROW[1] Input KEYIN signal input 1  55 GPIO_33 Input UART_RXD for Bluetooth module  56 GPIO_17 Output PCM data output for Bluetooth module  57 ADD[11] Output Processor address bus 11  58 ADD[9] Output Processor address bus 9  59 ADD[5] Output Processor address bus 5  60 ADD[3] Output Processor address bus 3  61 GND — Ground  62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output SBB  64 MC_DAT[1] Input/Output  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	48	GPO_1	Output	Analog baseband transmit section control (TXON)
Output	49	OSCIN	Input	32.768 kHz crystal oscillator input
Input   (Hardware version select)   52   GND	50	MC_CMD		SD interface CMD (SD_CMD)
53KEYPADROW[3]InputKEYIN signal input 354KEYPADROW[1]InputKEYIN signal input 155GPIO_33InputUART_RXD for Bluetooth module56GPIO_17OutputPCM data output for Bluetooth module57ADD[11]OutputProcessor address bus 1158ADD[9]OutputProcessor address bus 959ADD[5]OutputProcessor address bus 560ADD[3]OutputProcessor address bus 361GND—Ground62VCCInputCore power supply 1.7 - 1.9 V (VCORE)63PWRONOutputSystem power control for analog BB64MC_DAT[1]Input/OutputSD interface data bus 165GND—Ground66VEXTInput/OutputSIM power supply 2.4 - 3.3 V (VINT)67KEYPADCOL[0]OutputKEYIN signal output 068VEXTInput/SIM power supply 2.4 - 3.3 V (VINT)69GPIO_15Input/SIM power supply 2.4 - 3.3 V (VINT)69GPIO_15Input/SIM power supply 2.4 - 3.3 V (VINT)69GPIO_16Output/SIM power supply 2.4 - 3.3 V (VINT)70GPIO_16Output/SIM power supply 2.4 - 3.3 V (VINT)71ADD[13]Output/SIM processor address bus 1372ADD[12]Output/SIM processor address bus 8	51	GPIO_55	Input	
54KEYPADROW[1]InputKEYIN signal input 155GPIO_33InputUART_RXD for Bluetooth module56GPIO_17OutputPCM data output for Bluetooth module57ADD[11]OutputProcessor address bus 1158ADD[9]OutputProcessor address bus 959ADD[5]OutputProcessor address bus 560ADD[3]OutputProcessor address bus 361GND—Ground62VCCInputCore power supply 1.7 - 1.9 V (VCORE)63PWRONOutputSystem power control for analog BB64MC_DAT[1]Input/OutputSD interface data bus 165GND—Ground66VEXTInputSIM power supply 2.4 - 3.3 V (VINT)67KEYPADCOL[0]OutputKEYIN signal output 068VEXTInputSIM power supply 2.4 - 3.3 V (VINT)69GPIO_15InputPCM data input for Bluetooth module70GPIO_16OutputPCM SYNC output for Bluetooth module71ADD[13]OutputProcessor address bus 1372ADD[12]OutputProcessor address bus 8	52	GND	_	Ground
Section 233	53	KEYPADROW[3]	Input	KEYIN signal input 3
56 GPIO_17 Output PCM data output for Bluetooth module 57 ADD[11] Output Processor address bus 11 58 ADD[9] Output Processor address bus 9 59 ADD[5] Output Processor address bus 5 60 ADD[3] Output Processor address bus 3 61 GND — Ground 62 VCC Input Core power supply 1.7 - 1.9 V (VCORE) 63 PWRON Output System power control for analog BB 64 MC_DAT[1] Input/Output SD interface data bus 1 65 GND — Ground 66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 67 KEYPADCOL[0] Output KEYIN signal output 0 68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input PCM data input for Bluetooth module 70 GPIO_16 Output PCM SYNC output for Bluetooth module 71 ADD[13] Output Processor address bus 13 72 ADD[12] Output Processor address bus 8	54	KEYPADROW[1]	Input	KEYIN signal input 1
Dutput   module	55	GPIO_33	Input	UART_RXD for Bluetooth module
58 ADD[9] Output Processor address bus 9 59 ADD[5] Output Processor address bus 5 60 ADD[3] Output Processor address bus 3 61 GND — Ground 62 VCC Input Core power supply 1.7 - 1.9 V (VCORE) 63 PWRON Output System power control for analog BB 64 MC_DAT[1] Input/Output SD interface data bus 1 65 GND — Ground 66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 67 KEYPADCOL[0] Output KEYIN signal output 0 68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input PCM data input for Bluetooth module 70 GPIO_16 Output PCM SYNC output for Bluetooth module 71 ADD[13] Output Processor address bus 13 72 ADD[8] Output Processor address bus 8	56	GPIO_17	Output	
59ADD[5]OutputProcessor address bus 560ADD[3]OutputProcessor address bus 361GND—Ground62VCCInputCore power supply 1.7 - 1.9 V (VCORE)63PWRONOutputSystem power control for analog BB64MC_DAT[1]Input/OutputSD interface data bus 165GND—Ground66VEXTInputSIM power supply 2.4 - 3.3 V (VINT)67KEYPADCOL[0]OutputKEYIN signal output 068VEXTInputSIM power supply 2.4 - 3.3 V (VINT)69GPIO_15InputPCM data input for Bluetooth module70GPIO_16OutputPCM SYNC output for Bluetooth module71ADD[13]OutputProcessor address bus 1372ADD[12]OutputProcessor address bus 8	57	ADD[11]	Output	Processor address bus 11
60 ADD[3] Output Processor address bus 3 61 GND — Ground 62 VCC Input Core power supply 1.7 - 1.9 V (VCORE) 63 PWRON Output System power control for analog BB 64 MC_DAT[1] Input/ Output SD interface data bus 1 65 GND — Ground 66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 67 KEYPADCOL[0] Output KEYIN signal output 0 68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input PCM data input for Bluetooth module 70 GPIO_16 Output PCM SYNC output for Bluetooth module 71 ADD[13] Output Processor address bus 13 72 ADD[12] Output Processor address bus 8	58	ADD[9]	Output	Processor address bus 9
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62 VCC Input Core power supply 1.7 - 1.9 V (VCORE)  63 PWRON Output System power control for analog BB  64 MC_DAT[1] Input/ Output SD interface data bus 1  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	60	ADD[3]	Output	Processor address bus 3
Input   (VCORE)	61	GND	_	Ground
64 MC_DAT[1] Input/ Output SD interface data bus 1  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	62	VCC	Input	
Output  65 GND — Ground  66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	63	PWRON	Output	
66 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  67 KEYPADCOL[0] Output KEYIN signal output 0  68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	64	MC_DAT[1]		SD interface data bus 1
Input   (VINT)	65	GND		Ground
68 VEXT Input SIM power supply 2.4 - 3.3 V (VINT) 69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	66	VEXT	Input	
Input (VINT)  69 GPIO_15 Input PCM data input for Bluetooth module  70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	67	KEYPADCOL[0]	Output	KEYIN signal output 0
70 GPIO_16 Output PCM SYNC output for Bluetooth module  71 ADD[13] Output Processor address bus 13  72 ADD[12] Output Processor address bus 12  73 ADD[8] Output Processor address bus 8	68	VEXT	Input	
71 ADD[13] Output Processor address bus 13 72 ADD[12] Output Processor address bus 12 73 ADD[8] Output Processor address bus 8	69	GPIO_15	Input	
72 ADD[12] Output Processor address bus 12 73 ADD[8] Output Processor address bus 8	70	GPIO_16	Output	•
73 ADD[8] Output Processor address bus 8	71	ADD[13]	Output	Processor address bus 13
	72	ADD[12]	Output	Processor address bus 12
74 ADD[6] Output Processor address bus 6	73	ADD[8]	Output	Processor address bus 8
	74	ADD[6]	Output	Processor address bus 6

Pin			
No.	Terminal name	Input/ Output	Description of terminal
	GPO 22	Output	VPP control for flash memory 1
	GPIO 14	Output	PCM clock output for
	_	Output	Bluetooth module
	GPIO_10	Input	USB detection
78	GPIO_12	Output	Reset output for main LCD controller/ Sub LCD driver/Power management IC
79	VMEM	Input	Memory power supply 2.7 - 3.3 V (VMEM)
80	ADD[14]	Output	Processor address bus 14
81	GND	_	Ground
82	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
83	ADD[10]	Output	Processor address bus 10
84	CLKOUT	Output	13 MHz clock output for analog BB (CLKOUT)
85	MC_DAT[3]	Input/ Output	SD interface data bus 3
86	GND	_	Ground
87	GND	_	Ground
88	GPIO_13	Input	Interrupt input from camera module
89	GPIO_7	Input	Hands free kit (earphone) detection
90	GPIO_9	Input	Manufacturer specific input from I/O connector
91	ADD[19]	Output	Processor address bus 19
92	ADD[17]	Output	Processor address bus 17
93	ADD[18]	Output	Processor address bus 18
94	ADD[15]	Output	Processor address bus 15
95	ADD[16]	Output	Processor address bus 16
96	CSFS	Output	Control serial port framing signal output to analog BB
97	MC_CLK	Input	SD interface clock (SD_CLK)
98	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
99	GPIO_11	Input	Flip switch detection
100	GPIO_8	Input	Stereo/monaural detection for hands free kit (earphone)
101	GPIO_5	Input	SD card detection
102	GPIO_6	Input	Interrupt input from main LCD controller
103	ADD[22]	Output	Processor address bus 22
	ADD[21]	Output	Processor address bus 21
	GPIO_40	Output	13 MHz clock output for main LCD controller & Sound generator IC
106	ADD[20]	Output	Processor address bus 20
	GND		Ground
	ADD[23]	Output	Processor address bus 23
	GND		Ground
	VEXT	Input	SIM power supply 2.4 - 3.3 V (VINT)
111	GND	_	Ground
	GPIO_4	Output	UART CTS for Bluetooth module
11/			
	GPIO 2	Outnut	LUSB charge current control
113	GPIO_2 GPIO_3	Output	USB charge current control  UART_RTS for Bluetooth module

Pin No.	Terminal name	Input/ Output	Description of terminal
115	DATA[2]	Input/ Output	Processor data bus 2
116	DATA[0]	Input/ Output	Processor data bus 0
117	DATA[5]	Input/ Output	Processor data bus 5
118	DATA[1]	Input/ Output	Processor data bus 1
119	DATA[3]	Input/ Output	Processor data bus 3
120	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
121	DMINUS	Input	USB D-
122	GPIO_18	Output	JTAG TCK
123	GND	_	Ground
124	GPIO_1	Input	IrDA receive data
125	USC[5]	Input	USC pin (CTS/Ginie_TX)
			,
126	GPIO_0	Output	IrDA transmit data
127	DATA[4]	Input/ Output	Processor data bus 4
128	VMEM	Input	SIM power supply 2.7 - 3.3 V (VMEM)
129	GND	_	Ground
130	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
131	USC[6]	Input	USC pin (GPIO_31/Ginie_RX)
132	VCC	Input	Core power supply 1.7 - 1.9 V (VCORE)
133	USC[2]	Input	USC pin (TXD)
134	USC[4]	Input	USC pin (RTS/Ginie_RX)
135	DATA[7]	Input/ Output	Processor data bus 7
136	DATA[6]	Input/ Output	Processor data bus 6
137	GND	_	Ground
138	DATA[9]	Input/ Output	Processor data bus 9
139	DATA[13]	Input/ Output	Processor data bus 13
140	NROMCS1	Output	Chip select for flash memory 1
141	GPIO_42	Output	Chip select for main LCD controller
142	CLKIN	Input	13 MHz clock input
143	VSIM	Input	SIM power supply 1.7 - 3.3 V (VSIM)
144	GND	_	Ground
145	USC[3]	Input	Pull up to VINT
146	USC[1]	Input	USC pin (RXD)
147	GND	put	Ground
		Innut	
148	USC[0]	Input	USC pin (Ginie_TX)
149	DATA[10]	Input/ Output	Processor data bus 10
150	DATA[8]	Input/ Output	Processor data bus 8
151	NRD	Output	Processor read strobe
152	DATA[14]	Input/ Output	Processor data bus 14

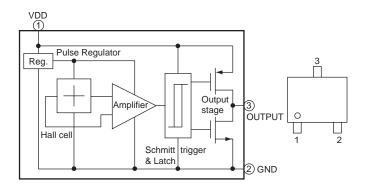
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Pin No.	Terminal name	Input/ Output	Description of terminal
153	GND	<del>-</del>	Ground
154	NRAMCS2	Output	Chip select for SRAM 2
155	GPIO_44	Input	Wakeup mode select
156	VSSUSB	_	USB ground
157	GPIO_47	Output	Camera module reset
158	GPIO_20	Output	JTAG TDI
159	CLKON	Output	13 MHz oscillator power control signal (VCXOEN)
160	VCC	Input	Core power supply 1.7-1.9V (VCORE)
161	GPO_18	Output	SYNTH enable for RF (SYNTHEN)
162	GPO_21	Output	SYNTH clock output for RF (SYNTHCLK)
163	DATA[12]	Input/ Output	Processor data bus 12
164	DATA[11]	Input/ Output	Processor data bus 11
165	NWE	Output	Processor write strobe
166	VEXT	Input	SIM power supply 2.4 - 3.3 V (VINT)
167	GPO_11	Output	Band select 4 for RF (BS4)
168	GPO_20	Output	SYNTH data output for RF (SYNTHDATA)
169	DATA[15]	Input/ Output	Processor data bus 15
170	VMEM	Input	Memory power supply 2.7 - 3.3 V (VMEM)
171	NADV	Output	Address latch enable for flash memory 2
172	NGPCS1	Output	Chip select for flash memory 2
173	VMEM	Input	Memory power supply 2.7 - 3.3 V (VMEM)
174	GPIO_45	Output	Chip select for 4M SRAM
175	GPIO_46	Output	Chip select for sound generator IC
176	DPLUS	Input	USB D+
177	SIMCLK	Output	System interface clock output
178	JTAGEN	Input	JTAG enable
179	VEXT	Input	SIM power supply 2.4 - 3.3 V (VINT)
180	GPO_3	Output	Incoming LED OFF control
181	GPO_4	Output	Mode select 1 for interface IC
182	GPO_7	Output	Bluetooth module power ON/OFF control
183	GPO_16	Output	Band select 1 for RF (BS1)
184	GPO_17	Output	Band select 2 for RF (BS2)
185	NHWR/NUSB	Output	Processor high write strobe
186	GPO_19	Output	Mode select 3 for interface IC
187	NLWR/NLSB	Output	Processor low write strobe
188	NWAIT	Input	Processor wait input
189	NRESET	Input	System reset input
190 <sup>*</sup>	BURSTCLK	Output	Not used
191	NRAMCS1	Output	Chip select for SRAM 1
192	NAUXCS1	Output	Command latch enable for flash memory 2
193	GPIO_43	Output	Chip select for Camera module
	l .	-	1

Pin No.	Terminal name	Input/ Output	Description of terminal
194	VDDUSB	Input	USB power supply 2.8 - 3.3 V (VUSB)
195	GPIO_23	Output	SIM interface reset
196	SIMDATAIO	Input/ Output	SIM interface data input/output
197	GPIO_24	Output	Sound generator IC reset
198	GPIO_19	Output	JTAG TMS
199	GPIO_21	Output	JTAG TDO
200	GPO_2	Output	Write protect control for flash memory 1
201	GND	_	Ground
202	GPO_8	Output	IrDA power ON/OFF control
203	GPO_9	Output	Band select 3 for RF (BS3)
204	GPO_10	Output	BUF OFF for main LCD controller

In this unit, the terminal with asterisk mark (\*) is (open) terminal which is not connected to the outside.

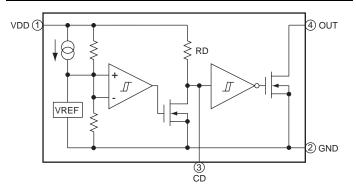
### ■ IC107 VHIEW6671++-1R (EW6671): HALL

Pin No.	Terminal name	Input/Output	Description of terminal
1	VDD	Input	Input
2	GND	_	Ground
3	OUT	Output	Output



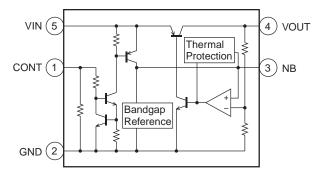
### ■ IC108 VHIR3112Q26-1L (R3112Q261A): VOLTAGE DETECTOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VDD	_	Power supply
2	GND	_	Ground
3	CD	Input	External condenser connection terminal for delay
4	OUT	Output	Output terminal (L: when output is detected, H: when output is canceled)



### ■ IC109 VHINJ287130-1L (NJM2871F03): 3.0 V REGULATOR

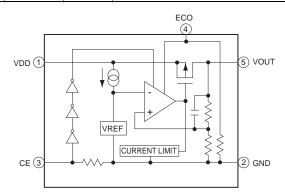
Pin No.	Terminal name	Input/ Output	Description of terminal
1	CONT	Input	Control
2	GND	_	Ground
3	NB	_	Noise bypass
4	VOUT	Output	Output
5	VIN	Input	Input



# ■ IC111 VHIR116030B-1L (R1160N301B): REGULATOR

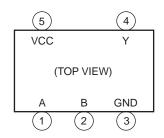
### ■ IC703 VHIR116018B-1L (R116018B): 1.8 V REGULATOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VDD	Input	Input
2	GND	_	Ground
3	CE	Input	Chip enable
4	ECO	Input	High speed/low consumption selector switch
5	VOUT	Output	Output



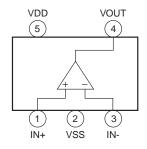
### ■ IC113, 706 VHITC7SZ08A-1L (TC7SZ08A): AND GATE/LOGIC

Pin No.	Terminal name	Input/ Output	Description of terminal
1	Α	Input	Signal input
2	В	Input	Signal input
3	GND	_	Ground
4	Υ	Output	Logic value output
5	VCC	Input	Power supply



## ■ IC114 RH-IXA007AFZZL (HA1631S03CME): COMPARATOR

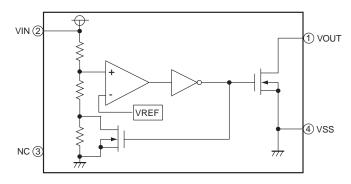
Pin No.	Terminal name	Input/ Output	Description of terminal
1	IN+	Input	Input
2	VSS	_	Ground
3	IN-	Input	Input
4	VOUT	Output	Output
5	VDD	_	Power supply



### ■ IC115 VHIXC61CN27-1L (XC61CN27): REGULATOR

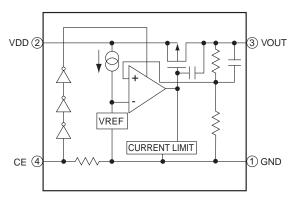
Pin No.	Terminal name	Input/ Output	Description of terminal
1	VOUT	Output	Output
2	VIN	Input	Supply voltage input
3*	NC		Not used
4	GND	_	Ground

In this unit, the terminal withasterisk mark (\*) is (open) terminal which is not connected to the outside.



#### ■ IC116 VHIRQ5RW45B-1L (RQ5RW45B): 4.5 V REGULATOR

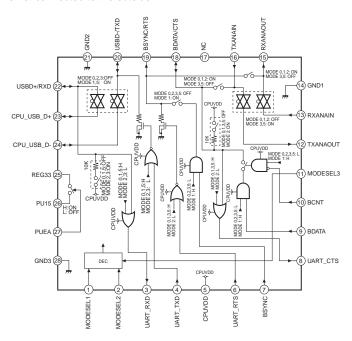
Pin No.	Terminal name	Input/ Output	Description of terminal
1	GND		Ground
2	VDD	_	Power supply
3	VOUT	Output	Output
4	CE	Input	Chip enable



#### ■ IC502 VHIBU7870KN-1L (BU7870KN): USB CONTROLLER

_ 103	UZ VIIIDO707	)	BU/8/UKN): USB CONTROLLER
Pin No.	Terminal name	Input/ Output	Description of terminal
1	MODESEL1	Input	Operation mode switching 1
2	MODESEL2	Input	Operation mode switching 2
3	UART_RXD	Output	UART_RXD output
4	UART_TXD	Input	UART_TXD input
5	CPUVDD	_	Digital power supply
6	UART_RTS	Input	UART_RTS input
7	BSYNC	Input	BSYNC input
8	UART_CTS	Output	UART_CTS output
9	BDATA	Input	BDATA input
10	BCNT	Input	BDATA input control
11	MODESEL3	Input	Operation mode switching 3
12	TXANAOUT	Output	Hands free sending external output
13	RXANAIN	Input	Hands free receiving external input
14	GND1	_	Ground
15	RXANAOUT	Output	Hands free receiving output
16	TXANAIN	Input	Hands free sending input
17*	NC	_	Not used
18	BDATA/CTS	Input/ Output	BDATA/CTS switching external input/output
19	BSYNC/RTS	Output	BSYNC/RTS switching external output
20	USBD-/TXD	Input/ Output	USBD-/TXD switching external input/output
21	GND2	_	Ground
22	USBD+/RXD	Input/ Output	USBD+/RXD switching external input/output
23	CPU_USB_D+	Input/ Output	CPU_USB_D+ input/output
24	CPU_USB_D-	Input/ Output	CPU_USB_D- input/output
25	REG33	_	Power supply voltage for USB
26	PU15	Output	PMOS open drain output
27	PUEA	Input	PU15 control input
28	GND3	_	Ground

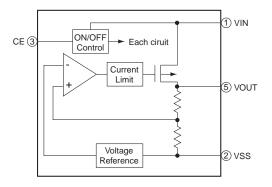
In this unit, the terminal withasterisk mark (\*) is (open) terminal which is not connected to the outside.



### ■ IC505 VHIXC620930-1L (XC620930): REGULATOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VIN	Input	Input
2	VSS	_	Ground
3	CE	Input	ON/OFF Control
4	NC	_	Not used
5	VOUT	Output	Output

In this unit, the terminal withasterisk mark (\*) is (open) terminal which is not connected to the outside.



### ■ IC506 RUNTZA005AFZZL (UGNZ2): BLUETOOTH MODULE

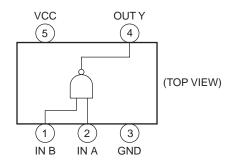
Pin No.	Terminal name	Input/ Output	Description of terminal
1*	USBP	Input/ Output	USB DATA+ (Not used)
2*	USBN	Input/ Output	USB DATA- (Not used)
3	UART_RTS	Output	UART/Ready to send to DTE
4	GND	_	Ground
5	GND	_	Ground
6	UART_TxD	Output	UART/TxD to DTE
7	UART_RxD	Input	UART/RxD from DTE
8	UART_CTS	Input	UART/Clear to send from DTE
9	PIO8	Input/ Output	General purpose I/O
10	VCC_IO	Input	Positive supply voltage for IO voltage Connect the VCC, if IO voltage is same as VCC
11	VCC	Input	Main supply voltage input 1 Regulated DC source recommended
12	PCM_OUT	Output	PCM data stream output
13	PCM_SYNC	Input/ Output	Connection to PCM frame sync Input/ output of 8 kHz
14*	XTAL_IN	Input	Ext clock in (Not used)
15*	XTAL_OUT	Input	Ext clock out (Not used)
16	RESETB	Input	System reset
17	VDD18V	Output	VDD_CORE decupling capacitor
18	PCMCLK	Input/ Output	Connction to PCM reference Clock input/output of 256 kHz
19	PCM_IN	Input	PCM data stream input
20	PIO5	Input/ Output	General purpose I/O

Pin No.	Terminal name	Input/ Output	Description of terminal
21	PIO6 Input/ Output		General purpose I/O
22	PIO3	Input/ Output	General purpose I/O
23	GND	_	Ground
24	SPIMOSI	Input/ Output	For factory use only
25	SPICLK	Input/ Output	For factory use only
26	PIO4	Input/ Output	General purpose I/O
27	PIO7	Input/ Output	General purpose I/O
28	PIO1	Input/ Output	General purpose I/O
29	RF_IO Input/ Output		RF input/output
30	GND	_	Ground
31	SPIMISO	Input/ Output	For factory use only
32*	SPICSB	Input/ Output	For factory use only (Not used)
33	PIO2	Input/ Output	General purpose I/O
34	PIO0	Input/ Output	General purpose I/O

In this unit, the terminal withasterisk mark (\*) is (open) terminal which is not connected to the outside.

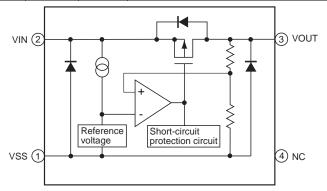
### ■ IC507 VHITC7SET00FU- (TC7SET00FU): LOGIC

Pin No.	Terminal name	Input/ Output	Description of terminal
1	INB	Input	Input B
2	INA	Input	Input A
3	GND	_	Ground
4	OUT Y	Output	Output Y
5	VCC	_	Power supply



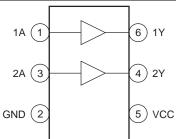
### ■ IC508 VHI817A30NB-1R (817A30NB): 3.0V REGULATOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VSS		Ground (GND)
2	VIN	Input	Input voltage (VDD)
3	VOUT	Output	Output voltage
4	NC	_	Not used (CE)



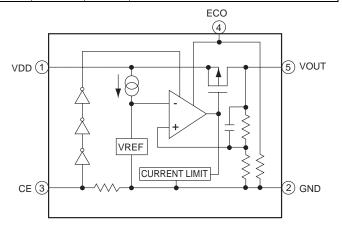
## ■ IC509 VHILVC2G34P-1R (LVC2G34P): BUFFER

Pin No.	Terminal name	Input/ Output	Description of terminal
1	1A	Input	Input
2	GND	_	Ground
3	2A	Input	Input
4	2Y	Output	Output
5	VCC	_	Power supply
6	1Y	Output	Output



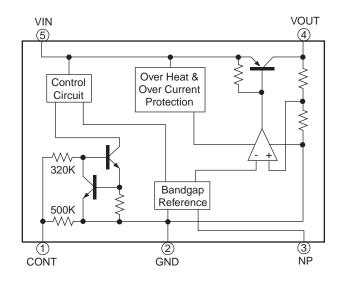
#### ■ IC701 VHIR116025B-1L (R116025B): 2.5V REGULATOR

	•		(
Pin No.	Terminal name	Input/ Output	Description of terminal
1	VDD	Input	Input
2	GND	_	Ground
3	CE	Input	Chip enable
4	ECO	Input	High speed/low consumption selector switch
5	VOUT	Output	Output



## ■ IC702 VHITK11131C-1R (TK11131C): REGULATOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	CONT	Input	Control
2	GND	_	Ground
3	NP	Input	Capacitor (Vref)
4	VOUT	Output	Output
5	VIN	Input	Input



## ■ IC704 (LR38863): DISPLAY CONTROLLER

Pin No.	Terminal name	Input/ Output	Description of terminal
1	DUMMY4	_	Dummy 4
2	VDDPLL	_	PLL Power supply 1.8 V (1.6 V~ 2.0 V)
3	PLLGND	_	PLL Ground
4	PLLDIV0	Input	PLL multiply switching signal
5	PLLDIV1	Input	PLL multiply switching signal
6	HSD0	Input/ Output	Data bus for high-speed serial transfer
7	HSD1	Input/ Output	Data bus for high-speed serial transfer
8	HSD2	Input/ Output	Data bus for high-speed serial transfer
9	HSWRD	Input/ Output	Read/Write determination signal for high-speed serial transfer
10	HSEN	Input/ Output	High-speed serial data effective signal High is active
11	HSCK	Input/ Output	Standard clock for high-speed serial transfer (5 to 33 MHz)
12	DUMMY3	_	Dummy 3
13	PWM1/PORT8	Output	PWM output 1 General-purpose PORT output (default) (Not used)
14	PLLDIV2	Input	PLL multiply switching signal
15	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
16	GND	_	Logic ground
17	SUBWR_B	Input/ Output	Light signal for External display

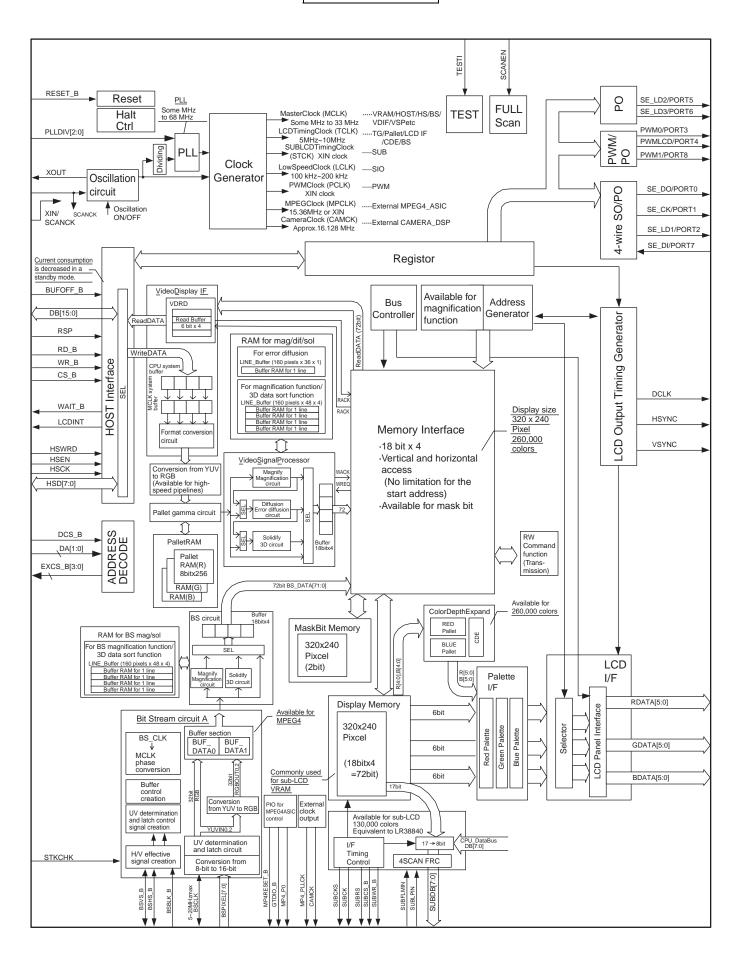
Pin No.	Terminal name	Input/ Output	Description of terminal
18	GND	_	Logic ground
19	VDDCORE		CORE Power supply 1.8 V (1.6 V~ 2.0 V)
20	PWM0/PORT3	Output	PWM output 0 General-purpose PORT output (default)
21	SUBCS_B	Input/ Output	Chip select signal for External display
22	CS_B	Input/ Output	Device select signal (Display is active when CS_B is "Low")
23	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
24	LCDINT	Output	External interrupt signal (Starting varies when interruption occurs.)
25	GTDIO_B	Output	MPEG4ASIC internal core powercut signal ("Low" is active.)
26	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
27	SUBDB1	Input/ Output	Data bus for External display
28	BDATA[5] (B5)	Output	Display panel B output signa
29	BDATA[5] (B4)	Output	Display panel B output signa
30	BDATA[5] (B3)	Output	Display panel B output signa
31	GND	_	Logic ground
32	TESTI	Input	Test terminal (Connected to GND normally)
33	BSHS_B	Input/ Output	External Bit Stream horizontal synchronization signal ("Low" is active)
34	WR_B	Input/ Output	Host write strobe signal
35	SUBRS	Input/ Output	Data determination signal for External display
36	MP4 RESET_B	Output	MPEG4ASIC reset control signal ("Low" is active)
37	HSD6	Input/ Output	Data bus for high-speed serial transfer
38	BDATA[2] (B2)	Output	Display panel B output signal
39	BDATA[2] (B1)	Output	Display panel B output signal
40	BDATA[2] (B0)	Output	Display panel B output signal
41*	EXCS_B1	Input/ Output	Chip select output 1 (internal decode output) (Not used)
42*	XOUT	Output	Oscillation circuit output (Not used)
43	VDDIO		IO Power supply 3.0 V (2.7 V~ 3.3 V)
44	GND	_	Logic ground
45	SCANEN	Input	Full scan effective signal "High" is active (Connected to GND normally)
46	RD_B	Input/ Output	Host read strobe signal
47	RSP	Input/ Output	Register selection signal HOST_IF section: RSP =LowDisplay access RSP = HighControl access Hyper_Serial section: RSP = LowControl acces RSP = HighDisplay access
48	GND	_	Logic ground
49	HSD3	Input/ Output	Data bus for high-speed serial transfer
50	DCLK	Input/ Output	Data sampling clock (display clock)

			<u> </u>
Pin No.	Terminal name	Input/ Output	Description of terminal
51	VSYNC	Input/ Output	Vertical synchronization signal
52	HSYNC	Input/ Output	Horizontal synchronization signal
53*	EXCS_B3	Input/ Output	Chip select output 3 (internal decode output) (Not used)
54	XIN	Input	Oscillation circuit input/External clock input signal Clock input for full scan
55	SUBDB6	Input/ Output	Data bus for External display
56	RESET_B	Input	Master reset (All registers are initialized when Low is activated)
57	SUBDB0	Input/ Output	Data bus for External display
58	SUBDB2	Input/ Output	Data bus for External display
59	HSD5	Input/ Output	Data bus for high-speed serial transfer
60	DB0	Input/ Output	Data bus
61	HSD4	Input/ Output	Data bus for high-speed serial transfer
62*	EXCS_B2	Input/ Output	Chip select output 2 (internal decode output) (Not used)
63	GDATA[5] (G5)	Output	Display panel G output signal
64	GDATA[4] (G4)	Output	Display panel G output signal
65	GDATA[3] (G3)	Output	Display panel G output signal
66	SUBDB3	Input/ Output	Data bus for External display
67	SUBDB4	Input/ Output	Data bus for External display
68	HSD7	Input/ Output	Data bus for high-speed serial transfer
69	DB1	Input/ Output	Data bus
70	DB2	Input/ Output	Data bus
71	DB3	Input/ Output	Data bus
72	DB4	Input/ Output	Data bus
73	STKCHK	Input	Setting BS-related output terminal to Hi-z when a stack is installed (Connected to GND normally)
74	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
75	GND	_	Logic ground
76	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
77	GDATA[2] (G2)	Output	Display panel G output signal
78	SUBDB5	Input/ Output	Data bus for External display
79	BSCLK	Input/ Output	External Bit Stream data clock
80	SUBCK	Output	Clock for External display
81	DB5	Input/ Output	Data bus
82	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
83	GND	_	Logic ground
	1	II.	1

Pin No.	Terminal name	Input/ Output	Description of terminal
84	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
85	CAMCK	Output	Clock for camera operation
86	GDATA[1] (G1)	Output	Display panel G output signal
87	GDATA[0] (G0)	Output	Display panel G output signal
88	RDATA[5] (R5)	Output	Display panel R output signal
89	RDATA[4] (R4)	Output	Display panel R output signal
90	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
91*	PWMLCD/ PORT4	Output	PWM LCD output General-purpose PORT output (default) (Not used)
92	BSBLK_B	Input/ Output	External Bit Stream data effective signal ("High" is active when transferring the data)
93	DB6	Input/ Output	Data bus
94	DB7	Input/ Output	Data bus
95	DB8	Input/ Output	Data bus
96	DB9	Input/ Output	Data bus
97	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
98	RDATA[3] (R3)	Output	Display panel R output signal
99	RDATA[2] (R2)	Output	Display panel R output signal
100	RDATA[1] (R1)	Output	Display panel R output signal
101	RDATA[0] (R0)	Output	Display panel R output signal
102*	MP4_P0	Output	MPEG4 control
103*	EXCS_B0	Input/ Output	Chip select output 0 (internal decode output) (Not used)
104	BSPIXEL7	Input/ Output	External Bit Stream data bus
105	BSVS_B	Input/ Output	External Bit Stream vertical synchronization signal ("Low" is active)
106	DB10	Input/ Output	Data bus
107	DB11	Input/ Output	Data bus
108	DB12	Input/ Output	Data bus
109*	MP4_PLLCK	Output	MPEG4ASIC clock 15.36 MHz/CPU supply XIN clock (Not used)
110	SUBDB7	Input/ Output	Data bus for External display
111	GND	_	Logic ground
112	DA0	Input/ Output	Address input for chip select decode
113	BSPIXEL0	Input/ Output	External Bit Stream data bus
114	DCS_B	Input	Chip select input dedicated for chip select decode
115	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
116	BSPIXEL6	Input/ Output	External Bit Stream data bus
117	SE_DO/PORT0	Output	Data output for 4-wire serial IF (default) General-purpose PORT output
118	DB13	Input/ Output	Data bus

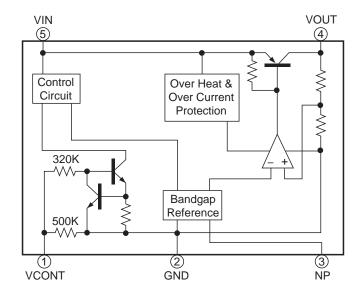
Pin No.	Terminal name	Input/ Output	Description of terminal
119	DB14	Input/ Output	Data bus
120	DB15	Input/ Output	Data bus
121	WAIT_B	Output	External wait signal ("Low" is active)
122	SUBFLMIN	Input	Driver FLM signal input for External display
123	SUBCKS	Output	Clock switching signal for External display
124	DA1	Input/ Output	Address input for chip select decode
125	BSPIXEL1	Input/ Output	External Bit Stream data bus
126	BSPIXEL4	Input/ Output	External Bit Stream data bus
127	GND	_	Logic ground
128	BSPIXEL5	Input/ Output	External Bit Stream data bus
129	SE_CK/PORT1	Output	Control clock for 4-wire serial IF (default) General-purpose PORT output
130	SE_LD2/PORT5	Output	Load signal 2 for 4-wire serial IF General-purpose PORT output (default)
131	BUFOFF_B	Input	Buffer Gated switching signal for I/O through current prevention (High when Host_IF signal is activated)
132	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
133	DUMMY2	_	Dummy 2
134*	SE_LD3/PORT6	Output	Load signal 3 for 4-wire serial IF General-purpose PORT output (default) (Not used)
135	VDDIO	_	IO Power supply 3.0 V (2.7 V~ 3.3 V)
136	SUBLPIN	Input	Driver LP input External display
137	BSPIXEL2	Input/ Output	External Bit Stream data bus
138	BSPIXEL3	Input/ Output	External Bit Stream data bus
139	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
140	SE_DI/PORT7	Input/ Output	4-wire serial input (default) General- purpose PORT output
141	SE_LD1/PORT2	Output	Load signal 1 for 4-wire serial IF (default) General-purpose PORT output
142	GND	_	Logic ground
143	VDDCORE	_	CORE Power supply 1.8 V (1.6 V~ 2.0 V)
144	DUMMY1	_	Dummy 1Dummy 4

In this unit, the terminal with asteriskmark (\*) is (open) terminal which is not connected to the outside.



### ■ IC708 VHITK11130C-1R (TK11130C): REGULATOR

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VCONT	Input	Control
2	GND	_	Groun
3	NP	_	Capacitor (Vref)
4	VOUT	Output	Output
5	VIN	Input	Input



## ■ IC801 VHIHD155155-1L(HD155155NP): RF

Pin No.	Terminal name	Input/ Output	Description of terminal
1	VCCLNA	Input	VCC for LNA transistor and LNA Bias
2	PCSGND	_	GND for Emitter of LNA transistor (PCS)
3	PCSLNAI	Input	Positive input for LNA transistor (PCS)
4	PCSLNAIB	Input	Negative input for LNA transistor (PCS)
5	PCSDCSGND	_	GND for Emitter of LNA transistor (PCS,DCS)
6	DCSLNAI	Input	Positive input for LNA transistor (DCS)
7	DCSLNAIB	Input	Negative input for LNA transistor (DCS)
8	DCSGSMGND	_	GND for Emitter of LNA transistor (DCS,GSM)
9	GSMLNAI	Input	Positive input for LNA transistor (GSM)
10	GSMLNAIB	Input	Negative input for LNA transistor (GSM)
11	GSMGND	_	GND for Emitter of LNA transistor (GSM)
12	PLLOUT	Output	Current output to control and modulate TXVCO
13	VCCOPLL	Input	VCC for OPLL and Phase comparator
14	VCCTXVCO		VCC for TXVCO
15	GNDTXVCOD	_	GND for DCS/PCS TxVCO
16	GNDTXVCODB	_	GND for DCS/PCS TxVCO
17	TXOUTG	Output	Tx output for GSM
18	COMMONGND		GND for common
19	TXOUTD	Output	Tx output for DCS/PCS
20	TXVCOGB	Input	Negative TxVCO output for GSM
21	TXVCOG	Input	Positive TxVCO output for GSM
22	VCCIQ	Input	VCC for IQ modulator
23	IOUT/IIN	Input/ Output	Positive output/input of I channel/modulator

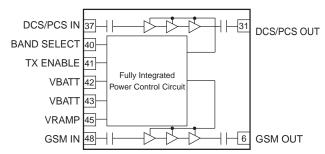
Pin	Terminal	Input/	Description of terminal
No.	name	Output	·
24	IOUTB/IINB	Input/	Negative output/input of I channel/modulator
	00117/011	Output	
25	QOUT/QIN	Input/ Output	Positive output/input of Q channel/modulator
26	QOUTB/QIN	Input/ Output	Negative output/input of Q channel/modulator
27	VCCIFSYN	Input	VCC for IFVCO Buffer and Divider, and IF Synthesiser
28	CPIFSYN	Output	Charge Pump output of IF Synthesiser
29	LE	Input	Load enable for serial data
30	CLK	Input	Clock for serial data
31	VCXOOUT	Output	Output for VCXO
32	SDATA	Input	Serial Data
33*		_	GND for VCXO (Not used)
34*	VCXOE	_	Emitter of VCXO transistor (Not used)
35	VCXOB	Input	Base of VCXO transistor
36	VCCVCXO	Input	VCC for VCXO
37	VCCRFSYN	Input	VCC for RF Synthesiser
38	CPRFSYN	Output	Charge Pump output of RF Synthesise
39	FLOCK	Output	FLOCK,Output,Fast Lock control for RF Synthesiser
40	VCCBB	Input	VCC for Base band and State Logic
41	VCCRFVCO	Input	VCC for RF VCO
42	DIVON	Output	VCXOOUT divider control input
43	VCCRFLO	Input	VCC for RF Local Buffer and Divider
44	CAPQB	Output	Capacitor for Q channel LPF (Negative output)
45	CAPQ	Output	Capacitor for Q channel LPF (Positive output)
46	CAPIB	Output	Capacitor for I channel LPF (Negative output)
47	CAPI	Output	Capacitor for I channel LPF (Positive output)
48	VCCMIX	Input	VCC for Direct conversion Mixer
49	GNDLNA	_	GND for LNA Bias

In this unit, the terminal with asterisk mark (\*) is (open) terminal which is not connected to the outside.

### ■ IC802 RF3146

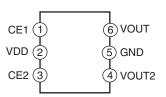
Pin No.	Teminal name	Description of terminal
1	NC	Internal circuit node. Do not externally connect.
2	VCC2 GSM	Contorolled voltage input to the GSM driver stage This voltage is part of the power control function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.
3	NC	Internal circuit node. Do not externally connect.
4	GND	Internally connected to the package base.
5	GND	Internally connected to the package base.
6	GSM900 OUT	RF output for the GSM bands. This is a $50\Omega$ output. The output matching circuit and DC-block are internal to the package.
7	GND	Internally connected to the package base.
8	NC	Internal circuit node. Do not externally connect.
9	NC	Internal circuit node. Do not externally connect.
10	NC	Internal circuit node. Do not externally connect.
11	NC	Internal circuit node. Do not externally connect.
12	NC	Internal circuit node. Do not externally connect.
13	NC	No internal or external connection.
14	NC	Internal circuit node. Do not externally connect.
15	NC	Internal circuit node. Do not externally connect.
16	NC	Internal circuit node. Do not externally connect.
17	NC	Internal circuit node. Do not externally connect.
18	VCC3 GSM	Controlled voltage input to the GSM outpu stage. This voltage is part of the power contro function for the module. This node must be connected to VCC OUT. This pin should be externally decoupled.
19	VCC OUT	Controlled voltage output to feed VCC2 and VCC3. This voltage is part of the power control function for the module. It cannot be connected to any pins other than VCC2 and VCC3.
20	VCC OUT	Controlled voltage output to feed VCC2 and VCC3. This voltage is part of the power control function for the module. It cannot be connected to any pins other than VCC2 and VCC3.
21	VCC3 DCS/PCS	Controlled voltage input to the DCS/PCS out put stage. This voltage is part of the powe control function for the module. This node must be connected to VCC OUT. This pir should be externally decoupled.
22	NC	Internal circuit node. Do not externally connect.
23	NC	Internal circuit node. Do not externally connect.
24	NC	No internal or external connection.
25	NC	Internal circuit node. Do not externally connect.
26	NC	Internal circuit node. Do not externally connect.
27	NC	Internal circuit node. Do not externally connect.
28	NC	Internal circuit node. Do not externally connect.
29	NC	Internal circuit node. Do not externally connect.
30	GND	Internally connected to the package base.
31	DCS/PCS OUT	RF output for the DCS/PCS bands. This is a $50\Omega$ output. The output matching circuit and DC-block are internal to the package.
32	GND	Internally connected to the package base.
33	NC	Internal circuit node. Do not externally connect.
34	GND	Internally connected to the package base.
35	VCC2 DCS/PCS	Controlled voltage input to the DCS/PCS driver stage. This voltage is part of the powe control function for the module. This node must be connected to VCC OUT. This pir should be externally decoupled.

Pin No.	Teminal name	Description of terminal	
36	NC	No internal connection. Connect to ground plane close to the package pin.	
37	DCS/PCS IN	RF input for the DCS/PCS band. This is a $50\Omega$ output.	
38	NC	No internal connection. Connect to ground plane close to the package pin.	
39	VCC1 DCS/PCS	Controlled voltage input to the DCS/PCS driver stage. This voltage is applied internal to the package. This pin should be externally decoupled.	
40	BAND SEL	Allows external control to select the GSM or DSC/PCS bands with a logic high or low. A logic low enables the GSM bands, whereas a logic high enables the DCS/PCS bands.	
41	TX ENABLE	This signal enables the PA module for operation with a logic high. Both bands are disabled with a logic low.	
42	VBATT	Power supply for the module. This pin should be externally decoupled and connected to the battery.	
43	VBATT	Power supply for the module. This pin should be externally decoupled and connected to the battery.	
44	NC	Internal circuit node. Do not externally connect.	
45	VRAMP	Ramping signal from DAC. A simple RC filter may be required depending on the selected baseband.	
46	VCC1 GSM	Internally connected to VCC1 (pin39). No external connection required.	
47	GND1 GSM	Ground connection for the GSM preamplifier stage. Connect to ground plane close to the package pin.	
48	GSM900 IN	RF input to the GSM band. This is a $50\Omega$ input.	
Pkg base	GND	Connect to groung plane with mulitiple via holes. See revommended footprint.	



## ■ IC804 VHIR5322N29-1L(R5322N002B): POWER SUPPLY

Pin No.	Terminal name	Input/ Output	Description of terminal
1	CE1	Input	Chip Enable1
2	VDD	Input	Power supply
3	CE2	Input	Chip Enable2
4	VOUT2	Output	VCC for VRF
5	GND	_	Ground
6	VOUT1	Output	VCC for VTCXO



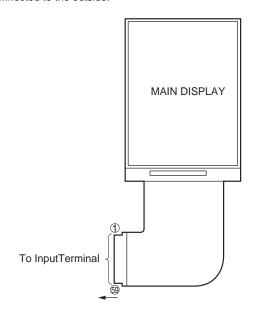
# [2] FUNCTION TABLE OF DISPLAY

# ■ LCD1000 RLCUB0048AF03: MAIN DISPLAY

Pin No.	Terminal name	Input/ Output	Description of terminal	
1	T-COM	Input	COM electric potential input for CS	
2	T-COM	Input	COM electric potential input for CS	
3	TFT-COM	Input	COM voltage input	
4	COMC	Output	COM signal output	
5	COMC	Output	COM signal output	
6	COMDC	Output	COM center voltage output	
7	VCOMH	Output	COM amplitude voltage output	
8	B0	Input	Blue data signal (LSB)	
9	B1	Input	Blue data signal	
10	B2	Input	Blue data signal	
11	B3	Input	Blue data signal	
12	B4	Input	Blue data signal	
13	B5	Input	Blue data signal (MSB)	
14	G0	Input	Green data signal (LSB)	
15	G1	Input	Green data signal	
16	G2	Input	Green data signal	
17	G3	Input	Green data signal	
18	G4	Input	Green data signal	
19	G5	Input	Green data signal (MSB)	
20	R0	Input	Red data signal (LSB)	
21	R1	Input	Red data signal	
22	R2	Input	Red data signal	
23	R3	Input	Red data signal	
24	R4	Input	Red data signal	
25	R5	Input	Red data signal (MSB)	
26	DCLK	Input	Data sampling clock	
27	HSY	Input	Horizontal sync signal	
28	VSY	Input	Vertical sync signal	
29	SO	Output	serial data output	
30	SI	Input	serial data input	
31	SCLK	Input	serial clock input	
32	CS	Input	serial interface chip select	
33	RESET	Input	Hardware reset	
34	VCC		Logic power	
35	GND	_	Ground	
36	GND		Ground	
37	VDC	_	Analog power	
38	VDC	_	Analog power	
39	COM2	_	COM control for CS	
40	VCLAMP	Output	Voltage for CS output	
41	VSS2	Output	DC/DC converter output	
42	VSS1	Output	DC/DC converter output	
43*	NC	_	Not used	
44	VDD2	Output	DC/DC converter output	
45	C5-		Booster capacitor connection terminal	
46	C5+		Booster capacitor connection terminal	
_				

Pin No.	Terminal name	Input/ Output	Description of terminal	
47	C4-	_	Booster capacitor connection terminal	
48	C4+	_	Booster capacitor connection terminal	
49	C3-	_	Booster capacitor connection terminal	
50	C3+	_	Booster capacitor connection terminal	
51	C2-	_	Booster capacitor connection terminal	
52	C2+	_	Booster capacitor connection terminal	
53	C1-	_	Booster capacitor connection terminal	
54	C1+	_	Booster capacitor connection terminal	
55	VDC2	Output	DC/DC converter output	
56	VDC2	Output	DC/DC converter output	
57	VR	Output	Reference power supply output	
58	VS	Output	Source power supply output	
59	VS	Output	Source power supply output	

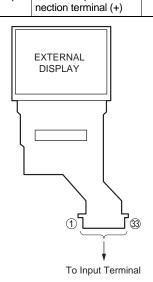
In this unit, the terminal with asterisk mark (\*) is (open) terminal which is not connected to the outside.



### ■ LCD001 RLCUB0049AFZZ : EXTERNAL DISPLAY

Pin No.	Terminal name	Input/ Output	Description of terminal	Notes
1	V0	_	Display drive power supply terminal	_
2	V1	_	Display drive power supply terminal	_
3	V2	_	Display drive power supply terminal	_
4	V3	_	Display drive power supply terminal	_
5	V4	_	Display drive power supply terminal	_
6	GND	_	Ground	_
7	RESB	Input	Reset signal	_
8	CSB	Input	Chip select signal	_
9	RS	Input	Register select signal	"0": Display RAM data "1": Command data
10	WRB	Input	Write signal	"L": Activated
11	RDB	Input	Read signal	"L": Activated
11	RDB	Input	Read signal	"L": Activated

Pin No.	Terminal name	Input/ Output	Description of terminal	Notes
12	D0	Input/ Output	Data signal	_
13	D1	Input/ Output	Data signal	_
14	D2	Input/ Output	Data signal	_
15	D3	Input/ Output	Data signal	_
16	D4	Input/ Output	Data signal	_
17	D5	Input/ Output	Data signal	_
18	D6	Input/ Output	Data signal	_
19	D7	Input/ Output	Data signal	_
20	LP	Input/ Output	Latch signal	_
21	FLM	Output	Display sync signal	_
22	GND (VSS)	_	Ground	_
23	CK	Input	Master clock external input terminal	_
24	CKS	Input	Master clock input selection terminal	"L": Built-in oscillation
25	VDD/VEE	_	Logic system power supply terminal	_
26	VREG	Output	Output terminal for generating constant voltage	_
27	VOUT	Output	Built-in step-up circuit output terminal	_
28	CAP1-	Output	Booster capacitor connection terminal (-)	_
29	CAP1+	Output	Booster capacitor con- nection terminal (+)	_
30	CAP2-	Output	Booster capacitor con- nection terminal (-)	_
31	CAP2+	Output	Booster capacitor con- nection terminal (+)	_
32	CAP3-	Output	Booster capacitor con- nection terminal (-)	_
33	CAP3+	Output	Booster capacitor con- nection terminal (+)	_





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