

## PAL devices

### 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### FEATURES

- Ultra high-speed
  - $t_{PD} = 5\text{ns}$  and  $f_{MAX} = 118\text{MHz}$
- 100% functionality and pin-for-pin compatible with industry standard 20-pin PAL® ICs
- Power-up reset function to enhance state machine design and testability
- Design support provided via SLICE and other CAD tools for Series 20 PAL devices
- Field-programmable on industry standard programmers
- Security fuse
- Individual 3-State control of all outputs
- Register Preload for testability
- Power-up 3-State
- 20-Pin DIP and 20-Pin PLCC

### DESCRIPTION

The Signetics PLQ16XX family consists of ultra high-speed 5ns versions of Series 20 PAL devices.

The PLQ16XX family is 100% functional and pin-compatible with the 16L8, 16R8, 16R6, and 16R4 Series devices.

The sum of products (AND-OR) architecture is comprised of 64 programmable AND gates and 8 fixed OR gates. Multiple bidirectional pins provide variable input/output pin ratios. Individual 3-State control of all outputs and registers with feedback (R8, R6, R4) is also provided. Proprietary designs can be protected by programming the security fuse.

The PLQ16R8, R6, and R4 have D-type flip-flops which are loaded on the Low-to-High transition of the clock input.

In order to facilitate state machine design and testing, a power-up reset function has been incorporated into these devices to reset all internal registers to active-Low after a specific period of time.

The Signetics State-of-the-Art BiCMOS process, known as QUBiC, has been

employed to achieve higher levels of operating performance for the PLQ16XX family of PLDs. The QUBiC transistors have been optimized to provide two-thirds more speed at less than half the power consumed from products using our last generation of bipolar technology. QUBiC reduces on-chip delays and provides high output drive currents while consuming power at very low levels.

The PLQ16XX family of devices are field programmable, enabling the user to quickly generate custom patterns using standard programming equipment. See the programmer section for qualified programmers.

The SLICE software package from Signetics supports easy design entry for the PLQ16XX series as well as other PLD devices from Signetics. The PLQ16XX series are also supported by other standard CAD tools for PAL-type devices.

Order codes are listed in the Ordering Information table.

DEVICE NUMBER	DEDICATED INPUTS	COMBINATORIAL OUTPUTS	REGISTERED OUTPUTS
PLQ16L8	10	8 (6 I/O)	0
PLQ16R8	8	0	8
PLQ16R6	8	2 I/O	6
PLQ16R4	8	4 I/O	4

### ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Plastic Dual-In-Line 300mil-wide	PLQ16R8-5N PLQ16R6-5N PLQ16R4-5N PLQ16L8-5N
20-Pin Plastic Leaded Chip Carrier (PLCC)	PLQ16R8-5A PLQ16R6-5A PLQ16R4-5A PLQ16L8-5A

#### NOTE:

The PLQ16XX series of devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Signetics Military Data Handbook.

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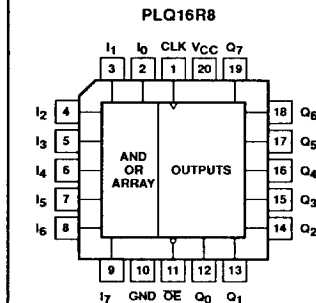
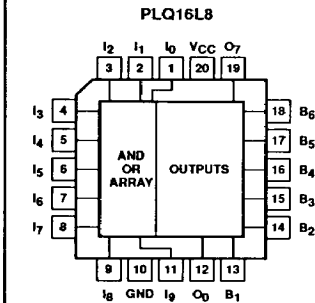
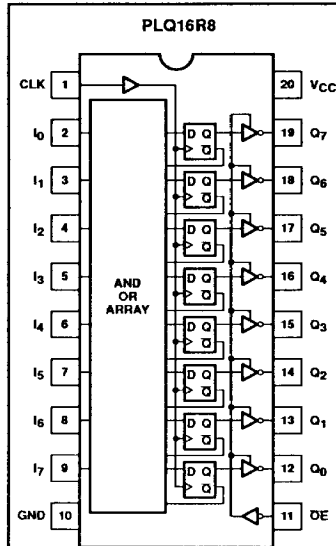
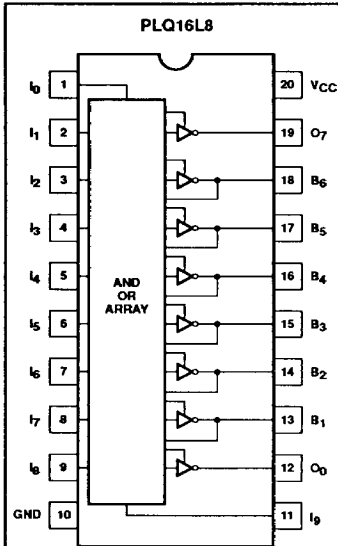
March 16, 1992

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# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### PIN CONFIGURATIONS



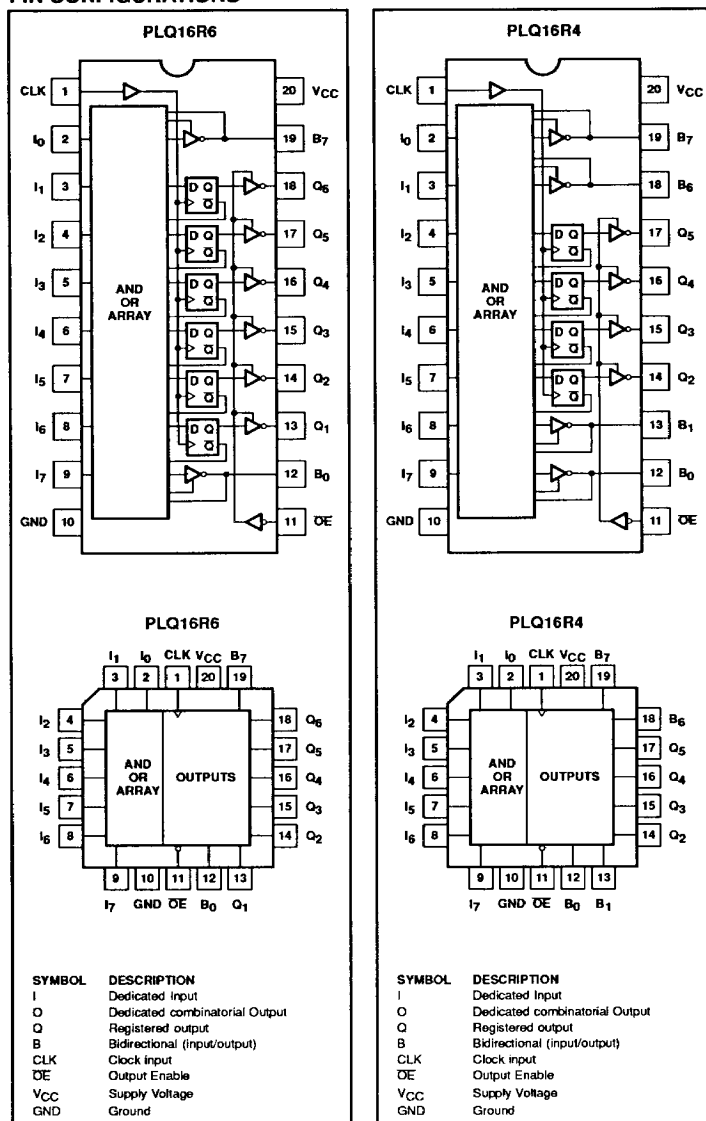
SYMBOL	DESCRIPTION
I	Dedicated Input
O	Dedicated combinational Output
Q	Registered output
B	Bidirectional (input/output)
CLK	Clock input
OE	Output Enable
V <sub>CC</sub>	Supply Voltage
GND	Ground

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# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### PIN CONFIGURATIONS

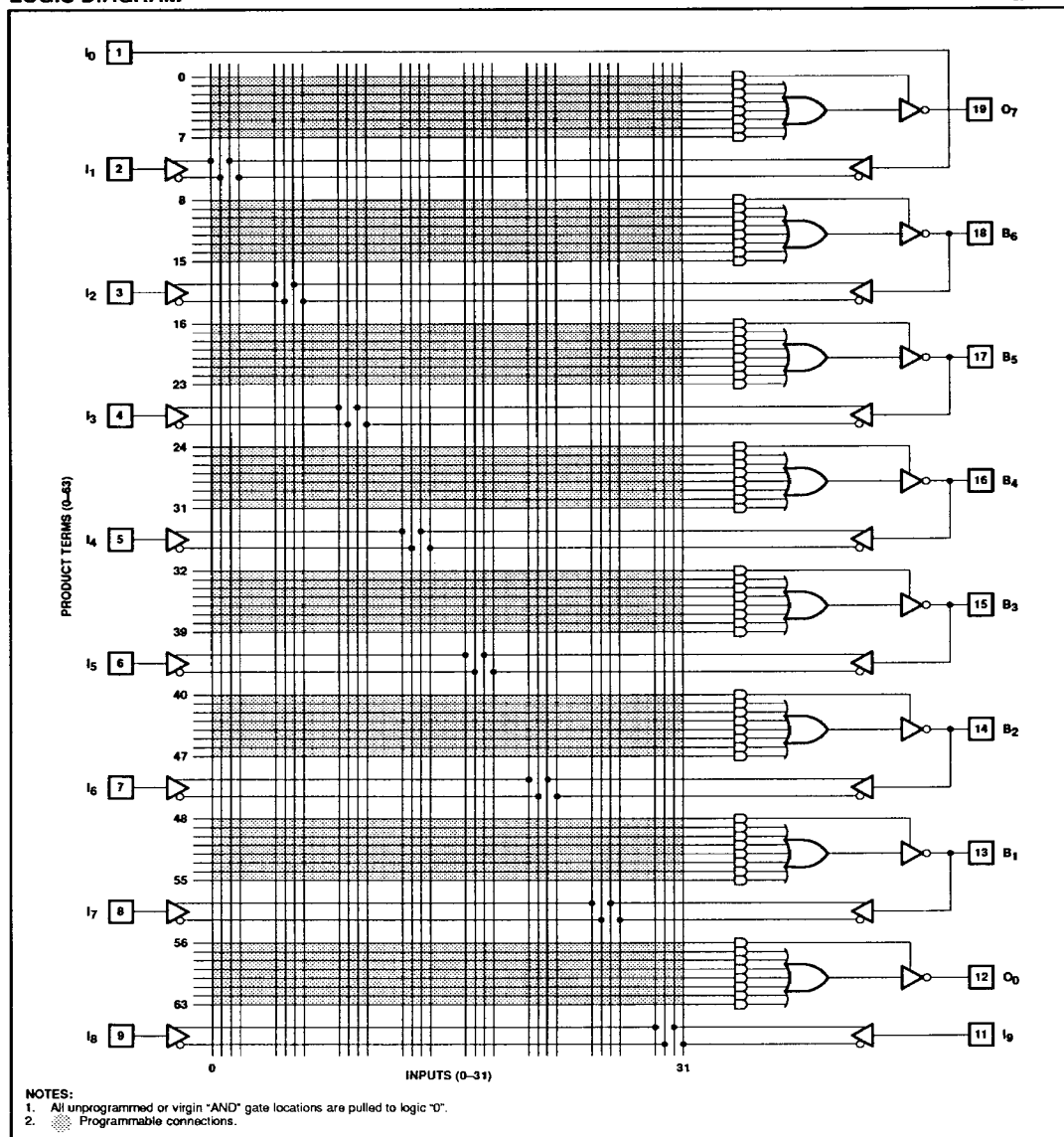


# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### LOGIC DIAGRAM

PLQ16L8

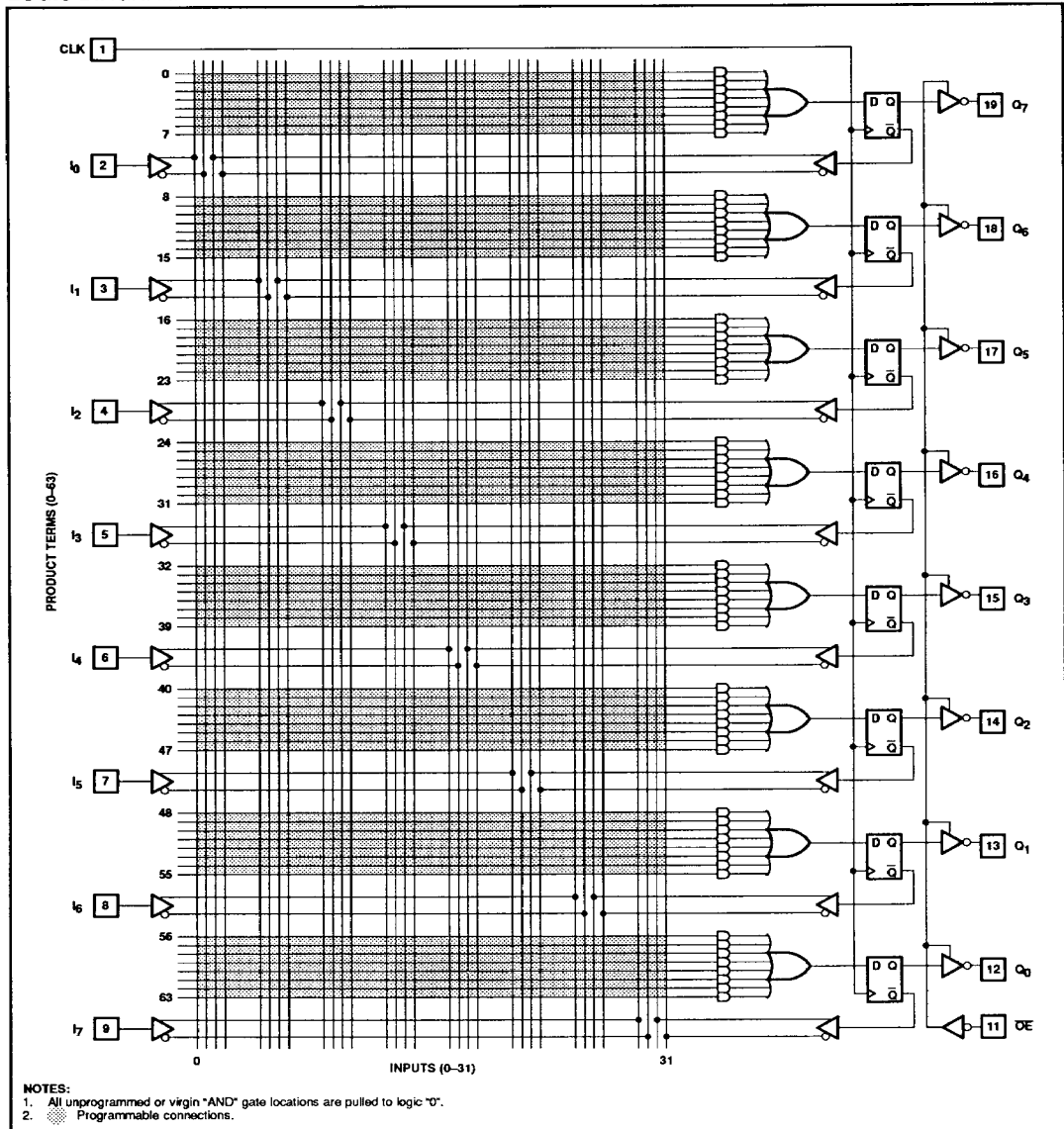


# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### LOGIC DIAGRAM

PLQ16R8

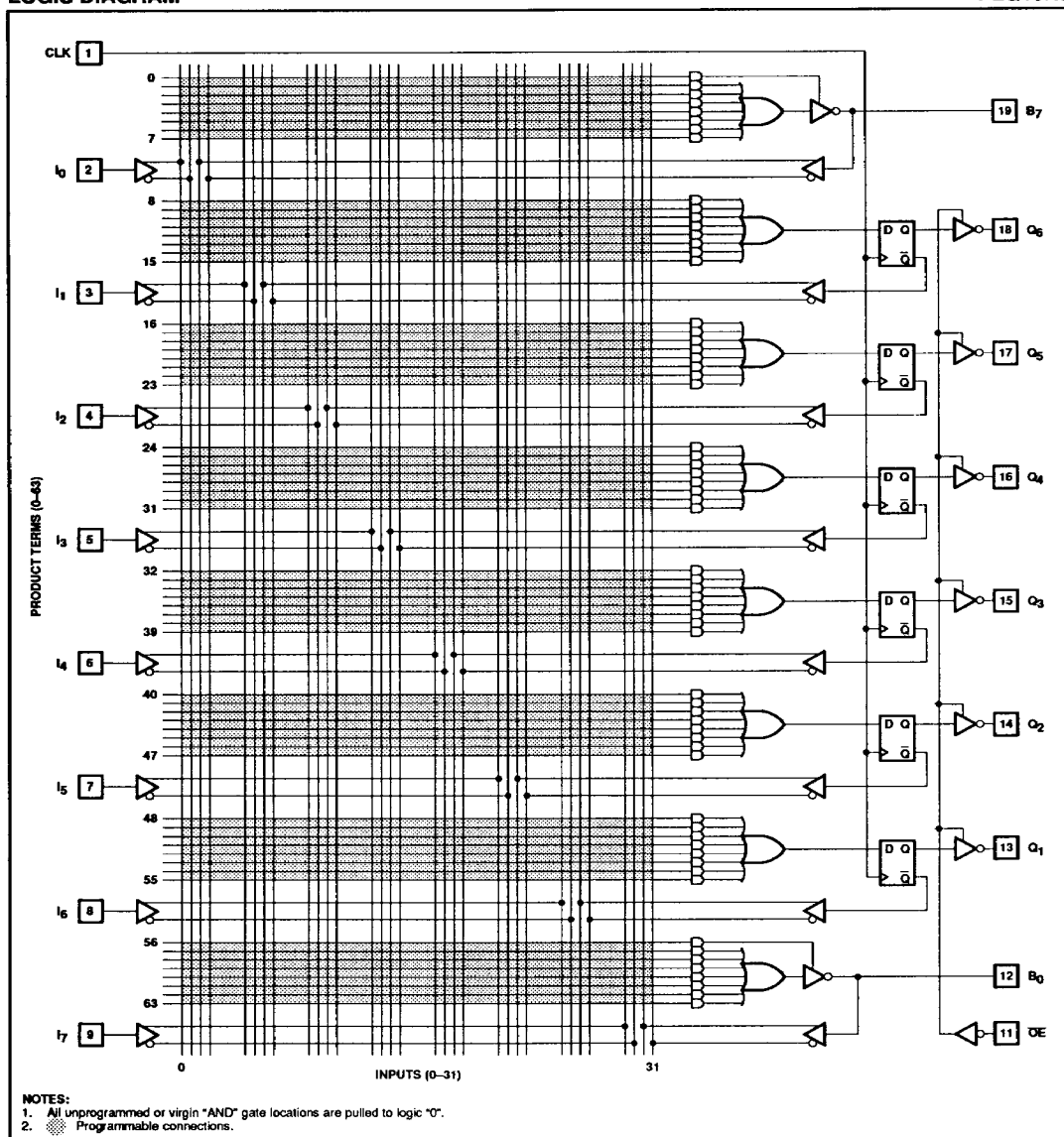


# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### LOGIC DIAGRAM

PLQ16R6

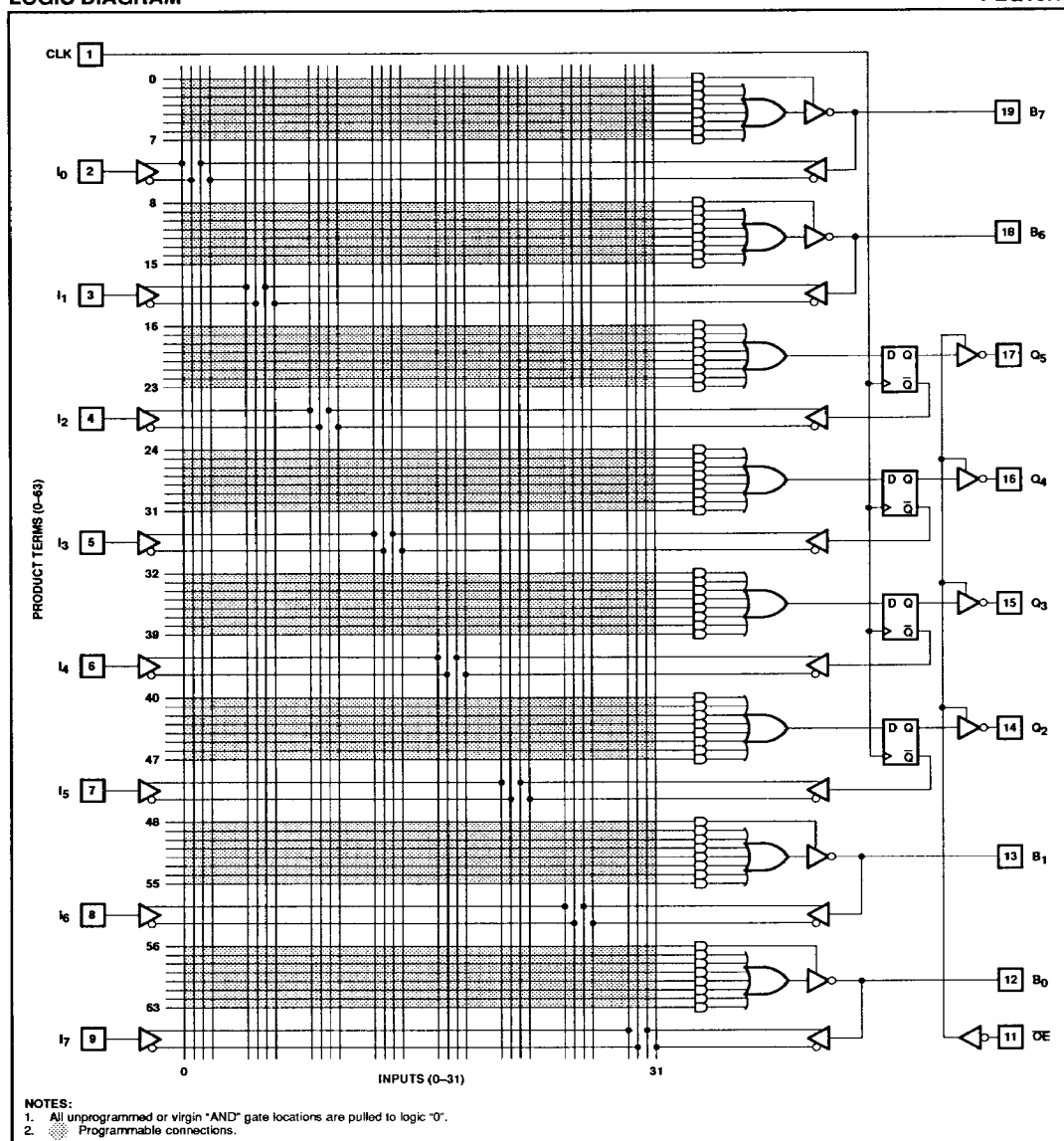


# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### LOGIC DIAGRAM

PLQ16R4



## PAL devices

### 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### FUNCTIONAL DESCRIPTIONS

The PLQ16XX series utilizes the familiar sum-of-products implementation consisting of a programmable AND array and a fixed OR array. These devices are capable of replacing an equivalent of four or more SSI/MSI integrated circuits to reduce package count and board area occupancy, consequently improving reliability and design cycle over Standard Cell or gate array options. By programming the security fuse, proprietary designs can be protected from duplication.

The PLQ16XX series consists of four PAL-type devices. Depending on the particular device type, there are a variable number of combinatorial and registered outputs available to the designer. The PLQ16L8 is a combinatorial part with 8 user configurable outputs (6 bidirectional), while the other three devices, PLQ16R8, PLQ16R6, PLQ16R4, have respectively 8, 6, and 4 output registers.

### 3-State Outputs

The PLQ16XX series devices also feature 3-State output buffers on each output pin which can be programmed for individual control of all outputs. The registered outputs (On) are controlled by an external input (/OE), and the combinatorial outputs (On, Bn) use a product term to control the enable function.

### Programmable Bidirectional Pins

The PLQ16XX products feature variable Input/Output ratios. In addition to 8 dedicated inputs, each combinatorial output pin of the registered devices can be individually programmed as an input or output. The PLQ16L8 provides 10 dedicated inputs and 6 Bidirectional I/O lines that can be individually configured as inputs or outputs.

### Output Registers

The PLQ16R8 has 8 output registers, the 16R6 has 6, and the 16R4 has 4. Each output register is a D-type flip-flop which is loaded on the Low-to-High transition of the clock input. These output registers are capable of feeding the outputs of the registers back into the array to facilitate design of synchronous state machines.

### Power-up Reset

By resetting all flip-flops to a logic Low, as the power is turned on, the PLQ16R8, R6, R4 enhance state machine design and initialization capability.

### Register Preload

Preload function allows the register to be loaded from the output pins. This feature allows functional testing of sequential patterns by loading output states.

### Power-up 3-State

All outputs will be disabled when  $V_{CC}$  is  $3.0V \pm 20\%$  (25°C). This special feature keeps outputs 3-States during power-up. Only when  $V_{CC}$  reaches its normal operating range will device function normally.

### Software Support

Like other Programmable Logic Devices from Signetics, the PLQ16XX series are supported by SLICE, the PC-based software development tool from Signetics. The PLQ16XX family of devices are also supported by standard CAD tools for PAL devices, including ABEL and CUPL.

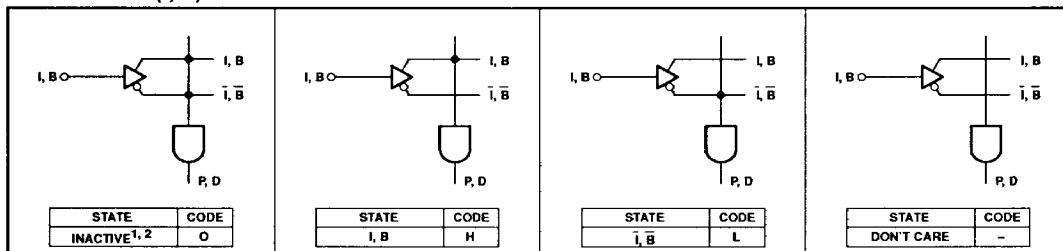
SLICE is available free of charge to qualified users.

### Logic Programming

The PLQ16XX series is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics SLICE and SNAP design software packages. ABEL™ CUPL™ and PALASM® 90 design software packages also support the PLQ16XX architecture.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

### AND ARRAY – (I, B)



### VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All  $P_n$  terms are disabled.
2. All  $P_n$  terms are active on all outputs.

ABEL is a trademark of Data I/O Corp.  
CUPL is a trademark of Logical Devices, Inc.  
PALASM is a registered trademark of AMD Corp.



**PAL devices**  
**16L8, 16R8, 16R6, 16R4**

**PLQ16R8-5 SERIES**

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	-0.5	+7.0	V <sub>DC</sub>
V <sub>IN</sub>	Input voltage	-1.2	+7.0	V <sub>DC</sub>
V <sub>OUT</sub>	Output voltage		+5.5	V <sub>DC</sub>
I <sub>IN</sub>	Input currents	-30	+30	mA
I <sub>OUT</sub>	Output currents		+100	mA
T <sub>stg</sub>	Storage temperature range	-65	+150	°C

**NOTE:**

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

**THERMAL RATINGS**

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

**OPERATING RANGES**

SYMBOL	PARAMETER	RATINGS		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	+4.75	+5.25	V <sub>DC</sub>
T <sub>amb</sub>	Operating free-air temperature	0	+75	°C

# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}, 4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
Input voltage <sup>2</sup>						
V <sub>IL</sub>	Low	V <sub>CC</sub> = MIN	2.0		0.8	V
V <sub>IH</sub>	High	V <sub>CC</sub> = MAX			V	
V <sub>IC</sub>	Clamp	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA			V	
Output voltage						
V <sub>OL</sub>	Low	V <sub>CC</sub> = MIN, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>OL</sub> = 24mA	2.4		0.5	V
V <sub>OH</sub>	High	I <sub>OH</sub> = -3.2 mA			V	
Input current						
I <sub>IL</sub>	Low <sup>3</sup>	V <sub>CC</sub> = MAX V <sub>IN</sub> = 0.40V			-250	μA
I <sub>IH</sub>	High <sup>3</sup>	V <sub>IN</sub> = 2.7V			25	μA
I <sub>I</sub>	Maximum input current	V <sub>IN</sub> = 5.5V, V <sub>CC</sub> = MAX			100	μA
Output current						
I <sub>OZH</sub>	Output leakage	V <sub>CC</sub> = MAX V <sub>OUT</sub> = 2.7V	-30		100	μA
I <sub>OZL</sub>	Output leakage	V <sub>OUT</sub> = 0.4V			-100	μA
I <sub>OS</sub>	Short circuit <sup>4, 5</sup>	V <sub>OUT</sub> = 0.5V			-130	mA
I <sub>CC</sub>	V <sub>CC</sub> supply current	V <sub>CC</sub> = MAX		160	180	mA
Capacitance <sup>6</sup>						
C <sub>IN</sub>	Input	V <sub>CC</sub> = 5V V <sub>OUT</sub> = 2.0V		8		pF
C <sub>B</sub>	I/O (B)	V <sub>OUT</sub> = 2V, f = 1MHz		8		pF

#### NOTES:

1. All typical values are at  $V_{\text{CC}} = 5\text{V}, T_{\text{amb}} = +25^{\circ}\text{C}$ .
2. All voltage values are with respect to network ground terminal.
3. Leakage current for bidirectional pins is the worst case of  $I_{\text{IL}}$  and  $I_{\text{OZL}}$  or  $I_{\text{IH}}$  and  $I_{\text{OZH}}$ .
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. These parameters are not 100% tested but periodically sampled.

# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### AC ELECTRICAL CHARACTERISTICS

 $R_1 = 200\Omega$ ,  $R_2 = 390\Omega$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$ 

SYMBOL	PARAMETER	FROM	TO	LIMITS		UNIT
				MIN <sup>1</sup>	MAX	
Pulse Width						
t <sub>CKH</sub>	Clock High	CLK+	CLK–	3.0		ns
t <sub>CKL</sub>	Clock Low	CLK–	CLK+	3.0		ns
t <sub>CKP</sub>	Period	CLK+	CLK+	6.0		ns
Setup & Hold time						
t <sub>IS</sub>	Input	Input or feedback	CLK+	4.0		ns
t <sub>IH</sub>	Input	CLK+	Input or feedback	0		ns
Propagation delay						
t <sub>CKO</sub>	Clock	CLK±	Q±		4.5	ns
t <sub>CKF</sub>	Clock <sup>3</sup>	CLK±	Q		2.5	ns
t <sub>PD</sub>	Output (16L8, R6, R4) <sup>2</sup>	I, B	Output		5.0	ns
t <sub>OE1</sub>	Output enable <sup>4</sup>	OE	Output enable		6.0	ns
t <sub>OE2</sub>	Output enable <sup>4,5</sup>	I	Output enable		8.0	ns
t <sub>OD1</sub>	Output disable <sup>4</sup>	OE	Output disable		6.0	ns
t <sub>OD2</sub>	Output disable <sup>4,5</sup>	I	Output disable		8.0	ns
t <sub>SKW</sub>	Output	Q	Q		1.0	ns
t <sub>PPR</sub>	Power-Up Reset	V <sub>CC</sub> +	Q+		8.0	ns
Frequency (16R8, R6, R4)						
f <sub>MAX</sub>	No feedback 1/ (t <sub>CKL</sub> + t <sub>CKH</sub> ) <sup>6</sup>				167	MHz
	Internal feedback 1/ (t <sub>IS</sub> + t <sub>CKF</sub> ) <sup>6</sup>				154	MHz
	External feedback 1/ (t <sub>IS</sub> + t <sub>CKO</sub> ) <sup>6</sup>				118	MHz

\* For definitions of the terms, please refer to the Timing/Frequency Definitions tables.

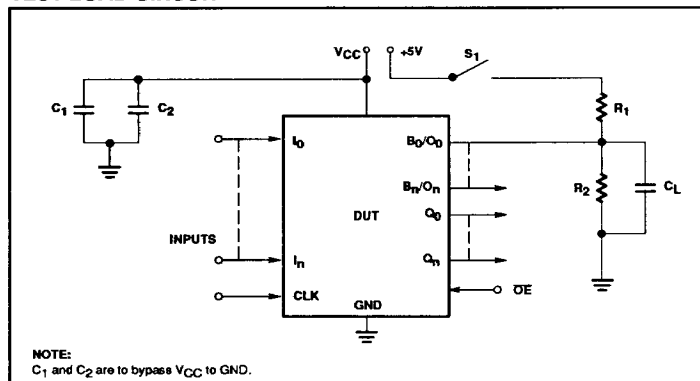
#### NOTES:

- CL = 0pF while measuring minimum output delays.
- $t_{\text{PD}}$  test conditions:  $C_L = 50\text{pF}$  (with jig and scope capacitance),  $V_{\text{IH}} = 3\text{V}$ ,  $V_{\text{IL}} = 0\text{V}$ ,  $V_{\text{OH}} = V_{\text{OL}} = 1.5\text{V}$ .
- $t_{\text{CKF}}$  was calculated from measured Internal  $f_{\text{MAX}}$ .
- For 3-State output; output enable times are tested with  $C_L = 50\text{pF}$  to the 1.5V level, and  $S_1$  is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with  $C_L = 5\text{pF}$ . High-to-High impedance tests are made to an output voltage of  $V_T = (V_{\text{OH}} - 0.5\text{V})$  with  $S_1$  open, and Low-to-High impedance tests are made to the  $V_T = (V_{\text{OL}} + 0.5\text{V})$  level with  $S_1$  closed.
- Same function as  $t_{\text{OE1}}$  and  $t_{\text{OD1}}$ , with the difference of using product term control.
- Not 100% tested, but calculated at initial characterization and at any time a modification in design takes place which may affect the frequency.

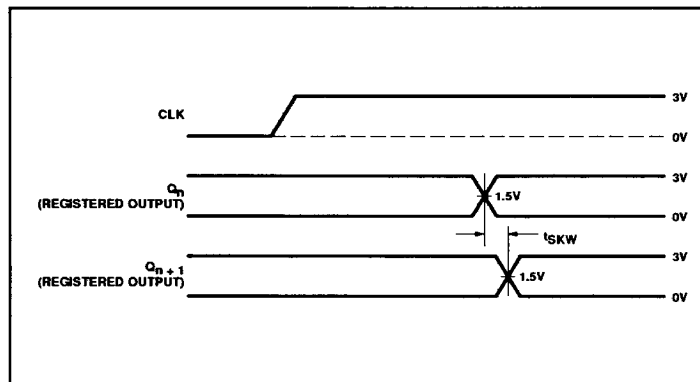
# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

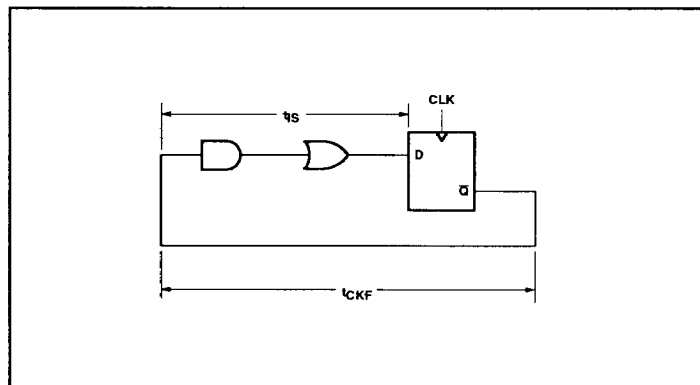
### TEST LOAD CIRCUIT



### OUTPUT REGISTER SKEW



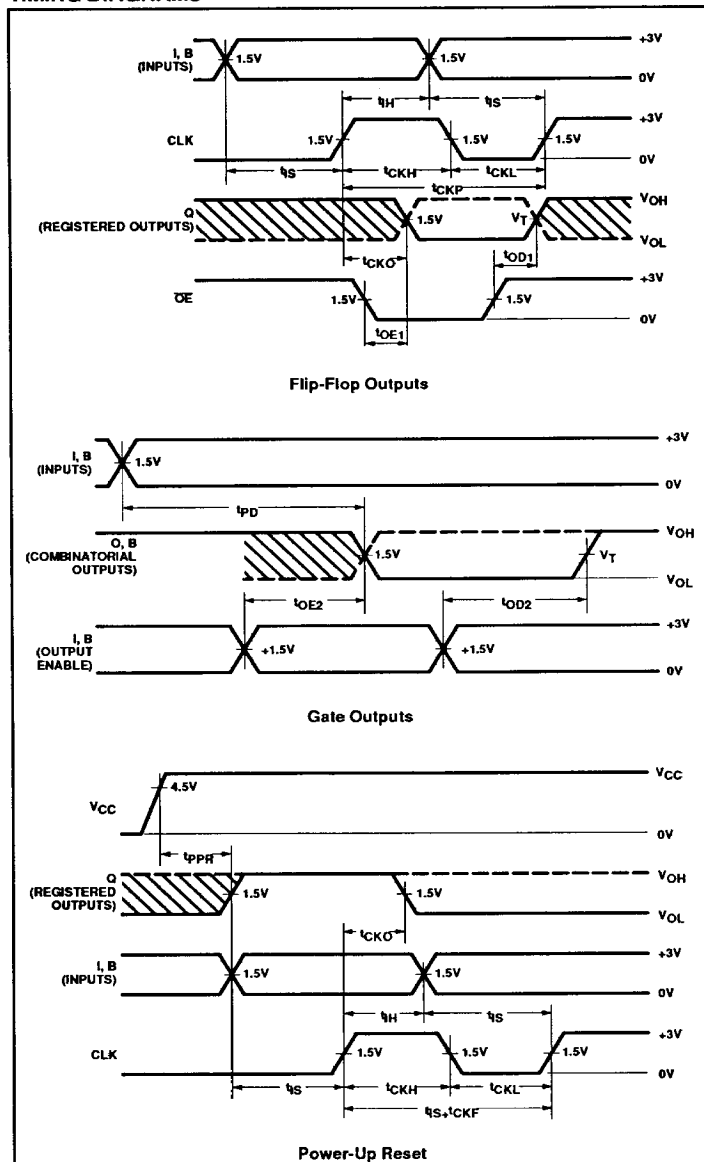
### CLOCK TO FEEDBACK PATH



# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### TIMING DIAGRAMS<sup>1, 2</sup>



#### NOTES:

- Input pulse amplitude is 0V to 3V.
- Input rise and fall times are 2.0ns typical.

### TIMING DEFINITIONS

SYMBOL	PARAMETER
$t_{KH}$	Width of input clock pulse.
$t_{CKL}$	Interval between clock pulses.
$t_{CKP}$	Clock period.
$t_{is}$	Required delay between beginning of valid input and positive transition of clock.
$t_{ih}$	Required delay between positive transition of clock and end of valid input data.
$t_{CKF}$	Delay between positive transition of clock and when internal Q output of flip-flop becomes valid.
$t_{CKO}$	Delay between positive transition of clock and when outputs become valid (with OE Low).
$t_{OE1}$	Delay between beginning of Output Enable Low and when outputs become valid.
$t_{OD1}$	Delay between beginning of Output Enable High and when outputs are in the Off-State.
$t_{OE2}$	Delay between predefined Output Enable High, and when combinational outputs become valid.
$t_{OD2}$	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
$t_{PPR}$	Delay between V <sub>CC</sub> (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
$t_{PD}$	Propagation delay between combinational inputs and outputs.
$t_D$	Delay between each input change.

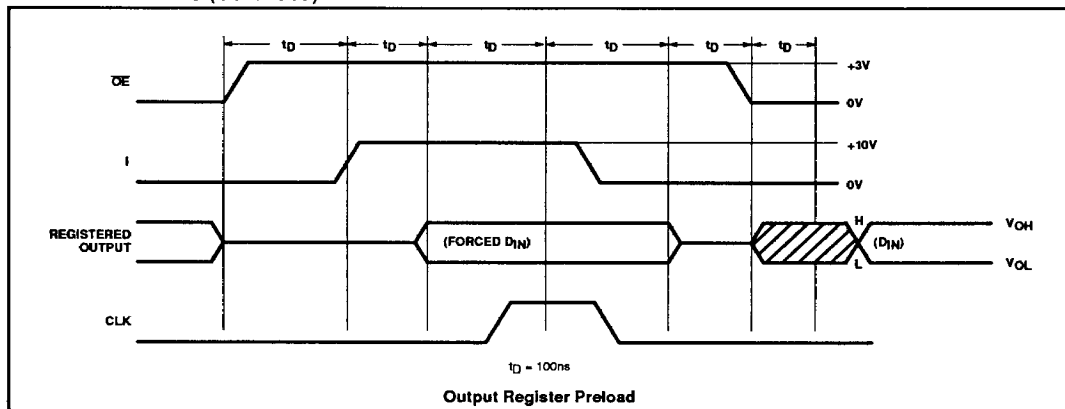
### FREQUENCY DEFINITIONS

$f_{MAX}$	<b>No feedback:</b> Determined by the minimum clock period, $1/(t_{CKL} + t_{CKH})$ . <b>Internal feedback:</b> Determined by the internal delay from flip-flop outputs through the internal feedback and array to the flip-flop inputs, $1/(t_{is} + t_{CKF})$ . <b>External feedback:</b> Determined by clock-to-output delay and input setup time, $1/(t_{is} + t_{CKO})$ .
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**PAL devices**  
16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### TIMING DIAGRAMS (Continued)



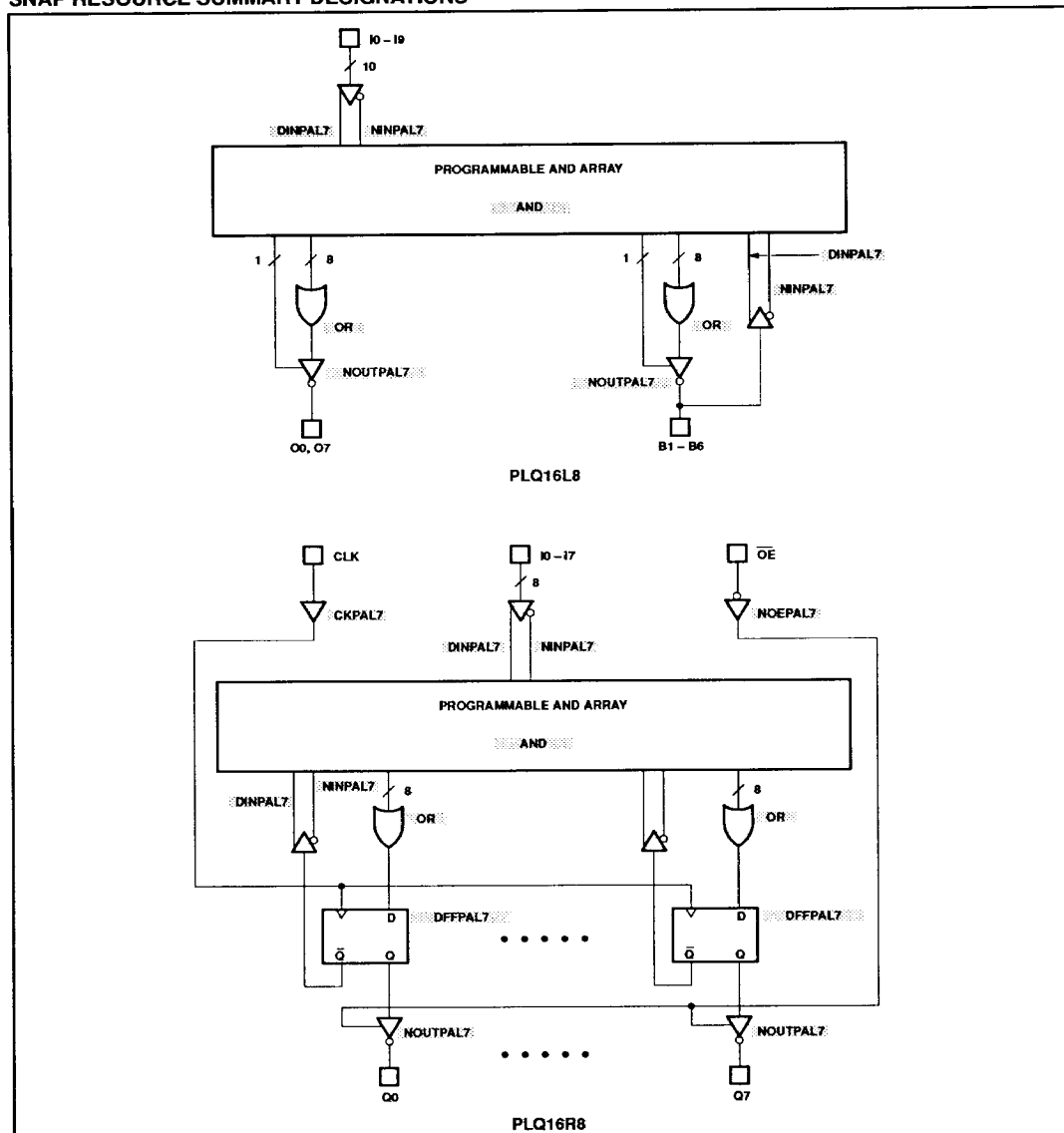
## PROGRAMMING/SOFTWARE

Refer to Section 8 (*Development Software*) and Section 9 (*Third-Party Programmer/Software Support*) of this data handbook for additional information.

# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### SNAP RESOURCE SUMMARY DESIGNATIONS



# PAL devices 16L8, 16R8, 16R6, 16R4

## PLQ16R8-5 SERIES

### SNAP RESOURCE SUMMARY DESIGNATIONS (Continued)

