# DATA SHEET


## PCA24S08

1024 × 8-bit CMOS EEPROM
with access protection

Product data

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# 1024 × 8-bit CMOS EEPROM with access protection PCA24S08

## DESCRIPTION

The PCA24S08 provides 8192 bits of serial electrically erasable and programmable Read-only memory (EEPROM) organized as 1024 words of 8 bits each. Data bytes are received and transmitted via the serial $I^2C$-bus.

Access permissions limiting reads or writes are set via the $I^2C$-bus to isolate blocks of memory from improper access.

The PCA24S08 is intended to be pin compatible with standard 24C08 serial EEPROM devices except for pins 1, 2, and 3, which are address pins in the standard part. Other exceptions to the PCA24C08 serial EEPROM datasheet are noted the “Serial EEPROM Exception” section later in this document.

All bits are sent to or read from the device, most significant bit first, in a manner consistent with the 24C08 serial EEPROM. The bit fields in this document are correspondingly listed with the MSB on the left and the LSB on the right.

The EEPROM memory is broken up into 8 blocks of 1 k bits (128 bytes) each. Within each block, the memory is physically organized in to 8 pages of 128 bits (16 bytes) each. In addition to these 8 k bits, there are two more 128-bit pages that are used to store the access protection and ID information. There are a total of 8448 bits of EEPROM memory available in the PCA24S08.

Access protection (both read and write) is organized on a block basis for blocks 1 through 7 and on a page and a block basis for block 0. Protection information for these blocks and pages is stored in one of the additional pages of EEPROM memory that is addressed separately from the main data storage array. See “Access Protection” for more details.

The ID value (see “ID Configuration”) is located in the ID page of the EEPROM, the second of the additional 16 byte pages.

Writes from the serial interface may include from one to 16 bytes at a time, depending on the protocol followed by the bus master. All page accesses must be properly aligned to the internal EEPROM page.

The EEPROM memory offers an endurance of 100,000 write cycles per byte, with 10 year data retention. Writes to the EEPROM take less than 5 ms to complete.

After manufacturing, all EEPROM bits will be set to a value of ‘1’.

## FEATURES

- Non-volatile storage of 8 kbits organized as 8 blocks of 128 bytes each
- $I^2C$ interface logic
- Compatible with 24C08 Serial EEPROM, and alternate source of Atmel AT24RF08C without the RF interface
- Write operation:
  - Byte write mode
  - 16-byte page write mode
- Read operation:
  - Sequential read
  - Random read
- Programmable access protection to limit reads and writes
- Lock/unlock function
- Write protect feature protecting the full memory array against write operations
- Self timed write cycle
- Internal power-on reset
- High reliability:
  - Ten years non-volatile data retention time
  - 100,000 write cycle endurance
- Low power CMOS technology
- Operating power supply voltage range of 2.5 V to 3.6 V
- 0 to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8

## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE | TOPSIDE MARK | DRAWING NUMBER |
|---|---|---|---|---|
| 8-pin plastic SO | –40 °C to +85 °C | PCA24S08D | P24S08 | SOT96-1 |
| 8-pin plastic TSSOP | –40 °C to +85 °C | PCA24S08DP | PS08 | SOT505-1 |

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

## PIN CONFIGURATION

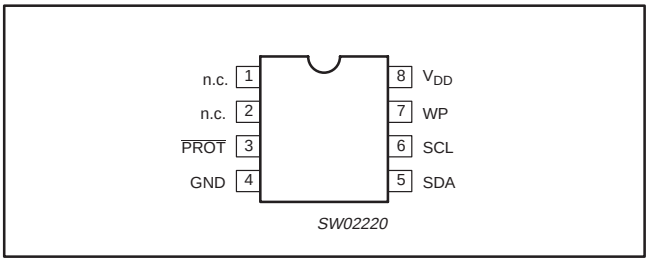



**Figure 1. 8 pin configuration**

## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2 | n.c. | not connected |
| 3 | $\overline{\text{PROT}}$ | Active-LOW protect reset input |
| 4 | GND | Ground |
| 5 | SDA | Serial data open drain I/O |
| 6 | SCL | Serial clock open drain input |
| 7 | WP | Active-HIGH write protect input |
| 8 | $V_{DD}$ | Supply voltage |

## BLOCK DIAGRAM

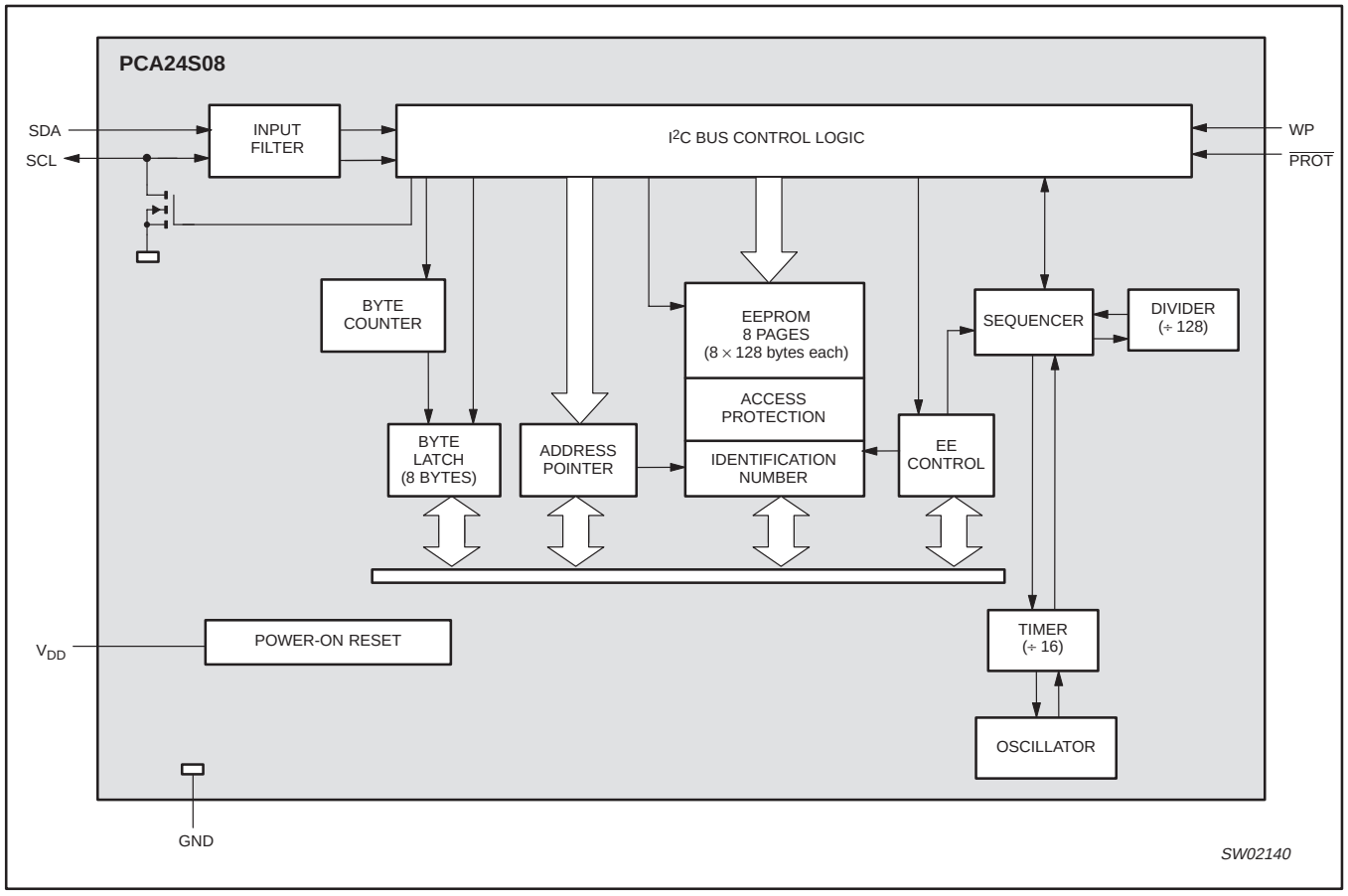



**Figure 2. Block diagram**

## DEVICE ADDRESSING

Following a START condition, the bus master must output the address of the slave it is accessing. The address of the PCA24S08 is shown in Figure 3.

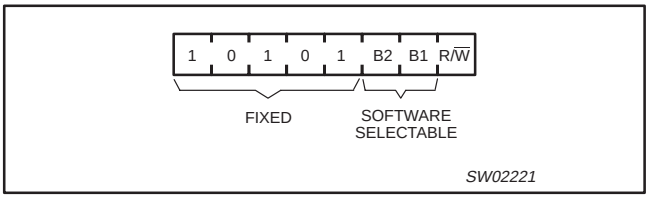



**Figure 3. Slave address**

The last bit of the slave address defines the operation to be performed. When set to logic 1, a read operation is selected, while logic 0 selects a write operation. Bits B2 and B1 in the slave address represent the 2 most significant bits of the word to be addressed. The third device address bit in the $I^2C$ protocol that is usually matched to $A_2$ (pin 3) on a standard 24C08 serial EEPROM is internally connected HIGH, so device addresses A8h through AFh (hex) are used to access the memory on the chip.

## WRITE OPERATIONS

Write operations on the device can be performed only when WP is held LOW. When WP pin is held HIGH, content of the full memory is protected (Block 0 to Block 7, APP Registers, ID Page), and no write operation is allowed.

**Byte/word write:** Write command may be used to set the address for a subsequent Read command. For a write operation, the PCA24S08 requires a second address field. The address field associated with the two software selectable bits in the slave address is a word address providing access to the 1024 bytes of memory, as shown in Figure 4. Upon receipt of the word address, the PCA24S08 responds with an acknowledge and awaits the next eight bits of data, again responding with an acknowledge. Word address is automatically incremented. Figure 5 shows how the memory array is addressed when the slave address byte and address field byte are sent. The master terminates the transfer by generating a STOP condition. After this STOP condition, the Erase/Write (E/W) cycle starts and the $I^2C$-bus is free for another transmission. Up to 16 bytes of data can be written in the slave writing sequence (E/W cycle).

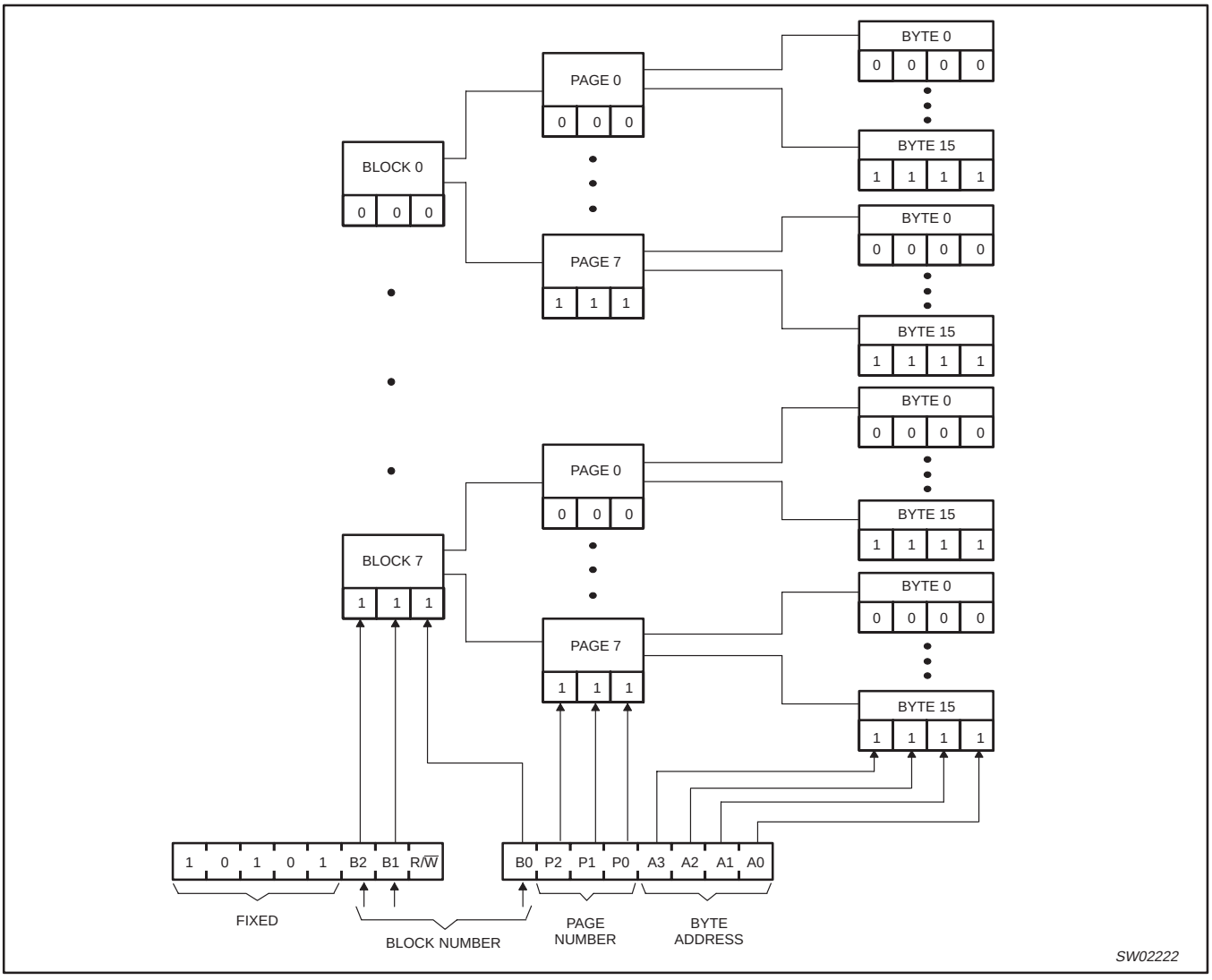



**Figure 4. Memory addressing**

The general command encoding used by the serial port for EEPROM accesses is shown below in Device Access Examples, where $B_{2-0}$ is the block number, $P_{2-0}$ is the page number within the block and $A_{3-0}$ is the byte address within the page. Bits denoted as "x" are ignored by the device.

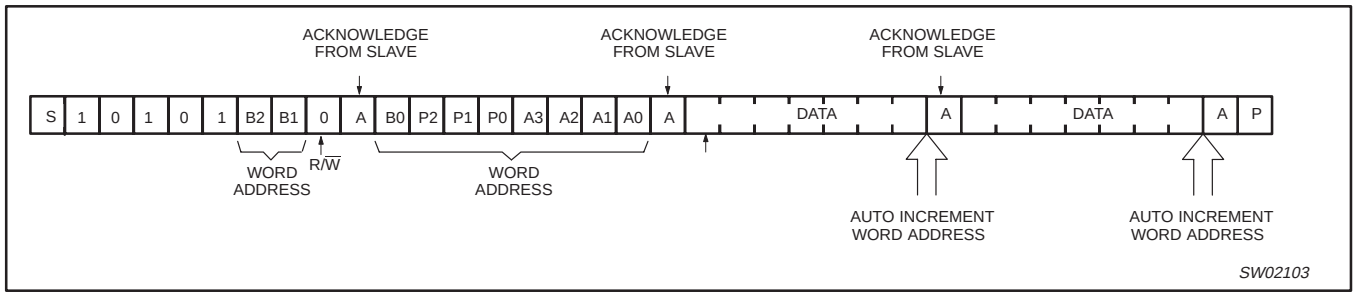



**Figure 5. Auto-increment memory word address; two byte write**

**Page write:** The PCA24S08 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte write operation. The master can transit 16 data bytes within one transmission. After receipt of each byte, the PCA24S08 will respond with an acknowledge. The typical E/W time in this mode is 5 ms.

After the receipt of each data byte, the four low-order bits of the word address are internally incremented. The six high-order bits of the address remain unchanged. The slave acknowledges the reception of each data byte with an ACK. The $I^2C$-bus data transfer is terminated by the master after the 16$^{th}$ byte of data with a STOP condition. After a write to the last byte in a page, the internal address is wrapped around to point to the beginning of that page. If the master transmits more than 16 bytes prior to generating the STOP condition, no acknowledge will be given on the 17$^{th}$ (and following) data bytes and the whole transmission will be ignored and no programming will be done. As in the byte write operation, all inputs are disabled until completion of the internal write cycles.

After this STOP condition, the E/W cycle starts and the $I^2C$-bus is free for another transmission.

During the E/W cycle the slave receiver does not acknowledge if addressed via the $I^2C$-bus.

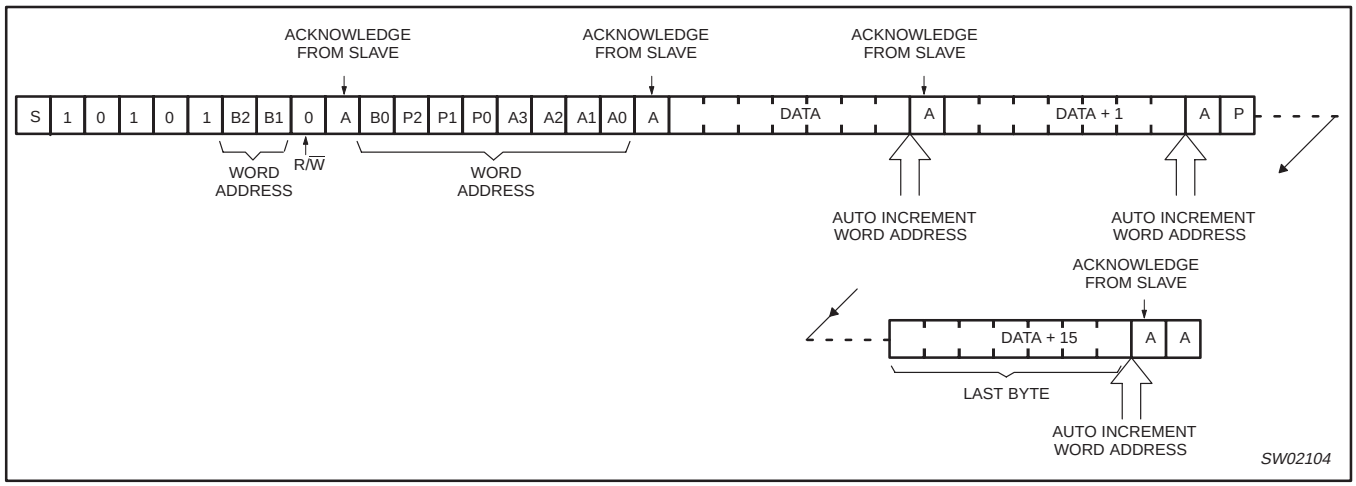



**Figure 6. Page write operation: 16 bytes**

## READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the LSB of the slave address is set to logic 1.

The lower 7 bits of the word address are incremented after each transmission of a data byte during a read. The three MSBs of the word address are not changed when the word counter overflows. Thus, the word address overflows from 127 to 0, and from 255 to 128. After the read of the last byte within a block, the internal serial address wraps around to point at the beginning of that block.

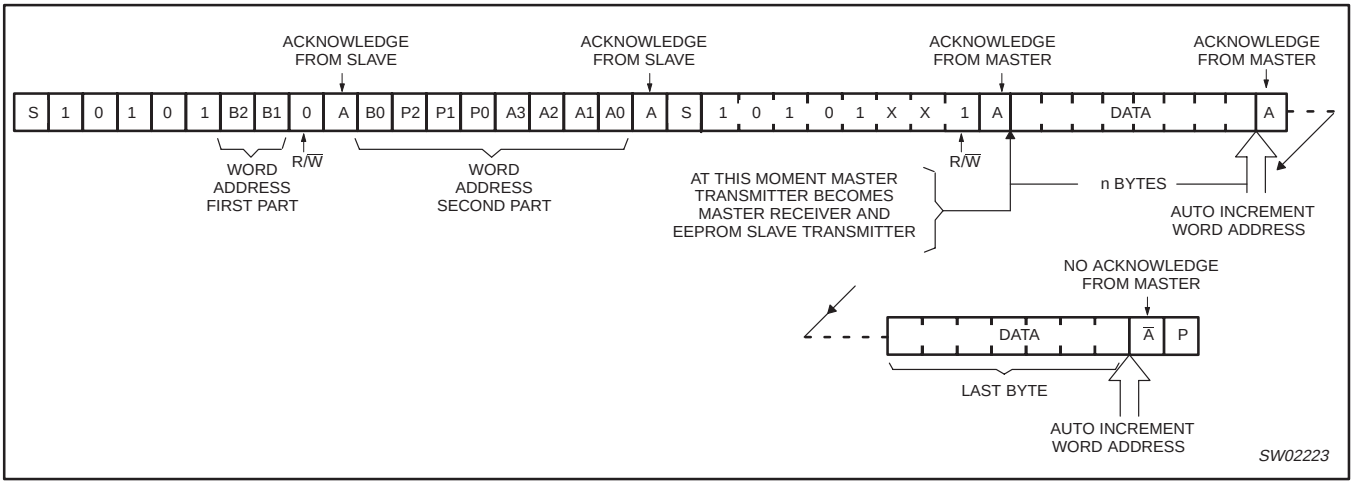



**Figure 7. Master reads PCA24S08 slave after setting word address (write word address: read data); sequential read**

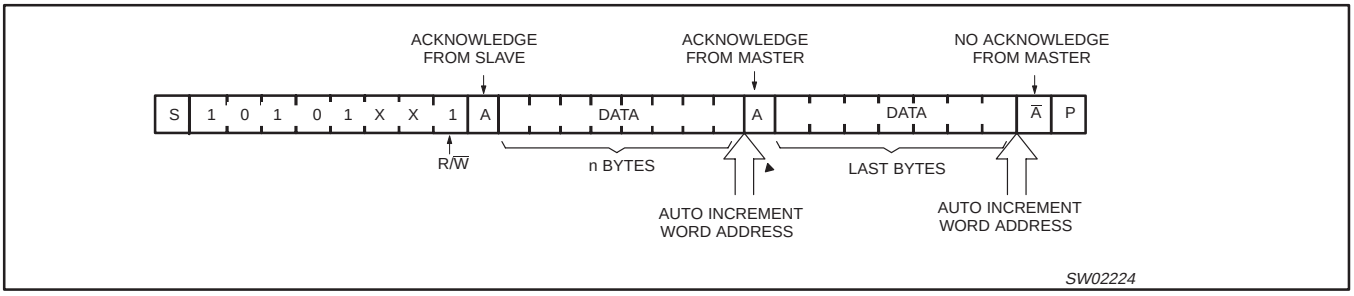



**Figure 8. Master read PCA24S08 immediately after first byte (read mode); current address read**

## ACCESS PROTECTION

Write operation on the Access protection registers can be performed when WP pin LOW. If the WP pin is HIGH all write operations are prohibited from the serial port, although write commands may be used to set the address for a subsequent read command.

All access protection bits are stored on a separate page of the EEPROM that is not accesses using the normal commands of a PCA24C08 memory. See the “Access Protection Page” section for more detail on this information.

## RFID ACCESS FIELDS (RF)

Even though the PCA24S08 does not have the RFID capability, RFID access fields (RF) can be stored in order to keep existing software compatibility. The fields are stored in the EEPROM and organized as follows:

| MSB | LSB | FUNCTION |
|---|---|---|
| 0 | 0 | No accesses permitted from RFID port |
| 0 | 1 | No accesses permitted from RFID port |
| 1 | 0 | Read only from RFID port |
| 1 | 1 | No restrictions for RFID accesses |

## PROTECTION BITS (PB)

The protection bits fields in the Access Protection Page determine what type of accesses will be permitted via the serial port for each of the blocks on the chip. If an illegal access is attempted, the command will be NACK’ed. The MSB, if clear, prohibits all access to the block, and the LSB if clear prohibits writes. The fields are stored in the EEPROM and are organized as follows:

| MSB | LSB | FUNCTION |
|---|---|---|
| 0 | 0 | No accesses permitted in the block |
| 0 | 1 | No accesses permitted in the block |
| 1 | 0 | Read only, writes cause a NACK |
| 1 | 1 | Read/write —No access constraints for data within this block |

Accessed within the Access Protection Page is an individual CMOS Sticky Bit (SB) for each of the 8 blocks on the device. When the value of the sticky bit is ‘0’, the Protection Bits (PB) for the corresponding block may not be changed via the software. These bits are all set to one when power is initially applied or when the $\overline{\text{PROT}}$ pin is LOW. These sticky bits may be written only to a ‘0’ via the serial interface using the standard serial write operations. Reading the sticky bits does not affect their state.

Because permissions are set individually for each of the blocks, all reads via serial port will only read bytes within the block that was specified when the current address was latched in the device (with a write command). The block address bits ($B_2$ or $B_1$) that are sent with the write command are ignored on a read command.

When a sticky bit is cleared (programmed at 0), the byte containing the sticky bit cannot be changed anymore. If a write operation to this byte is attempted, it will be normally acknowledged but no change will happen in the byte value. The device does not go to an E/W cycle and can be accessed immediately.

If a block is protected and only read operation is allowed (the corresponding APP register has its PB bits programmed to 10), a write operation to this block is not acknowledged (Slave Address and Register pointer only are acknowledged). The device does not go to an E/W cycle and can be accessed immediately.

S – Addr+W – ACK – Reg Pointer – ACK – Data – NACK

This applies to:

- EEPROM Block 0 to Block 7, controlled by $PB_0$ to $PB_7$
- The last 7 bytes of the APP block (09H to 0FH) and the ID page (10H to 1FH) controlled by PBAP

If a block is protected and neither read operation nor write operation is allowed (the corresponding APP register has its PB bits programmed to 00 or 01), a write operation to this block is not acknowledged (Slave Address and Register pointer only are acknowledged).

S – Addr+W – ACK – Reg Pointer – ACK – Data – NACK

A read operation to this block is not allowed.

S – Addr+W – ACK – Reg Pointer – ACK – Sr – Addr+R – NACK

S – Addr+W – ACK – Reg Pointer – ACK – P – S – Addr+R – NACK

This applies to:

- EEPROM Block 0 to Block 7, controlled by $PB_0$ to $PB_7$
- The last 7 bytes of the APP block (09H to 0FH) and the ID page (10H to 1FH) controlled by PBAP

## BLOCK 0 WRITE PROTECTION BITS

The PCA24S08 provides a mechanism to divide block 0 into eight 128-bit (16 byte) pages that can be individually protected against writes. These eight write protection (WPN) bits are stored within a byte of the access protection page and are organized such that the LSB protects the first 128 bits and so on. If a bit in this byte is set to a one and the $PB_0$ field is set to 11, then writes are permitted on the page corresponding to the WPN bit. If the WPN bit is set to a 0 or the $PB_0$ is any value other than 11, then writes are not permitted in that page.

The Write Protection hierarchy for serial accesses is shown in Figure 6. In this drawing the bits within the boxes to the left of the arrows are the only thing that determine whether or not the bit in the box to the right of the arrow can be written. Read access control is not shown in this diagram. Addresses listed in this diagram are for the serial port assuming that the R/W bit in the command byte is set to ‘0’.

For example, when $SB_1$ is a 1, the $PB_1$ field can be written to any value by the system. When the $PB_1$ field is 11, Block 1 can be written to by the system. Note that the state of the $SB_1$ bit does not affect whether or not Block 1 can be written.

There is no individual page Write Protection for any other block other than block 0 within the device. Within the remaining blocks on the chip, access permissions are controlled on a block basis (BP bits) or full chip basis (WP pin) only.

## WRITE PROTECTION FLOW

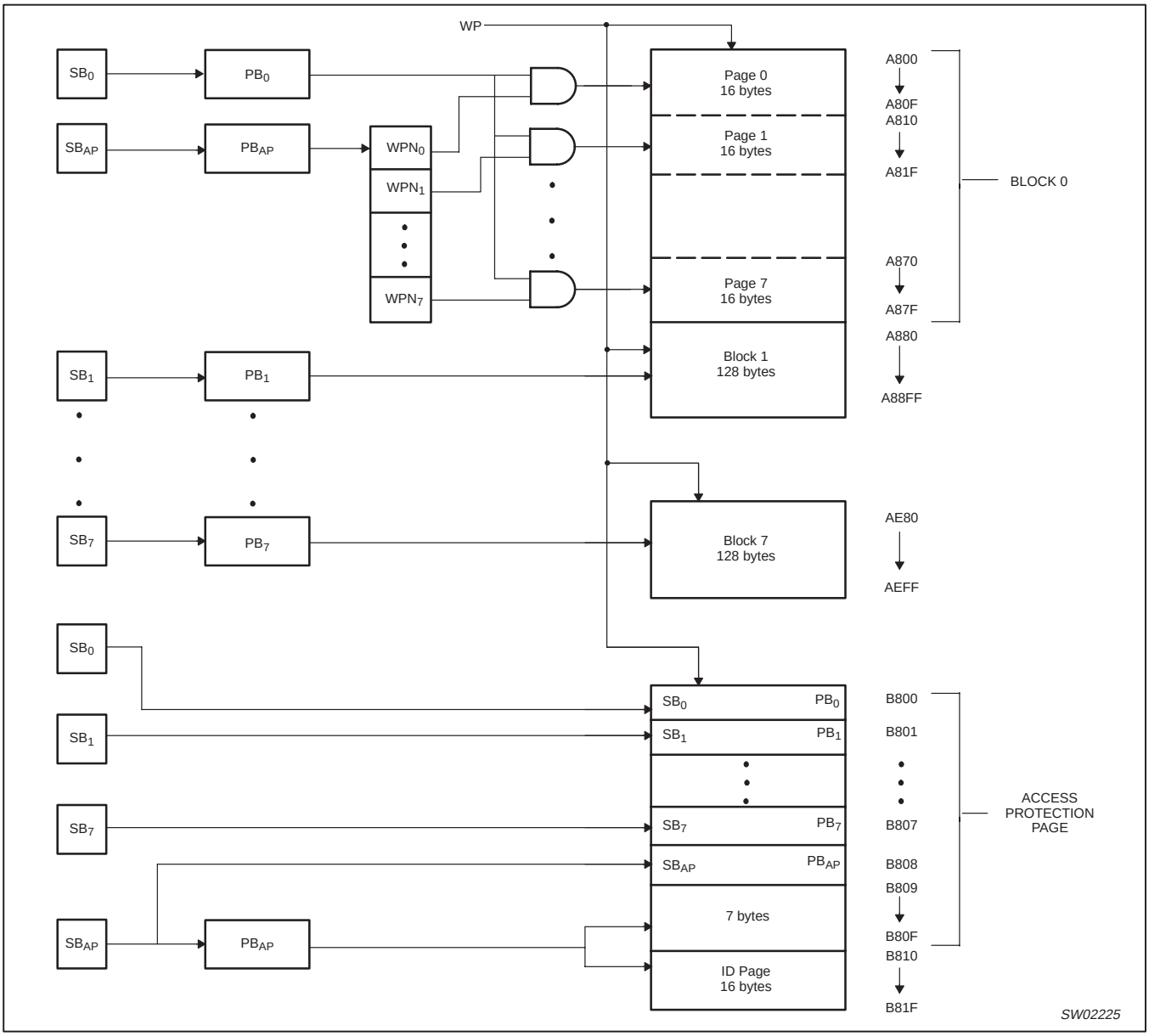



**Figure 9. Write protection example**

## ACCESS PROTECTION PAGE

The serial port may be used to read and write the Access Protection Page (APP) and ID Page using device access codes B8h and B9h instead of the normal value of A8h through AFh (hex) that are used to access the rest of the EEPROM memory. The second byte of write commands (the word address) should be in the range of 00h through 0Fh for the APP page and 10h through 1Fh for the ID page. This coding is shown in the Access Protection Page Examples section.

Reads and writes to these two pages may take place on a single byte basis only. Multi-byte operations will be NACK'ed.

As an example, the bit encoding for a single byte read and write command are shown in the Access Protection Page Examples section.

The PCA24S08 will acknowledge all device addresses of B8h or B9h. If the most significant three its of the word address are not all 0 (indicating an address outside the Access protection and ID pages), the chip will NACK the access.

Bytes 0 through 7 of the APP contain 8 identical set of access control fields (PBx and SBx) for each of the eight blocks of memory on the chip, which operate according to the table listed in the Access Protection section above. When the sticky bit in one of these bytes is set, that byte can be written by the system. Once a sticky bit is reset (written to zero) by the software, the byte containing it can no longer be modified by the software until the next power cycle. These bytes can always be read by the system.

Byte 8 contains another PB field ($PB_{AP}$) as bits 0 and 1 and an additional sticky bit ($SB_{AP}$) as bit 7. The value of the $PB_{AP}$ bits controls read and write access to the last 7 bytes (9–15) of the APP and all 16 bytes of the ID page according to the encoding listed in the "Access Protection" section above. The value of the $PB_{AP}$ bits can only be changed, a write from the serial port, when $SB_{AP}$ is HIGH. This byte can always be read by the system. Bit 0 through 6 of this byte are stored in EEPROM memory and do not change when the power is cycled or the $\overline{PROT}$ pin changes state.

Byte 9 contains the 8 block 0 write protection bits (WPN) for each page within block 0.

Byte 10 emulates a coil detection feature to keep compatibility with existing software controlling device.

Even though the PCA24S08 does not have the RFID capability of the AT24RF03C, it gives a "coil non detected" information when the detection feature is initiated.

The detection feature uses the Detection Enable bit (DE) and the Detect Coil bit (DC). At power-up, DE = 0 and DC = 1. Detection is enabled by setting DE bit at 1. Since no coil is detected, DC is then automatically reset and equal to 0.

DE is a Read/Write bit, DC is a Read Only bit. Attempt to write to this bit will be ignored.

Bit 0 in the same byte emulates a Tamper bit and is always equal to 0.

TAMPER is a Read Only bit. Attempt to write a '1' to this bit will be ignored.

Bytes 11 through 14 are currently reserved and should not be used by the system. Byte 14 may not be written by the device at any time.

Byte 11 to 13 are read/write bytes that are stored in the EEPROM.

Byte 14 is a read only byte and the returned value during a read operation is FFh. A write on it is acknowledged but the write will be ignored.

### Device Access Examples

**For Write Operations:**

1 0 1 1 1 0 0 0  0 0 0 $P_0$ $A_3$ $A_2$ $A_1$ $A_0$  $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$

$P_0$: used to distinguish between the APP and RFID pages
$P_0$ = 0: APP pages
$P_0$ = 1: RFID pages

**For Read Operations:**

1 0 1 1 1 0 0 1  $D_7$ $D_6$ $D_5$ $D_4$ $D_3$ $D_2$ $D_1$ $D_0$

Byte 15 contains device revision information stored in the EEPROM. It is set at the wafer production facility and cannot be changed in the field, so any write to this byte will be ignored but acknowledged. The value of this byte is 10h.

The memory map for the access protection page is shown in the APP Memory Map table. In this table, an X means that the value is a don't care upon writing and that it is undefined upon reading. The PB fields are all two bits wide, and the Device Revision field is 8 bits wide. All other fields are on bit wide.

With the exception of the 9 sticky bits (SB) the two coil detect bits (DE and DC), the tamper bit (TAMPER) and bytes 14 and 15, all bits within the Access Protection Page are stored in EEPROM memory. Their state does not change if power is removed or when the $\overline{PROT}$ pin is held LOW.

The following page of memory (accessed with $A_4$ = 1) emulate the ID field that would be transmitted by the device from the RFID port. Bytes within it are accessed with the address byte at B8h or B9h (write/read). Reading and writing to this page is permitted when $PB_{AP}$ is 11.

## APP MEMORY MAP

| ADDRESS | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|
| 0 | $SB_0$ | X | $RF_0$ | | X | X | $PB_0$ | |
| 1 | $SB_1$ | X | $RF_1$ | | X | X | $PB_1$ | |
| 2 | $SB_2$ | X | $RF_2$ | | X | X | $PB_2$ | |
| 3 | $SB_3$ | X | $RF_3$ | | X | X | $PB_3$ | |
| 4 | $SB_4$ | X | $RF_4$ | | X | X | $PB_4$ | |
| 5 | $SB_5$ | X | $RF_5$ | | X | X | $PB_5$ | |
| 6 | $SB_6$ | X | $RF_6$ | | X | X | $PB_6$ | |
| 7 | $SB_7$ | X | $RF_7$ | | X | X | $PB_7$ | |
| 8 | $SB_{AP}$ | X | X | X | X | X | $PB_{AP}$ | |
| 9 | WPN7 | WPN6 | WPN5 | WPN4 | WPN3 | WPN2 | WPN1 | WPN0 |
| 10 | DE | DC | X | X | X | X | X | TAMPER |
| 11 | Reserved R/W | | | | | | | |
| 12 | Reserved R/W | | | | | | | |
| 13 | Reserved R/W | | | | | | | |
| 14 | Reserved R only | | | | | | | |
| 15 | Device Revision | | | | | | | |

## $\overline{\text{PROT}}$ PIN

The $\overline{\text{PROT}}$ pin is used as a power good signal. When this pin is held LOW, the serial port is held in reset and all sticky bits are set to one. When HIGH, activity on the serial bus is permitted and sticky bits can be set to their values.

## SERIAL EEPROM EXCEPTIONS

In general, the two-wire serial interface on the PCA24S08 functions identically to the 24C08. The following exceptions exist, as noted elsewhere in this document.

- Pins 1, 2, and 3 have different usage.
- Access to various blocks may be restricted via the access protection circuitry.
- The two block address bits (B2 and B1) in the command byte are ignored with all read commands. they are set only via the write command.
- Multi-byte reads do not cross block boundaries, but instead wrap to the beginning of the block.
- The serial port will be reset whenever the $\overline{\text{PROT}}$ pin is LOW.
- If more than 16 bytes are written to the EEPROM with a page write, overlapping bytes will have their values corrupted.
- If $V_{DD}$ is 0 V, the device draws current on the SDA, SCL, WP, and $\overline{\text{PROT}}$ pins when they are brought above 0 V.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation under these conditions is not implied.

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| | voltage on $V_{DD}$ with respect to ground | — | 4.6 | V |
| | voltage on SDA, SCL, $\overline{PROT}$, and WP | –0.1 to $V_{DD}$ | +0.3 | V |
| $T_{stg}$ | storage temperature | –55 | +125 | °C |
| $T_{amb}$ | operating temperature | –40 | +85 | °C |

## DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 2.5 V to 3.6 V; $V_{SS}$ = 0 V; $T_{amb}$ = –40 °C to +85 °C; unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 2.5 | — | 3.6 | V |
| $I_{DDR}$ | supply current, EEPROM reads | $V_{DD}$ = 3.6 V; $f_{SDA}$ = 100 kHz | — | 50 | 100 | µA |
| $I_{DDW}$ | supply current, EEPROM writes | $V_{DD}$ = 3.6 V; $f_{SDA}$ = 100 kHz | — | 0.325 | 1.0 | mA |
| $I_{stb}$ | standby current | $V_{DD}$ = 3.6 V; SDA, SCL = $V_{SS}$ | — | 11.4 | 15 | µA |
| $I_{LIO}$ | input/output current, $\overline{PROT}$, SDA, SCL | $V_{IN}$ = $V_{DD}$ or $V_{SS}$ | — | 0.25 | 3.0 | µA |
| $I_{LWP}$ | input current on WP | $V_{WP}$ = $V_{DD}$ = 5.5 V | — | — | 20 | µA |
| $V_{IL}$ | LOW-level input voltage | | –0.1 | — | $V_{DD} \times 0.3$ | V |
| $V_{IH}$ | HIGH-level input voltage | | $V_{DD} \times 0.7$ | — | $V_{DD}$ | V |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 2.1 mA | — | — | 0.4 | V |
| $C_I$ | input capacitance | SCL, $\overline{PROT}$, WP not tested | — | — | 6 | pF |
| $C_{IO}$ | input/output capacitance | SDA not tested | — | — | 8 | pF |

## AC SPECIFICATIONS

$C_L$ = 1 TTL gate and 100 pF, except as noted. $V_{DD}$ = 2.5 V to 3.6 V.

| SYMBOL | PARAMETER | STANDARD MODE I²C-bus | | FAST MODE I²C-bus | | UNITS |
|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | |
| $f_{SCL}$ | Operating frequency | 0 | 100 | 0 | 400 | kHz |
| $t_{BUF}$ | Bus free time between STOP and START conditions | 4.7 | — | 1.3 | — | µs |
| $t_{HD;STA}$ | Hold time after (repeated) START condition | 4.0 | — | 0.6 | — | µs |
| $t_{SU;STA}$ | Repeated START condition setup time | 4.7 | — | 0.6 | — | µs |
| $t_{SU;STO}$ | Setup time for STOP condition | 4.0 | — | 0.6 | — | µs |
| $t_{HD;DAT}$ | Data in hold time | 0 | — | 0 | — | ns |
| $t_{VD;ACK}$ | Valid time for ACK condition[2] | — | 600 | — | 600 | ns |
| $t_{VD;DAT}$ (L) | Data out valid time[3] | — | 600 | — | 600 | ns |
| $t_{VD;DAT}$ (H) | Data out valid time[3] | — | 1500 | — | 600 | ns |
| $t_{SU;DAT}$ | Data setup time | 250 | — | 100 | — | ns |
| $t_{LOW}$ | Clock LOW period | 4.7 | — | 1.3 | — | µs |
| $t_{HIGH}$ | Clock HIGH period | 4.0 | — | 0.6 | — | µs |
| $t_F$ | Clock/Data fall time | — | 300 | 20 + 0.1 $C_b$[1] | 300 | ns |
| $t_R$ | Clock/Data rise time | — | 1000 | 20 + 0.1 $C_b$[1] | 300 | ns |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by the input filters | — | 50 | — | 50 | ns |

**NOTES:**
1. $C_b$ = total capacitance of one bus line in pF.
2. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.
3. $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

## EEPROM MEMORY

| NAME | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Retention | Data retention at operating temperature | 10 | — | — | Years |
| Endurance | Per byte | 100,000 | — | — | Cycles |

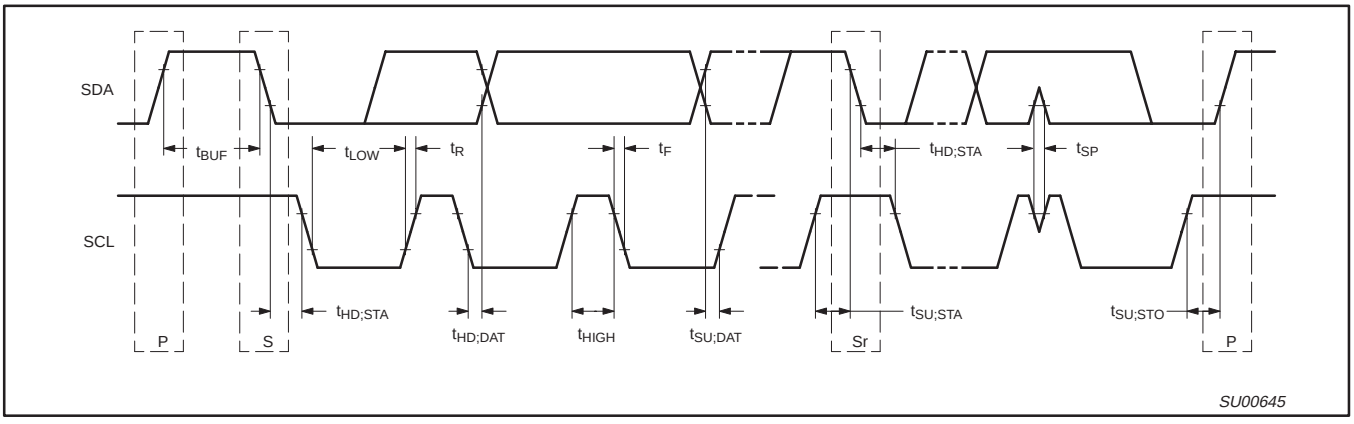
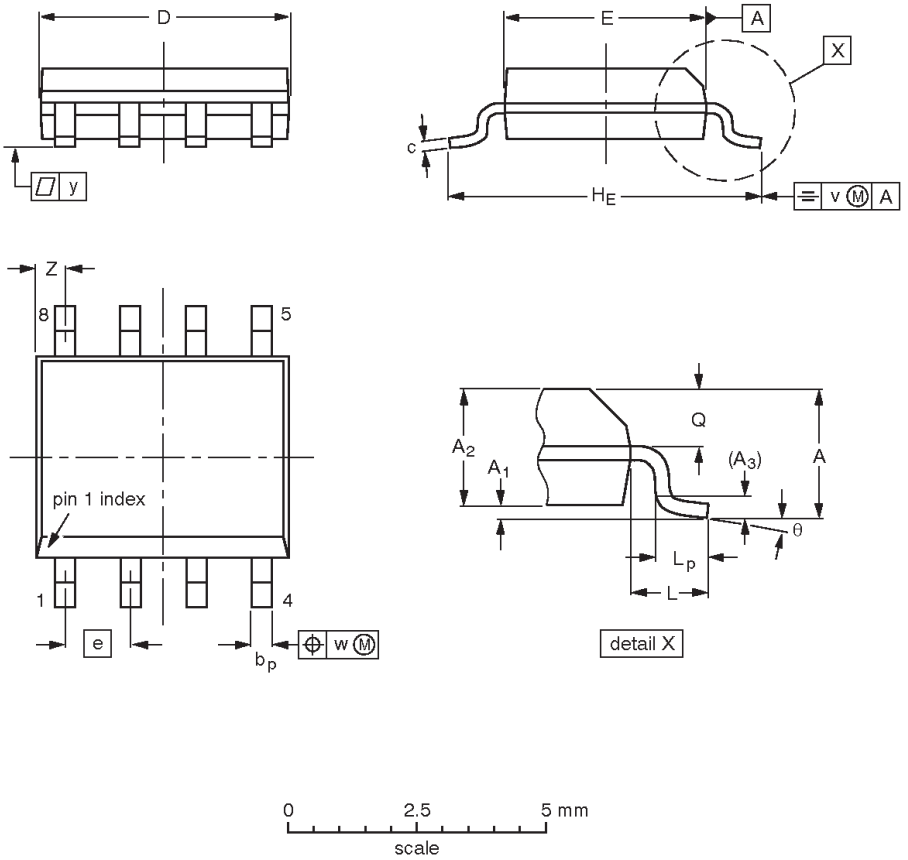



**Figure 10. Timing diagram for serial interface AC specifications**

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

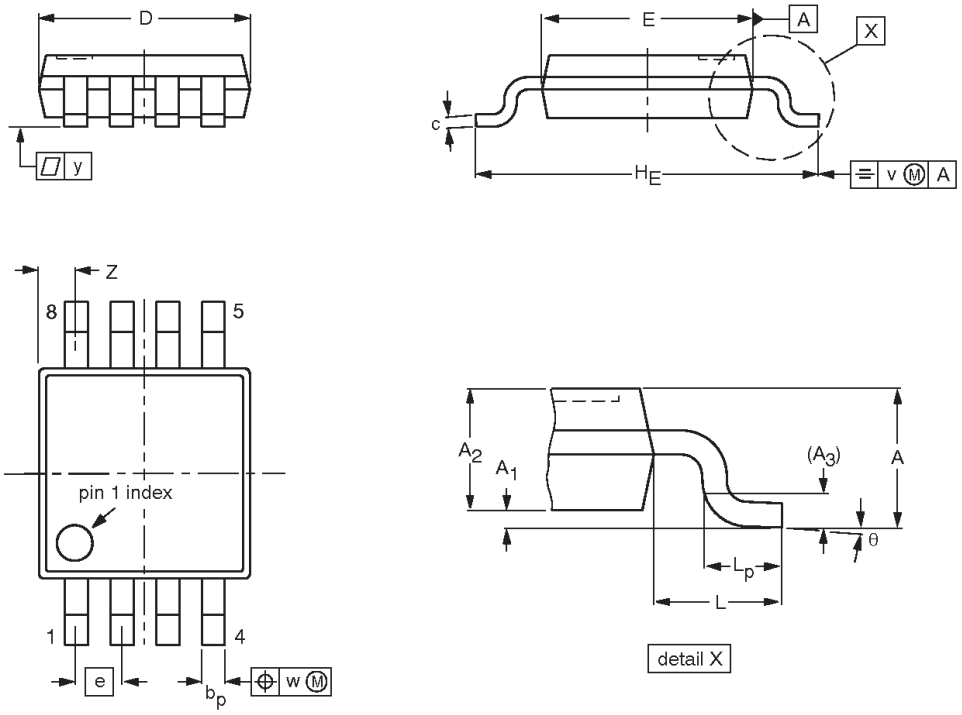
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm** **SOT505-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.45<br>0.25 | 0.28<br>0.15 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 5.1<br>4.7 | 0.94 | 0.7<br>0.4 | 0.1 | 0.1 | 0.1 | 0.70<br>0.35 | 6°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-1 | | | | | | ~~99-04-09~~<br>03-02-18 |

## REVISION HISTORY

| Rev | Date | Description |
|---|---|---|
| _1 | 20040510 | Product data (9397 750 13015) |

# 1024 × 8-bit CMOS EEPROM with access protection PCA24S08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|---|---|---|---|
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## Contact information

For additional information please visit
**http://www.semiconductors.philips.com**. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to:
**sales.addresses@www.semiconductors.philips.com**.



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