Specification for Approval

PRODUCT NAME: 1.0 Full Colour OLED
PRODUCT NO.: PFO12801

CUSTOMER
APPROVED BY
DATE:

PACER INTERNATIONAL APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2005. 12. 15	
X02	Modify panel electrical specification Modify reliability test conditions Modify FPC layout	2005. 12. 27	Page 8, 16 & 17
X03	Modify lifetime specification Modify CIEx coordinate of green Modify reliability test conditions Modify protective film dimension	2006. 01. 20	Page 6, 8, 16, 17 & 22
A01	■ Add the information of module weight ■ Modify lifetime specification ■ Add the operating conditions for different luminance ■ Modify the D.C electrical characteristics ■ Modify the panel electrical specification – current, power consumption, luminance, CIE & contrast setting ■ Modify DC-DC circuit ■ Add the packing specification	2006. 06. 20	Page 5, 6, 7, 8, 15 & 18

CONTENTS

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Pacer Display. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

Pacer display warrants that the products delivered pursuant to this specification(or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Pacer Display is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications.

Nevertheless, Pacer Display is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

- Small Molecular Organic Light Emission Diode.
- Color : 65k Full colors
- Panel matrix : 96*3*64
- Driver IC : SSD1331Z
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design : 1.45 mm
- High contrast : 500:1
- Wide viewing angle : 160□
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral.
- Wide range of operating temperature : -40 to 70°C

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x (RxGxB) x 64 (H)	dot
2	Dot Size	0.057 (W) x 0.19 (H)	mm^2
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm^2
4	Aperture Rate	74	%
5	Active Area	20.147 (W) x 13.42 (H)	mm^2
6	Panel Size	24.8 (W) x 22.42 (H)	mm^2
7	Panel Thickness	1.45 ± 0.1	mm
8	Module Size	24.8 (W) x 30.22 (H) x 1.45 (D)	mm^3
9	Diagonal A/A size	1.0	inch
10	Module Weight	1.69 ± 10%	

5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage(Vcc)	9	13.5	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Storage Humidity		85	%		
Life Time	13,000	-	Hrs	120 cd/m², checkerboard	Note (1)
Life Time	16,000	-	Hrs	100 cd/m², checkerboard	Note (2)
Life Time	20,000	-	Hrs	80 cd/m², 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 13 Volts, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m² :

- Master contrast setting : 0x0DH
- Frame rate : 85 Hz
- Duty setting : 1/64

(2) Setting of 100 cd/m² :

- Master contrast setting : 0x0AH
- Frame rate : 85 Hz
- Duty setting : 1/64

(3) Setting of 80 cd/m² :

- Master contrast setting : 0x07H
- Frame rate : 85 Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

(V_{SS}=0V, V_{DD}=2.4 to 3.5V, Ta=25°C)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	Ta=-20 □C to +60□C	12.5	13	13.5	V
V_{DD}	Operating voltage	Ta=-20 □C to +60□C	2.4			
I_{DD}	Operating current for V_{DD}	V_{DD}=2.7V, V_{CC}=11V, Display ON, Contrast =FF, No panel attached	-	170	500	uA
I_{CC}	Operating current for V_{CC}	V_{DD}=2.7V, V_{CC}=11V, Display ON, Contrast =FF, No panel attached	-	700	1200	uA
V_{IH}	High logic input level	Iout=100uA, 3.3MHz	0.8* V_{DD}	-	V_{DD}	V
V_{IL}	Low logic input level	Iout=100uA, 3.3MHz	0	-	0.2* V_{DD}	V
V_{OH}	High logic output level	Iout=100uA, 3.3MHz	0.9* V_{DD}	-	V_{DD}	V
V_{OL}	Low logic output level	Iout=100uA, 3.3MHz	0	-	0.1* V_{DD}	V
I_{SEG}	Segment output current setting V_{DD}=2.7V, V_{CC}=8V, I_{REF}=10uA, All one pattern, Display on,	Contrast=FF	142	155	168	uA
		Contrast=7F	-	78	-	uA
		Contrast=3F	-	39	-	uA
		Contrast=1F	-	19	-	uA
		Contrast=0F	7	9	11	uA

Note 1: V_{DD}=2.7V□V_{CC}= 13V□ Frame rate=85Hz□No panel attached.

Note 2: The V_{CC} input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		16	18	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		208	234	mW	All pixels on (1)
Standby mode power consumption		13	26	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m^2	Display Average
Standby mode Luminance		10		cd/m^2	
CIEx(White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy(White)	0.28	0.32	0.36		
CIEx(Red)	0.61	0.65	0.69		
CIEy(Red)	0.30	0.34	0.38		
CIEx(Green)	0.21	0.25	0.29		
CIEy(Green)	0.52	0.56	0.60		
CIEx(Blue)	0.07	0.11	0.15		
CIEy(Blue)	0.13	0.17	0.21		
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		µs	

(1) Normal mode condition :

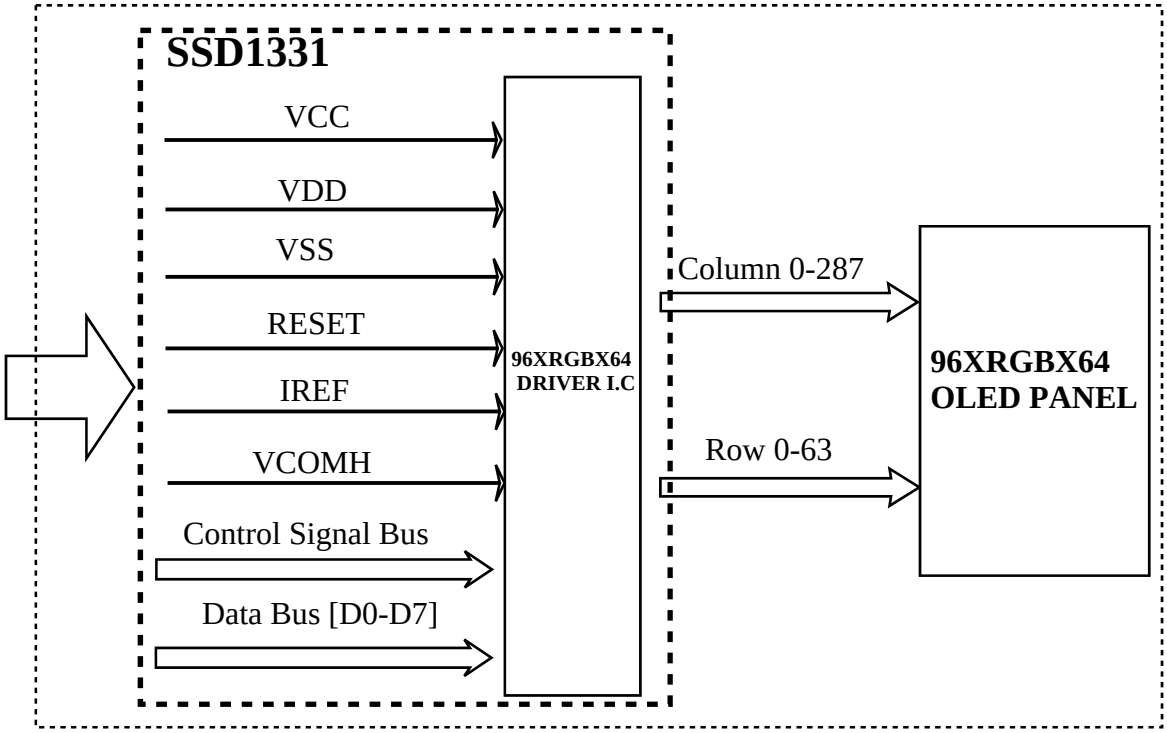
- Driving Voltage : 13 V
- Master contrast setting : 0x0AH
- Frame rate : 85 Hz
- Duty setting : 1/64

(2) Standby mode condition :

- Driving Voltage : 13V
- Master contrast setting : 0x01H
- Frame rate : 85 Hz
- Duty setting : 1/64

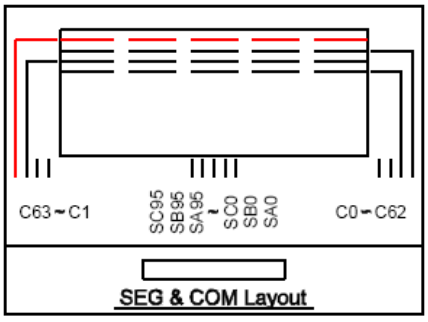
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



PACER DISPLAY 96XRGBX64 Full Colour OLED Module

7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

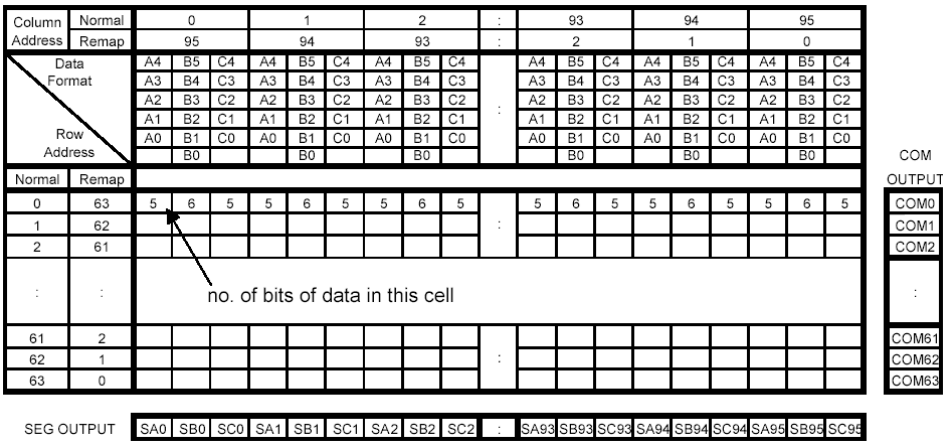
PIN NO	PIN NAME	TYPE	DESCRIPTION
1	NC	-	No connection.
2	VSS	I	Ground pin.
3	NC	-	No connection.
4	VCC	I	Positive high voltage power supply.
5	VCOMH	O	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}.
6	D7	I/O	This pin is bi-direction data signal.
7	D6	I/O	This pin is bi-direction data signal.
8	D5	I/O	This pin is bi-direction data signal.
9	D4	I/O	This pin is bi-direction data signal.
10	D3	I/O	This pin is bi-direction data signal.
11	D2	I/O	This pin is bi-direction data signal.
12	D1	I/O	This pin is bi-direction data signal.
13	D0	I/O	This pin is bi-direction data signal.
14	E/RD#	I	MCU interface input. Data read operation is initiated when it's pull low.
15	R/W#	I	MCU interface input. Data write operation is initiated when it's pull low.
16	D/C#	I	Data/ command control. Pull high for write/read display data. Pull low for write command or read status.
17	RES#	I	Hardware reset signal. When it's low, initialization of SSD1331 is executed.
18	CS#	I	Chip select input ("Low" enable).
19	IREF	I	Reference current input pin. A resistor should be connected between this pin and V_{SS}.
20	BS2	I	MCU parallel interface selection input.
21	BS1	I	MCU parallel interface selection input.
22	VDD	I	Power supply for logic.
23	NC	-	No connection.
24	VCC	I	Positive high voltage power supply.
25	VDD	I	Power supply for logic.
26	VSS	I	Ground pin.
27	NC	-	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

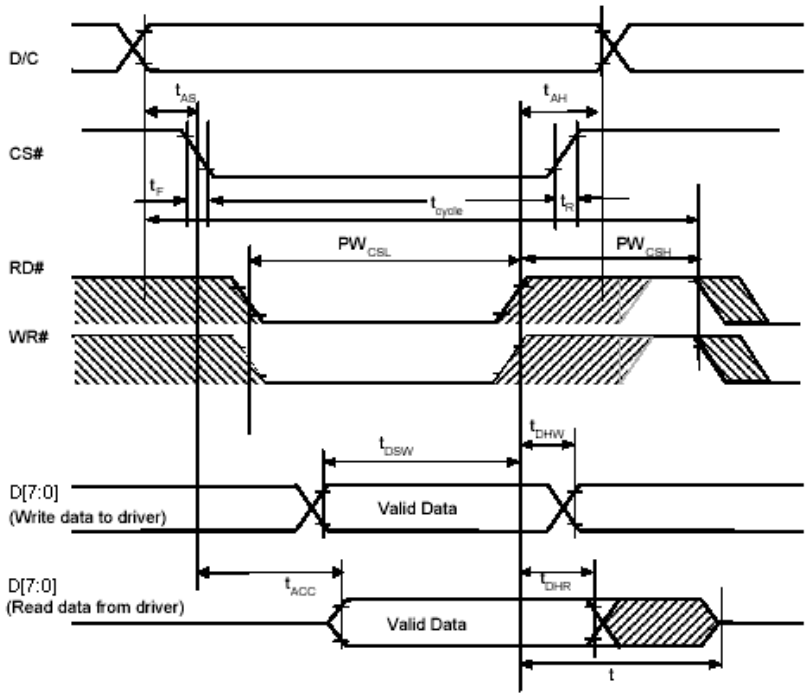
Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 5 bits, 6 bits and 5 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.



7.5 INTERFACE TIMING CHART

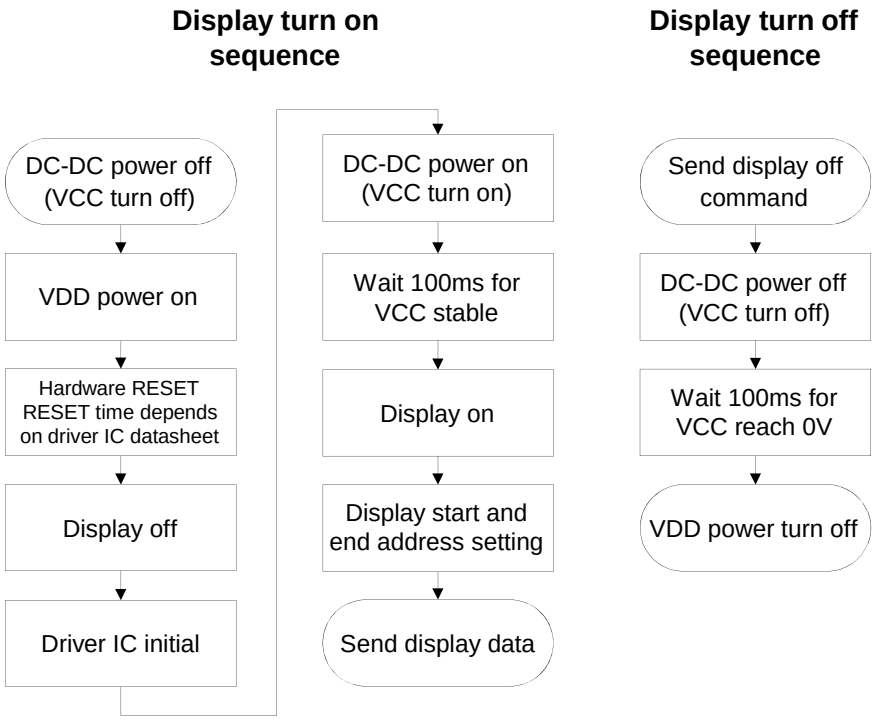
(V_{DD}-V_{SS}=2.4 to 3.5V, T_A=-40 to 95°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



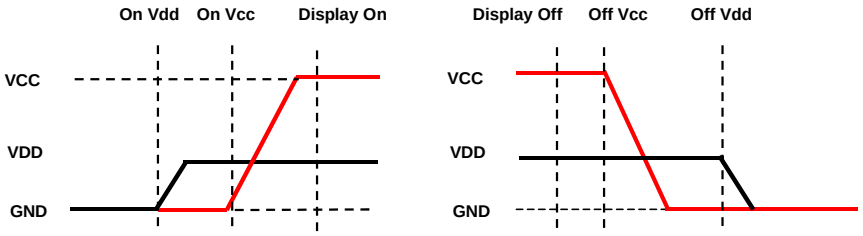
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

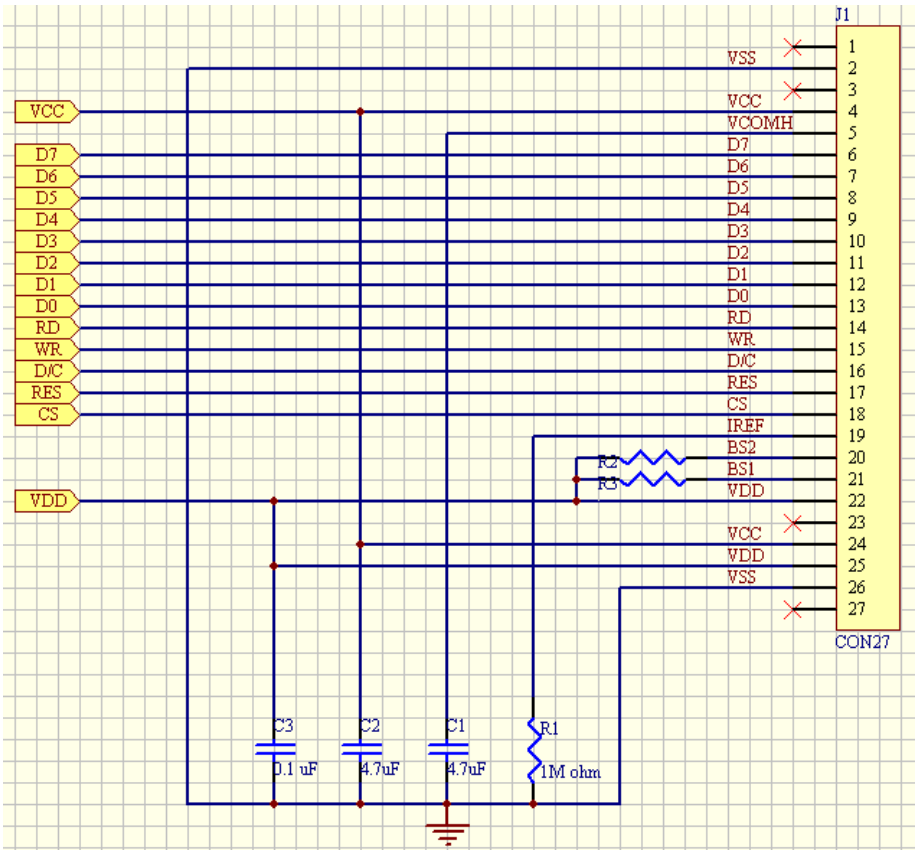
1. **Power up Vdd**
2. **Hardware RESET**
3. **Send display off command**
4. **Power up Vcc**
5. **Delay 100ms (when Vcc is stable)**
6. **Send Display on command**

Power down Sequence:

1. **Send Display off command**
2. **Power down Vcc**
3. **Delay 100ms (When Vcc is reach 0 and panel is completely discharges)**
4. **Power down Vdd**



8.2 APPLICATION CIRCUIT



Recommend components:

The C1 and C2: 4.7uF (0805) / 16V

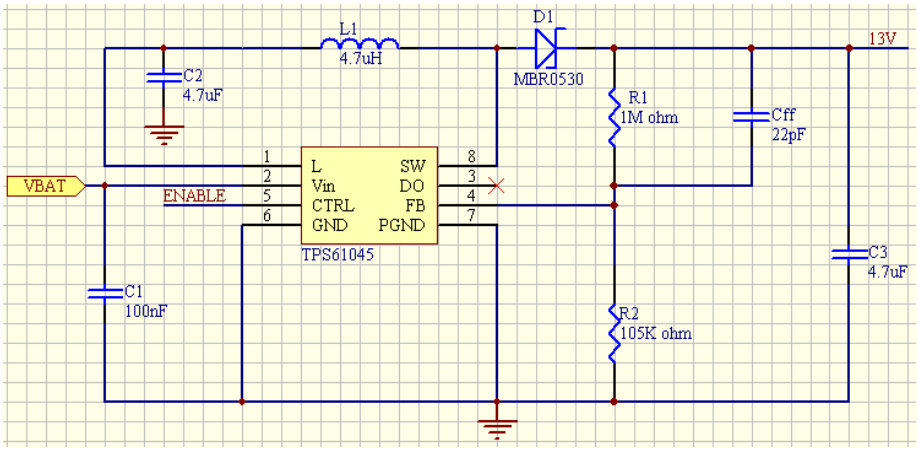
The C3: 0.1uF (0603) / 16V

The R1: 1M ohm (0603), 1%

The R2 &R3: Pull high resistor 10K ohm, or connect to VDD directly.

This circuit is designed for 8080 interface.

DC-DC Circuit



Customer should tune the R1 and R2 value.

(The value of each component can refer to tps61045 IC datasheet)

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1331

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle□3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

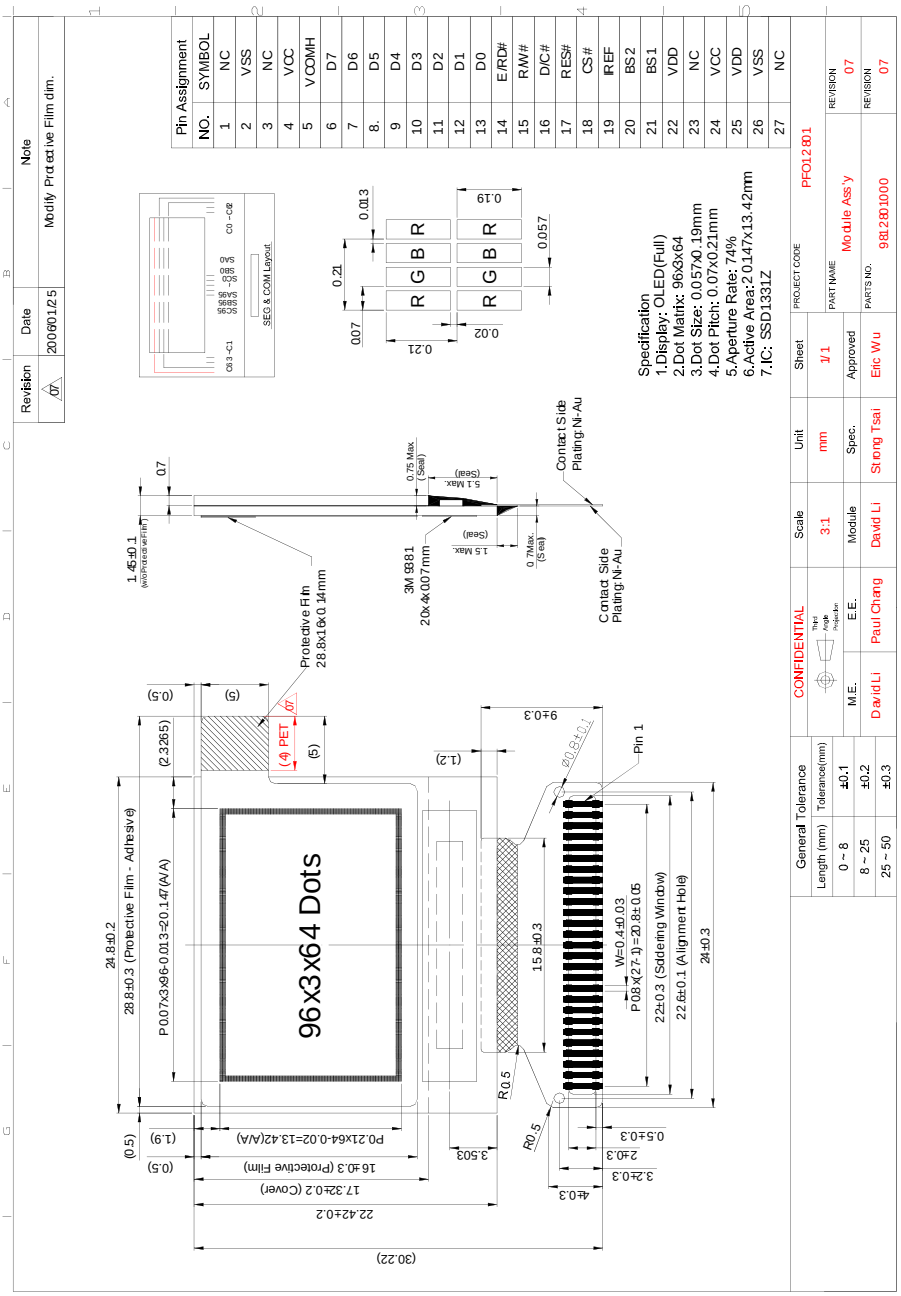
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.

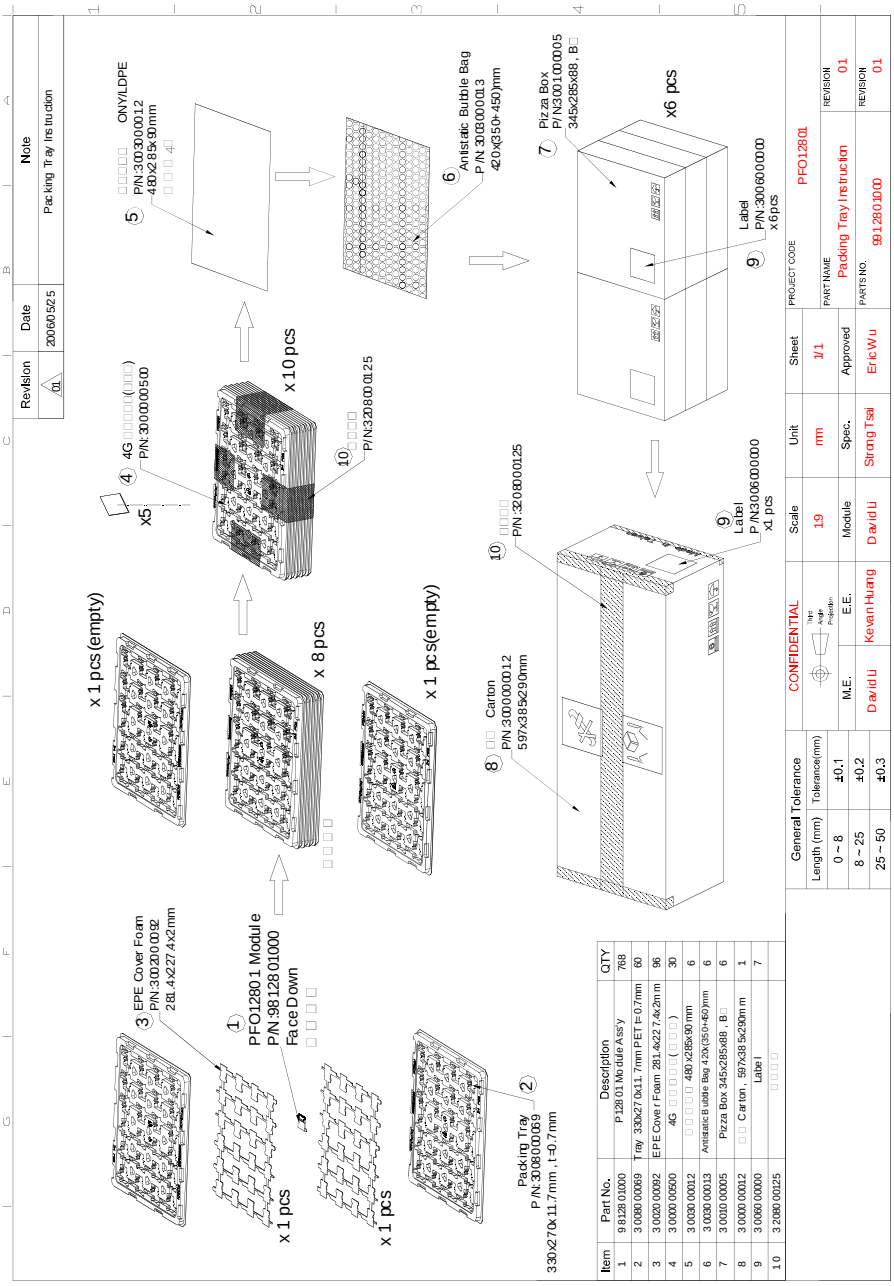
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

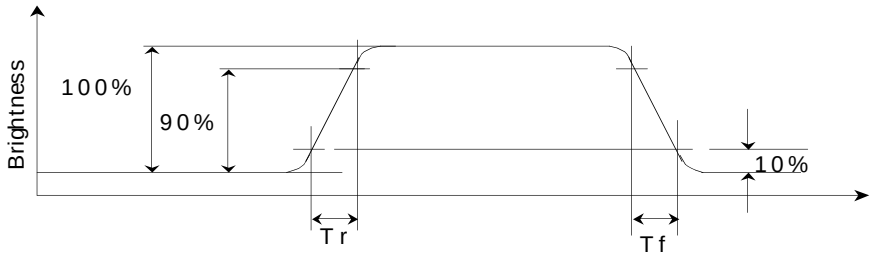
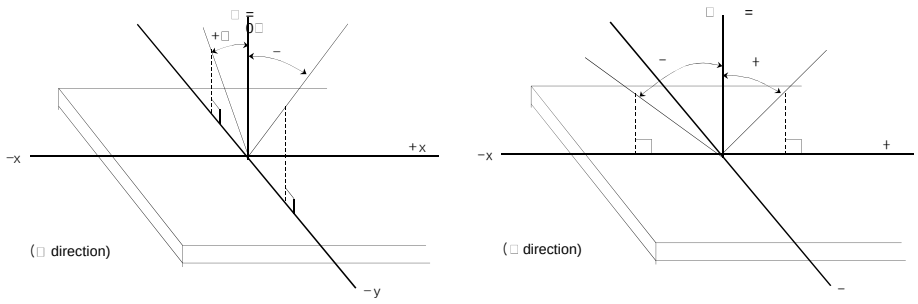


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.



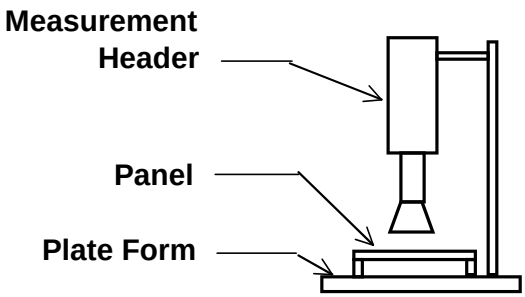
Vertical angles **Horizontal angles**

Figure 3 Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

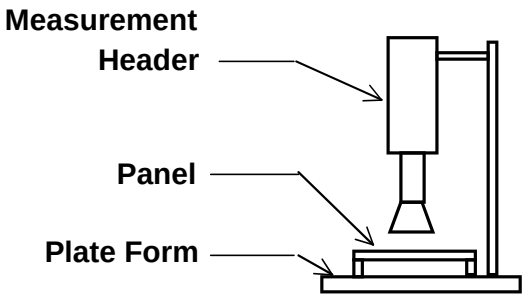
PHOTO RESEARCH PR-705, MINOLTA CS-100



PR-705 / MINOLTA CS-100 Color Analyzer

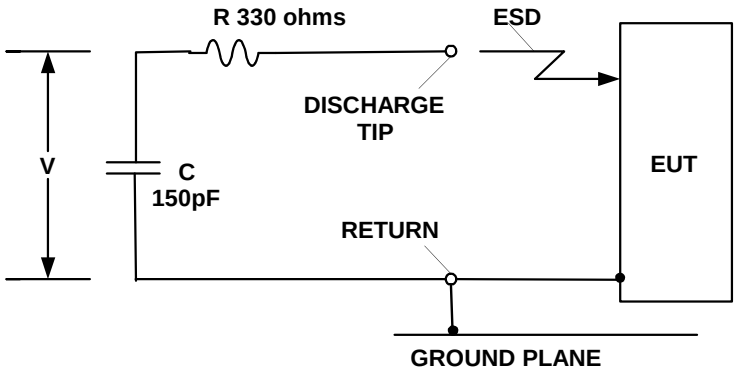
B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



Westar FPM-510 Display Contrast / Response time / View angle Analyzer

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.