

Specification for Approval

PRODUCT NAME:

PRODUCT NO.: P F O 9 5 0 6

CUSTOMER
APPROVED BY
DATE:

PACER PLC APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ Initial release	2005. 07. 06	
A01	■ Transfer from X version ■ Add warranty ■ Add module weight ■ Modify CIE specification ■ Modify dark room contrast ■ ■ Modify interface timing chart ■ Add application circuit ■ Modify packing specification	2005. 07. 21	Page 4, 5, 8, 12, 14 & 17

CONTENTS

ITEM	PAGE
<u>1. SCOPE</u>	4
<u>2. WARRANTY</u>	4
<u>3. FEATURES</u>	4
<u>4. MECHANICAL DATA</u>	5
<u>5. MAXIMUM RATINGS</u>	6
<u>6. ELECTRICAL CHARACTERISTICS</u>	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
<u>7. INTERFACE</u>	9
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
<u>8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT</u>	13
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 RECOMMEND DC-DC CIRCUIT	
8.4 COMMAND TABLE	
<u>9. RELIABILITY TEST CONDITIONS</u>	15
<u>10. EXTERNAL DIMENSION</u>	16
<u>11. PACKING SPECIFICATION</u>	17
<u>12. APPENDIXES</u>	18

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by Pacer. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

Pacer warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Pacer is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, Pacer is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- small molecular organic light emitting diode.
- Color : 262 K color and 65K colors
- Panel resolution : 128*128
- Driver IC : SSD1339
- Excellent Quick response time : 10μs
- Extremely thin thickness for best mechanism design. : 2.05 mm
- High contrast : 500:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 16-bit 6800-series Parallel Interface, 16-bit 8080-series Parallel Interface, 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface Serial Peripheral Interface.
- Wide range of operating temperature : -20 to 70°C

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 3x 128	dot
2	Dot Size	0.045 (W) x 0.19 (H)	mm ²
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm ²
4	Aperture Rate	58	%
5	Active Area	26.855 (W) x 26.86 (H)	mm ²
6	Panel Size	36.0 (W) x 36.0 (H)	mm ²
7	Panel Thickness	2.05 ± 0.1	mm
8	Module Size	36.0 (W) x 58.5 (H) x 2.05 (T)	mm ³
9	Diagonal A/A size	1.5	inch
10	Module Weight	5.70 ± 10%	gram

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})		3.5	V	$T_a = 25^{\circ}\text{C}$	
Supply Voltage (V_{CC})		18	V	$T_a = 25^{\circ}\text{C}$	
Operating Temp.	-20	70	$^{\circ}\text{C}$		
Storage Temp	-40	85	$^{\circ}\text{C}$		
Humidity		85	%		
Operating Life Time	2200	-	Hrs	80 cd/m ² , 50% Check board	Note (1)
Operating Life Time	3000	-	Hrs	60 cd/m ² , 50% Check	Note (2)
Operating Life Time	7000	-	Hrs	40 cd/m ² , 50% Check	Note (3)
Storage Life Time	20000	-	Hrs	$T_a = 25^{\circ}\text{C}$, 50% RH	

Note:

(A) Under $V_{CC} = 17$ Volts, $T_a = 25^{\circ}\text{C}$, 50% RH.

(B) End-of-life is defined when the luminance has decayed to less than 50% of the initial luminance.

(1) Setting of 80cd/m² :

- ☐ Master contrast setting : 0x09H
- ☐ Frame rate : 85 Hz
- ☐ Duty setting : 1/128

(2) Setting of 60cd/m² :

- ☐ Master contrast setting : 0x06H
- ☐ Frame rate : 85 Hz
- ☐ Duty setting : 1/128

(3) Setting of 40cd/m² :

- ☐ Master contrast setting : 0x03H
- ☐ Frame rate : 85 Hz
- ☐ Duty setting : 1/128

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	$T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	16.5	17	17.5	V
V_{DD}	Logic operating voltage	$T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	2.4	2.7	3.5	V
V_{DDIO}	Logic I/O operating voltage	$T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	1.5	1.8	3.5	V
V_{OH}	Hi logic output level	$I_{out} = 100\text{ }\mu\text{A}$, 3.3MHz	$0.9 \cdot V_{DDIO}$		V_{DDIO}	V
V_{OL}	Low logic output level	$I_{out} = 100\text{ }\mu\text{A}$, 3.3MHz	0		$0.1 \cdot V_{DDIO}$	V
V_{IH}	Hi logic input level	$I_{out} = 100\text{ }\mu\text{A}$, 3.3MHz	$0.8 \cdot V_{DDIO}$		V_{DDIO}	V
V_{IL}	Low logic output level	$I_{out} = 100\text{ }\mu\text{A}$, 3.3MHz	0		$0.2 \cdot V_{DDIO}$	V
I_{CC}	Operating current for V_{CC} (No panel attached)	Contrast=FF		1.3		mA
I_{DD}	Operating current for V_{DD} (No panel attached)	Contrast=FF		0.4		mA
I_{SEG}	Segment output current (No panel attached)	Contrast=FF		160		μA
		Contrast=AF		110		μA
		Contrast=5F		60		μA
		Contrast=00		0		μA

Note : $V_{DD} = 2.7$ Volts □ $V_{CC} = 17$ Volts □ Frame rate = 85 Hz □ No panel attached.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current	-	21	23	mA	All pixels on (1)
Standby mode current		1.5	4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	357	391	mW	All pixels on (1)
Standby mode power consumption		15	40	mW	Standby mode 10% pixels on (2)
Pixel Luminance	50	60		cd/m ²	Display Average
Standby Luminance		20		cd/m ²	
CIE _x (Red)	0.61	0.66	0.71		CIE1931
CIE _y (Red)	0.28	0.33	0.38		CIE1931
CIE _x (Green)	0.25	0.30	0.35		CIE1931
CIE _y (Green)	0.55	0.60	0.65		CIE1931
CIE _x (Blue)	0.09	0.14	0.19		CIE1931
CIE _y (Blue)	0.13	0.18	0.23		CIE1931
CIE _x (White)	0.24	0.29	0.34		CIE1931
CIE _y (White)	0.27	0.32	0.37		CIE1931
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		µs	

Normal mode condition :

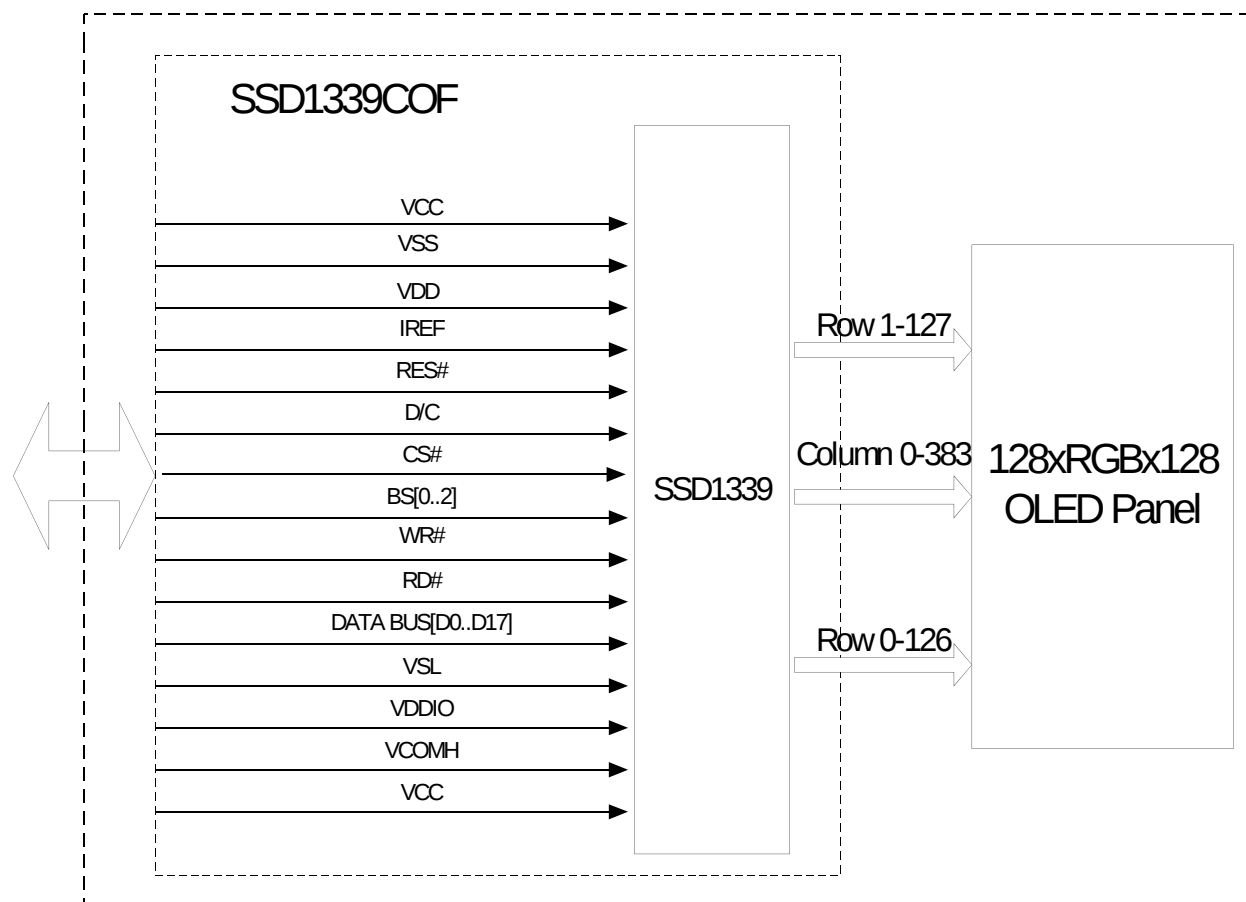
- Driving Voltage : 17 V
- Contrast setting : 0x06H
- Frame rate : 85 Hz
- Duty setting : 1/128

Standby mode condition :

- Driving Voltage : 10V
- Contrast setting : 0x04H
- Frame rate : 85 Hz
- Duty setting : 1/128

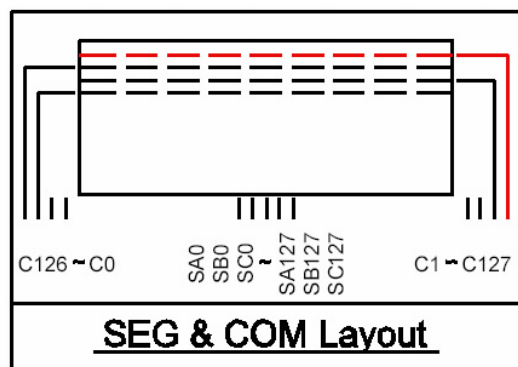
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



PACER 128xRGBx128 OLED Module

7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VSS	2	Ground.
TEST	3	No connection.
VDD	4	Digital voltage power supply.
TEST	5	No connection.
TEST	6	No connection.
TEST	7	No connection.
IREF	8	A resistor should be connected between this pin and VSS.
RES#	9	Hardware Reset pin (Low active).
D/C	10	H: Data; L: Command.
CS#	11	Chip select pin.
BS2	12	Interface select pin.
BS1	13	Interface select pin.
BS0	14	Interface select pin.
R/W#	15	8080: data write enable pin; 6800: Read/Write select pin.
E/RD#	16	8080: data read enable pin; 6800: Read/Write enable pin.
D0	17	16 /18 bits data bus.
D1	18	
D2	19	
D3	20	
D4	21	
D5	22	
D6	23	
D7	24	
D8	25	
D9	26	
D10	27	
D11	28	
D12	29	
D13	30	
D14	31	
D15	32	
D16	33	
D17	34	
VSL	35	This is segment voltage reference pin.
VDDIO	36	I/O voltage power supply.
VCOMH	37	A capacitor should be connected between this pin and VSS.
VCC	38	Analog power supply.
NC	39	No connection

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 132 x 132 x 18bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown below.

Column Address	Normal	Remap	0			1			2			:	129			130			131			
			131			130			129			:	2			1			0			
Data Format Row Address			A5	B5	C5	A5	B5	C5	A5	B5	C5	:	A5	B5	C5	A5	B5	C5	A5	B5	C5	
			A4	B4	C4	A4	B4	C4	A4	B4	C4		A4	B4	C4	A4	B4	C4	A4	B4	C4	
			A3	B3	C3	A3	B3	C3	A3	B3	C3		A3	B3	C3	A3	B3	C3	A3	B3	C3	
			A2	B2	C2	A2	B2	C2	A2	B2	C2		A2	B2	C2	A2	B2	C2	A2	B2	C2	
			A1	B1	C1	A1	B1	C1	A1	B1	C1		A1	B1	C1	A1	B1	C1	A1	B1	C1	
			A0	B0	C0	A0	B0	C0	A0	B0	C0		A0	B0	C0	A0	B0	C0	A0	B0	C0	
Normal	Remap																					
0	132	6	6	6	6	6	6	6	6	6	:	6	6	6	6	6	6	6	6	6		
1	131										:											
2	130										:											
:	:	no. of bits of data in this cell																				
130	2										:											
131	1										:											
132	0										:											

SEG OUTPUT

SA0	SB0	SC0	SA1	SB1	SC1	SA2	SB2	SC2	:	SA129	SB129	SC129	SA130	SB130	SC130	SA131	SB131	SC131
-----	-----	-----	-----	-----	-----	-----	-----	-----	---	-------	-------	-------	-------	-------	-------	-------	-------	-------

COM OUTPUT

COM0	COM1	COM2	:	COM130	COM131	COM132
------	------	------	---	--------	--------	--------

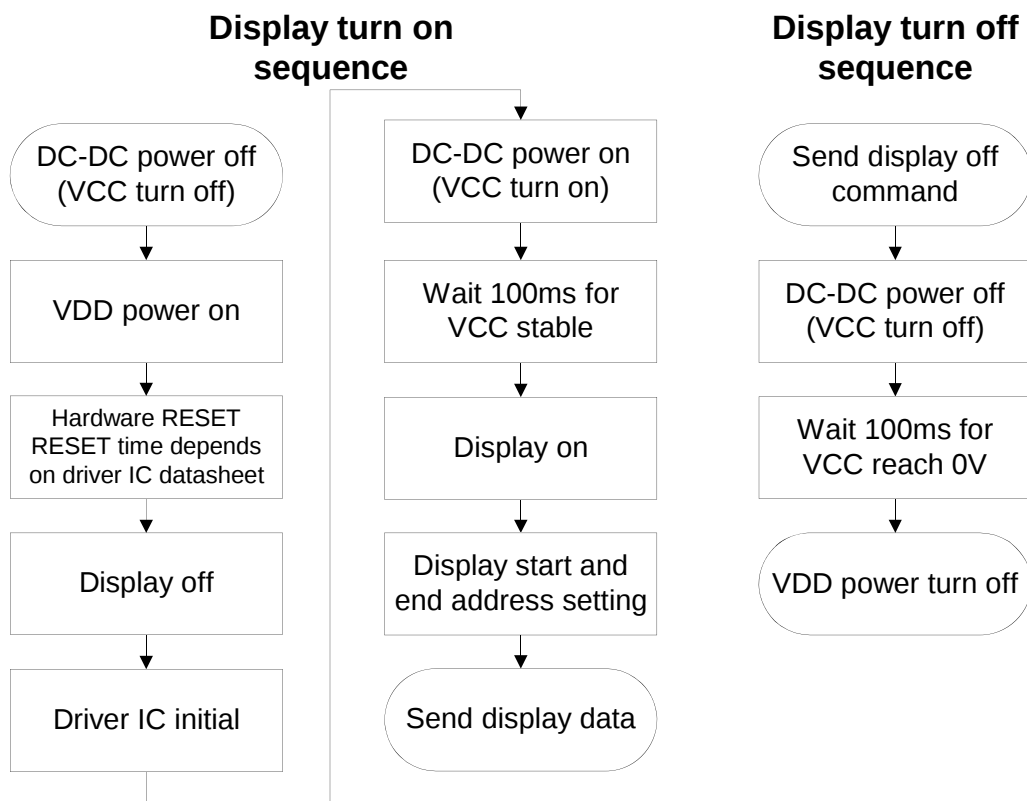
7.5 INTERFACE TIMING CHART

Column	Normal	0			1			2			:	129			130			131		
Address	Remap	131			130			129			:	2			1			0		
Data Format Row Address		A5	B5	C5	A5	B5	C5	A5	B5	C5	:	A5	B5	C5	A5	B5	C5	A5	B5	C5
		A4	B4	C4	A4	B4	C4	A4	B4	C4	:	A4	B4	C4	A4	B4	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	B3	C3	:	A3	B3	C3	A3	B3	C3	A3	B3	C3
		A2	B2	C2	A2	B2	C2	A2	B2	C2	:	A2	B2	C2	A2	B2	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	B1	C1	:	A1	B1	C1	A1	B1	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	B0	C0	:	A0	B0	C0	A0	B0	C0	A0	B0	C0
Normal	Remap																			COM
0	132	6	6	6	6	6	6	6	6	6	:	6	6	6	6	6	6	6	6	COM0
1	131										:									COM1
2	130										:									COM2
:	:	no. of bits of data in this cell																		:
130	2										:									COM130
131	1										:									COM131
132	0										:									COM132

SEG OUTPUT	SA0	SB0	SC0	SA1	SB1	SC1	SA2	SB2	SC2	:	SA129	SB129	SC129	SA130	SB130	SC130	SA131	SB131	SC131
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8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



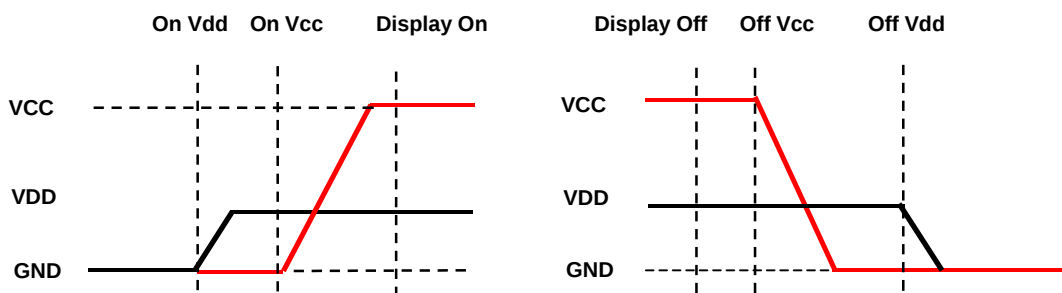
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

1. Power up Vdd
2. Hardware RESET
3. Send display off command
4. Power up Vcc
5. Delay 100ms (when Vcc is stable)
6. Send Display on command

Power down Sequence:

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
4. Power down Vdd



8.2 APPLICATION CIRCUIT

Column	Normal	0			1			2			:	129			130			131		
Address	Remap	131			130			129			:	2			1			0		
Data Format Row Address	A5	B5	C5	A5	B5	C5	A5	B5	C5	:	A5	B5	C5	A5	B5	C5	A5	B5	C5	
	A4	B4	C4	A4	B4	C4	A4	B4	C4	:	A4	B4	C4	A4	B4	C4	A4	B4	C4	
	A3	B3	C3	A3	B3	C3	A3	B3	C3	:	A3	B3	C3	A3	B3	C3	A3	B3	C3	
	A2	B2	C2	A2	B2	C2	A2	B2	C2	:	A2	B2	C2	A2	B2	C2	A2	B2	C2	
	A1	B1	C1	A1	B1	C1	A1	B1	C1	:	A1	B1	C1	A1	B1	C1	A1	B1	C1	
	A0	B0	C0	A0	B0	C0	A0	B0	C0	:	A0	B0	C0	A0	B0	C0	A0	B0	C0	
	A0	B0	C0	A0	B0	C0	A0	B0	C0	:	A0	B0	C0	A0	B0	C0	A0	B0	C0	
Normal	Remap																			
0	132	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6		
1	131																			
2	130																			
:	:	no. of bits of data in this cell																		
130	2																			
131	1																			
132	0																			

COM

OUTPUT

COM0
COM1
COM2
:
COM130
COM131
COM132

SEG OUTPUT

SA0	SB0	SC0	SA1	SB1	SC1	SA2	SB2	SC2	:	SA129	SB129	SC129	SA130	SB130	SC130	SA131	SB131	SC131
-----	-----	-----	-----	-----	-----	-----	-----	-----	---	-------	-------	-------	-------	-------	-------	-------	-------	-------

8.3 RECOMMEND DC-DC CIRCUIT : LM2731YML or TPS61040

Refer to application notes.

8.4 COMMAND TABLE

Refer to IC Spec.: SSD1339

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	3
2	Low temp. (Non-operation)	-40°C, 240hrs	2
3	High temp. (Operation)	70°C, 120hrs	3
4	Low temp. (Operation)	-20°C, 120hrs	2
5	High temp. / High humidity (Non-operation)	85°C, 85%RH, 120hrs	5
6	High temp. / High humidity (Operation)	65°C, 90%RH, 96hrs	5
7	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	2
8	OLB Peel strength (Non-operation)	500g/cm (Speed~ 50mm/min)	5
9	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
10	Drop	Height: 120cm Sequence : 1 angle□3 edges and 6 faces Cycles: 1	1 Carton
11	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

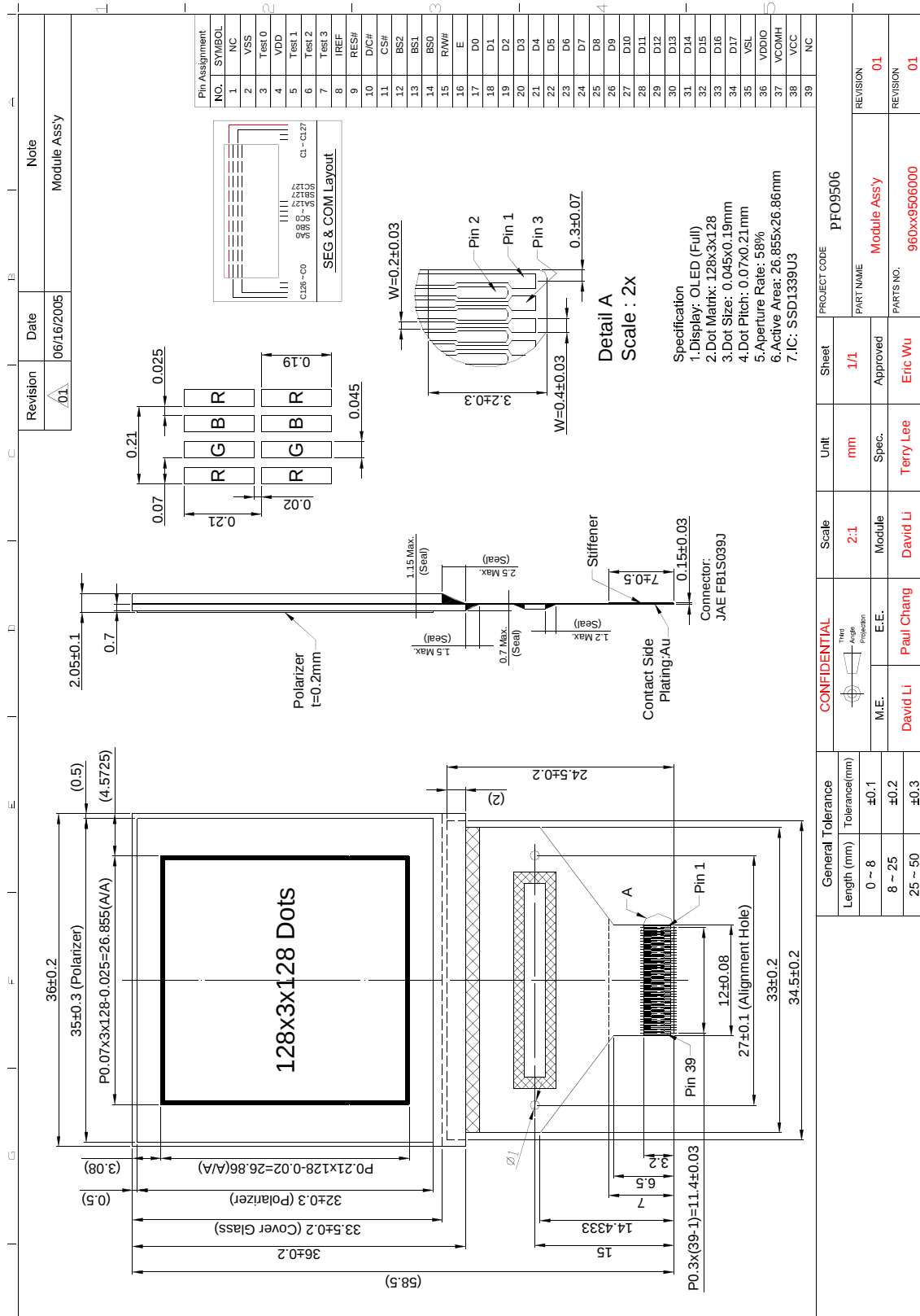
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. The test pattern at operating condition is 50% alternating check board.
3. The degradation of Polarizer are ignored for item 1, 5 & 6.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm$ 50% of initial value.

10. EXTERNAL DIMENSION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

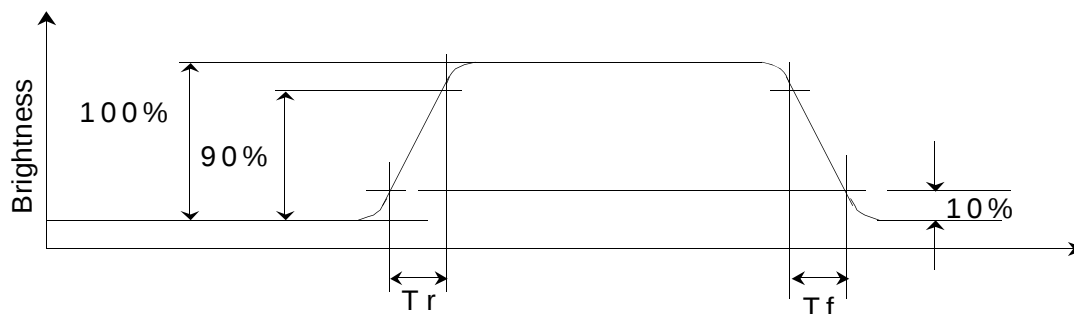


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

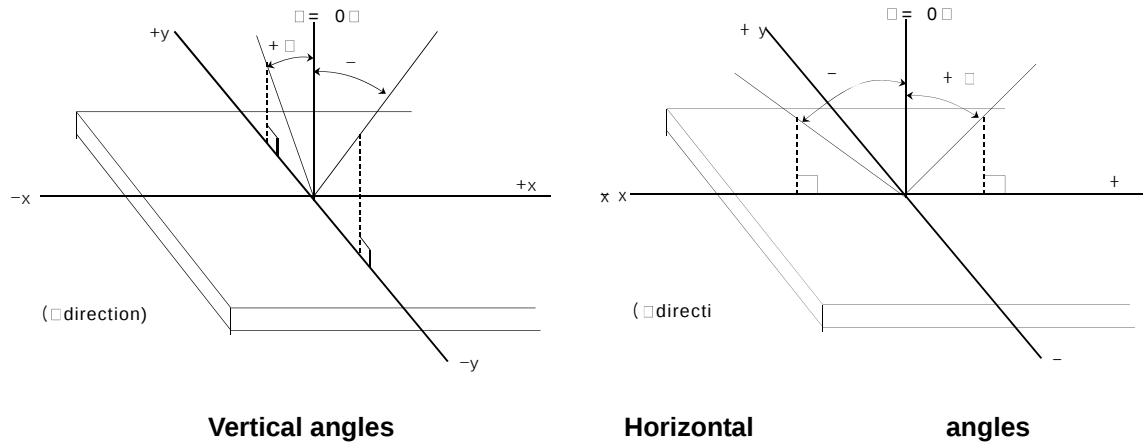
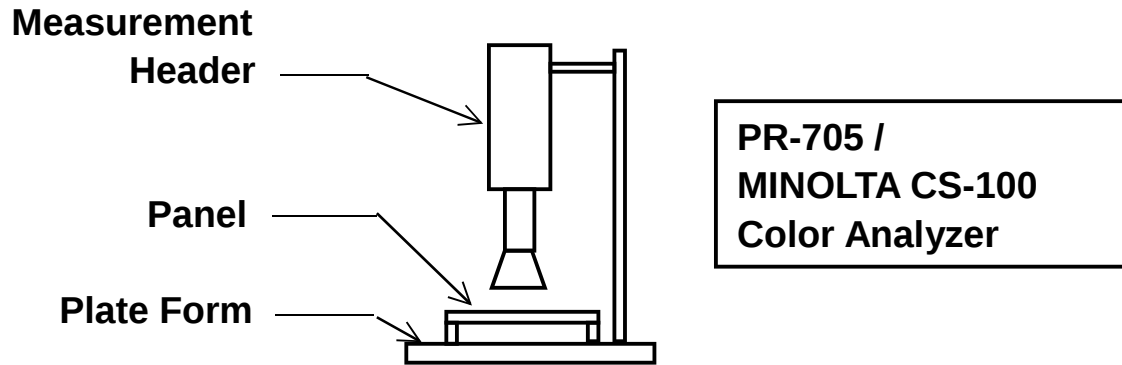


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

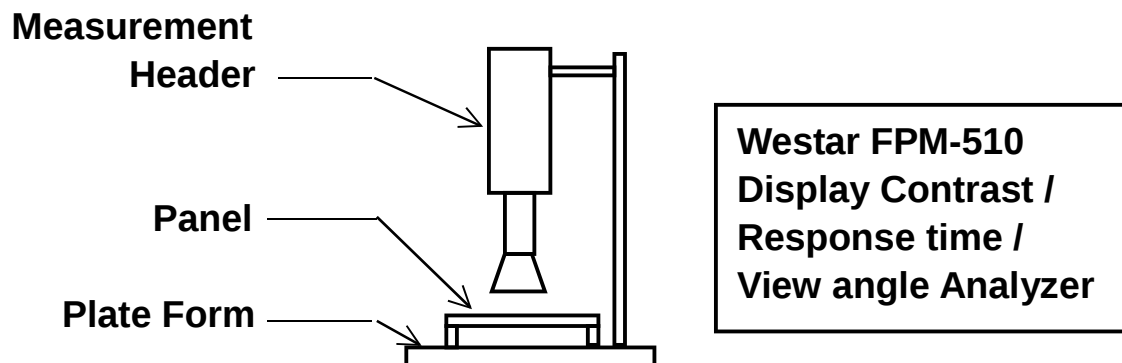
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

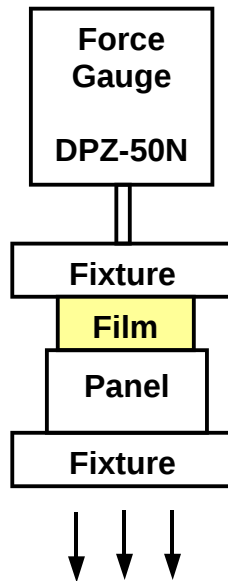


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

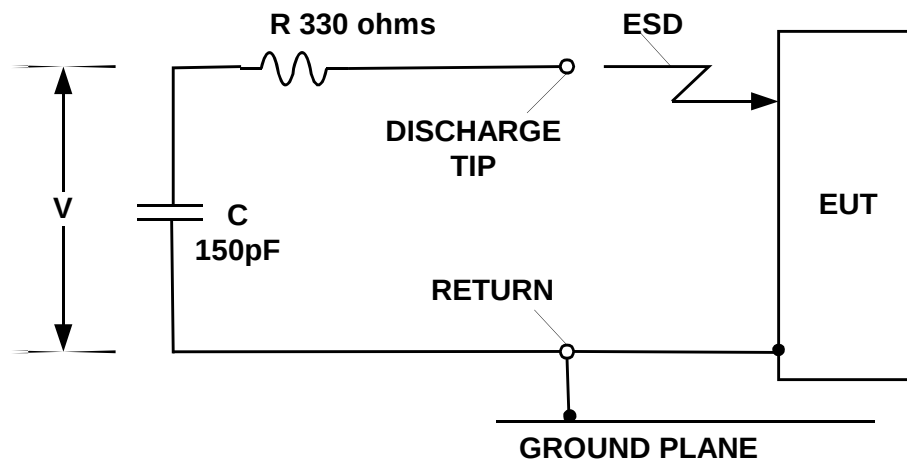
WESTAR CORPORATION FPM-510



C. PEEL STRENGTH



D. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.