OXFORD SEMICONDUCTOR

UG-0037 23 Sep 2008

EV-TD12x-PCI
Evaluation Board User Guide

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Contents

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This guide documents the EV-TD122-PCI and EV-TD124-PCI evaluation boards and hardware.

Throughout the guide, where text applies to both EV-TD122-PCI and EV-TD124-PCI evaluation boards, the term EV-TD12x-PCI is used.

The EV-TD12x-PCI evaluation board consists of:

- An EVB122 or EVB124 board, containing a TD122 or TD124 USB host controller.
  Throughout the guide, where text applies to both EVB122 and EVB124 boards, the term EVB12x is used
- PCI104 bridge board

For details about the architecture of the EV-TD12x-PCI, see Chapter 1 Introduction. For details about the EVB12x board, see Chapter 2 EVB12x Hardware Operation and Configuration. For details about the PCI104 bridge board, see Chapter 3 PCI104 Bridge Board.

Revision Information

The following table documents the revisions of this guide.

Table I Revision Information

Revision	Modification
23 Sep 2008	Correction to names of boards
Mar 2007	Changed the corporate address on the title page.
Nov 2006	First publication

Typographic Conventions

In this document, the following conventions apply.

Convention	Meaning
Italic Letters With Initial Capital Letters	A cross-reference to another publication
Title	A cross-reference to another section within the document
1, 2, 3	A numbered list where the order of list items is significant
■	A list where the order of items is not significant
	Significant additional information
`Courier`	Software code, or information displayed on a screen
Bold	Significant names, for example of files or directories Text you type

Ordering Information

The following boards are available:

- EV-TD122-PCI evaluation board
- EV-TD124-PCI evaluation board

Contacting Oxford Semiconductor

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Introduction

The EV-TD12x-PCI evaluation board is a system for TD122 and TD124 customer evaluations and internal software development in the PC environment. The EV-TD12x-PCI evaluation board allows you to install and use the TD122 or TD124 (on an EVB12x board) in any PCI-based computer. Application software running on the system has access to the TD122 or TD124 using the PCI memory space. You can use the EVB12x board with or without the PCI104 PCI bridge board.

You can use the EV-TD12x-PCI to:

- Evaluate the Oxford Semiconductor TD122 and TD124 USB host controller
- Run TD122 and TD124 demonstrations
- Develop user software for EV-TD12x-PCI-based applications

The EV-TD12x-PCI evaluation board is a two-board combination of the following:

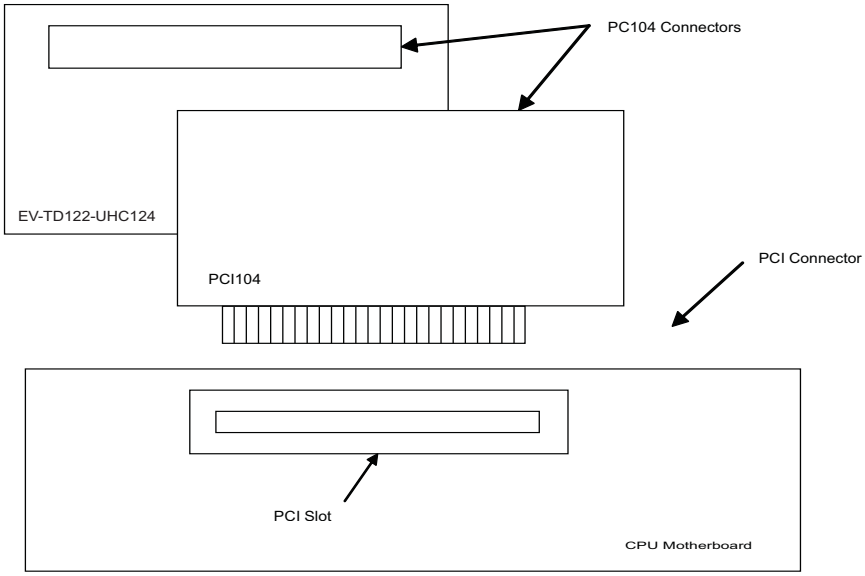
- An EVB122 evaluation board with 2 USB host ports, or an EVB124 evaluation board with 4 USB host ports
- A 33 MHz, 32 bit PCI PCI104 bridge board

The EVB12x evaluation board contains the TD122 or the TD124 and all the USB-specific hardware.

The PCI104 bridge board contains the PCI9030 PCI bridge chip that bridges the PCI bus to the TD122 or TD124. Power and control signals to the PCI bus are maintained by the PCI bridge chip, while initialization and configuration of the PCI bridge chip is maintained by the on-board serial EEPROM.

Figure 1-1 illustrates the orientation of the two boards. The EV-TD12x-PCI is a double-width PCI board, approximately 3 cm thick, that occupies one PCI slot. The two or four host USB connectors are easily accessible through the openings in the computer case.

Figure 1-1 EV-TD12x-PCI System Board Orientation



For a description of the EV-TD12x-PCI evaluation board, see Chapter 2 EVB12x Hardware Operation and Configuration. For a description of the PCI104 bridge board, see Chapter 3 PCI104 Bridge Board. For complete information about the TD122 device, see MU1203: *TDUHC122 USB Host Controller Technical Manual*. For complete information about the TD124 device, see MU1002: *UHC124 USB Host Controller Data Sheet*.

Although you can use the EV-TD12x-PCI to evaluate the TD122 and TD124, it does not result in optimal performance due to the long access times of the PCI bus. For optimal performance, place the TD122 or TD124 directly on the system bus, as described in Chapter 2 EVB12x Hardware Operation and Configuration.

PCI Operation

Every PCI implementation has a PCI configuration space, where the PCI configuration registers are found. PCI configuration registers are accessed with reads/writes to the configuration space, which is separate from memory and I/O space. Table 1-1 lists the standard PCI configuration register space for all PCI functions on the PCI bus.

Table 1-1 Standard PCI Configuration Register Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR 0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2)				18h
Base Address Register 3 (BAR 3)				1Ch
Base Address Register 4 (BAR 4)				20h
Base Address Register 5 (BAR 5)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h
Reserved				38h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3Ch

The PCI104 can be identified on the PCI bus during enumeration by the following PCI configuration registers.

Table 1-2 PCI Configuration Registers

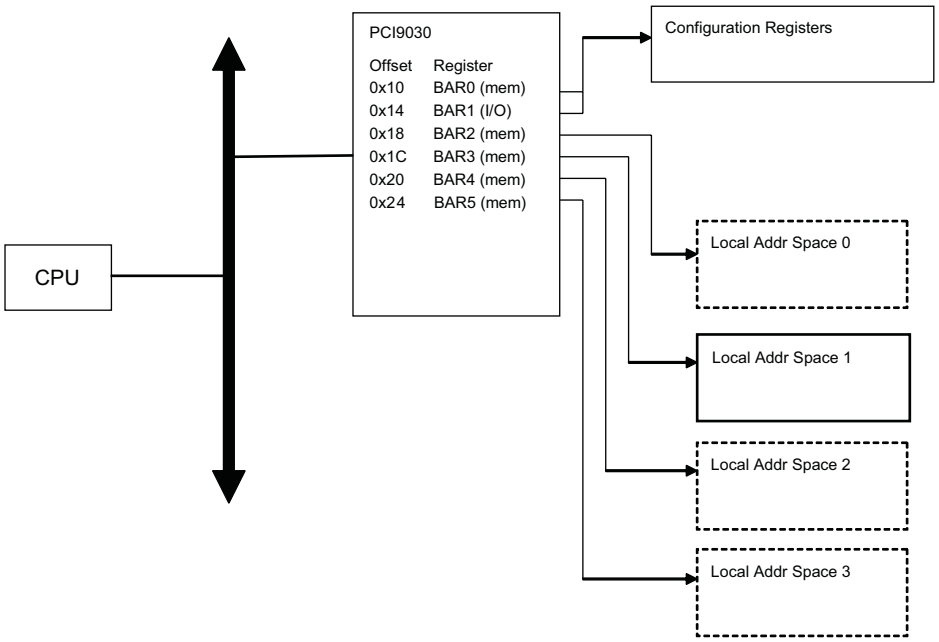
Register	Power-On Value
Vendor ID	192Eh
Device ID	012Fh
Revision	0001h
Class Code	0680h
Subsystem ID	012Fh
Subsystem Vendor ID	192Eh

Most operating systems provide functions for finding devices on the PCI bus. These functions typically key off the vendor and device IDs, or the class code. Because the class code for the PCI104 appears as a PCI bridge with sub class code “other”, we recommend that you key the search to the vendor and device IDs.

Configuration

The EV-TD12x-PCI has two memory mapped register spaces and one I/O mapped register space. The address locations of the various spaces are determined by the base address registers of the PCI configuration registers. Base Address Register 0 (BAR0) contains the address of the memory mapped PCI bridge controller registers. BAR1 contains the I/O address for the same PCI bridge controller registers. The PCI bridge controller registers are mapped into both memory and I/O space, so that these registers can be accessed using memory accesses or I/O addressing. BAR3 contains the address of the memory mapped TD122 or TD124 registers. Figure 1-2 illustrates the register mappings within a PCI system.

Figure 1-2 PCI104 Register Mappings



The base address registers are typically initialized by the system BIOS or by the operating system. Software generally does not have to set the addresses of the mapped locations, however, this is system dependent. If these registers are not initialized, the three spaces should be manually mapped into system memory and I/O space accordingly. Care must be taken to ensure no conflicts exist between the mapped regions and other devices on the PCI bus.

Serial EEPROM Registers

The PCI9030 PCI bridge chip provides an interface to program the attached serial EEPROM. The serial EEPROM is pre-programmed with the default values in Table 1-3. The table is for informational purposes only. If you modify the default values, the behavior of the PCI104 changes.

Table 1-3 Serial EEPROM Registers		
Offset	Description	Default
00h	PCI device ID	012Fh
02h	PCI vendor ID	192Eh
04h	PCI Status Register	0290h
06h	PCI Command Register	0003h
08h	PCI class code	0680h
0Ah	PCI class code / revision number	0001h
0Ch	PCI subsystem ID	016Bh
0Eh	PCI subsystem vendor ID	192Eh
10h	MSB new capability pointer	0000h
12h	LSB new capability pointer	0040h
14h	(Maximum latency and minimum grant are not loadable)	0000h
16h	Interrupt pin (interrupt line routing is not loadable)	0100h
18h	MSW of power management capabilities	4801h
1Ah	LSW of power management next capability pointer / power management capability ID	4801h
1Ch	MSW of power management data /PMCSR bridge support extension	0000h
1Eh	LSW of power management control/status	0000h
20h	MSW of hot swap control/status	0000h
22h	LSW of hot swap next capability pointer / hot swap control	4C06h
24h	PCI vital product data address	0000h
26h	PCI vital product data next capability pointer / PCI vital protocol data control	0003h
28h	MSW of local address space 0 range	0000h
2Ah	LSW of local address space 0 range	0000h
2Ch	MSW of local address space 1 range	FFFFh
2Eh	LSW of local address space 1 range	F000h
30h	MSW of local address space 2 range	0000h
32h	LSW of local address space 2 range	0000h
34h	MSW of local address space 3 range	0000h
36h	LSW of local address space 3 range	0000h
38h	MSW of expansion ROM range	0000h
3Ah	LSW of expansion ROM range	0000h
3Ch	MSW of local address space 0 local base address (remap)	0000h
3Eh	LSW of local address space 0 local base address (remap)	0000h
40h	MSW of local address space 1 local base address (remap)	0000h
42h	LSW of local address space 1 local base address (remap)	0001h
44h	MSW of Local address space 2 local base address (remap)	0000h
46h	LSW of local address space 2 local base address (remap)	0000h
48h	MSW of Local address space 3 local base address (remap)	0000h
4Ah	LSW of local address space 3 local base address (remap)	0000h

Table 1-3 Serial EEPROM Registers

Offset	Description	Default
4Ch	MSW of expansion ROM local base address (remap)	0010h
4Eh	LSW of expansion ROM local base address (remap)	0000h
50h	MSW of local address space 0 bus region descriptor	0080h
52h	LSW of local address space 0 bus region descriptor	0000h
54h	MSW of local address space 1 bus region descriptor	4013h
56h	LSW of local address space 1 bus region descriptor	F940h
58h	MSW of local address space 2 bus region descriptor	0000h
5Ah	LSW of local address space 2 bus region descriptor	0000h
5Ch	MSW of local address space 3 bus region descriptor	0080h
5Eh	LSW of local address space 3 bus region descriptor	0000h
60h	MSW of expansion ROM bus region descriptor	0000h
62h	LSW of expansion ROM bus region descriptor	0000h
64h	MSW of chip select 0 base address	0BFFh
66h	LSW of chip select 0 base address	FFC1h
68h	MSW of chip select 1 base address	0000h
6Ah	LSW of chip select 1 base address	4001h
6Ch	MSW of chip select 2 base address	0000h
6Eh	LSW of chip select 2 base address	0000h
70h	MSW of chip select 3 base address	0000h
72h	LSW of chip select 3 base address	0000h
74h	Serial EEPROM write-protected address boundary	0030h
76h	LSW of interrupt control/status	0041h
78h	MSW of target response, serial EEPROM, and initialization control	0870h
7Ah	LSW of target response, serial EEPROM, and initialization control	0000h
7Ch	MSW of general purpose I/O control	0024h
7Eh	LSW of general purpose I/O control	9864h
80h	MSW of hidden 1 power management data select	0000h
82h	LSW of hidden 1 power management data select	0000h
84h	MSW of hidden 2 power management data select	0000h
86h	LSW of hidden 2 power management data select	0000h

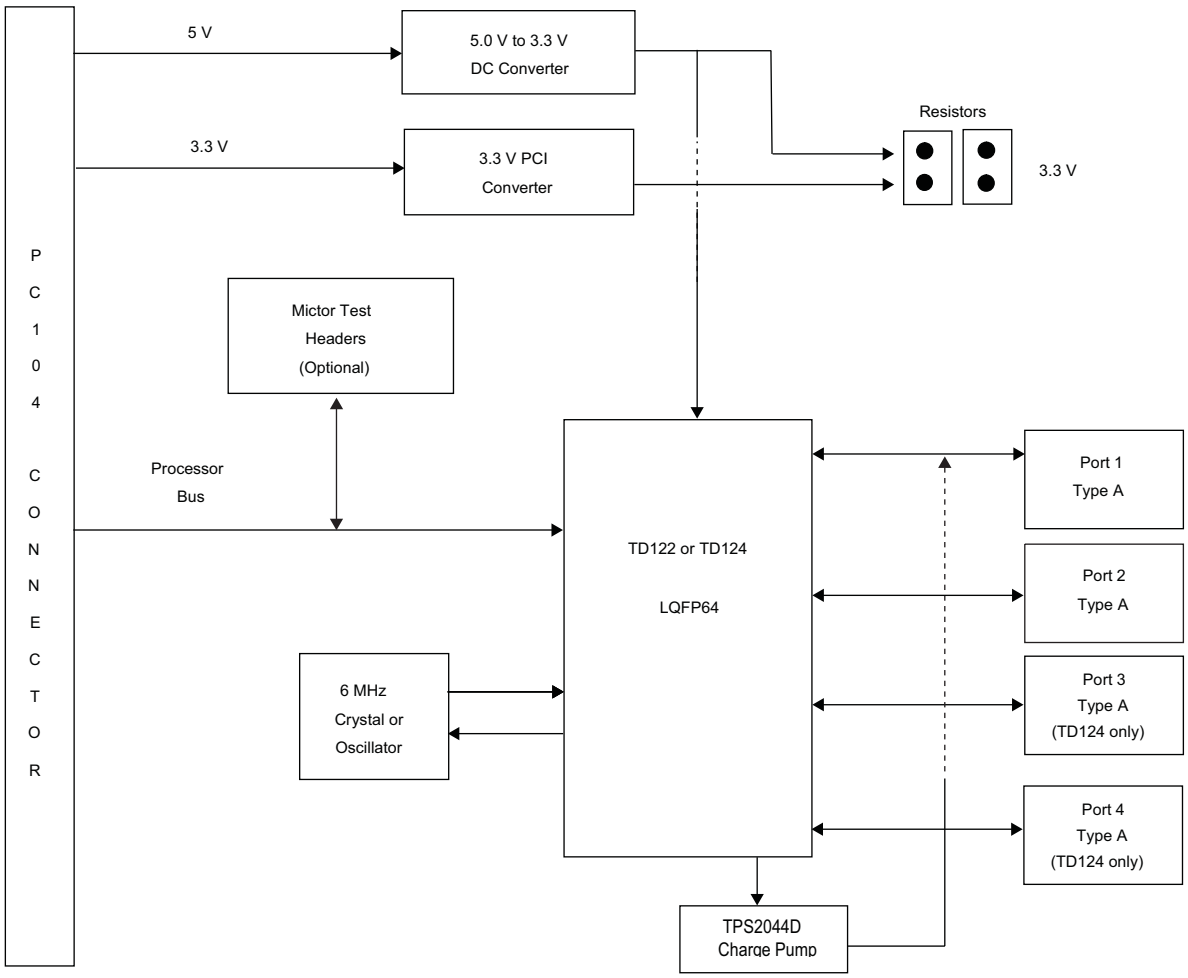
EVB12x Hardware Operation and Configuration

This chapter describes the hardware operation and configuration options available for the EVB12x in stand-alone mode (that is, without the PCI104 bridge board).

For details on how the EVB12x fits in to the EV-TD12x-PCI, see Chapter 1 Introduction.

These options enable you to directly connect the TD122 or TD124 to an embedded processor or CPU using a local bus. The use of this board without the PCI bridge card increases performance and enables you to develop drivers in real-world applications of the product. Figure 2-1 shows the EVB12x block diagram.

Figure 2-1 EVB12x Block Diagram



Board Operation Requirements

When used with the PCI104 board, the EVB12x board is powered by the PCI bus.

When the EVB12x board is used without the PCI104, the EVB12x requires a DC power source capable of supplying 5 V ± 10% at 1.0 A through a power switch.

Power Supply

Power can be supplied at 5 V or 3.3 V.

5 V Power Supply

The EVB12x 5 V power is supplied by one of the following sources (the source is resistor selectable):

- From the PC104 connector, by installing R54 and R55 (0 Ω) near the PC104 connector (default setting)
- From an external power supply connected to JP9.3. Protection circuitry is not provided (remove R54 and R55)

3.3 V Power Supply

The EVB12x 3.3 V power is supplied by one of the following sources:

- From U12, a 5 V-to-3.3 V DC converter (default setting).
- From the PC104 connector. Install R47 (0_1206 Ω; 0 Ω 1206 footprint) and remove R49
- From an external power supply connected to the test pin on JP7.3. Protection circuitry is not provided (remove R47 and R49)

Reset

The /RESET pin of the TD122 or TD124 is connected to the PC104 connector. You can control /RESET through a CPU GPIO.

D_P/D_M Signals

Each of the D_P/D_M pairs has a 2 pin, 0.1 inch spacing, connector to support attachment of a differential probe (JP1-JP4).

These traces are impedance controlled to 90 Ω $\pm$ 10%.

LEDs

To enable monitoring of the normal operation of the board, the EVB12x has the following LEDs :

- D1-D4–Type A VBUS power indicator
- D5–3.3 V power rail indicator
- D6–5 V power rail indicator

Oscillator Input

We recommend you use a 6 MHz crystal, instead of a crystal oscillator to lower EMI. The only footprint provided in the EVB12x board uses a 6 MHz crystal located at Y1 (Ecliptek Corp., E2SAA18-6.000M, 18 pF internal load).

Mounting Holes

The EVB12x board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146 inch in diameter. The placement matches the PCI104 PCI board which together with the EVB12x make the EV-TD12x-PCI.

Test Points

The following test points are furnished on the EVB12x:

- Ground Test Points JP5, JP6, JP8, and JP10
- Power Test Points TP1-TP4, TP5

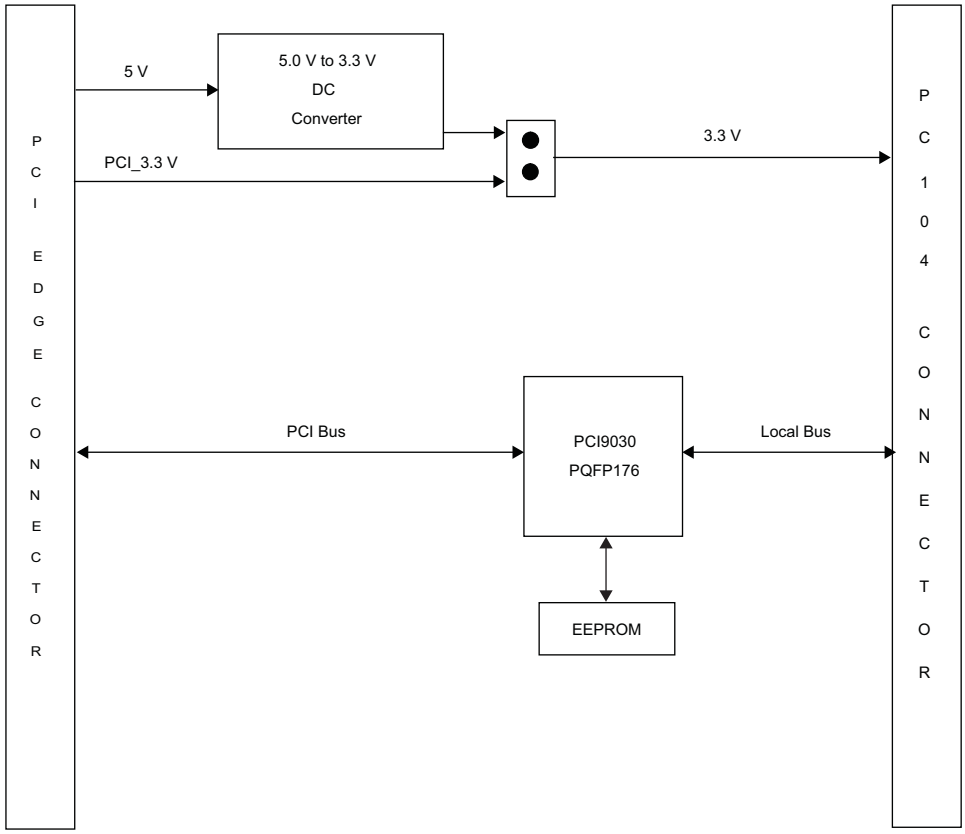
PCI104 Bridge Board

The PCI104 contains a PLX Technology PCI9030 bridge chip, an Atmel AT93C66A-10PI-2.7 EEPROM, a ROM socket, and three connectors.

For details on how the PCI104 fits with the EVB12x to make up the EV-TD12x-PCI, see Chapter 1 Introduction.

The PCI104 board bridges between the PCI bus and a local bus. The local bus is routed out to the standard PC104 connectors (J1 and J2). The EVB12x interfaces to the PCI104 bridge card using these three female connectors. Another proprietary, non-PC104 connector (J3) supports a 32 bit interface and additional signals not included in the PC104 signal definition. Figure 3-1 shows the PCI104 block diagram.

Figure 3-1 PCI104 Bridge Board



The PCI104 board uses the PCI9030 bridge device. The PCI configuration registers are stored in an on-board EEPROM.

Power Supply

The PCI104 board 5 V power supply is from the standard PCI bus edge connector (U2 – eight 5 V pins). The 5 V supply is routed directly to the TD122 using the PC104 connectors (J1.D16, J2.B3, J2.B29).

The PCI104 board 3.3 V power is supplied by one of the following sources:

- 5.0 V-to-3.3 V DC regulator (U1). Install jumper on JP2 pin 1-2, 3-4 (default setting)
- The standard PCI bus edge connector (U2 – twelve 3.3 V pins). Install jumper on JP2 pin 5-6, 7-8

Local Bus Configuration

The PCI9030 local bus is connected directly to the EVB12x board using the PC104 connectors. For a detailed explanation of its operation, see the *PCI9030 Data Book*.

PCI9030 CS1L chip select is routed to the EVB12x. Register space 1 of the PCI9030 controls CS1L. The number values programmed into space 1 registers of the EEPROM are:

- Space 1 range 0xFFFF_F000
- Space 1 remap 0x0000_0001
- Space 1 descriptor 0x4013_F940
- Space 1 base address 0x0000_0801
- Space 1 initialization control 0x0030_0041

To change the values in the EEPROM, you need an application from PLX operating across the PCI bus. Space 1 has 8 bit local and PCI space and contains 4 Kb memory space size. There is no prefetch on space 1.

Local Bus Speed

LCLK, the local bus clock, operates at frequencies up to 60 MHz and is asynchronous to the PCI bus clock, BCLK. BCLK is routed back into LCLK, setting the default local bus speed at 33 MHz.

An oscillator up to 60 MHz can be soldered at the U4/U5 dual-footprint by the customer to increase the local bus speed. R10 (33 Ω) must be installed and R11 removed in this configuration. More WAIT states may have to be added to meet the TD122 or TD124 interface timing when increasing the local bus frequency.

LEDs

The PCI104 has two LEDs to enable verification of the normal operation of the board:

- D1–3.3 V power rail indicator
- D2–5.0 V power rail indicator

Mounting Holes

The PCI104 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146” in diameter. The placement matches the EVB12x evaluation board which together with the PCI104 make the EV-TD12x-PCI.

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Schematics

This chapter provides the EVB12x and PCI104 schematics. U10 is shown as a **TD12x**, which refers to either the TD122 or TD124 USB host controller.

Figure 4-1 EVB12x Top-Level Schematic

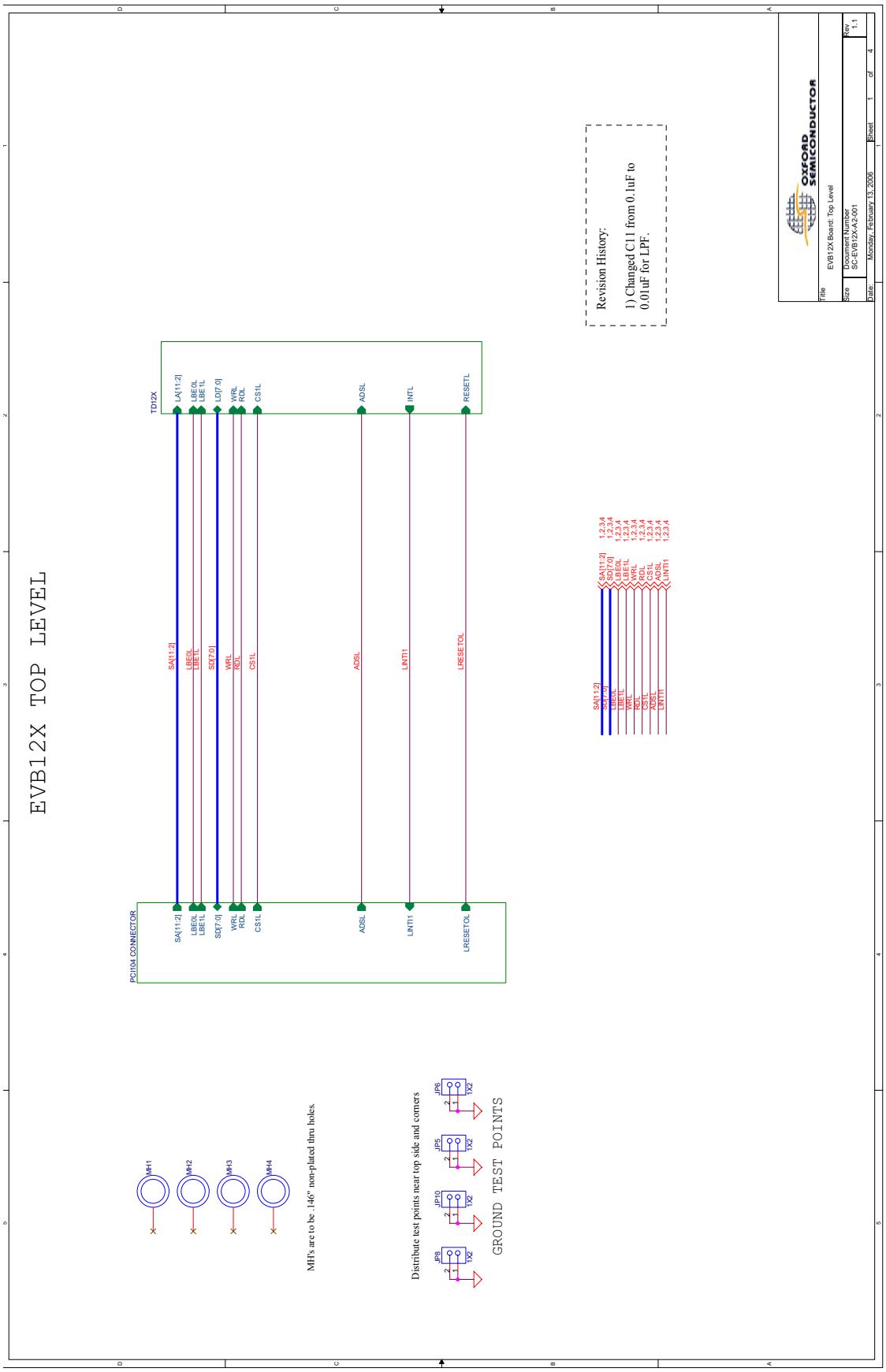

Figure 4-2 EVB12x Test Headers

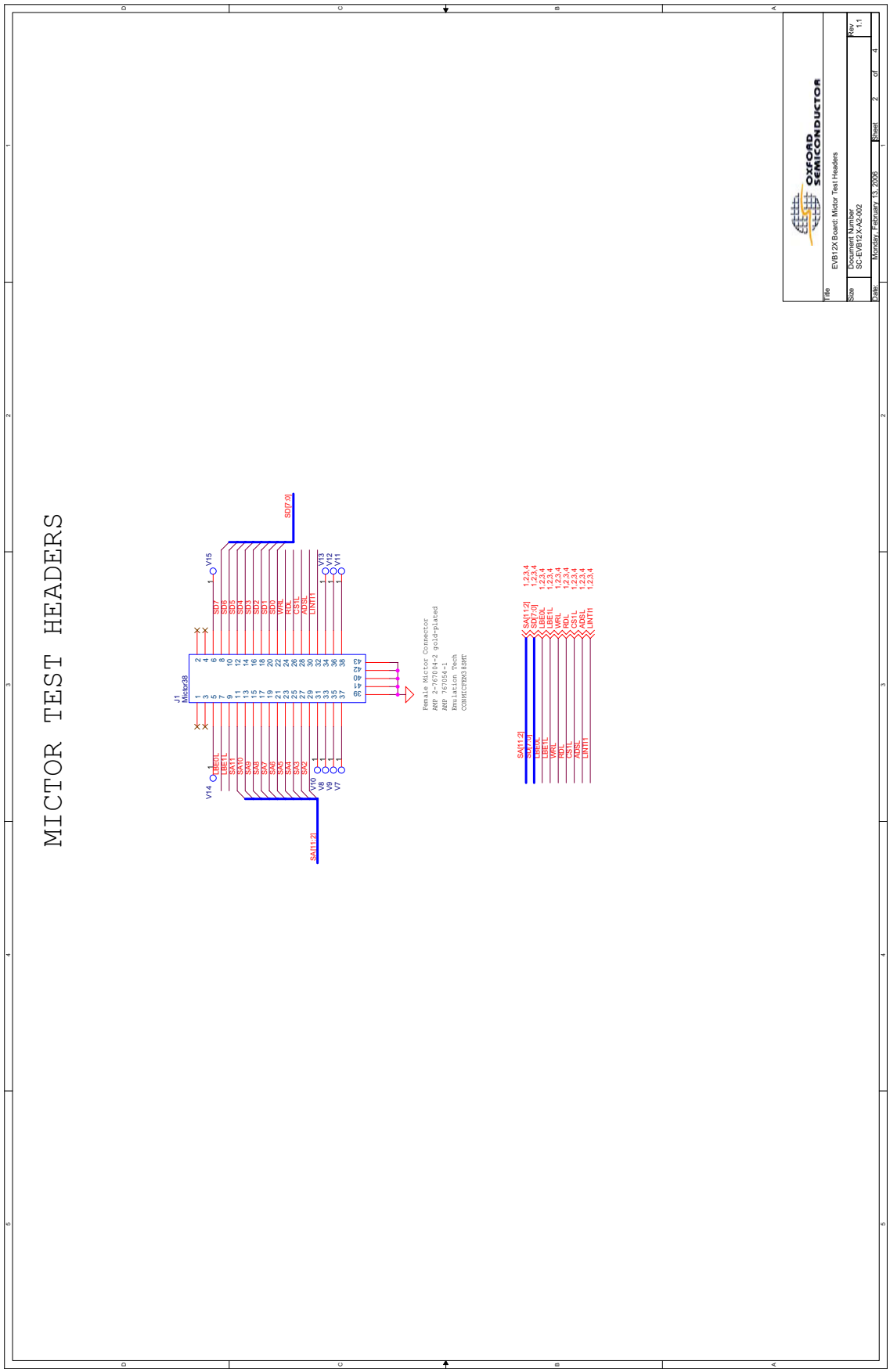

Figure 4-3 EVB12x PC104 Connector

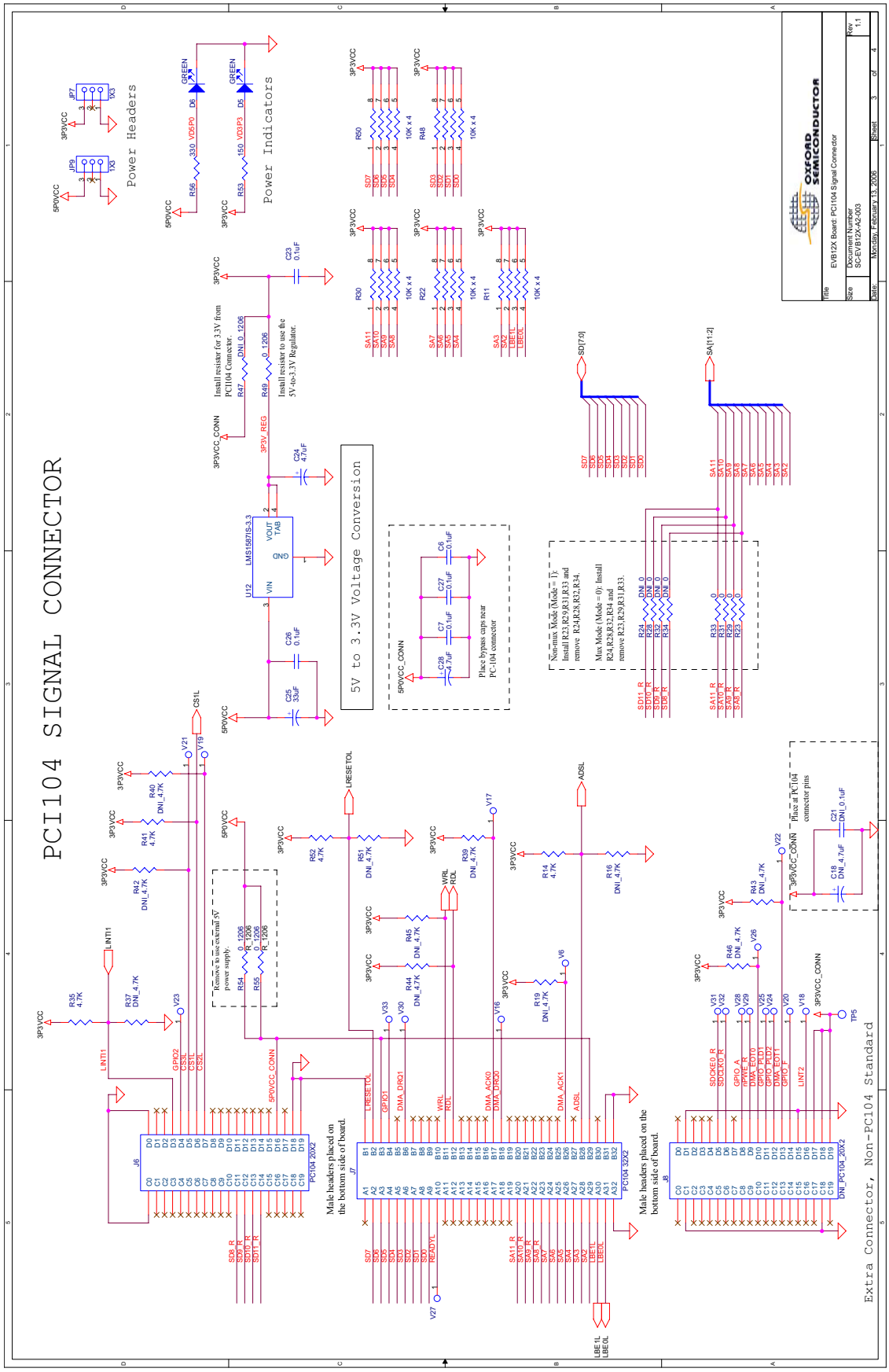

Figure 4-4 EVB12x - TD12x and USB Ports Schematic

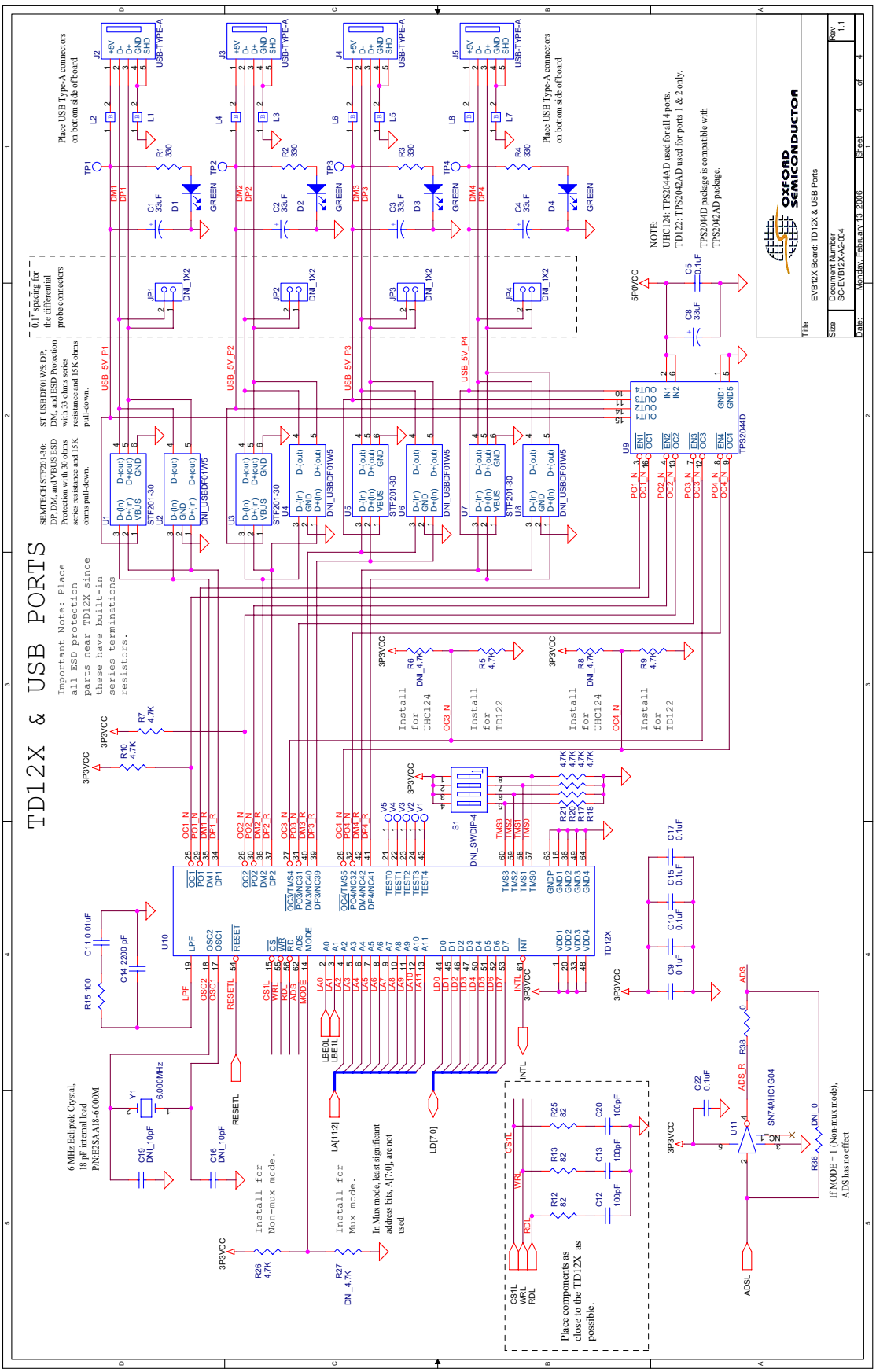

Figure 4-5 PCI104 Top-Level Schematic

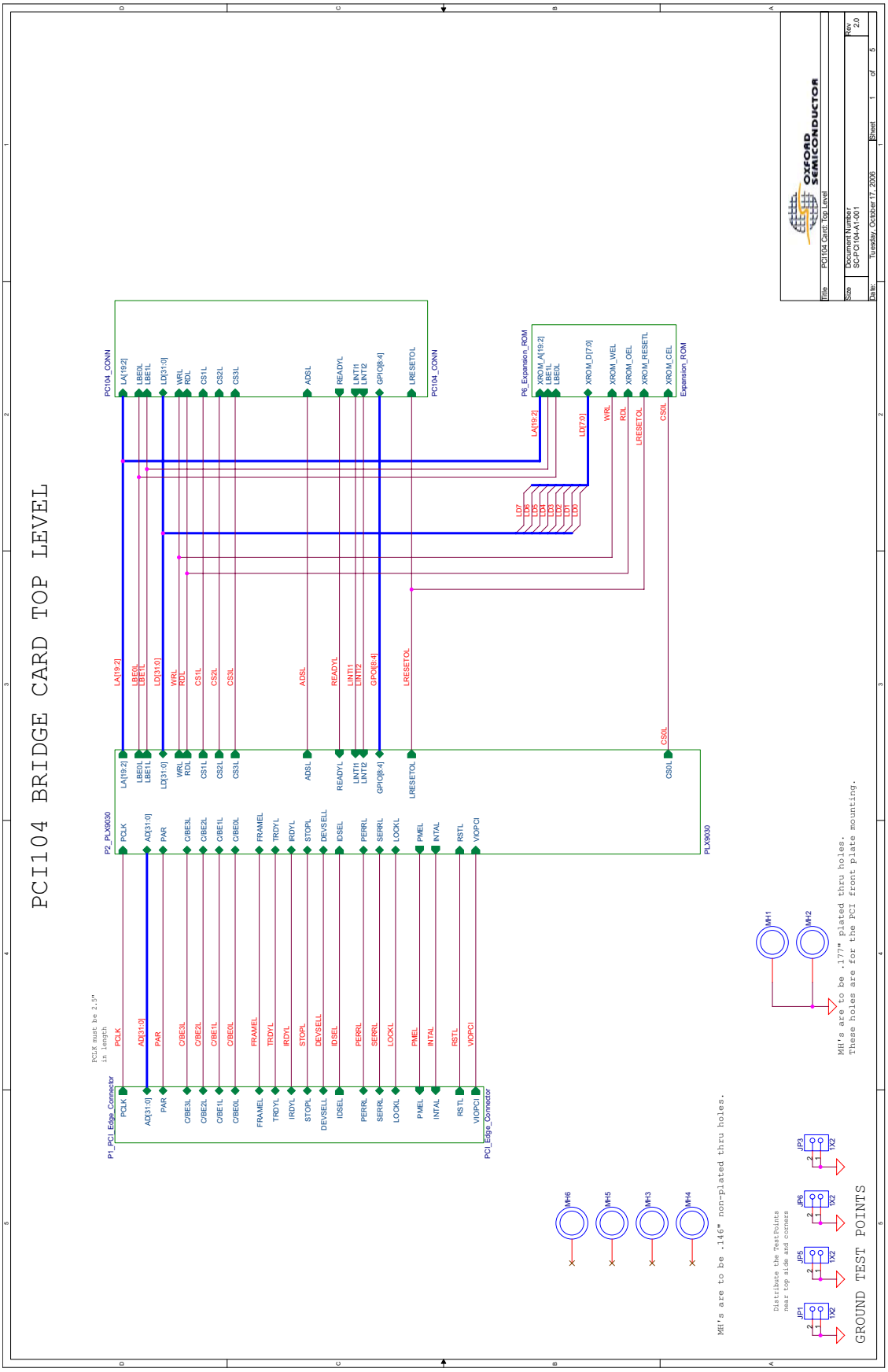

Figure 4-6 PCI104 PCI Connector

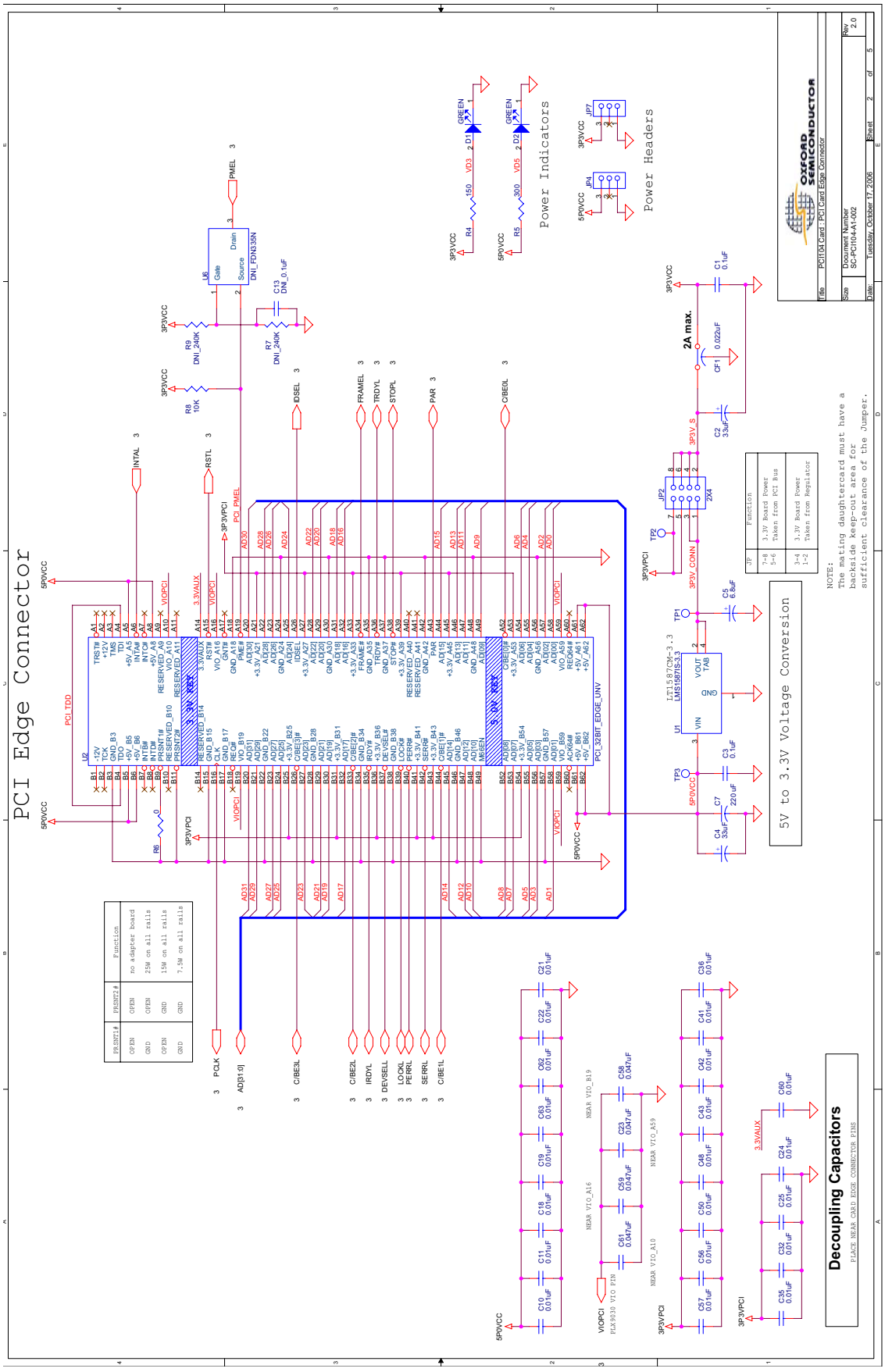

Figure 4-7 PCI9030 Bridge Chip

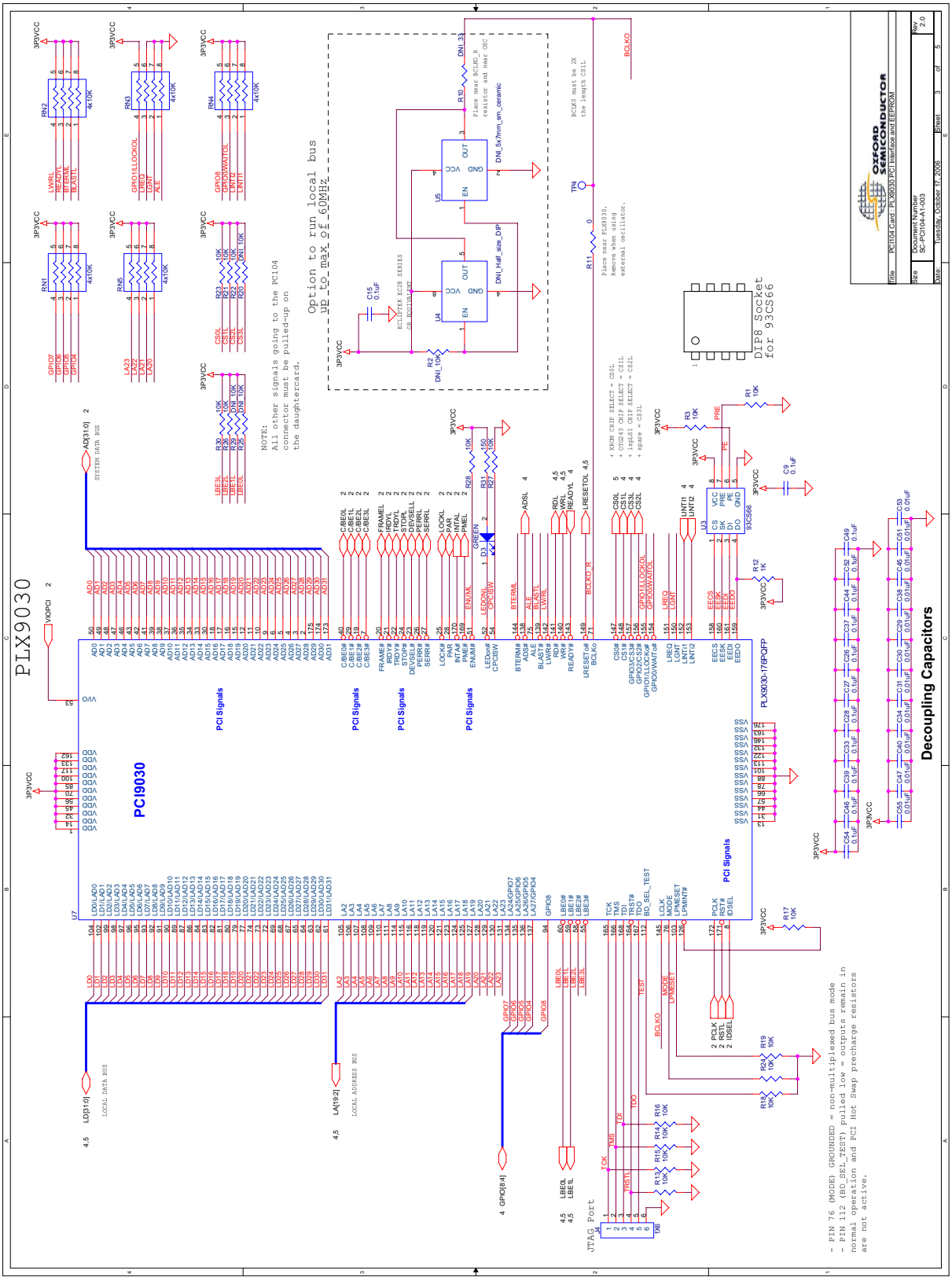

Figure 4-8 PC104 Connectors

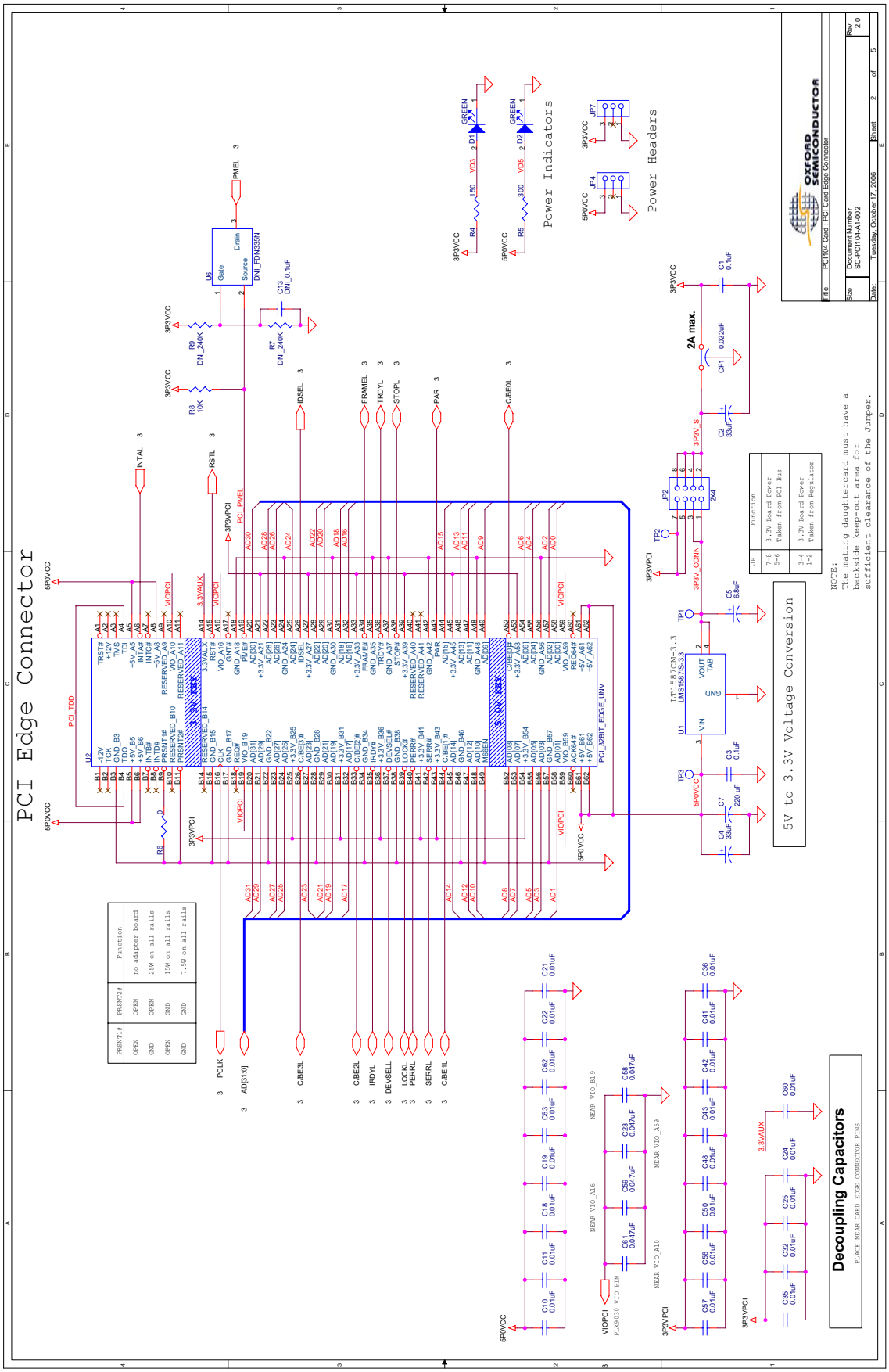

Figure 4-9 PC104 Expansion ROM