OXFORD SEMICONDUCTOR

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EV-OXU210-PCI and EV-OXU210 Evaluation Board User Guide

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HI-SPEED CERTIFIED USB

Contents

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This manual documents the EV-OXU210-PCI and EV-OXU210 Evaluation Board hardware.

Revision Information

Table I documents the revisions of this manual

Table I Revision Information

Revision	Modification
Jul 2006	First publication
Aug 2006	In the Overview section, added “, the PCI104” to the end of the second bullet. In Table 1-3, corrected the default values for offsets 2Ch, 54h, 56h, and 68h. In Figure 2-1, changed “Charge Pump” to “Power Switch”. In the V_{BUS} Source section, added “to select the TPS2044BD” at the end of the first bullet. In the V_{BUS} Source section, corrected a few port numbers. In the Local Bus Configuration section, changed “256 Kb memory space size “ to “128 Kb memory space size” . In the Schematics chapter, replaced the Rev. 1.0 schematics with Rev. 2.1 schematics. Change the footer to read “External—Free Release”
Nov 2006	In the Preface, deleted “development kit” in the first sentence. Updated the schematics in Figure 4-1 through Figure 4-8 to Revision 2.2
Feb 2007	Changed the corporate address on the cover page. Added the Certified USB logo to the cover page. In the Test Points section, changed the AMP/Tyco Electronics part number from “2-767004-2” to “2-5767004-2”

Typographic Conventions

In this manual, the conventions listed in Table II apply.

Table II Typographic Conventions

Convention	Meaning
Italic Letters With Initial Capital Letters	A cross-reference to another publication
`Courier Font`	Software code, or text typed in via a keyboard
1, 2, 3	A numbered list where the order of list items is significant
■	A list where the order of items is not significant
"Title"	Cross-refers to another section within the document
	Significant additional information

Ordering Information

The following boards are available:

- EV-OXU210-PCI Evaluation Board (EV-OXU210-PCI-110)
- EV-OXU210 Evaluation Board (EV-OXU210-110)
- PCI104 Bridge Board (TDPCI104-1000-01)

Contacting Oxford Semiconductor

See the Oxford Semiconductor website (http://www.oxsemi.com) for further details about Oxford Semiconductor devices, or email sales@oxsemi.com.

Chapter 1

EV-OXU210-PCI

Overview

The EV-OXU210-PCI Evaluation Board is a system for OXU210HP customer evaluations and internal software development in the PC environment. The EV-OXU210-PCI Evaluation Board allows the user to install and use the EV-OXU210 in any PCI-based computer. Application software running on the system has access to the OXU210HP via the PCI memory space.

The EV-OXU210-PCI Evaluation Board is a two-board combination of the following:

- An EV-OXU210 Evaluation Board
- A 33 MHz, 32-bit PCI Bridge Board, the PCI104

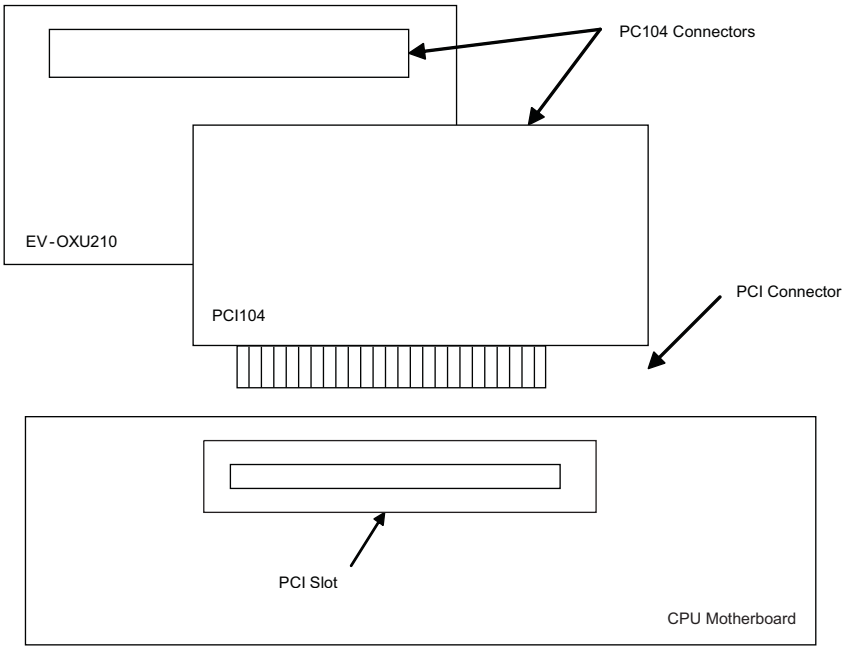
The EV-OXU210 Evaluation Board contains the OXU210HP and all the USB-specific hardware.

The PCI104 Bridge Board contains a PCI-to-local-bus bridge chip that bridges the PCI bus to the OXU210HP. Power and control signals to the PCI bus are maintained by the PCI bridge chip set, while initialization and configuration of the PCI bridge chip is maintained by the on-board serial EEPROM.

Figure 1-1 illustrates the orientation of the two boards. The combined boards are approximately one inch thick and require space for two PCI devices, but only one PCI slot. The OXU210HP OTG and host USB connectors are easily accessible through the openings in the computer case.

Chapter 2 describes the EV-OXU210 Evaluation Board. Chapter 3 describes the PCI104 Bridge Board. For complete information about the OXU210HP device, see the *OXU210HP Hardware Reference Manual*.

Figure 1-1 EV-OXU210-PCI System Board Orientation



PCI Operation

Every PCI implementation has a PCI configuration space, where the PCI configuration registers are found. PCI configuration registers are accessed with read/write to configuration space, which is separate from memory and I/O space. Table 1-1 lists the standard PCI configuration register space for all PCI functions on the PCI bus.

Table 1-1 Standard PCI Configuration Register Space

Byte 3	Byte 2	Byte 1	Byte 0	Offset
Device ID		Vendor ID		00h
Status Register		Command Register		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Register 0 (BAR 0)				10h
Base Address Register 1 (BAR 1)				14h
Base Address Register 2 (BAR 2)				18h
Base Address Register 3 (BAR 3)				1Ch
Base Address Register 4 (BAR 4)				20h
Base Address Register 5 (BAR 5)				24h
CardBus CIS Pointer				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capabilities Pointer	34h

Table 1-1 Standard PCI Configuration Register Space				
Byte 3	Byte 2	Byte 1	Byte 0	Offset
Reserved				38h
Max Latency	Min Grant	Interrupt Pin	Interrupt Line	3Ch

The PCI104 can be identified on the PCI bus during enumeration by the following PCI configuration registers:

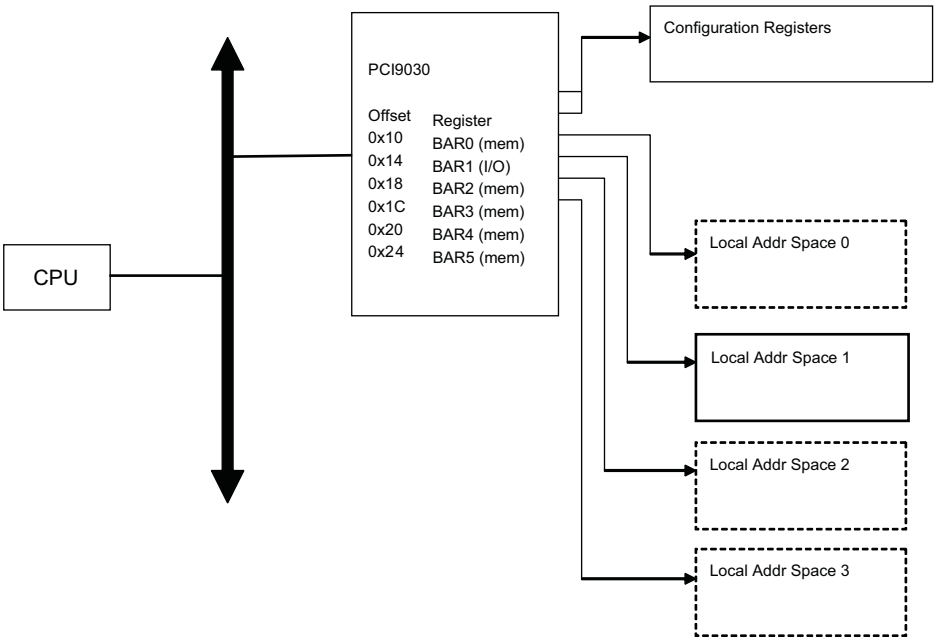
Table 1-2 PCI Configuration Registers	
Register	Power-On Value
Vendor ID	192Eh
Device ID	032Bh
Revision	0001h
Class Code	0680h
Subsystem ID	032Bh
Subsystem Vendor ID	192Eh

Most operating systems provide functions for finding devices on the PCI bus. These functions typically key off the Vendor and Device IDs, or the Class Code. Because the Class Code for the PCI104 appears as a PCI Bridge with sub class code “other”, the search should be keyeed to the Vendor and Device IDs.

Configuration

The EV-OXU210-PCI has two memory mapped register spaces and one I/O mapped register space. The address locations of the various spaces are determined by the Base Address Registers of the bridge controller registers. Base Address Register 0 (BAR0) of the PCI bridge controller registers contains the address of the memory mapped PCI bridge controller registers. BAR1 contains the I/O address for the same PCI bridge controller registers. The PCI bridge controller registers are mapped into both memory and I/O space, so that these registers can be accessed via memory accesses or I/O addressing. BAR3 contains the address of the memory mapped OXU210HP registers. Figure 1-2 illustrates the register mappings within a PCI system.

Figure 1-2 PCI104 Register Mappings



The Base Address Registers are typically initialized by the system BIOS or by the operating system. Software generally does not have to manually set the addresses of the mapped locations, however, this is system dependent. If these registers are not initialized, the three spaces should be manually mapped into system memory and I/O space accordingly. Care must be taken to ensure no conflicts exist between the mapped regions and other devices on the PCI bus.

Serial EEPROM Registers

The PCI9030 PCI bridge controller provides an interface to program the attached serial EEPROM. The serial EEPROM should be pre-programmed with the default values in Table 1-3. The table is for informational purposes only. If the default values are modified, the behavior of the PCI104 will change.

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
00h	PCI Device ID	032Bh
02h	PCI Vendor ID	192Eh
04h	PCI Status Register	0290h
06h	PCI Command Register	Reserved
08h	PCI Class Code	0680h
0Ah	PCI Class Code / Revision Number	0001h
0Ch	PCI Subsystem ID	032Bh
0Eh	PCI Subsystem Vendor ID	192Eh
10h	MSB New Capability Pointer	Reserved
12h	LSB New Capability Pointer	0040h

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
14h	(Maximum Latency and Minimum Grant are not loadable)	Reserved
16h	Interrupt Pin (Interrupt Line Routing is not loadable)	0100h
18h	MSW of Power Management Capabilities	4801h
1Ah	LSW of Power Management Next Capability Pointer / Power Management Capability ID	4801h
1Ch	MSW of Power Management Data /PMCSR Bridge Support Extension	Reserved
1Eh	LSW of Power Management Control/Status	0000h
20h	MSW of Hot Swap Control/Status	Reserved
22h	LSW of Hot Swap Next Capability Pointer / Hot Swap Control	4C06h
24h	PCI Vital Product Data Address	Reserved
26h	PCI Vital Product Data Next Capability Pointer / PCI Vital Protocol Data Control	0003h
28h	MSW of Local Address Space 0 Range	0000h
2Ah	LSW of Local Address Space 0 Range	0000h
2Ch	MSW of Local Address Space 1 Range	FFFEh
2Eh	LSW of Local Address Space 1 Range	0000h
30h	MSW of Local Address Space 2 Range	0000h
32h	LSW of Local Address Space 2 Range	0000h
34h	MSW of Local Address Space 3 Range	0000h
36h	LSW of Local Address Space 3 Range	0000h
38h	MSW of Expansion ROM Range	0000h
3Ah	LSW of Expansion ROM Range	0000h
3Ch	MSW of Local Address Space 0 Local Base Address (Remap)	0000h
3Eh	LSW of Local Address Space 0 Local Base Address (Remap)	0000h
40h	MSW of Local Address Space 1 Local Base Address (Remap)	0000h
42h	LSW of Local Address Space 1 Local Base Address (Remap)	0001h
44h	MSW of Local Address Space 2 Local Base Address (Remap)	0000h
46h	LSW of Local Address Space 2 Local Base Address (Remap)	0000h
48h	MSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ah	LSW of Local Address Space 3 Local Base Address (Remap)	0000h
4Ch	MSW of Expansion ROM Local Base Address (Remap)	0010h
4Eh	LSW of Expansion ROM Local Base Address (Remap)	0000h
50h	MSW of Local Address Space 0 Bus Region Descriptor	0080h
52h	LSW of Local Address Space 0 Bus Region Descriptor	0000h
54h	MSW of Local Address Space 1 Bus Region Descriptor	4080h
56h	LSW of Local Address Space 1 Bus Region Descriptor	A040h
58h	MSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ah	LSW of Local Address Space 2 Bus Region Descriptor	0000h
5Ch	MSW of Local Address Space 3 Bus Region Descriptor	0080h
5Eh	LSW of Local Address Space 3 Bus Region Descriptor	0000h

Table 1-3 Serial EEPROM Registers

Serial EEPROM Offset	Description	Default
60h	MSW of Expansion ROM Bus Region Descriptor	0000h
62h	LSW of Expansion ROM Bus Region Descriptor	0000h
64h	MSW of Chip Select 0 Base Address	0BFFh
66h	LSW of Chip Select 0 Base Address	FFC1h
68h	MSW of Chip Select 1 Base Address	0001h
6Ah	LSW of Chip Select 1 Base Address	0001h
6Ch	MSW of Chip Select 2 Base Address	0000h
6Eh	LSW of Chip Select 2 Base Address	0000h
70h	MSW of Chip Select 3 Base Address	0000h
72h	LSW of Chip Select 3 Base Address	0000h
74h	Serial EEPROM Write-Protected Address Boundary	0030h
76h	LSW of Interrupt Control/Status	0041h
78h	MSW of Target Response, Serial EEPROM, and initialization Control	0870h
7Ah	LSW of Target Response, Serial EEPROM, and initialization Control	0000h
7Ch	MSW of General Purpose I/O Control	0024h
7Eh	LSW of General Purpose I/O Control	9864h
80h	MSW of Hidden 1 Power Management Data Select	0000h
82h	LSW of Hidden 1 Power Management Data Select	0000h
84h	MSW of Hidden 2 Power Management Data Select	0000h
86h	LSW of Hidden 2 Power Management Data Select	0000h

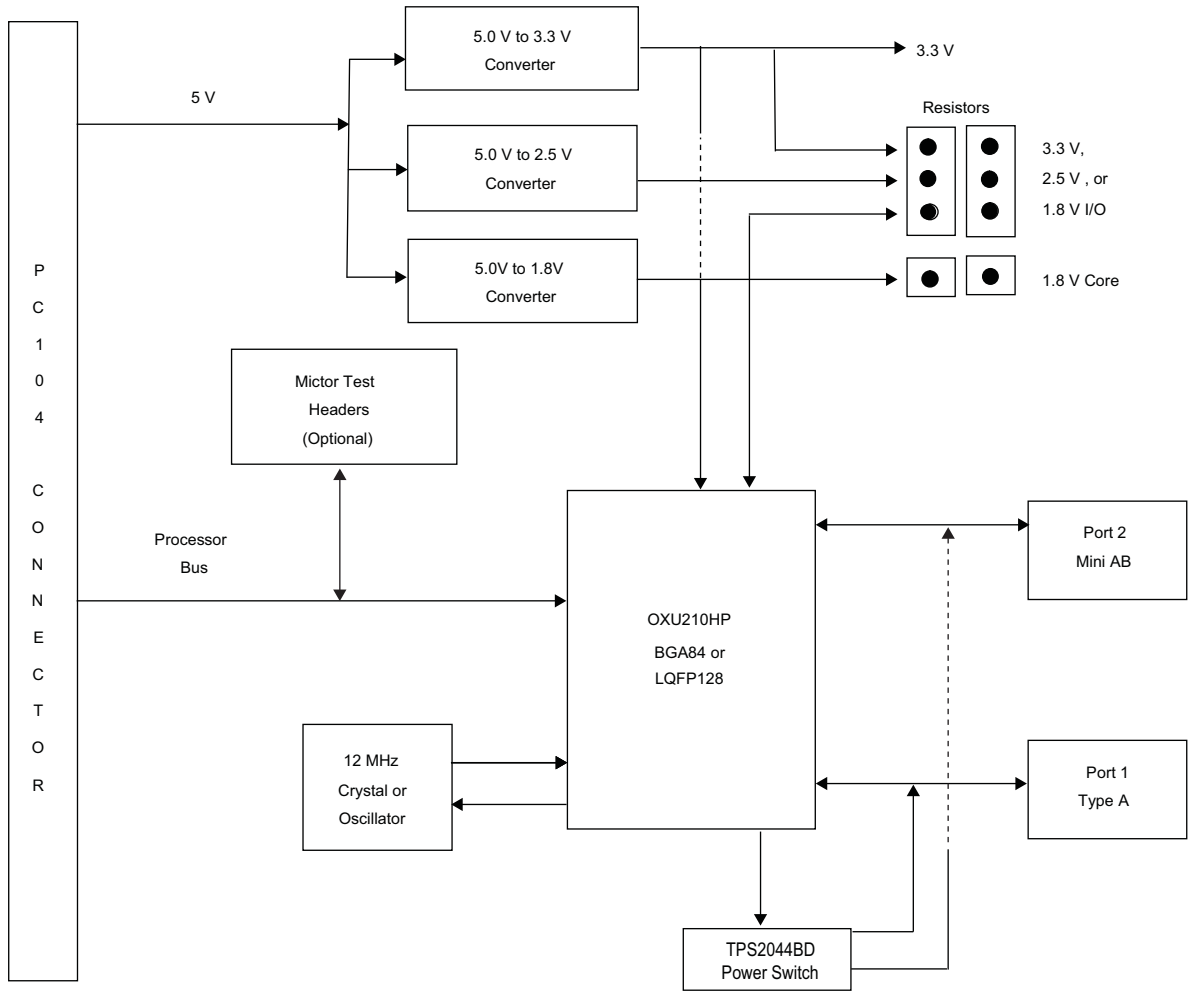
Chapter 2

EV-OXU210 Evaluation Board

Overview

This chapter describes the hardware operation and configuration options available for the EV-OXU210 in stand-alone mode. These options allow customers to directly connect the OXU210HP to their embedded processor or CPU without going through a PCI bus. The use of this board without the PCI bridge card increases performance and allows driver development in real-world applications of the product. Figure 2-1 shows the EV-OXU210 block diagram.

Figure 2-1 EV-OXU210 Block Diagram



Board Operation Requirement

The EV-OXU210 requires a DC power source capable of supplying 5 V ±10% at 1.0 A through a power switch.

OTG & Host Port Configurations

The EV-OXU210 supports both OXU210HP port configurations. Port 1 of the OXU210HP can function as either a host port, a peripheral port, or a full OTG port.

To select between the high-speed OTG or host-only modes, select one of these configurations:

- Install jumper on JP4 pin 1-2 (host-only mode).
- Install jumper on JP4 pin 2-3 (OTG mode).

High-speed USB host (Port 2) is fixed as a standard host mode. Refer to "VBUS Source" on page 2-5 for further configuration details.

Default Configurations

Zero-Ohm resistors are used to set the following factory default configurations:

- R10, R11 (0 Ω) populated to route 5 V from the PCI104 connectors
- R15, R16 (0 Ω) populated, R14 removed to use on-board 12 MHz crystal
- R18-R21 (0 Ω) populated for D_P/D_M signals
- R62 and R64 (0 Ω) populated for analog and digital 3.3 V
- R66 (0 Ω) populated, R67 and R68 removed to set V_{IO} to 3.3 V. Note that the V_{IO} wide range I/O power supply is named MVCC on the schematics
- R65 (0 Ω) populated to use 1.8 V voltage regulator for the 1.8 V core
- R42-R45 (0 Ω) populated to route DMA signals from PC104 connector to OXU210HP
- R46-R47, R53-R54 (0 Ω) populated to route INTL, WRL, RDL, and CS1L from PC104 connectors to OXU210HP
- R6 (0 Ω) populated, R5 removed to use the TPS2044BD 500 mA power switch (U1) as the source of V_{BUS} in OTG or host mode

Power Distribution

In the default mode, the EV-OXU210 receives all its power from the 5 V pins of the PC104 connector. The 5 V supply drives the 3.3 V, 2.5 V, and 1.8 V voltage regulators. Alternative power-supply options are described below. Note that the V_{IO} wide range I/O power supply is named MVCC on the schematics.

5 V Power Supply

The EV-OXU210 5 V power is supplied by one of two sources:

1. The PC104 connector 5 V pins: J6.D16, J7.B3, J7.B29 (default setting).
2. An external power supply connected to JP8.3. To enable this mode, remove R10 (0 Ω) and R11 (0 Ω). Protection circuitry is not provided.

3.3 V Power Supply

The EV-OXU210 3.3 V power is supplied by one of two sources:

1. 5 V-to-3.3 V DC regulator (U11). R62 (0 Ω) and L2 are installed to limit analog 3.3 V and allow current flow in the digital 3.3 V (default setting).

2. An external power supply connected to JP6.3. To enable this mode, remove R64 (0 Ω). Protection circuitry is not provided.

1.8 V Core Power Supply

The EV-OXU210 1.8 V power is supplied by one of two sources:

1. An on-board 5.0 V-to-1.8 V DC voltage regulator (U13). This is the default setting with R65 (0 Ω) installed.
2. An external power supply connected to JP7.3. To enable this mode, remove R65 (0 Ω). Protection circuitry is not provided.

3.3/2.5/1.8 V V_{IO} Wide Range I/O Power Supply

The EV-OXU210 provides either 1.8 V or 3.3 V for V_{IO}, the wide range power. The voltage is selected through the intallation or removal of resistors as described below. The EV-OXU210 gives the option of 3.3 V, 2.5 V, or 1.8 V through resistor settings. Any other value within this range is customer specific and is not directly supported by this evaluation board. The EV-OXU210 V_{IO} power is supplied by one of three sources:

1. From the 3.3 V power rail (default setting). Install R66 (0 Ω) and remove R67 (0 Ω) and R68 (0 Ω).
2. From the 2.5 V power rail. Install R68 (0 Ω) and remove R66 (0 Ω) and R67 (0 Ω).
3. 5.0 V-to-1.8 V DC regulator (U13). Install R67 (0 Ω) and remove R66 (0 Ω) and R68 (0 Ω).

Oscillator Input

The EV-OXU210 uses a 12 MHz crystal at Y1 for the OXU210HP XSCI/XSCO clock source. The external 22 pF capacitors are used to control the stability of the frequency and startup time.

A 12 MHz oscillator can be soldered at the U3/U4 dual-footprint by the customer and used as the OXU210HP clock source. To enable this mode, install R14 (33 W) and remove R15 (0 Ω). Also, remove R16 (0 Ω) because the XSCO pin must be floating in this configuration. Below are the part numbers that Oxford Semiconductor has used for internal design and testing. Other components meeting the OXU210HP requirements may be used (see the *OXU210HP, OXU140CM, OXU121HP, and OXU200 External Crystal Selection* application note).

- 12 MHz Crystal: Citizen America, HCM49-12.000MABJT, 18 pF internal load (or RoHS compliant HCM49-12.000MABJUT)
- 12 MHz Oscillator: Ecliptek, EH1345HSTS-12.000M, 50 ppm, 8-pin DIP (RoHS compliant)

V_{BUS} Source

V_{BUS} in Host Port Configuration

When the OXU210HP is in host configuration under OTG Port 1 (J4), the EV-OXU210 drives V_{BUS} via the TPS2044BD 500 mA Power Switch (U1), using the OXU210HP PO_N signal. Since Port 2 (J5) is a fixed host port, it is always driven by the TPS2044BD. To configure Port 1 (J4) for host port configuration, follow these steps:

- R6 (0 Ω) is installed and R5 is removed to select the TPS2044BD (default setting, charge pump not used).
- Install jumper on JP4 pin 1-2 (host-only mode).

V_{BUS} in OTG Port Configuration

When the OXU210HP is in OTG configuration, the EV-OXU210 can drive V_{BUS} for the OTG Port 1 (J4) with one of two sources:

1. The TPS2044BD 500 mA Power Switch (U1) using the OXU210HP EXT_VBO signal (default setting)
   - Install R6 (0 Ω) and remove R5
   - Install jumper on JP4 pin 2-3 (OTG mode)
2. The OXU210HP internal 100 mA charge pump
   - Install R5 (0 Ω) and remove R6
   - Install jumper on JP4 pin 2-3 (OTG mode)

OXU210HP Reset

The /RESET of the OXU210HP is brought out to the PC104 connector to allow control of the /RESET through a CPU GPIO. Push button S2 can also be used to assert /RESET manually.

D_P/D_M Signals

- R18-R21 (0 Ω) are installed
- Each of the D_P/D_M pairs has an external ESD protection device (U14, U15). The ID pin may also be protected by this device. Refer to the Oxford Semiconductor *OXU210HP External ESD Protection* application note for more detail
- Refer to the Oxford Semiconductor *OXU210HP Layout Requirements* application note for more detail

V_{BUS} Over-Voltage Protection

Besides the ESD transient protection provided by the external ESD devices, the OXU210HP V_{BUS} pin is also protected against steady-state voltages above 5.1 V (typical) by the voltage divider resistor (R23 = 390 Ω) and the Zener diode D4. When the OXU210HP is configured as a B-device in OTG mode and is connected to a host driving V_{BUS} greater than 5.1 V, the Zener diode protects the OXU210HP from damage.

- Zener diode: ON Semiconductor® BZX84C5V1LT1, 225mW, 5.1 V breakdown

LEDs

The EV-OXU210 has the following LEDs to enable monitoring of the normal operation of the board:

- D9: 5.0 V Power Rail indicator
- D7: 3.3 V Power Rail indicator
- D8: 1.8 V Power Rail indicator
- D1: V_{BUS} Power indicator for OTG port
- D2: V_{BUS} Power indicator for host port

Mounting Holes

The EV-OXU210 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146 inch in diameter. The placement matches the PCI104 PCI board which together make the EV-OXU210-PCI.

Test Points

The following test points are furnished on the EV-OXU210:

- Ground test points JP2, JP5, JP9 and JP10. 3P3VCC_CONN from PC104 connectors (TP11)
- USB_5V_P1 (TP2), USB_5V_P2 (TP5), DPHOST/DMHOST (JP3), DPOTG/DMOTG (JP4), ID (TP1)
- Internal charge pump components - L1: TP3 and TP4, C9 (TP6 and TP7), VOUT (TP7)
- Byte enable (BE0-BE3) has test points TP10, TP12-TP14
- Power supplies 5 V (JP8.3), 3.3 V (JP6.3), and 1.8 V (JP7.3)

All the microprocessor signals are routed to Mictor connectors, J1 and J2. The Mictor connectors are not installed but can be obtained from AMP/Tyco Electronics. Part Number: 2-5767004-2. Description: Receptacle, 38 positions, .025 vertical.

Chapter 3

PCI104 Bridge Board

Overview

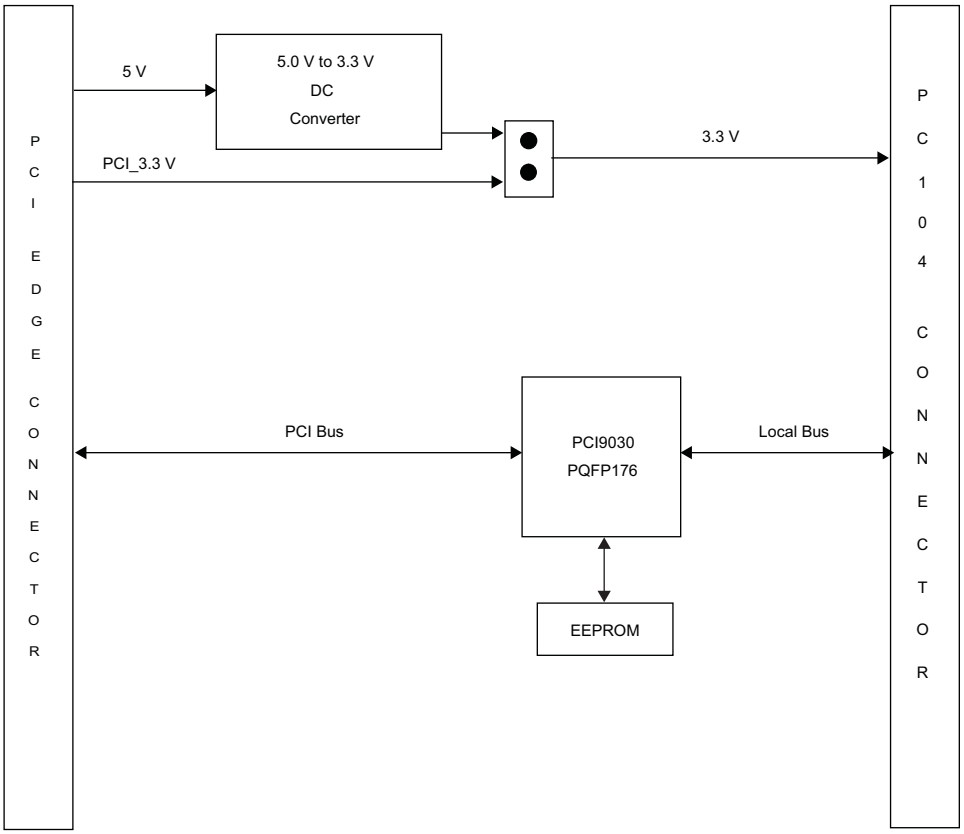
The PCI104 Bridge Board (measuring 5.55 in. (140.9 mm) by 3.00 in. (76.2 mm) can be employed to:

- Evaluate the Oxford Semiconductor OXU210HP USB OTG and host controller
- Run OXU210HP demonstrations
- Develop user software for OXU210HP based applications
- Serve as a subassembly in an OEM product to provide USB OTG and host controller functionality

While the EV-OXU210-PCI can be used to evaluate the OXU210HP, it will not result in optimal performance due to the long access times of the PCI bus and bridge. For optimal performance evaluation, the OXU210HP should be placed directly on the system bus using the EV-OXU210 board as described in Chapter 2.

The PCI104 board bridges between the PCI bus and the PCI9030 local bus. The local bus is routed out to the standard PC104 connectors (J6 and J7). Another proprietary, non-PC104 connector (J8) is added to support a 32-bit interface and additional signals not included in the PC104 signal definition. The EV-OXU210 interfaces to the PCI104 Bridge Card via these three female connectors. Figure 3-1 shows the PCI104 block diagram.

Figure 3-1 PCI104 Bridge Board



The PCI104 board uses the PCI9030 bridge device. The PCI configuration registers are stored in an on-board EEPROM.

The PCI edge connector supplies both 5 V and 3.3 V power. The PCI104 board can also receive its 3.3 V from a 5 V to 3.3 V regulator. This option is jumper selectable.

Power Distribution

The PCI104 board receives its 5 V power from the standard PCI bus edge connector (U2 – eight 5 V pins). The 5 V supply is routed directly to the EV-OXU210 via the PC104 connectors (J1.D16, J2.B3, J2.B29).

The PCI104 board 3.3 V power is supplied by one of two sources:

1. 5.0 V-to-3.3 V DC regulator (U1). Install jumper on JP2 pin 1-2, 3-4 (default setting) and remove 5-6 and 7-8.
2. The standard PCI bus edge connector (U2 – twelve 3.3 V pins). Install jumper on JP2 pin 5-6, 7-8 and remove 1-2 and 3-4.

Local Bus Configuration

The PCI9030 local bus is connected directly to the EV-OXU210 board via the PC104 connectors. Refer to the *PCI9030 Data Book* for a detailed explanation of its operation.

The PCI9030 CS1L chip select is routed to the EV-OXU210. Register Space 1 of the PCI9030 controls CS1L. The number values programmed into Space 1 registers of the EEPROM are shown below. Changing values in the EEPROM requires an application from the bridge chip operating across the PCI bus. Space 1 has 32-bit local and PCI space and contains 128 Kb memory space size. There is no pre-fetch on space 1.

- Space 1 Range 0x0FFE_0000
- Space 1 Remap 0x0000_0001
- Space 1 Descriptor 0x4080_A040
- Space 1 Base Address 0x0001_0001
- Space 1 Initialization GPIO Control 0x0024_9864

The local timing is one WAIT state for READs (address-to-data) and one for WRITEs (address-to-data) to make the PCI104 backwards compatible with previous Oxford Semiconductor chips. The other WAIT states are: zero RD (data-to-data), one RD/WR (data-to-address), zero WR (data-to-data), and one WR cycle hold. An optimum bus access will not create a significant increase in performance in the EV-OXU210-PCI system. For better performance evaluation, the OXU210HP should be embedded directly on the system bus using the EV-OXU210 board.

Local Bus Speed

LCLK, the local bus clock, operates at frequencies up to 60 MHz and is asynchronous to the PCI bus clock, BCLK. BCLK is routed back into LCLK, setting the default local bus speed at 33 MHz.

An oscillator up to 60 MHz can be soldered at the U4/U5 dual-footprint by the customer to increase the local bus speed. R10 (33 ohms) must be installed and R11 removed in this configuration. More WAIT states may have to be added to meet the OXU210HP interface timing when increasing the local bus frequency. See "Local Bus Configuration".

LEDs

The PCI104 has two LEDs to enable verification of the normal operation of the board.

- D1: 3.3V Power Rail Indicator
- D2: 5.0V Power Rail Indicator

Mounting Holes

The PCI104 board has four un-plated standoff holes, one near each corner of the board. Each hole is 0.146" in diameter. The placement matches the EV-OXU210 evaluation board which together make the EV-OXU210-PCI.

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Chapter 4

Schematics

Overview

This chapter provides the EV-OXU210 and PCI104 schematics. The EV-OXU210 uses a dual-footprint so either the LQFP128 (U5) or the BGA84 (U6) package can be installed, but not both.

Figure 4-1 EV-OXU210 Top-Level Schematic

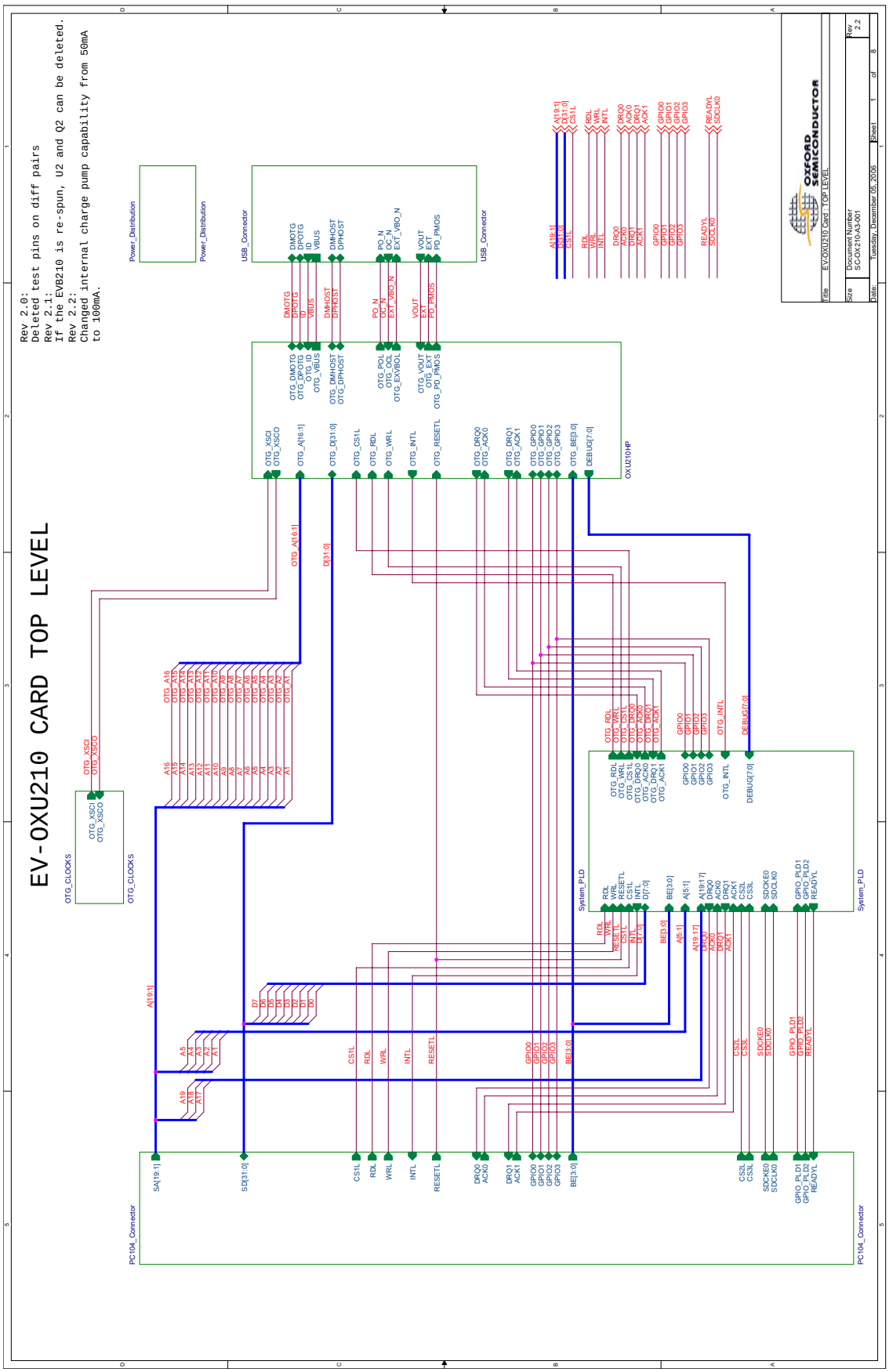

Figure 4-2 EV-OXU210 Test Headers

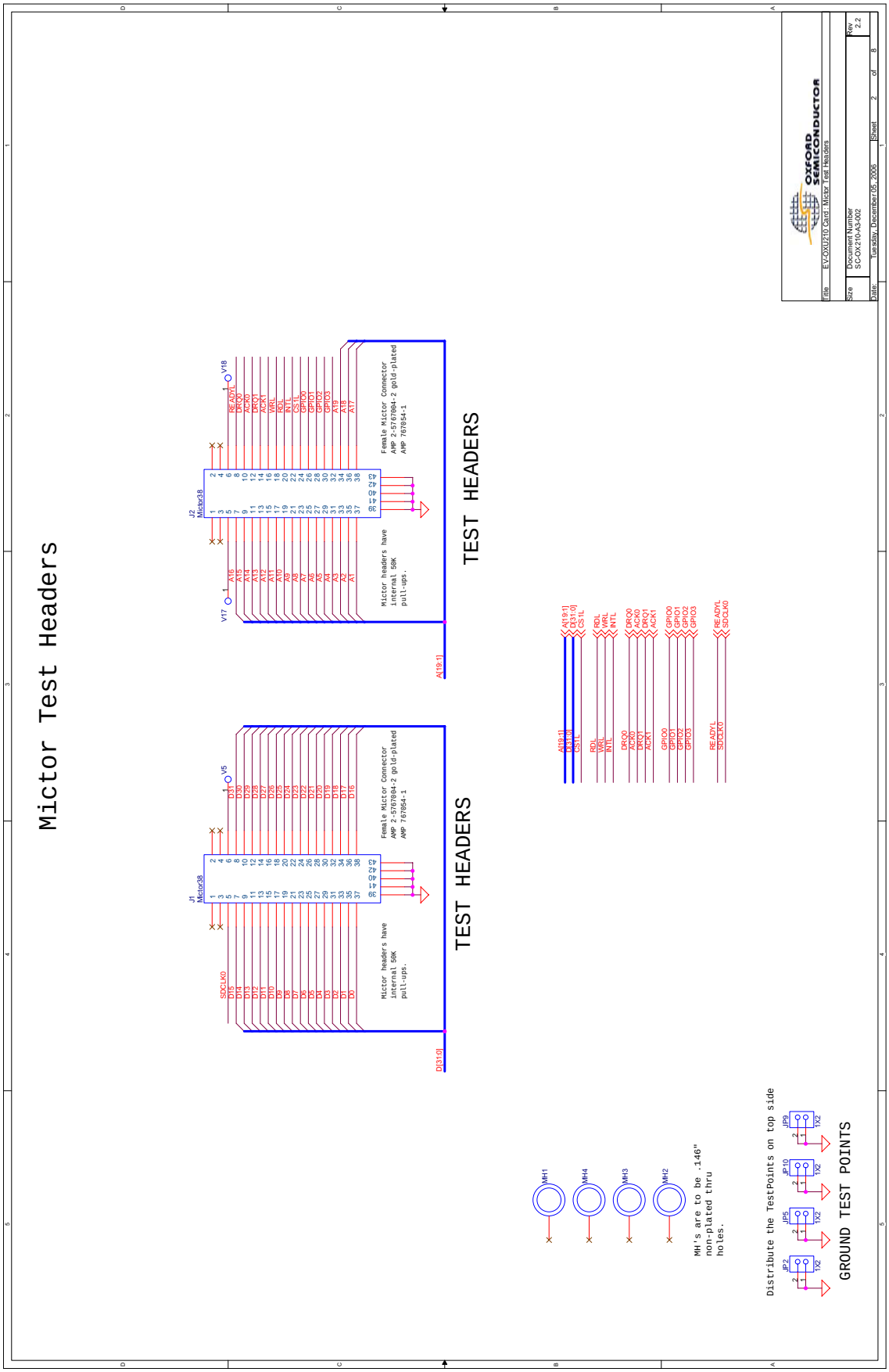

Figure 4-3 EV-OXU210 PC104 Connectors

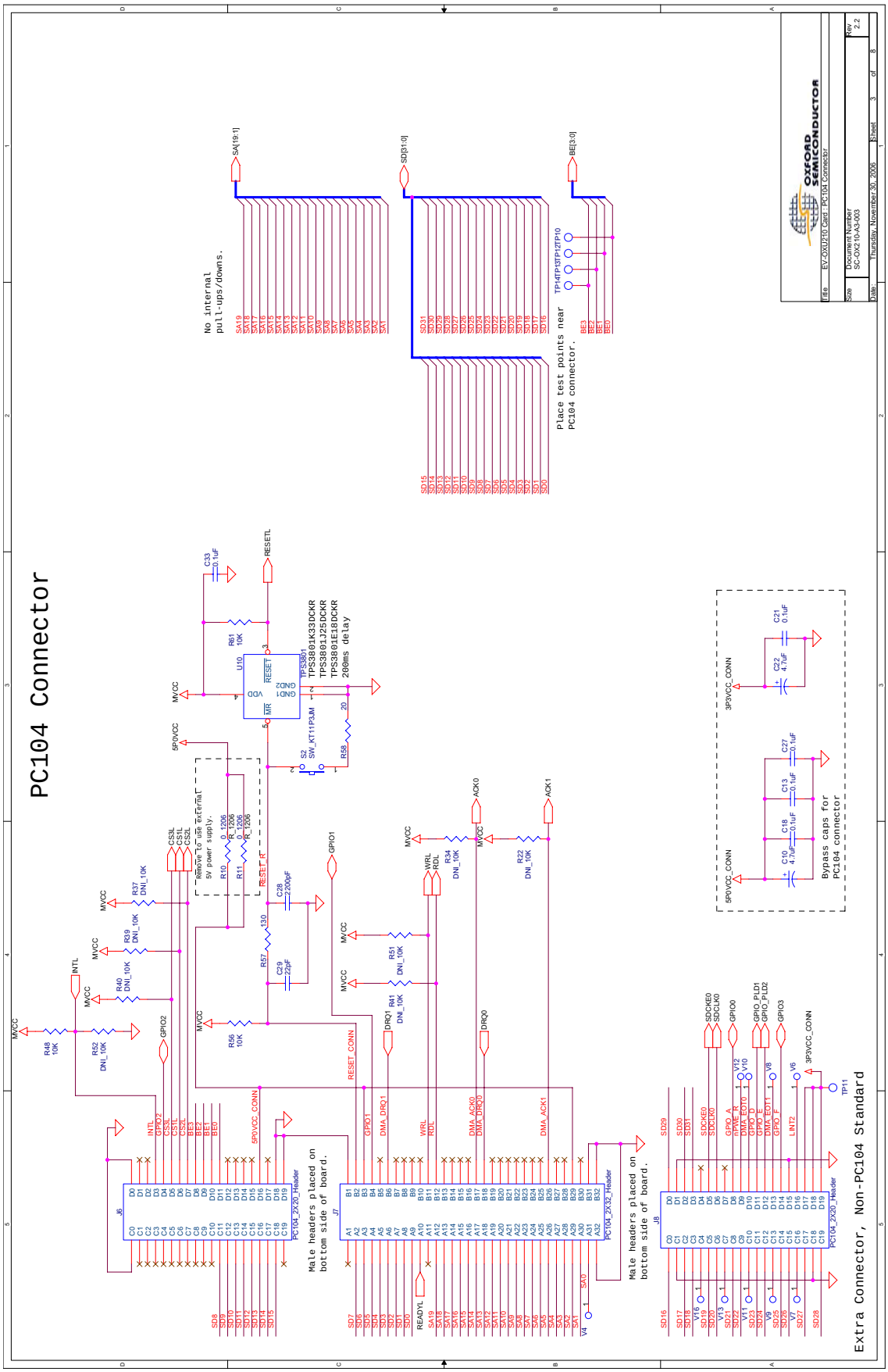

Figure 4-4 OXU210HP Schematic

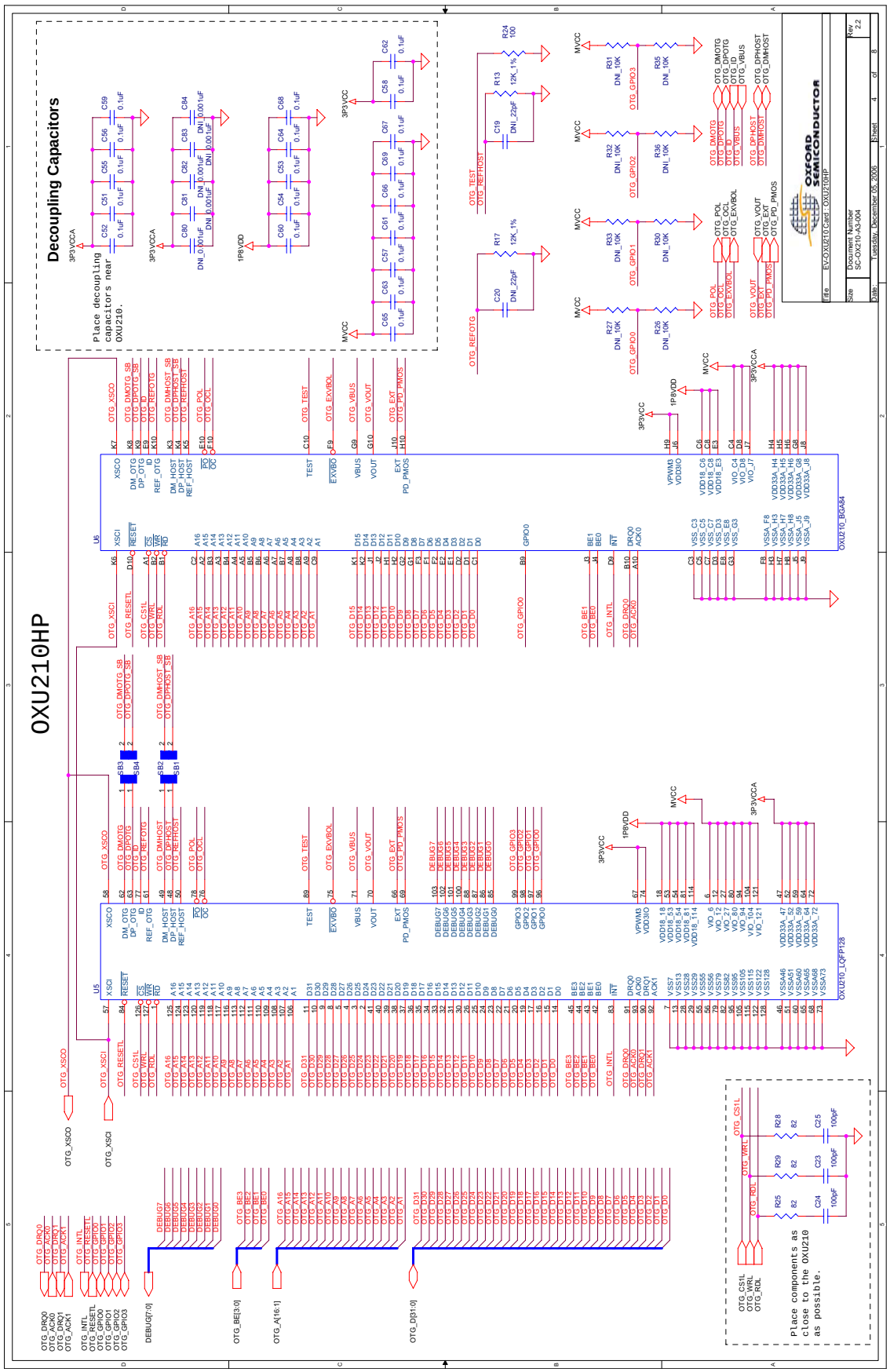

Figure 4-5 EV-OXU210 Clocks

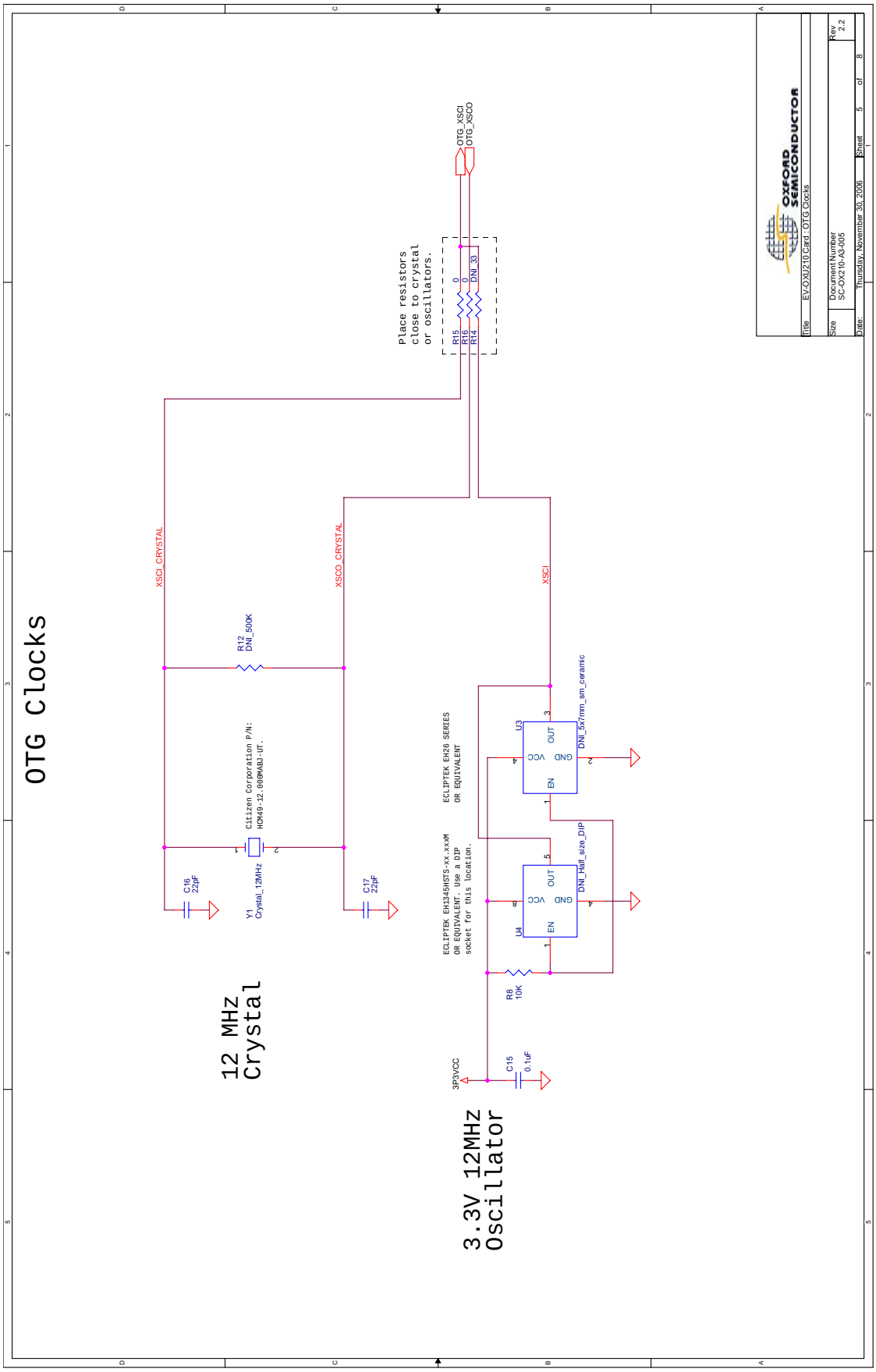

Figure 4-6 EV-OXU210 Power Distribution

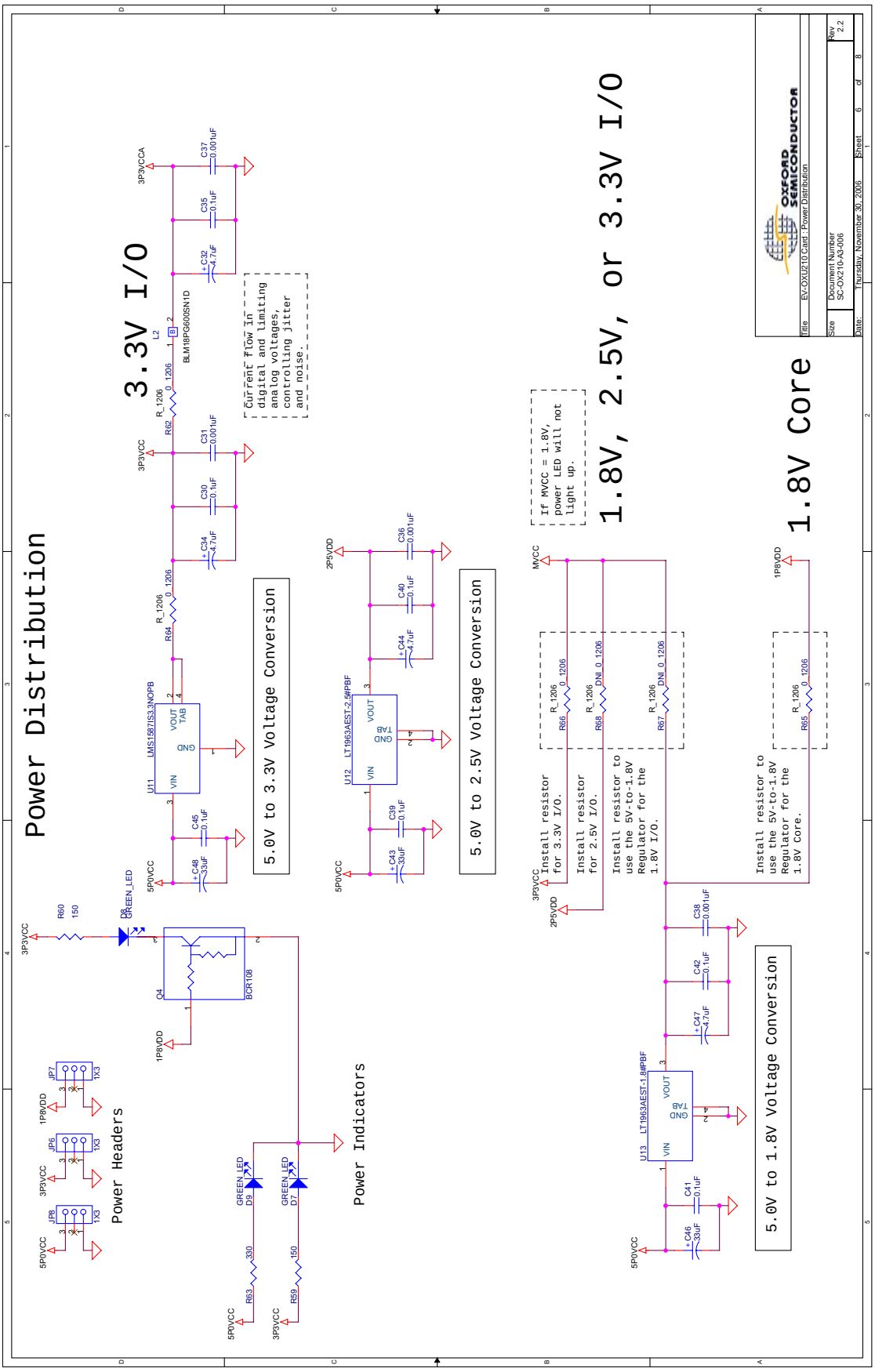

Figure 4-7 EV-OXU210 System CPLD (Not Populated)

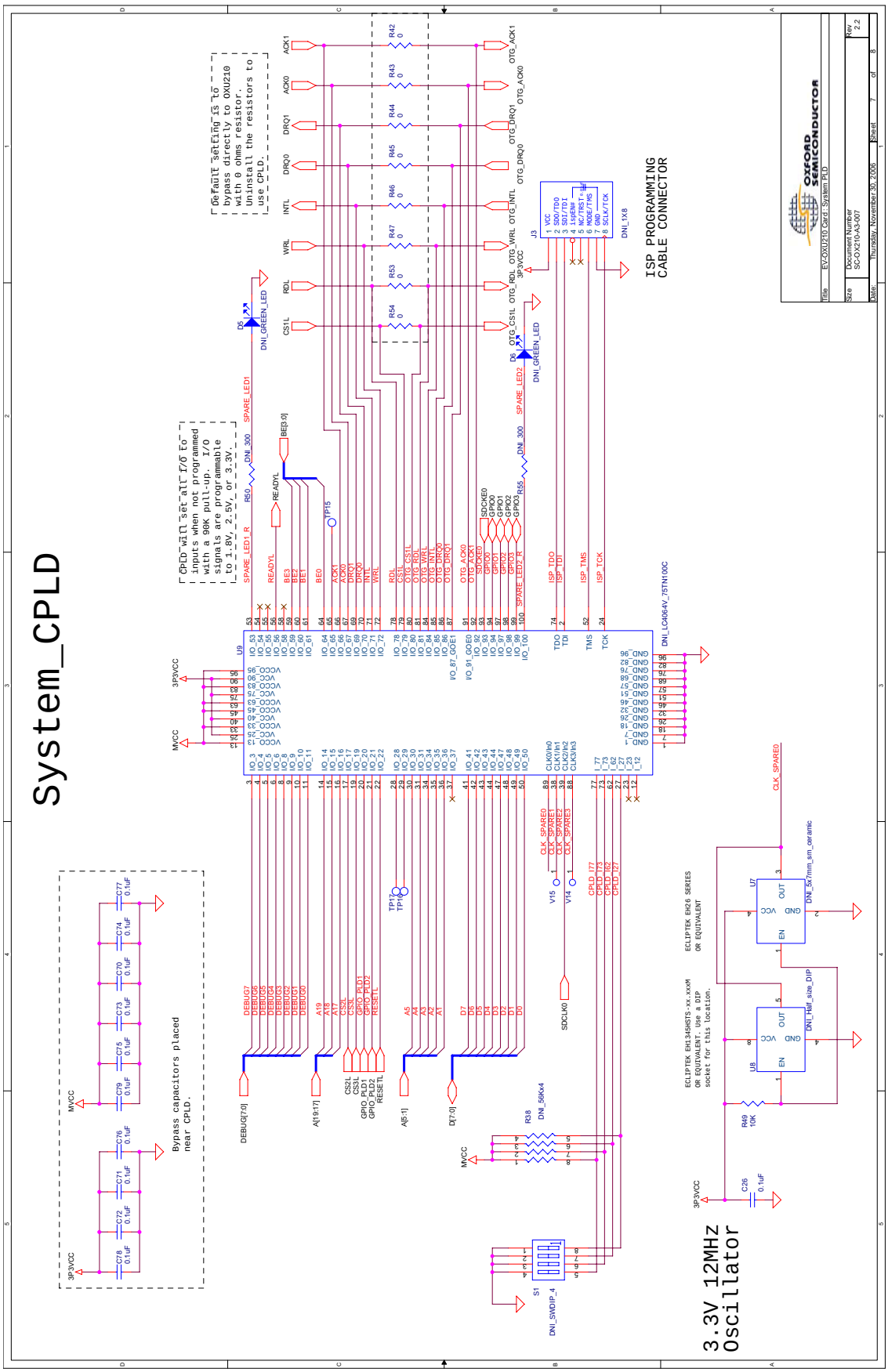

Figure 4-8 EV-OXU210 USB Ports

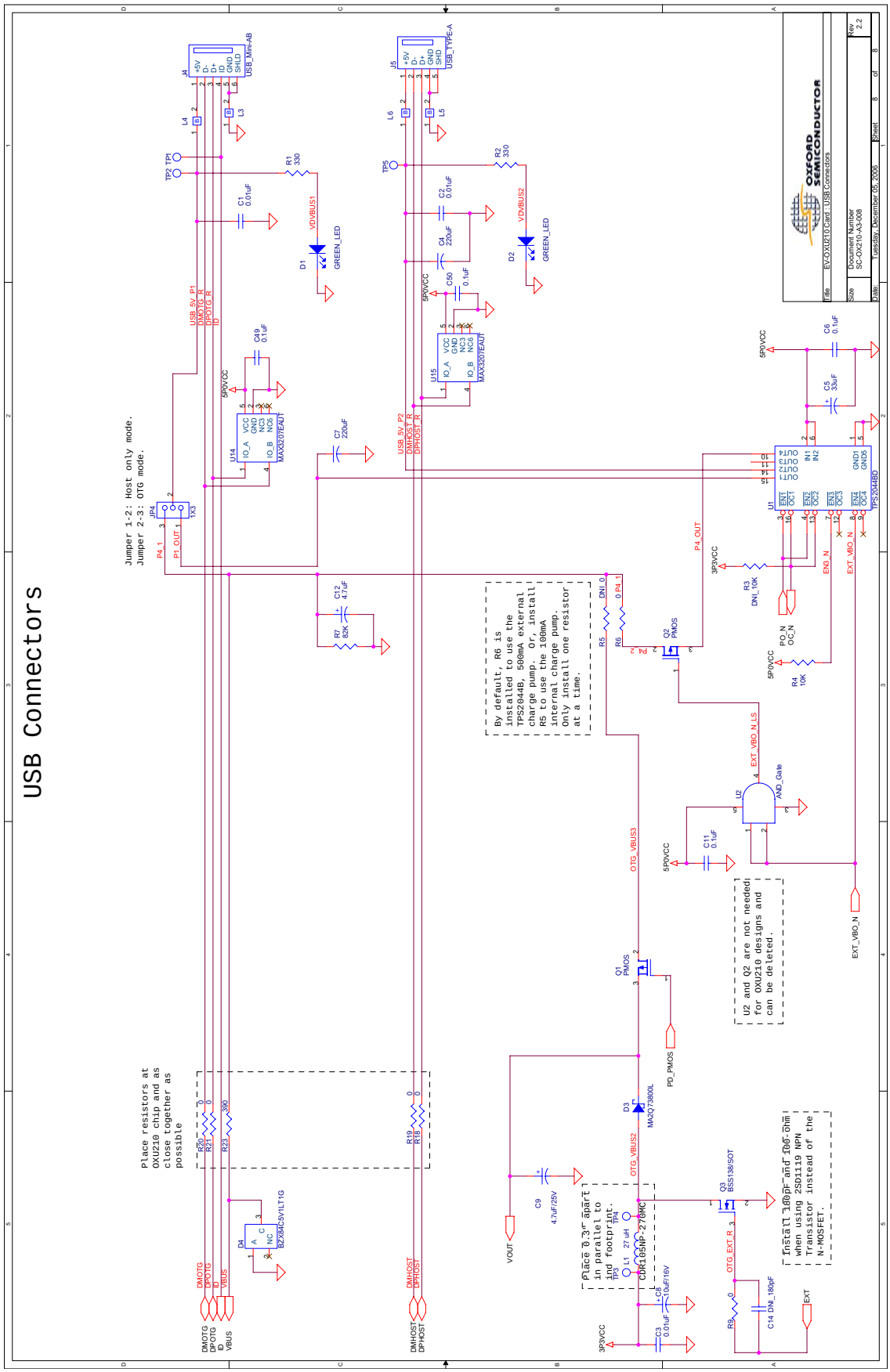

Figure 4-9 PCI104 Top-Level Schematic

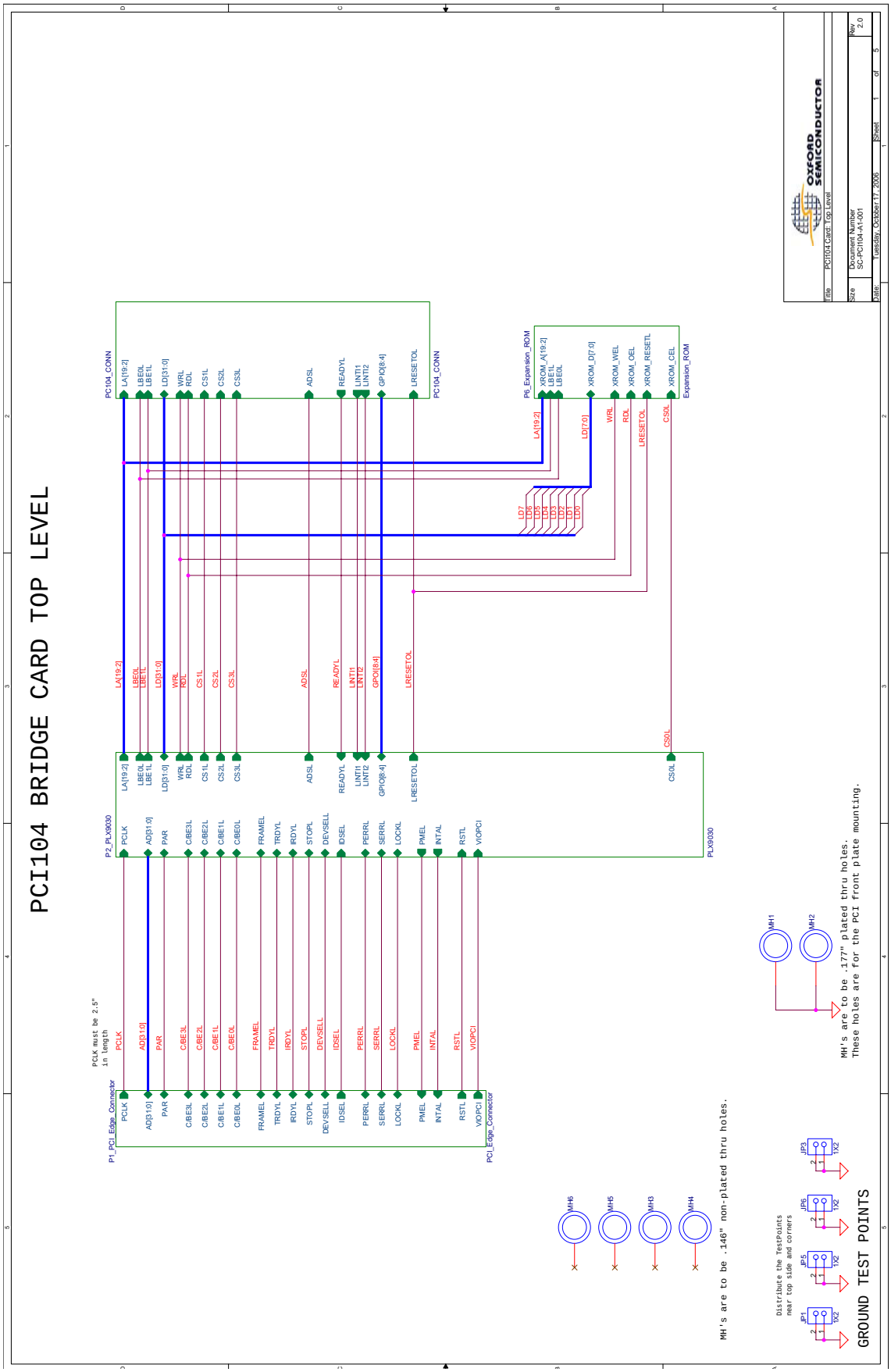

Figure 4-10 PCI104 PCI Connector

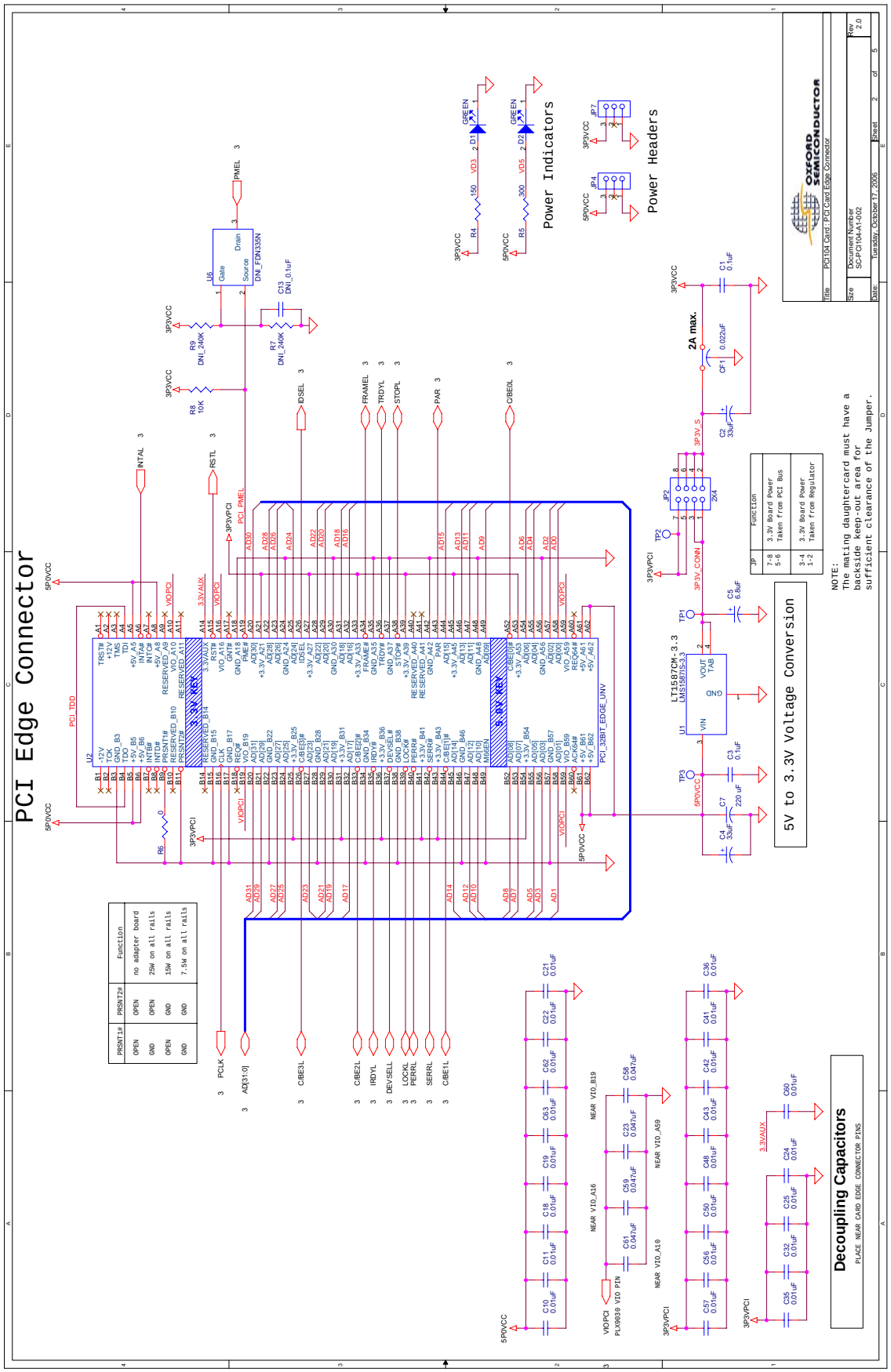

Figure 4-11 PCI9030 Bridge Chip

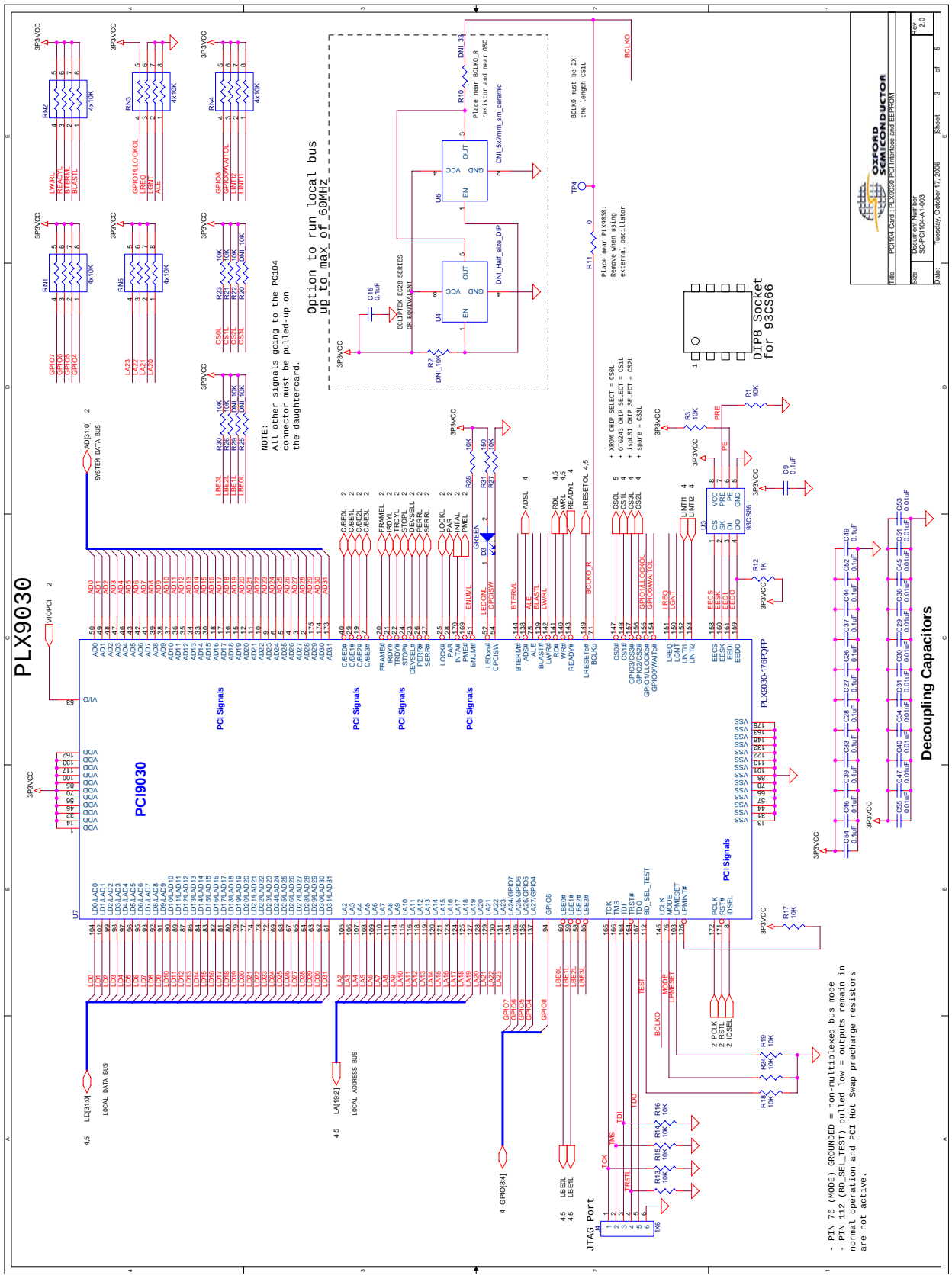

Figure 4-12 PC104 Connectors

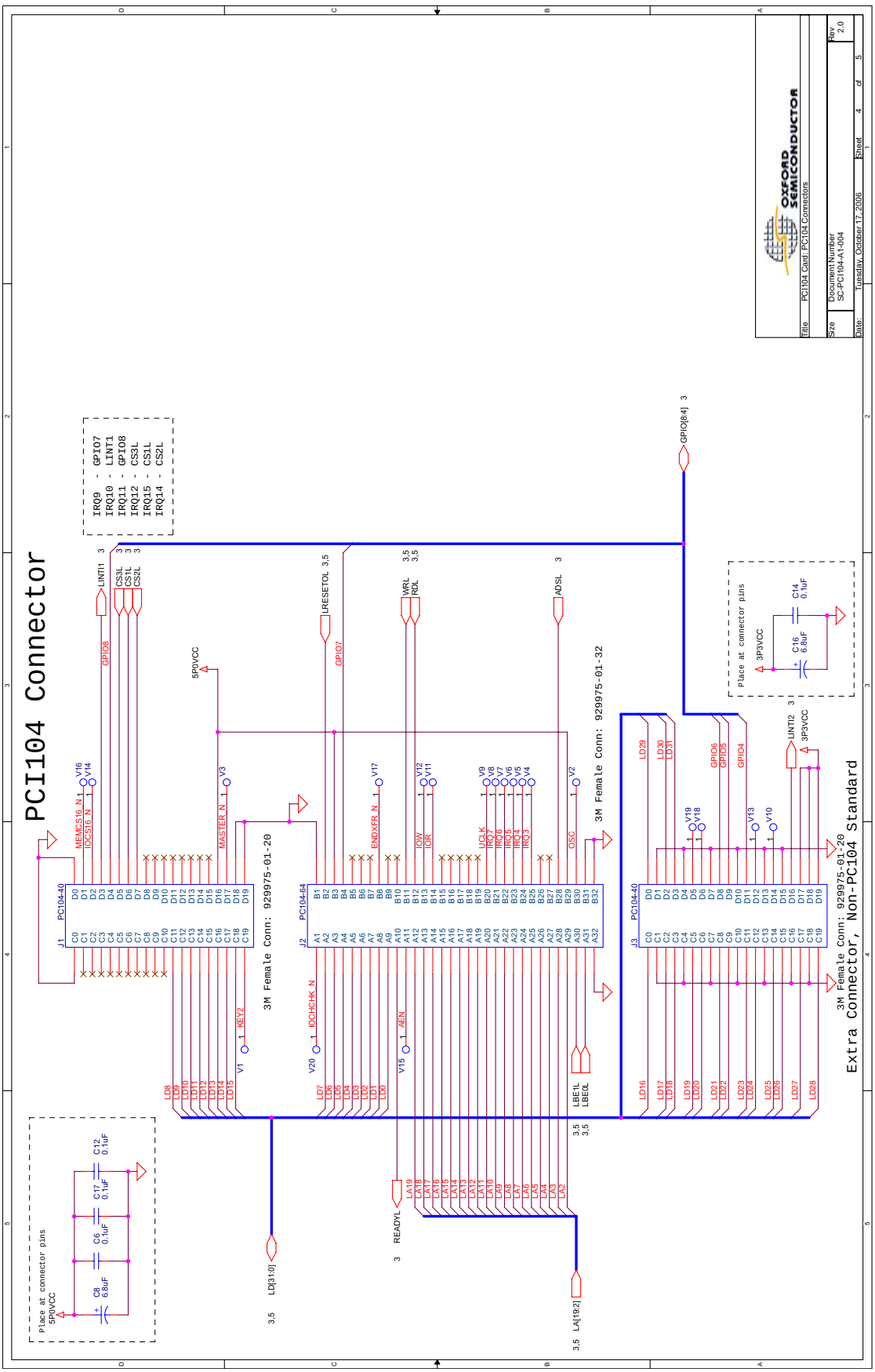

Figure 4-13 PC104 Expansion ROM