NIPPON PRECISION CIRCUITS LTD.

SM5835AF

2D Digital Image Filter

OVERVIEW

The SM5835AF is a two-dimensional digital filter for non-interlaced 8-bit images. It processes a 33-pixel image segment at the video data rate. It includes two horizontal line delays, for lines from 14 to 1037 pixels long, and filtering coefficients in ROM for averaging, Laplacian and two other types of filtering. These features allow any frame size to be processed without any need for external memory.

Other features include decimation registers to change filter characteristics, and independent gain settings for the filtered and unfiltered signal components. The net result is a flexible, high-performance two-dimensional filter IC.

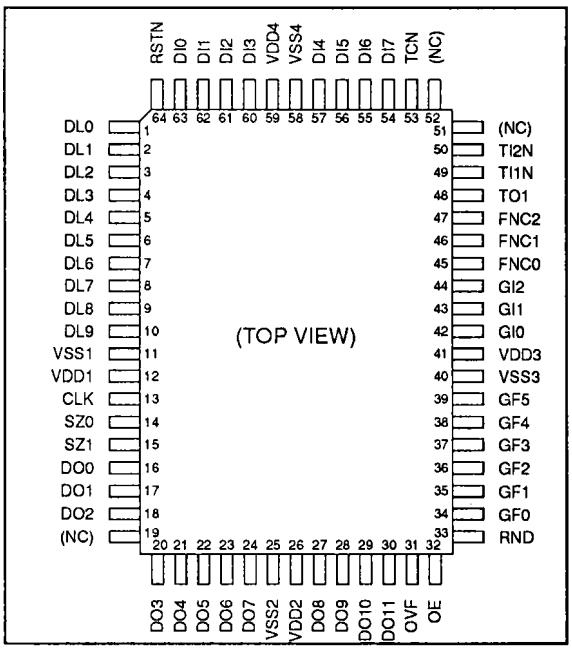
FEATURES

- 3 × 3-pixel two-dimensional filter
- Video signal rates up to 14.5 MHz
- 8-bit data input, selectable for unsigned magnitude or 2s-complement format
- 12-bit 2s-complement data output
- Two-line delay, variable in length from 14 to 1037 pixels
- Coefficients stored in internal ROM for two-dimensional averaging, Laplacian, and two other filters
- Decimation registers to vary filter characteristics
- Independent gain settings for filtered and unfiltered signal components
- Overflow limiting and overflow detection flag output
- Optional rounding for 8-bit output
- TTL-compatible input/output levels
- Tristate data outputs
- Single 5 V supply
- Moly-gate® CMOS process
- 64-pin QFP package

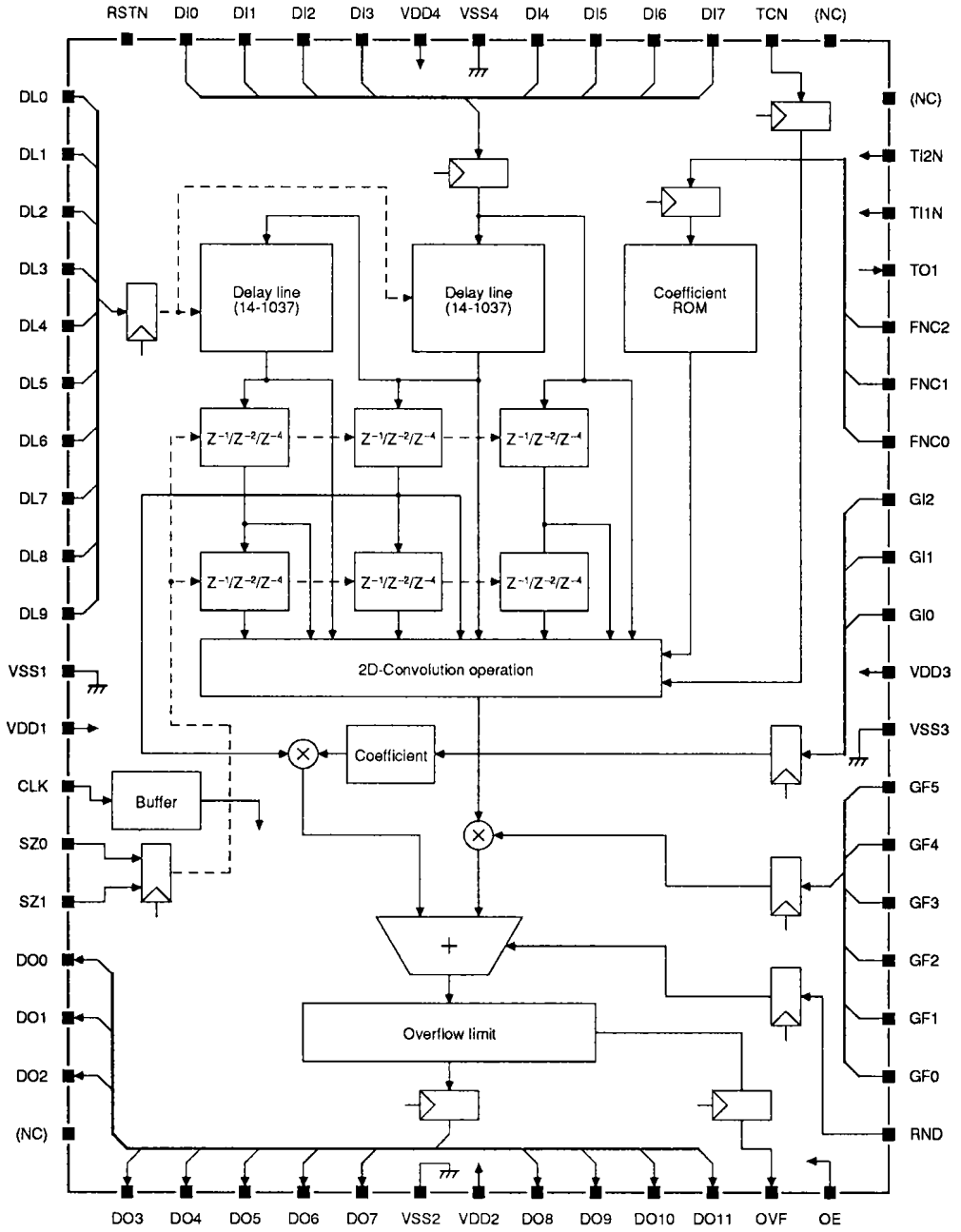
APPLICATIONS

- Image processing for copying machines
- Video signal processing

PINOUT



BLOCK DIAGRAM



PIN DESCIPTION

Pin number	Pin name	I/O	Description
1	DL0	ip	Delay line length select (lsb)
2	DL1	ip	Delay line length select (bit 1)
3	DL2	ip	Delay line length select (bit 2)
4	DL3	ip	Delay line length select (bit 3)
5	DL4	ip	Delay line length select (bit 4)
6	DL5	ip	Delay line length select (bit 5)
7	DL6	ip	Delay line length select (bit 6)

Pin number	Pin name	I/O	Description
8	DL7	ip	Delay line length select (bit 7)
9	DL8	ip	Delay line length select (bit 8)
10	DL9	ip	Delay line length select (msb)
11	VSS1		Ground pin 1
12	VDD1		5 V supply pin 1
13	CLK	i	Clock input
14	SZ0	ip	Decimation setting pin 0
15	SZ1	ip	Decimation setting pin 1
16	DO0	o	Data output (lsb)
17	DO1	o	Data output (bit 1)
18	DO2	o	Data output (bit 2)
19	(NC)		No connection
20	DO3	o	Data output (bit 3)
21	DO4	o	Data output (bit 4)
22	DO5	o	Data output (bit 5)
23	DO6	o	Data output (bit 6)
24	DO7	o	Data output (bit 7)
25	VSS2		Ground pin 2
26	VDD2		5 V supply pin 2
27	DO8	o	Output data (bit 8)
28	DO9	o	Output data (bit 9)
29	DO10	o	Output data (bit 10)
30	DO11	o	Output data (msb)
31	OVF	o	Overflow flag
32	OE	ip	Tristate output enable. HIGH = enabled; LOW = tristate
33	RND	ip	Output rounding enable. HIGH = enabled; LOW = disabled
34	GF0	ip	Filter gain coefficient (lsb)
35	GF1	ip	Filter gain coefficient (bit 1)
36	GF2	ip	Filter gain coefficient (bit 2)
37	GF3	ip	Filter gain coefficient (bit 3)
38	GF4	ip	Filter gain coefficient (bit 4)
39	GF5	ip	Filter gain coefficient (msb)
40	VSS3		Ground pin 3
41	VDD3		5 V supply pin 3
42	GI0	ip	Unfiltered signal gain select (lsb)
43	GI1	ip	Unfiltered signal gain select (bit 1)
44	GI2	ip	Unfiltered signal gain select (msb)
45	FNC0	ip	Function select (lsb)

Pin number	Pin name	I/O	Description
46	FNC1	ip	Function select (bit 1)
47	FNC2	ip	Function select (msb)
48	TO1	o	Test output 1
49	TI1N	ip	Test input 1 (tie HIGH for normal operation)
50	TI2N	ip	Test input 2 (tie HIGH for normal operation)
51	(NC)		No connection
52	(NC)		No connection
53	TCN	ip	Input format select. HIGH = unsigned absolute; LOW = 2s complement
54	DI7	ip	Input data (msb)
55	DI6	ip	Input data (bit 6)
56	DI5	ip	Input data (bit 5)
57	DI4	ip	Input data (bit 4)
58	VSS4	ip	Ground pin 4
59	VDD4	ip	5 V supply pin 4
60	DI3	ip	Input data (bit 3)
61	DI2	ip	Input data (bit 2)
62	DI1	ip	Input data (bit 1)
63	DI0	ip	Input data (lsb)
64	RSTN	ip	Reset

Note
i = input, ip = input with pull-up, o = output

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{STG}	–40 to 125	°C
Power dissipation	P_D	400	mW
Soldering temperature	T_{SLD}	255	°C
Soldering time	t_{SLD}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Conditions	Unit
Supply voltage	V_{DD}	4.75 to 5.25	V
Operating temperature	T_{OPR}	–20 to 70	°C

DC Electrical Characteristics

T_a = –20 to 70° C, V_{SS} = 0 V, V_{DD} = 4.75 to 5.25 V unless otherwise noted

Parameter	Pins	Symbol	Conditions	Rating			Unit
				min	typ	max	
Current consumption	*1	I_{DD}	See note.	–	60	80	mA
Input voltage	*3, *4	V_{IH}		2.4	–	–	V
		V_{IL}		–	–	0.5	
Output voltage	*5, *6	V_{OH}	I_{OH} = –0.4 mA	4.0	–	–	V
		V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	
Input current	*4	I_{IL}	V_{IN} = 0 V	–	10	20	µA
Input leakage current	*3, *4	I_{LH}	V_{IN} = V_{DD}	–	–	1	µA
	*3	I_{LL}	V_{IN} = 0 V	–	–	1	
Output high-impedance leakage current	*6	I_{LH}	V_{IN} = V_{DD}	–	–	5	µA
		I_{LL}	V_{IN} = 0 V	–	–	5	

Note

V_{DD} = 5.0 V, CLK frequency f_C = 14.5 MHz, all outputs unloaded.

Pin classification

Pin type	Pin type number	Pins
V_{DD} pins	*1	VDD1, VDD2, VDD3, VDD4
V_{SS} pins	*2	VSS1, VSS2, VSS3, VSS4
Input pins	*3	CLK
Input pins with pull-up	*4	DI0 to 7, DL0 to 9, SZ0 to 2, FNC0 to 2, TCN, RND, GI0 to 2, GF0 to 5, TI1N, TI2N, RSTN, OE
Output pins	*5	OVF, TO1
Tristate outputs	*6	DO0 to 11

AC Electrical Characteristics

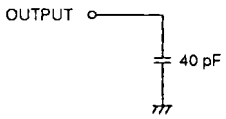
T_a = –20 to 70° C, V_{SS} = 0 V, V_{DD} = 4.75 to 5.25 V unless otherwise noted

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
CLK period	t_{CP}		68	–	1000	ns
CLK LOW-level interval	t_{CL}		30	–	500	ns
CLK HIGH-level interval	t_{CH}		30	–	500	ns
CLK rise time	t_{CR}	1.0 to 2.0 V	–	–	10	ns
CLK fall time	t_{CF}	1.0 to 2.0 V	–	–	10	ns
Input data setup time	t_S		30	–	–	ns
Input data hold time	t_H		0	–	–	ns

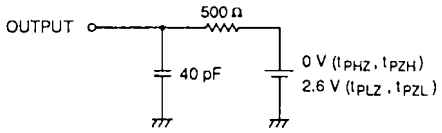
Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
CLK to data output delay	t_{OD1}	Load conditions 1 (Note 1)	–	–	50	ns
CLK to data output hold time	t_{OH1}		5	–	–	ns
CLK to OVF output delay	t_{OD2}		–	–	50	ns
CLK to OVF output hold time	t_{OH2}		5	–	–	ns
OE to data output enabled delay	t_{PZL}	Load conditions 2 (Note 2)	–	–	40	ns
	t_{PZH}		–	–	40	ns
OE to data output disabled delay	T_{PLZ}		–	–	40	ns
	t_{PHZ}		–	–	40	ns
RSTN pulsewidth	t_{RST}	1.0 to 2.0 V	50	–	–	ns
Input capacitance	C_{IN}	f_C = 1 MHz	–	–	10	pF
Output capacitance	C_{OUT}	f_C = 1 MHz	–	–	15	pF

Note

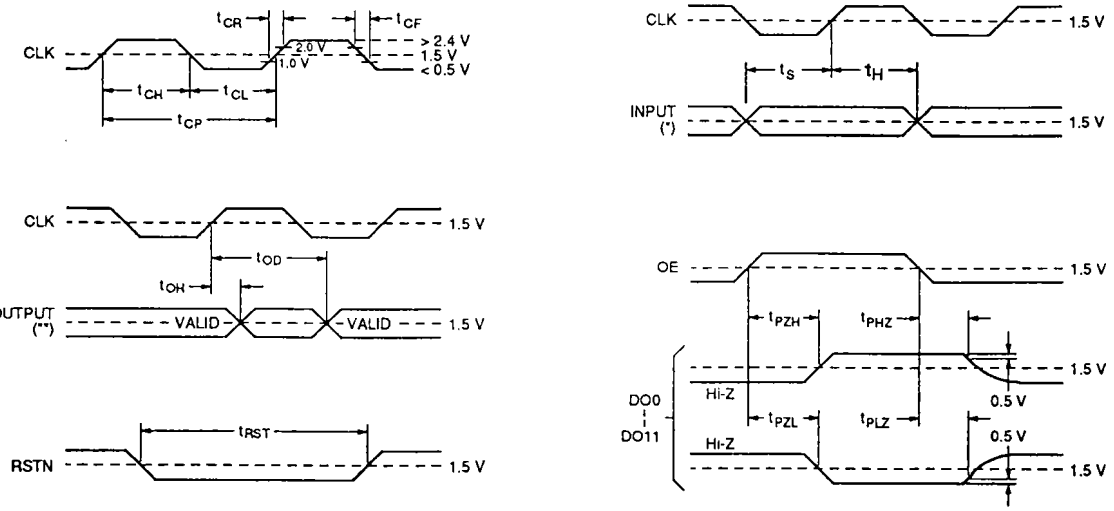
1. Load conditions 1



2. Load conditions 2



Timing Diagrams



FUNCTIONAL DESCRIPTION

The SM5835AF is a video-signal rate two-dimensional digital filter for non-interlaced 8-bit images. It contains eight sets of 3 × 3-pixel filter coefficients in ROM. Although it is not possible to program the SM5835AF with your own sets of coefficients, this configuration eliminates the need for an external coefficient loading chip. The internal variable-length delay lines support any frame size without the need for external memory.

3 × 3-element Filter

Basic operation

The two-dimensional filter calculation operates by scanning across the image. At each pixel, that pixel and the neighboring eight pixels are each multiplied by the corresponding coefficient. These products are summed to give the filter output for that pixel. For example, for image X and coefficients C,

$$y\ (i,\ j) = \sum_{n=0}^{2} \sum_{m=0}^{2} [C(n,\ m) \times X\ (i + n - 1,\ j + m - 1)]$$

C(0, 0)	C(0, 1)	C(0, 2)
C(1, 0)	C(1, 1)	C(1, 2)
C(2, 0)	C(2, 1)	C(2, 2)

Figure 1. 3 × 3 filter coefficient matrix

X(i–1, j–1)	X(i–1, j)	X(i–1, j+1)
X(j, j–1)	X(i, j)	X(i, j+1)
X(i+1, j–1)	X(i+1, j)	X(i+1, j+1)

Figure 2. 3 × 3 nearest-neighbour matrix (filter input)

	y(i, j)	

Figure 3. 3 × 3 filter output

Filter coefficients

Pins FNC0 to FNC2 select one of eight different sets of filter coefficients, from four different types of filter. In the following descriptions, the value FNC is the number represented by FNC0 to FNC2.

Averaging filter (noise reduction)

This filter takes the average of all nine pixels in the 3 × 3-pixel window, thus reducing the amplitude of the noise component by a factor of nine. This also has the side-effect of reducing the sharpness of the image. The SM5835AF requires filter coefficients to be a multiple of 1/2. Therefore, all coefficients are equal to 1/8, as shown in figure 4, instead of 1/9. The filter thus has a net gain 1.125 (9/8). To compensate, set the filter gain coefficients GF0 to GF5 to 001110. This corresponds to a gain of 14/16 = 0.875, bringing the net gain back to close to unity.

$$y\ (i,\ j) = (1/8) \sum_{n=0}^{2} \sum_{m=0}^{2} X(i + n - 1,\ j + m - 1)$$

1/8	1/8	1/8
1/8	1/8	1/8
1/8	1/8	1/8

[FNC = 000]

Figure 4. Averaging filter coefficients

Laplacian filters (image sharpening)

The Laplacian filters emphasize the high-frequency components of the image. The filter coefficients are equal to either

$$[-(1/8\nabla)^2 X(i,\ j)]$$

or

$$[-(1/4)\nabla^2 X(i,\ j)]$$

- Laplacian filter 1
  This filter uses the eight neighboring pixels:

$$y(i, j) = X(i, j) - 1/8[X(i-1, j-1) + X(i-1, j) + X(i-1, j+1) + X(i, j-1) + X(i, j+1) + X(i+1, j-1) + X(i+1, j) + X(i+1, j+1)]$$

- Laplacian filter 2
  This filter uses the four vertical and horizontal neighbors:

$$y(i, j) = X(i, j) - 1/4[X(i-1, j) + X(i, j-1) + X(i, j+1) + X(i+1, j)]$$

- Laplacian filter 3
  This filter uses the four diagonal neighbors:

$$y(i, j) = X(i, j) - 1/4[X(i-1, j-1) + X(i-1, j+1) + X(i+1, j-1) + X(i+1, j+1)]$$

−1/8	−1/8	−1/8
−1/8	1	−1/8
−1/8	−1/8	−1/8

Laplacian 1
[FNC = 001]

0	−1/4	0
−1/4	1	−1/4
0	−1/4	0

Laplacian 2
[FNC = 010]

−1/4	0	−1/4
0	1	0
−1/4	0	−1/4

Laplacian 3
[FNC = 011]

Figure 5. Laplacian filter coefficients

Template matching (line enhancement)

These two filters provide templates for enhancing horizontal and vertical lines. They are specific instances of the general principle by which image features can be enhanced by correlating image segment with a matching template.

- Vertical line detection

$$y(i, j) = (1/4)[X(i-1, j) + X(i, j) + X(i+1, j)] - (1/8)[X(i-1, j-1) + X(i-1, j+1) + X(i, j-1) + X(i, j+1) + X(i+1, j-1) + X(i+1, j+1)]$$

- Horizontal line detection

$$y(i, j) = (1/4)[X(i, j-1) + X(i, j) + X(i, j+1)] - (1/8)[X(i-1, j) + X(i-1, j-1) + X(i-1, j+1) + X(i+1, j-1) + X(i+1, j) + X(i+1, j+1)]$$

−1/8	1/4	−1/8
−1/8	1/4	−1/8
−1/8	1/4	−1/8

Vertical line detector output
[FNC = 100]

−1/8	−1/8	−1/8
1/4	1/4	1/4
−1/8	−1/8	−1/8

Horizontal line detector output
[FNC = 101]

Figure 6. Horizontal and vertical line detection

Differencing (edge enhancement)

The SM5835AF provides horizontal and vertical Sobel operators to enhance image edges. The Sobel processing is not completely performed by the SM5835AF, since square root and squaring operations are also required.

- Horizontal Sobel operation

$$yH(i, j) = -(1/4)[X(i-1, j-1) + 2*X(i, j-1) + X(i+1, j-1)] + (1/4)[X(i-1, j+1) + 2*X(i, j+1) + X(i+1, j+1)]$$

- Vertical Sobel operation

$$yV(i, j) = (1/4)[X(i-1, j-1) + 2*X(i-1, j) + X(i-1, j+1)] - (1/4)[X(i+1, j-1) + 2*X(i+1, j) + X(i+1, j+1)]$$

−1/4	0	1/4
−1/2	0	1/2
−1/4	0	1/4

Sobel operator (horizontal direction)
[FNC = 110]

1/4	1/2	1/4
0	0	0
−1/4	−1/2	−1/4

Sobel operator (vertical direction)
[FNC = 101]

Figure 7. Sobel operators

Two SM5835AFs are needed to process the signal in both horizontal and vertical directions, producing the outputs yH(i, J) and yV(i, j). Additional external processing is required to perform the complete operation, as follows.

$$y(i, j) = [[yH(i, j)]^2 + [yV(i, j)]^2]^{1/2}$$

Decimation Register

Pins SZ0 and SZ1 set the decimation factor to one (no decimation), two or four, as shown in table 1. With decimation enabled, the filter coefficients are multiplied by every second or fourth horizontal pixel, instead of every pixel. Figures 6 to 8 illustrate the effect of the different decimation settings.

Table 1. Decimation selection

SZ1	SZ0	Decimation
0	0	No decimation
1	1	
0	1	Decimate by two
1	0	Decimate by four

X(i−1, j−1)	X(i−1, j)	X(i−1, j+1)
X(j, j−1)	X(i, j)	X(i, j+1)
X(i+1, j−1)	X(i+1, j)	X(i+1, j+1)

Figure 8. Filter operation with no decimation

X(i−1, j−2)	D	X(i−1, j)	D	X(i−1, j+2)
X(j, j−2)	D	X(i, j)	D	X(i, j+2)
X(i+1, j−2)	D	X(i+1, j)	D	X(i+1, j+2)

Figure 9. Filter operation with decimation by two

X(i–1, j–4)	D	D	D	X(i–1, j)	D	D	D	X(i–1, j+4)
X(j, j–4)	D	D	D	X(i, j)	D	D	D	X(i, j+4)
X(i+1, j–4)	D	D	D	X(i+1, j)	D	D	D	X(i+1, j+4)

Figure 10. Filter operation with decimation by four

The decimation feature is provided to allow the filter characteristics to be changed. The following equations give the exact equations for the filter outputs.

1. No decimation (SZ0 = 0, SZ1 = 0, or SZ20 = 1, SZ1 = 1)

$$y(i, j) = \sum_{n=0}^{2} \sum_{m=0}^{2} [C(n, m) \times X(i + n - 1, j + m - 1)]$$

2. Decimation by two (SZ0 = 1, SZ1 = 0)

$$y(i, j) = \sum_{n=0}^{2} \sum_{m=0}^{2} [C(n, m) \times X(i + n - 1, j + 2m - 2)]$$

3. Decimation by four (SZ0 = 0, SZ1 = 1)

$$y(i, j) = \sum_{n=0}^{2} \sum_{m=0}^{2} [C(n, m) \times X(i + n - 1, j + 4m - 4)]$$

Variable-length Delay (DL0 to DL9)

The SM5835AF's inbuilt delay lines can be set to be lengths between 14 and 1037 pixels log. The length of the delay lines, L_H, is set by the DL0 to DL9 pins, as given by the following equation.

$$L_H = 14 + \sum_{k=0}^{9} DLk \times 2^k$$

Table 2. Delay line length settings

Length settings	DL9	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
14	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	1
16	0	0	0	0	0	0	0	0	1	0
17	0	0	0	0	0	0	0	0	1	1
18	0	0	0	0	0	0	0	1	0	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
512	0	1	1	1	1	1	0	0	1	0
513	0	1	1	1	1	1	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1024	1	1	1	1	1	1	0	0	1	0
1025	1	1	1	1	1	1	0	0	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1036	1	1	1	1	1	1	1	1	1	0
1037	1	1	1	1	1	1	1	1	1	1

Source and Filtered Signal Gains (GI0 to GI2, GF0 to GF5)

The SM5835AF allows the gains of the original source signal and the filtered signal to be independently controlled. GF0 to GF5 control the gain of the filtered signal. These six bits represent a 2s-complement fixed-point number, with two integer bits and four fractional bits. The value is given by the following equation.

$$G_{FL} = -GF5 \times 2 + \sum_{k=0}^{4} GFk \times 2^{k-4}$$

Table 3 summarises the effect of GF0 to GF5. GI0 to GI2 control the gain of the input signal. Table 4 lists the effect of these pins.

Table 3. Filtered signal gain control

Gain	GFk	GF5	GF4	GF3	GF2	GF1	GF0
	Weight	–2	1	1/2	1/4	1/8	1/16
1 + 15/16	= 1.9375	0	1	1	1	1	1
1 + 14/16	= 1.875	0	1	1	1	1	0
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	= 1.0	0	1	0	0	0	0
15/16	= 0.9375	0	0	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1/16	= 0.0625	0	0	0	0	0	1
0	= 0.0	0	0	0	0	0	0
–1/16	= –0.0625	1	1	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
–1	= –1.0	1	1	0	0	0	0
–1 – 1/16	= –1.0625	1	0	1	1	1	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
–1 – 15/16	= –1.9375	1	0	0	0	0	1
–2	= –2.0	1	0	0	0	0	0

Table 4. Source singnal gain control

Gain	GIN	GI2	GI1	GI0
0	= 0.0	0	0	0
1/2	= 0.5	0	0	1
3/4	= 0.75	0	1	0
7/8	= 0.875	0	1	1
15/16	= 0.9375	1	0	0
1	= 1.0	1	0	1
		1	1	0
		1	1	1

Clock Input (CLK)

The clock input, CLK, controls the operation of every part of the SM5835AF. The maximum clock frequency is 14.5 MHz, the minimum, 1 MHz. All input and output data transfer is synchronized to the system clock.

Input Data (DI0 to DI7)

The input data can be in either unsigned-magnitude or 2s complement format. The format is selected by the TCN pin—TCN = HIGH: Unsigned-magnitude, and TCN = LOW: 2s complement.

In unsigned-magnitude format, all eight bits represent an unsigned integer value—input values range from 0 to 255. In 2s complement format, the most-significant bit represents the sign of the number—input values range from –128 to +127. Internally, the SM5835AF uses 9-bit 2s-complement arithmetic.

Table 5. Input data table

8-bit unsigned magnitude									8-bit 2s complement								
(XLSB)	7	6	5	4	3	2	1	0	(XLSB)	7	6	5	4	3	2	1	0
+MAX (255)	1	1	1	1	1	1	1	1									
(254)	1	1	1	1	1	1	1	0									
⋮																	
(128)	1	0	0	0	0	0	0	0									
(127)	0	1	1	1	1	1	1	1	+MAX (127)	0	1	1	1	1	1	1	1
(126)	0	1	1	1	1	1	1	0	(126)	0	1	1	1	1	1	1	0
⋮									⋮								
+1LSB	0	0	0	0	0	0	0	1	+1LSB	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
									−1LSB	1	1	1	1	1	1	1	1
									⋮								
									(−127)	1	0	0	0	0	0	0	1
									−MAX (−128)	1	0	0	0	0	0	0	0

Output Data (DO0 to DO11, RND, OVF)

Output data format

The output data is in 12-bit unsigned-magnitude or 2s complement format. The output format is the same as the currently-selected input format, but with an additional four bits for numerical precision. That is, if the input data is treated as an 8-bit integer, then the output data has an effective decimal point between bits three and four.

TCN = H (Unsigned magnitude)

$$Xin = \sum_{k=0}^{7} (DIk) \times 2^{k}$$

$$Yout = \sum_{k=0}^{11} (DIk) \times 2^{k-4}$$

Table 6. Input/output data format (TCN = H)

Data	Integer								Decimal			
	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Input data DI0 to 7	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0				
Output data DO0 to 11	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

TCN = L (2s complement)

$$Xin = -(DI7) \times 2^7 + \sum_{k=0}^{6} (DIk) \times 2^k \qquad Yout = -(DO11) \times 2^7 + \sum_{k=0}^{10} (DIk) \times 2^{k-4}$$

Table 7. Input/output data format (TCN = L)

Data	Integer								Decimal			
	-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Input data DI0 to 7	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0				
Output data DO0 to 11	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

Overflow limiter

Although the internal arithmetic of the SM5835AF uses extra bits for precision, overflow can occur when the output signal is limited to the number of output bits. To prevent this, the SM5835AF includes an output limiting circuit. In unsigned-magnitude mode, the output data range is from 0 to 255, and in 2s-complement mode, the output data range is from −128 to +127.

Overflow flag

The OVF output goes HIGH when an internal overflow has been detected, and the overflow limiter has operated. If an overflow is detected, reduce the gain using the GI0 to GI2 and GF0 to GF5 control pins.

Output data rounding

An output rounding mode is provided for systems in which only the higher eight bits of the output are read. If the RND pin is HIGH, 1 is added to bit 3. That is, 2^{-1} is added to the output.

Tristate output

Output pins DO0 to Do11 are tristate outputs, enabled by the OE pin. They are enabled if OE is HIGH, and high-impedance if OE is LOW.

Reset (RSTN)

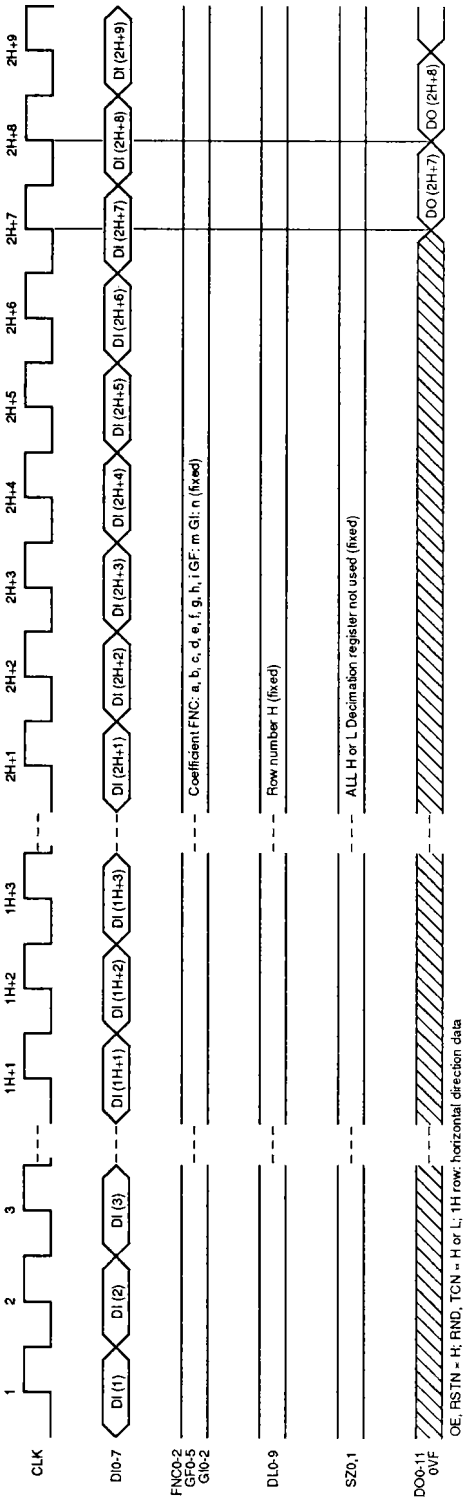
The SM5835AF requires a reset pulse to initialize its internal timing circuits. A reset pulse must be applied to the RTSN pin in the following circumstances.

- Power is applied
- The system clock is stopped for 10 μs or more.

For reset, RSTN must be held LOW for at least two CLK cycles.

TIMING CHARTS

Relation between Input and Output Data

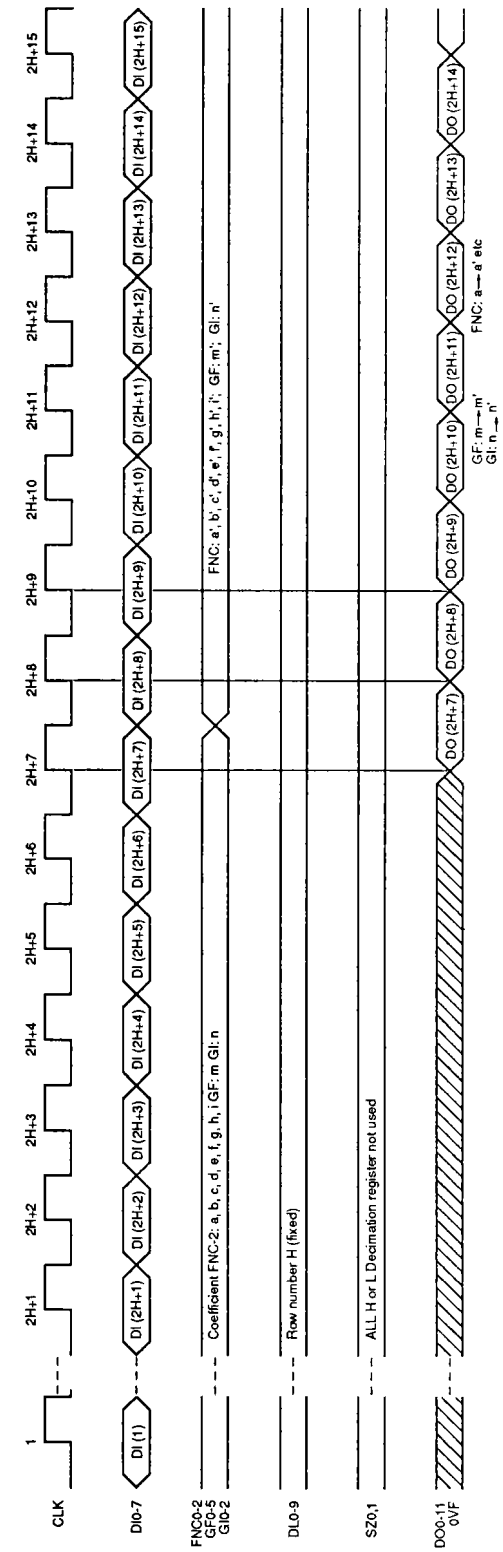


Output	DO (Y)	DO (1) - DO (4)	DO (5)	DO (6)	DO (7)	- - -	DO (1H + 5)	DO (1H + 6)	DO (1H + 7)	- - -	DO (2H + 5)	DO (2H + 6)	DO (2H + 7)	DO (2H + 8)
Term and coefficient	aY33	aX	aDI (1)	aDI (2)	aDI (3)		aDI (1H + 1)	aDI (1H + 2)	aDI (1H + 3)		aDI (2H + 1)	aDI (2H + 2)	aDI (2H + 3)	aDI (2H + 4)
	bY32	bX	bX	bDI (1)	bDI (2)		bDI (1H)	bDI (1H + 1)	bDI (1H + 2)		bDI (2H)	bDI (2H + 1)	bDI (2H + 2)	bDI (2H + 3)
	cY31	cX	cX	cX	cDI (1)		cDI (1H - 1)	cDI (1H)	cDI (1H + 1)		cDI (2H - 1)	cDI (2H)	cDI (2H + 1)	cDI (2H + 2)
	dY23	dX	dX	dX	dX		dDI (1)	dDI (2)	dDI (3)		dDI (1H + 1)	dDI (1H + 2)	dDI (1H + 3)	dDI (1H + 4)
	eY22	eX	eX	eX	eX		eX	eDI (1)	eDI (2)		eDI (1H)	eDI (1H + 1)	eDI (1H + 2)	eDI (1H + 3)
	fY21	fX	fX	fX	fX		fX	fX	fDI (1)		fDI (1H - 1)	fDI (1H)	fDI (1H + 1)	fDI (1H + 2)
	gY13	gX	gX	gX	gX		gX	gX	gX		gDI (1)	gDI (2)	gDI (3)	gDI (4)
	hY12	hX	hX	hX	hX		hX	hX	hX		hX	hDI (1)	hDI (2)	hDI (3)
	iY11	iX	iX	iX	iX		iX	iX	iX		iX	iX	iDI (1)	iDI (2)
	GF	m	m	m	m		m	m	m		m	m	m	m
	nY22	nX	nX	nX	nX		nX	nDI (1)	nDI (2)		nDI (1H)	nDI (1H + 1)	nDI (1H + 2)	nDI (1H + 3)

DO (Y) = m (iY11 + hY12 + gY13 + fY21 + eY22 + dY23 + cY31 + bY32 + aY33) + nY22; FNC0-2: a, b, c, e, f, g, h, i; GF: m; GI: n; X is a variable.

Figure 11. Relation between input data, output data and coefficients

Relation between Coefficients and Output Data



Output	DO (Y)	DO (1)	- - -	DO (2H + 7)	DO (2H + 8)	DO (2H + 9)	DO (2H + 10)	DO (2H + 11)	DO (2H + 12)	DO (2H + 13)	DO (2H + 14)
Term and coefficient	aY33	aX	- - -	aDI (2H + 3)	aDI (2H + 4)	aDI (2H + 5)	aDI (2H + 6)	aDI (2H + 7)	aDI (2H + 8)	a'DI (2H + 9)	a'DI (2H + 10)
	bY32	bX		bDI (2H + 2)	bDI (2H + 3)	bDI (2H + 4)	bDI (2H + 5)	bDI (2H + 6)	bDI (2H + 7)	b'DI (2H + 8)	b'DI (2H + 9)
	cY31	cX		cDI (2H + 1)	cDI (2H + 2)	cDI (2H + 3)	cDI (2H + 4)	cDI (2H + 5)	cDI (2H + 6)	c'DI (2H + 7)	c'DI (2H + 8)
	dY23	dX		dDI (1H + 3)	dDI (1H + 4)	dDI (1H + 5)	dDI (1H + 6)	dDI (1H + 7)	dDI (1H + 8)	d'DI (1H + 9)	d'DI (1H + 10)
	eY22	eX		eDI (1H + 2)	eDI (1H + 3)	eDI (1H + 4)	eDI (1H + 5)	eDI (1H + 6)	eDI (1H + 7)	e'DI (1H + 8)	e'DI (1H + 9)
	fY21	fX		fDI (1H + 1)	fDI (1H + 2)	fDI (1H + 3)	fDI (1H + 4)	fDI (1H + 5)	fDI (1H + 6)	f'DI (1H + 7)	f'DI (1H + 8)
	gY13	gX		gDI (3)	gDI (4)	gDI (5)	gDI (6)	gDI (7)	gDI (8)	g'DI (9)	g'DI (10)
	hY12	hX		hDI (2)	hDI (3)	hDI (4)	hDI (5)	hDI (6)	hDI (7)	h'DI (8)	h'DI (9)
	iY11	iX		iDI (1)	iDI (2)	iDI (3)	iDI (4)	iDI (5)	iDI (6)	i'DI (7)	i'DI (8)
	GF	m		m	m	m	m'	m'	m'	m'	m'
	nY22	nX		nDI (1H + 2)	nDI (1H + 3)	nDI (1H + 4)	n'DI (1H + 5)	n'DI (1H + 6)	n'DI (1H + 7)	n'DI (1H + 8)	n'DI (1H + 9)

DO (Y) = m (iY11 + hY12 + gY13 + fY21 + eY22 + dY23 + cY31 + bY32 + aY33) + nY22; FNC0-2: a, b, c, e, f, g, h, i; GF: m; GI: n; X is a variable.

Y11	Y12	Y13
Y21	Y22	Y23
Y31	Y32	Y33

3 x 3 filter grid

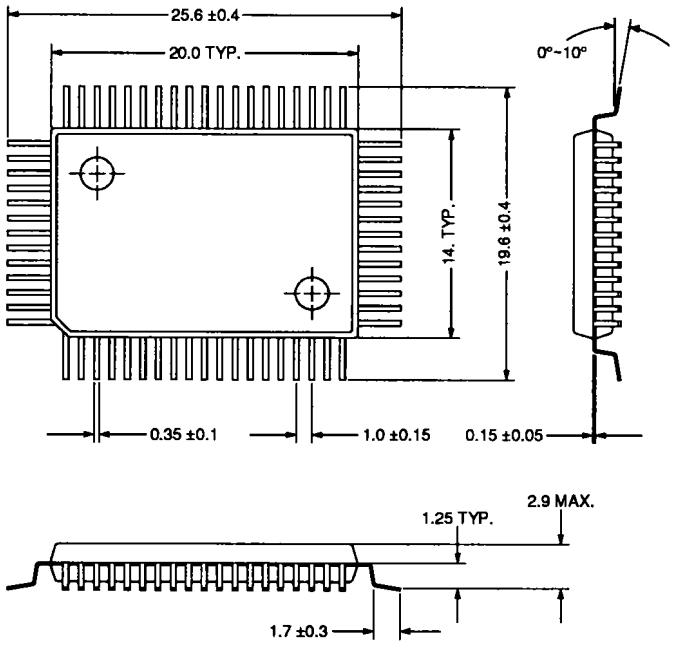
i	h	g
f	e	d
c	b	a

3 x 3 filter coefficient matrix

Figure 12. Relation between input data, output data and coefficients

PACKAGE OUTLINE

Unit: mm



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